IRHI7360SE

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-259AA)

400V, N-CHANNEL
RAD-Hard HEXFET TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D
IRHI7360SE	100 kRads(Si)	0.20Ω	24.3A

TO-259AA

Description

IR HiRel RAD-Hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low Rdson and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings **Pre-Irradiation**

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	24.3	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	15.3	
I_{DM}	Pulsed Drain Current ①	97.2	
P_D @T_C = 25°C	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.4	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	500	mJ
I_{AR}	Avalanche Current ①	24.3	A
E_{AR}	Repetitive Avalanche Energy ①	30	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	10.9 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	400	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.45	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.20	Ω	V_{GS} = 12V, I_D = 15.3A ④
		—	—	0.21		V_{GS} = 12V, I_D = 24.3A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	4.75	—	—	S	V_{DS} = 15V, I_D = 15.3A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	50	µA	V_{DS} = 320V, V_{GS} = 0V
		—	—	250		V_{DS} = 320V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	180	nC	I_D = 24.3A
Q_{GS}	Gate-to-Source Charge	—	—	75		V_{DS} = 200V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	100		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = 200V
tr	Rise Time	—	—	100		I_D = 24.3A
$t_{d(off)}$	Turn-Off Delay Time	—	—	100		R_G = 2.35Ω
t_f	Fall Time	—	—	100		V_{GS} = 12V
$L_S + L_D$	Total Inductance	—	8.7	—	nH	Measured from Drain lead (6mm / 0.25in from package) to Source lead (6mm / 0.25 in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	7500	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	1200	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	500	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	24.3	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	97.2		
V_{SD}	Diode Forward Voltage	—	—	1.4	V	T_J = 25°C, I_S = 24.3A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	750	ns	T_J = 25°C, I_F = 24.3A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	16	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.42	°C/W
$R_{\theta CS}$	Case -to-Sink	—	0.21	—	
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	30	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 1.7mH, Peak I_L = 24.3A, V_{GS} = 12V

③ I_{SD} ≤ 24.3A, di/dt ≤ 170A/µs, V_{DD} ≤ 400V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias. 320** volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 100 kRads (Si) [1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	400	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	50	µA	V_{DS} = 320V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	——	0.20	Ω	V_{GS} = 12V, I_D = 15.3A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-259AA)	——	0.20	Ω	V_{GS} = 12V, I_D = 15.3A
V_{SD}	Diode Forward Voltage	——	1.4	V	V_{GS} = 0V, I_D = 24A

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

Ion	LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V)				
				@VGS=0V	@VGS=-5V	@VGS=-10V	@VGS=-20V	@VGS=-25V
Cu	28	285	43	325	325	325	325	325
Br	36.8	305	39	325	325	325	320	

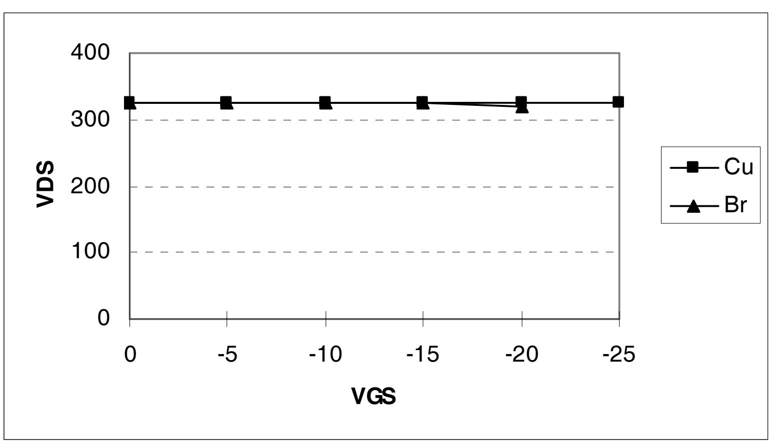


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

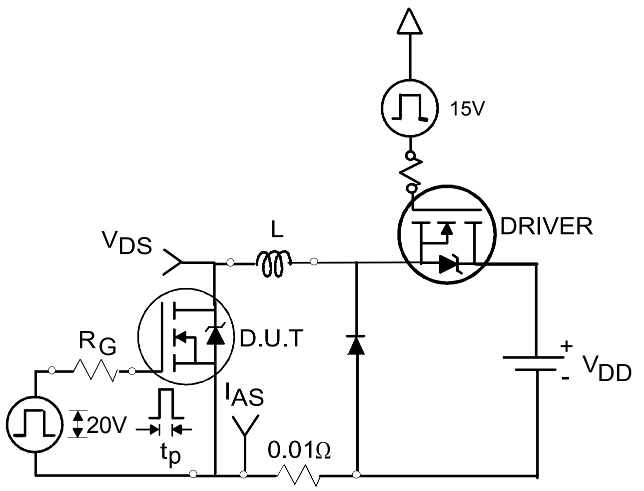


Fig 1a. Unclamped Inductive Test Circuit

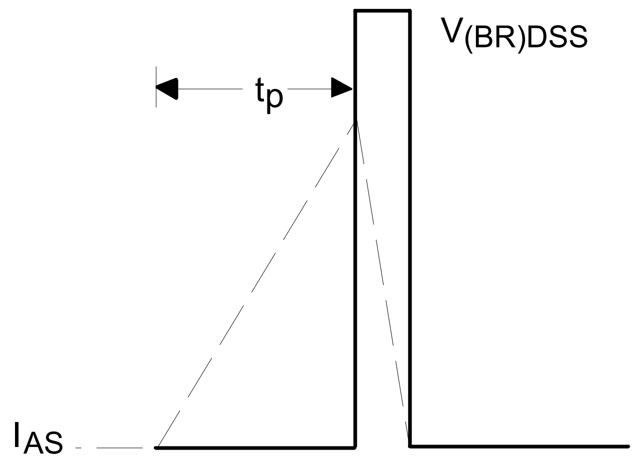


Fig 1b. Unclamped Inductive Waveforms

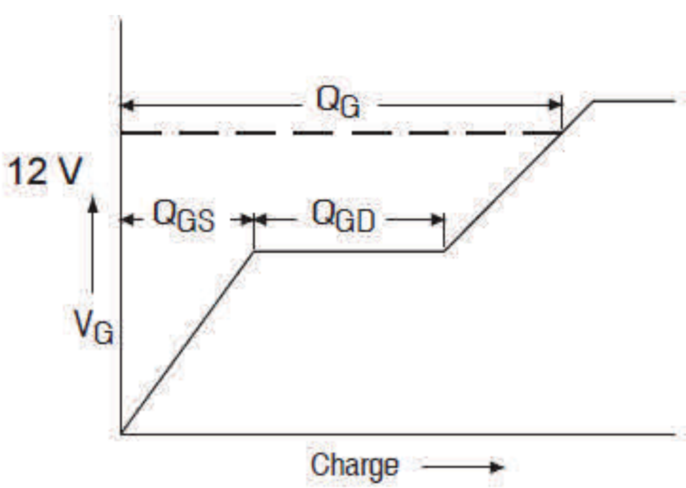


Fig 2a. Gate Charge Waveform

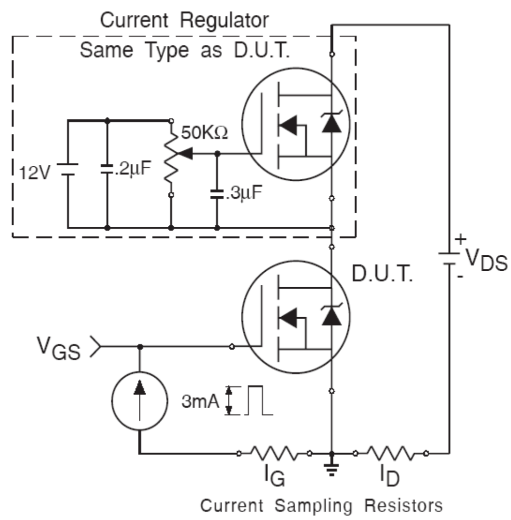


Fig 2b. Gate Charge Test Circuit

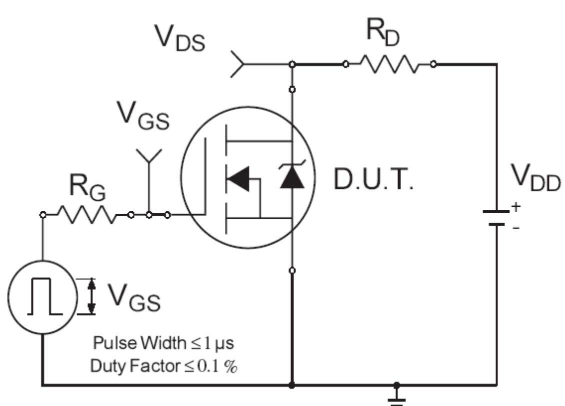


Fig 3a. Switching Time Test Circuit

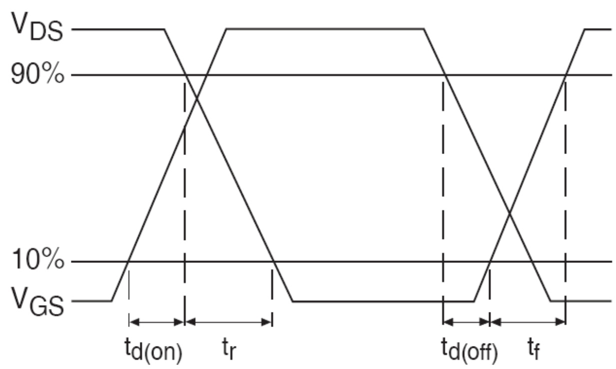
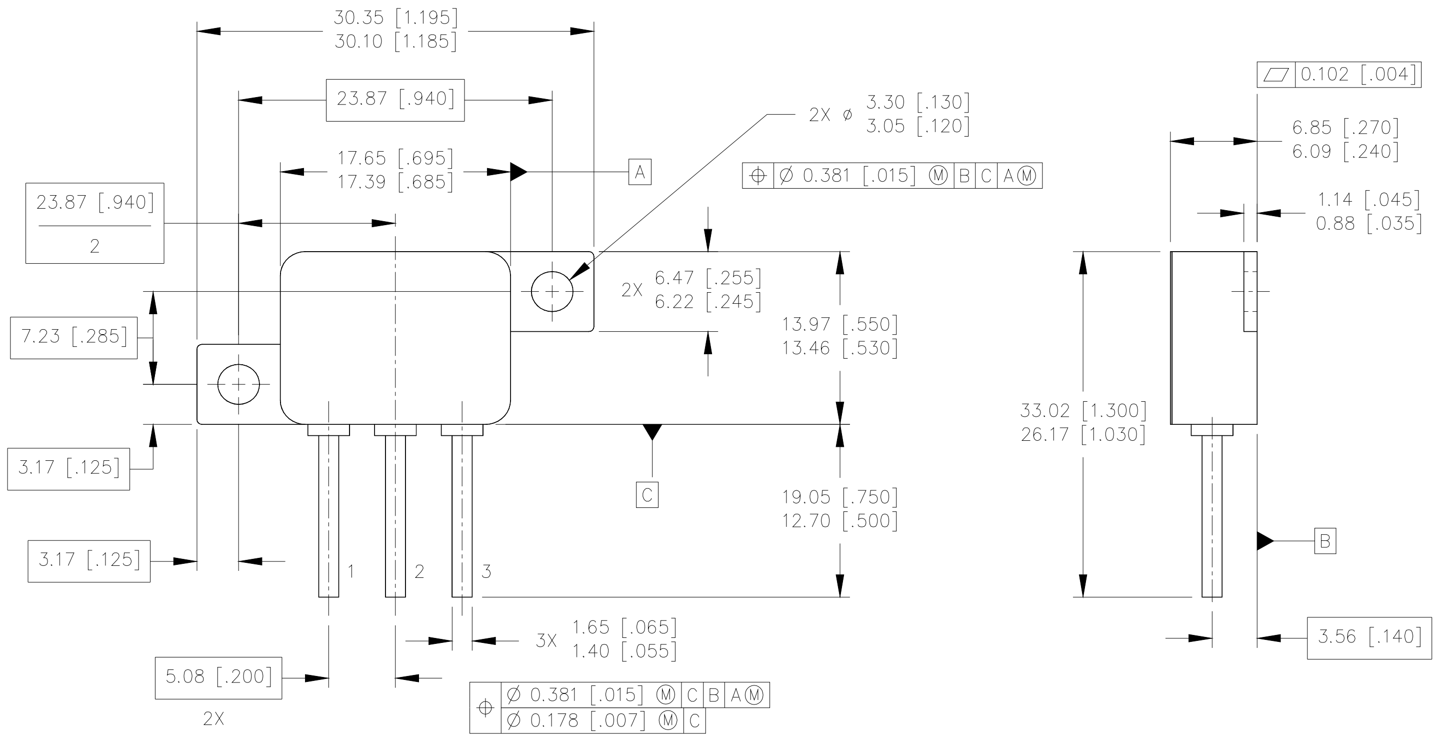


Fig 3b. Switching Time Waveforms

Case Outline and Dimensions — TO-259AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILILIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-259AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

An Infineon Technologies Company

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Data and specifications subject to change without notice.

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