

---

---

**Bluetooth® 4.2 Stereo Audio SoC**

---

---

**Features**

- Qualified for Bluetooth v4.2 specifications
- Supports HFP 1.6, HSP 1.2, A2DP 1.3, SPP 1.2 and AVRCP 1.6
- Supports Bluetooth Low Energy (BLE) (FW dependent):
  - Generic access service
  - Device information service
  - Proprietary services for data communication
  - Apple Notification Center Service (ANCS)
- Supports high resolution up to 24-bit, 96 kHz audio data format
- I<sup>2</sup>S digital audio (IS2064 only), MIC, analog audio, AUX-In
- Supports microphone inputs: 2 (IS2062) and 1 (IS2064)
- UART, GPIOs, and LEDs
- Supports firmware field upgrade
- Battery charging

**Baseband Features**

- 16 MHz main clock input
- Flash memory (8 Mbit)
- EEPROM (128 Kbit)
- Connects two hosts with HFP or A2DP profiles simultaneously, and SPP/BLE connection to one host
- Adaptive Frequency Hopping (AFH)

**RF Features**

- Class 2 output power (+2 dBm typical)
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Supports Bluetooth (BDR/EDR/BLE) specifications (FW dependent)
- Combined Tx/Rx RF terminal simplifies external matching and reduces external antenna switches
- Tx/Rx RF switch for Class 2 or Class 3 applications
- Integrated synthesizer requires no external voltage-controlled oscillator (VCO), varactor diode, resonator, loop filter
- Crystal oscillator with built-in digital trimming compensates for temperature or process variations

**DSP Audio Processing**

- 32-bit DSP core
- Supports 64 kbps A-Law,  $\mu$ -Law PCM format, Continuous Variable Slope Delta (CVSD) Modulation for Synchronous Connection-Oriented (SCO) channel operation
- Supports 8/16 kHz noise suppression
- Supports 8/16 kHz echo cancellation
- Packet loss concealment (PLC)
- Supports Serial Copy Management System (SCMS-T) content protection

**Audio Codec**

- Sub-band Coding (SBC) and optional Advanced Audio Coding (AAC) decoding
- 20-bit digital-to-analog (DAC) with 98 dB SNR
- 16-bit analog-to-digital (ADC) with 92 dB SNR
- Supports up to 24-bit, 96 kHz on I<sup>2</sup>S digital audio

**Peripherals**

- High-speed Host Controller Interface (HCI)-UART (supports up to 921,600 bps)
- USB2.0 compatible interface for FW/EEPROM upgrade (IS2064)
- Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
- Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO) regulator
- Built-in ADC for battery monitoring and voltage sensor and charger thermal protection
- Built-in undervoltage protection (UVP)
- LED drivers: 2 (IS2062) and 3 (IS2064)

**Operating Condition**

- Operating voltage: 3.2V to 4.2V
- Temperature range: -20°C to +70°C

**Package**

- IS2062: 7 mm x 7 mm, LGA-56 package
- IS2064: 8 mm x 8 mm, LGA-68 package
- 0.4 mm pitch

# IS2062/64

---

## Applications

- Soundbars and subwoofers
- Speaker phones
- Headsets and headphones

## Description

The IS2062/64 is a Stereo Audio SoC qualified for Bluetooth 4.2 with Enhanced Data Rate (EDR). It integrates a 32-bit DSP co-processor and a codec which is dedicated for voice and audio applications. For voice applications, Continuously Variable Slope Delta (CVSD) encoding/decoding, 8K/16K noise reduction, and echo cancellation are implemented. For audio applications, Sub-band coding (SBC) and AAC Low-Complexity (AAC-LC) decoding functions are used.

The IS2062/64 SoC features a 20-bit audio DAC in addition to an I<sup>2</sup>S digital audio interface that supports up to 24-bit, 96 kHz data formats. System optimizations include an integrated battery voltage sensor, battery charger, switching regulator, and LDO.

## Table of Contents

|   |    |
|---|----|
| 1.0 Device Overview .....                       | 5  |
| 2.0 Audio .....                                 | 15 |
| 3.0 Transceiver .....                           | 19 |
| 4.0 Microcontroller .....                       | 21 |
| 5.0 Power management unit .....                 | 23 |
| 6.0 Application Information .....               | 25 |
| 7.0 Antenna Placement Rule .....                | 35 |
| 8.0 Electrical Characteristics .....            | 37 |
| 9.0 Package Information .....                   | 45 |
| 10.0 Reflow Profile and Storage Condition ..... | 53 |
| 11.0 Ordering Information .....                 | 57 |
| Appendix A: Reference Circuit .....             | 59 |
| Appendix B: Revision History .....              | 69 |

## TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at [docerrors@microchip.com](mailto:docerrors@microchip.com) or fax the **Reader Response Form** in the back of this data sheet to (480) 792-4150. We welcome your feedback.

### Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

<http://www.microchip.com>

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

### Customer Notification System

Register on our web site at [www.microchip.com](http://www.microchip.com) to receive the most current information on all of our products.

# IS2062/64

---

NOTES:



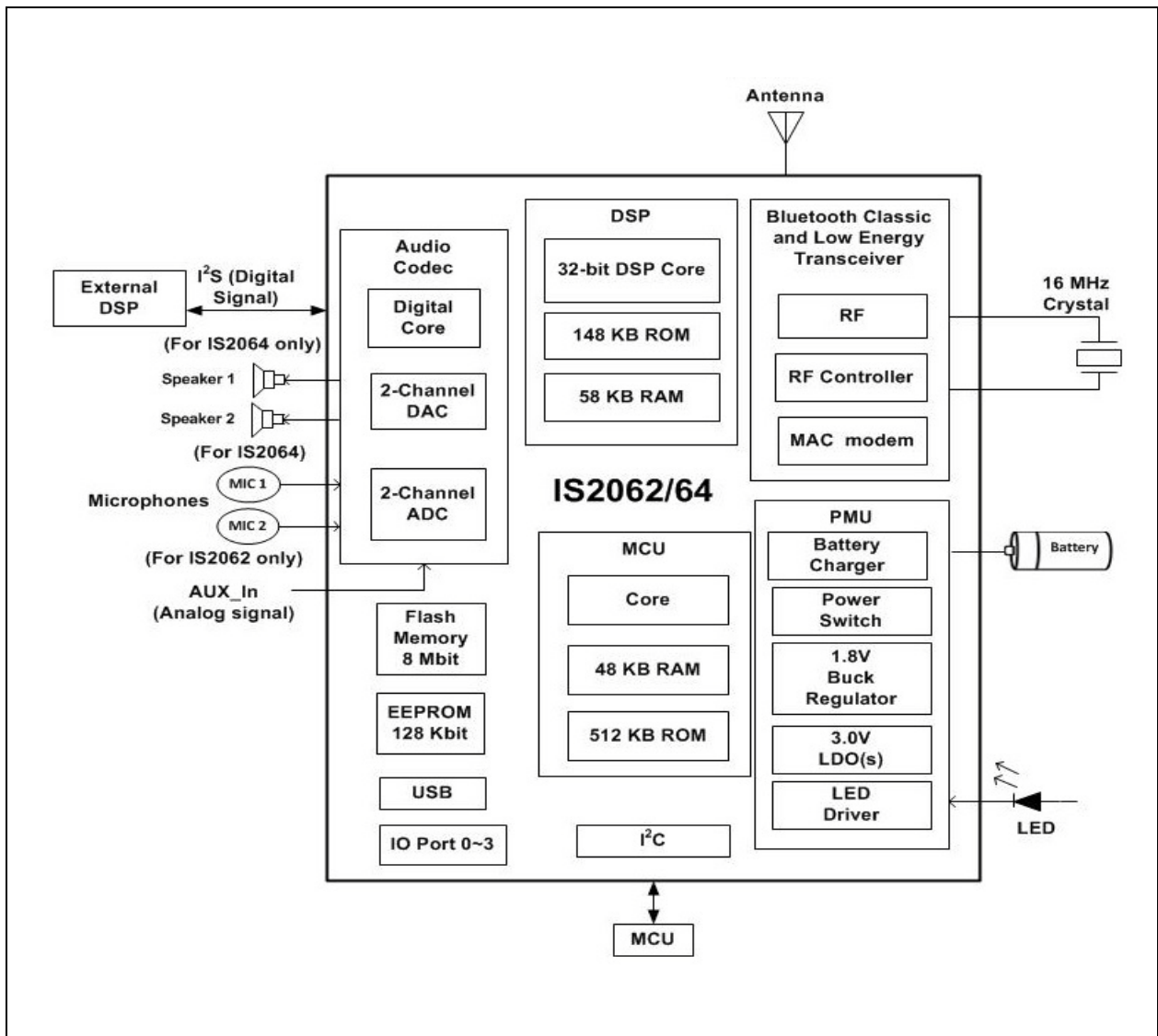
## 1.0 DEVICE OVERVIEW

The IS2062/64 SoC integrates a Bluetooth 4.2 dual-mode radio transceiver, a Power Management Unit (PMU), a Microcontroller (MCU), an audio codec, a crystal and a 32-bit DSP. The IS2062/64 SoC can be configured using a UI tool.

Figure 1-1 illustrates a typical block diagram of the IS2062/64 SoC.

**Note:** The UI tool is a Windows®-based configuration utility tool, which is available for download from the Microchip web site at: [www.microchip.com/IS2062](http://www.microchip.com/IS2062) and [www.microchip.com/IS2064](http://www.microchip.com/IS2064).

**FIGURE 1-1: IS2062/64 STEREO AUDIO SOC BLOCK DIAGRAM**



# IS2062/64

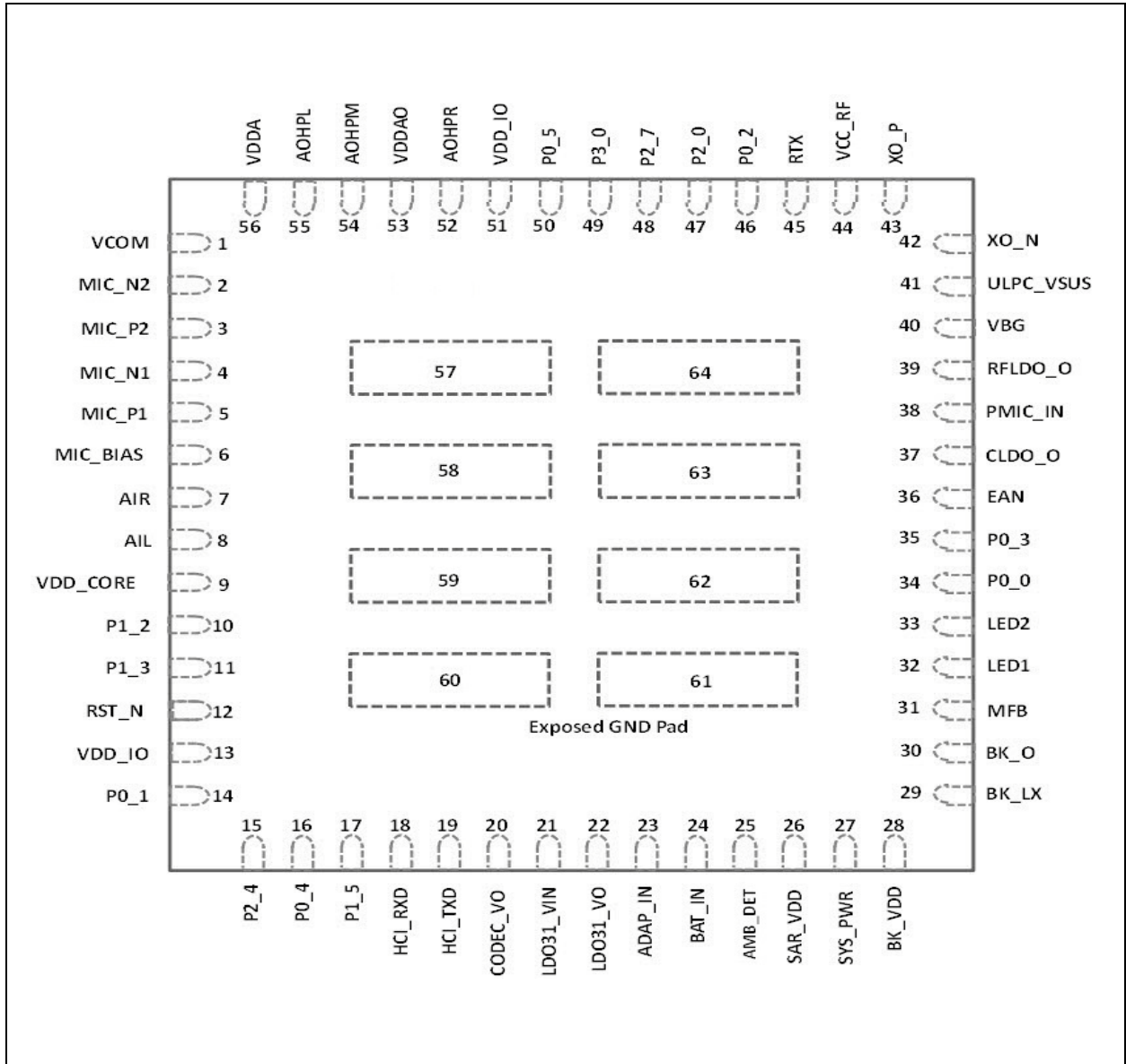
Table 1-2 provides the key features of the IS2062/64 SoC.

**TABLE 1-1: IS2062/64 KEY FEATURES**

| Feature                             | IS2062          | IS2064    |
|-------------------------------------|-----------------|-----------|
| Application                         | Headset/Speaker | Speaker   |
| Stereo/mono                         | Stereo          | Stereo    |
| Pin count                           | 56              | 68        |
| Dimensions (mm <sup>2</sup> )       | 7 x 7           | 8 x 8     |
| Audio DAC output                    | 2 Channel       | 2 Channel |
| DAC (single-ended) SNR at 2.8V (dB) | -98             | -98       |
| DAC (capless) SNR at 2.8V (dB)      | -96             | -96       |
| ADC SNR at 2.8V (dB)                | -92             | -92       |
| I <sup>2</sup> S digital interface  | No              | Yes       |
| Analog AUX-In                       | Yes             | Yes       |
| Mono microphones                    | 2               | 1         |
| External audio amplifier interface  | Yes             | Yes       |
| UART                                | Yes             | Yes       |
| LED driver                          | 2               | 3         |
| Internal DC-DC step-down regulator  | Yes             | Yes       |
| DC 5V adaptor input                 | Yes             | Yes       |
| Battery charger (350 mA max)        | Yes             | Yes       |
| ADC for thermal charger protection  | Yes             | Yes       |
| Undervoltage protection             | Yes             | Yes       |
| GPIO                                | 10              | 15        |
| Button support                      | 6               | 6         |
| NFC (triggered by external NFC)     | Yes             | Yes       |
| EEPROM                              | 128 K           | 128 K     |
| Customized voice prompt             | Store in EEPROM |           |
| Multi-tone                          | Yes             | Yes       |
| DSP sound effect                    | Yes             | Yes       |
| BLE                                 | Yes             | Yes       |
| Bluetooth profiles                  |                 |           |
| HFP                                 | 1.6             | 1.6       |
| AVRCP                               | 1.6             | 1.6       |
| A2DP                                | 1.3             | 1.3       |
| HSP                                 | 1.2             | 1.2       |
| SPP                                 | 1.2             | 1.2       |

Figure 1-2 illustrates the IS2062 SoC pin diagram. Table 1-2 provides the pin descriptions of the IS2062 SoC and these pins can be configured using the UI tool.

**FIGURE 1-2: IS2062 SOC PIN DIAGRAM**



# IS2062/64

**TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS**

| Pin No | Pin Type | Name      | Description   |
|--------|----------|-----------|---|
| 1      | P        | VCOM      | Internal biasing voltage for codec; connect to GND through a 1 $\mu$ F (X5R/X7R) capacitor  |
| 2      | I        | MIC_N2    | Mic 2 mono differential analog negative input   |
| 3      | I        | MIC_P2    | Mic 2 mono differential analog positive input   |
| 4      | I        | MIC_N1    | Mic 1 mono differential analog negative input   |
| 5      | I        | MIC_P1    | Mic 1 mono differential analog positive input   |
| 6      | P        | MIC_BIAS  | Electric mic biasing voltage  |
| 7      | I        | AIR       | R-channel, single-ended analog input  |
| 8      | I        | AIL       | L-channel, single-ended analog input  |
| 9      | P        | VDD_CORE  | Core 1.2V power input; connect to the CLDO_O pin; connect to GND through a 1 $\mu$ F (X5R/X7R) capacitor  |
| 10     | O        | P1_2      | I <sup>2</sup> C SCL (EEPROM)   |
| 11     | I/O      | P1_3      | I <sup>2</sup> C SDA (EEPROM), requires external pull-up resistor   |
| 12     | I        | RST_N     | System Reset (active-low)   |
| 13     | P        | VDD_IO    | I/O power supply input (3.0V~3.6V); connect to LDO31_VO (pin # 22); connect to GND through a 1 $\mu$ F (X5R/X7R) capacitor  |
| 14     | I/O      | P0_1      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• FWD key when class 2 RF (default), active-low</li> <li>• Class1 Tx control signal for external RF T/R switch, active-high</li> </ul>   |
| 15     | I        | P2_4      | System configuration pin along with P2_0 and EAN pins can be used to set the SoC in any one of the following modes: <ul style="list-style-type: none"> <li>• Application mode (for normal operation)</li> <li>• Test mode (to change EEPROM values)</li> <li>• Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 16     | I/O      | P0_4      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• NFC detection pin, active-low</li> <li>• Out_Ind_1</li> </ul>  |
| 17     | I/O      | P1_5      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• NFC detection pin, active-low</li> <li>• Out_Ind_1</li> <li>• Slide Switch Detector</li> </ul>   |
| 18     | I        | HCI_RXD   | HCI UART data input   |
| 19     | O        | HCI_TXD   | HCI UART data output  |
| 20     | P        | CODEC_VO  | LDO output for codec power  |
| 21     | P        | LDO31_VIN | LDO input, connect to SYS_PWR (pin # 27)  |
| 22     | P        | LDO31_VO  | 3V LDO output for VDD_IO power, do not calibrate  |
| 23     | P        | ADAP_IN   | 5V power adaptor input  |
| 24     | P        | BAT_IN    | Battery input. voltage range: 3.2V to 4.2V  |

TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS (CONTINUED)

| Pin No | Pin Type | Name      | Description  |
|--------|----------|-----------|--|
| 25     | I        | AMB_DET   | Analog input for ambient temperature detection   |
| 26     | P        | SAR_VDD   | SAR 1.8V input; connect to BK_O pin  |
| 27     | P        | SYS_PWR   | Power output from BAT_IN or ADAP_IN for IS2062 only  |
| 28     | P        | BK_VDD    | 1.8V buck VDD power Input; connect to SYS_PWR pin  |
| 29     | P        | BK_LX     | 1.8V buck PWM/PFM output   |
| 30     | P        | BK_O      | 1.8V buck feedback input   |
| 31     | I        | MFB       | <ul style="list-style-type: none"> <li>Multi-function button and power-on key</li> <li>UART RX IND, active-high</li> </ul>   |
| 32     | I        | LED1      | LED driver 1   |
| 33     | I        | LED2      | LED driver 2   |
| 34     | I/O      | P0_0      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>Slide Switch Detector, active-low</li> <li>UART TX_IND, active-low</li> </ul>   |
| 35     | I/O      | P0_3      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>REV key (default), active-low</li> <li>Buzzer signal output</li> <li>Out_Ind_2</li> <li>Class1 Rx Control signal of external RF T/R switch, active-high</li> </ul>  |
| 36     | I        | EAN       | System configuration pin along with the P2_4 and P2_0 pins can be used to set the SoC in any one of the following modes: <ul style="list-style-type: none"> <li>Application mode (for normal operation)</li> <li>Test mode (to change EEPROM values)</li> <li>Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 37     | P        | CLDO_O    | 1.2V core LDO output   |
| 38     | P        | PMIC_IN   | 1.8V power input for internal blocks; connect to BK_O (pin # 30)   |
| 39     | P        | RFLDO_O   | 1.28V RF LDO output  |
| 40     | P        | VBG       | Bandgap output reference for decoupling interference   |
| 41     | P        | ULPC_VSUS | ULPC 1.2V output power   |
| 42     | I        | XO_N      | 16 MHz crystal input negative  |
| 43     | I        | XO_P      | 16 MHz crystal input positive  |
| 44     | P        | VCC_RF    | RF power input (1.28V) for both synthesizer and Tx/Rx block  |
| 45     | I/O      | RTX       | RF path (transmit/receive)   |
| 46     | I        | P0_2      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>Play/Pause key (default), active-low</li> </ul>   |

# IS2062/64

**TABLE 1-2: IS2062 SOC PIN DESCRIPTIONS (CONTINUED)**

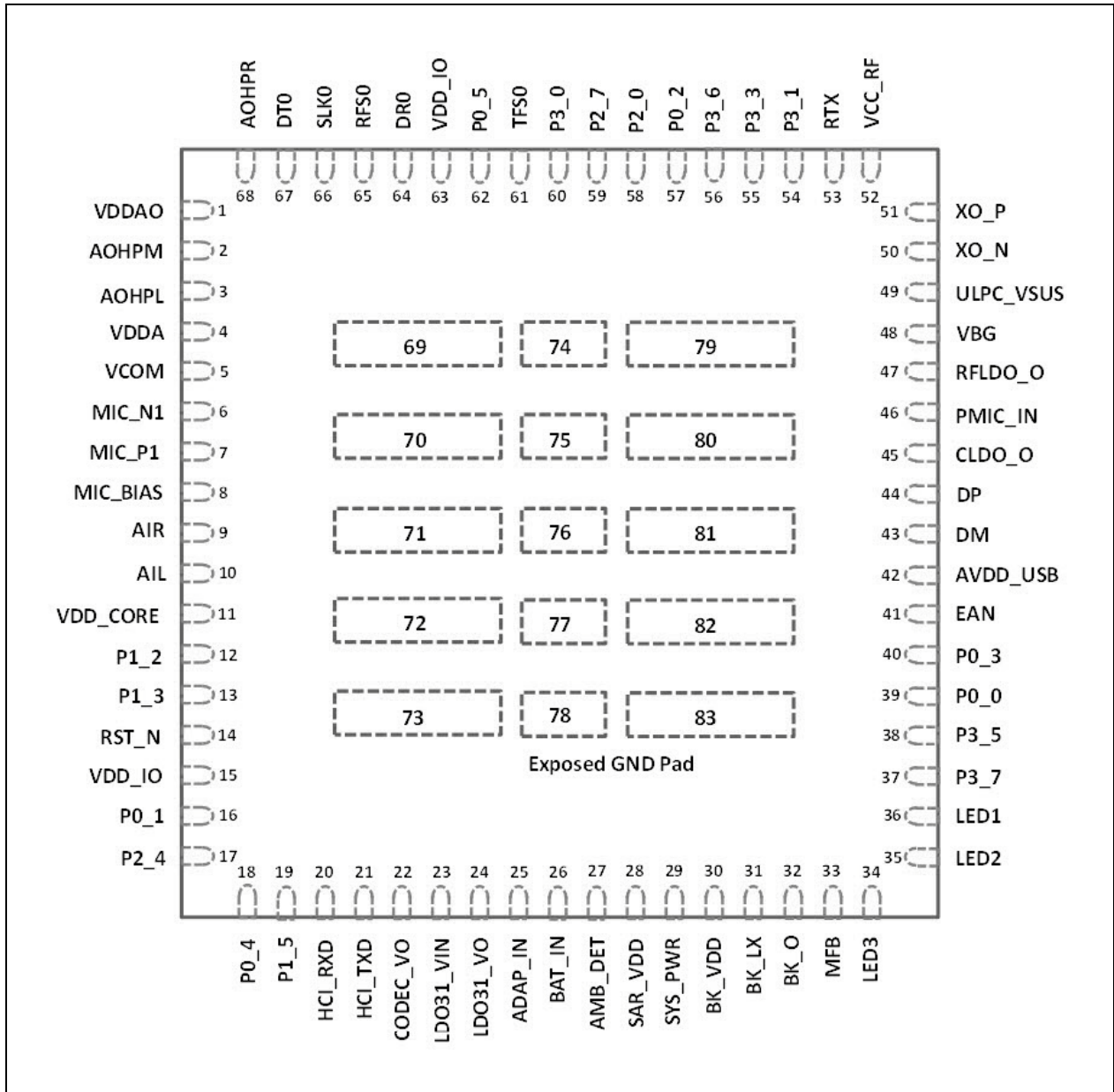
| Pin No | Pin Type | Name   | Description  |
|--------|----------|--------|--|
| 47     | I        | P2_0   | System configuration pin along with P2_4 and EAN pins can be used to set the SoC in any one of the following modes: <ul style="list-style-type: none"> <li>• Application mode (for normal operation),</li> <li>• Test mode (to change EEPROM values)</li> <li>• Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 48     | I        | P2_7   | Configurable control or indication pin (Internally pulled up if configured as an input)<br>Volume-up key (default)   |
| 49     | I        | P3_0   | Configurable control or indication pin (Internally pulled up if configured as an input)<br>AUX-In detector   |
| 50     | I        | P0_5   | Configurable control or indication pin (Internally pulled up if configured as an input)<br>Volume-up key (default)   |
| 51     | P        | VDD_IO | I/O power supply input (3.0V~3.6V); Connect to LDO31_VO pin  |
| 52     | O        | AOHPR  | R-channel analog headphone output,   |
| 53     | P        | VDDAO  | Power supply dedicated to codec output amplifiers; connect to CODEC_VO pin   |
| 54     | O        | AOHPM  | Headphone common mode output/sense input   |
| 55     | O        | AOHPL  | L-channel analog headphone output  |
| 56     | P        | VDDA   | Power supply or reference voltage for external codec; connect to CODEC_VO pin  |
| 57-64  | P        | EP     | Exposed pads. Used as ground (GND) pins  |

**Legend:** I= Input pin      O= Output pin      I/O= Input/Output pin      P= Power pin

**Note:** The IS2062 SoC pins can be configured using the UI tool.

Figure 1-3 illustrates the pin diagram of the IS2064 SoC.

**FIGURE 1-3: IS2064 SOC PIN DIAGRAM**



# IS2062/64

Table 1-3 provides the pin descriptions of the IS2064 SoC.

**TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS**

| Pin No | Pin Type | Name      | Description   |
|--------|----------|-----------|---|
| 1      | P        | VDDAO     | Power supply dedicated to codec output amplifiers; connect to the CODEC_VO pin  |
| 2      | O        | AOHPM     | Headphone common mode output or sense input   |
| 3      | O        | AOHPL     | Headphone output, left channel  |
| 4      | P        | VDDA      | Power supply or reference voltage for external codec; connect to the CODEC_VO pin   |
| 5      | P        | VCOM      | Internal biasing voltage for codec  |
| 6      | I        | MIC_N1    | Mic 1 mono differential analog negative input   |
| 7      | I        | MIC_P1    | Mic 1 mono differential analog positive input   |
| 8      | P        | MIC_BIAS  | Electric microphone biasing voltage   |
| 9      | I        | AIR       | R-channel single-ended analog input   |
| 10     | I        | AIL       | L-channel single-ended analog input   |
| 11     | P        | VDD_CORE  | Core 1.2V power input; connect to the CLDO_O pin  |
| 12     | O        | P1_2      | I <sup>2</sup> C SCL (EEPROM)   |
| 13     | I/O      | P1_3      | I <sup>2</sup> C SDA (EEPROM), requires external pull-up resistor   |
| 14     | I        | RST_N     | System Reset (active-low)   |
| 15     | P        | VDD_IO    | I/O power supply input (3.0V~3.6V); connect to LDO31_VO (pin # 24); connect to GND through a 1 $\mu$ F (X5R/X7R) capacitor  |
| 16     | I/O      | P0_1      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• FWD key when Class 2 RF (default), active-low</li> <li>• Class1 Tx control signal for external RF Tx/Rx switch, active-high</li> </ul>   |
| 17     | I        | P2_4      | System configuration pin along with the P2_0 and EAN pins, used to set the SoC in any one of the following modes: <ul style="list-style-type: none"> <li>• Application mode (for normal operation)</li> <li>• Test mode (to change EEPROM values)</li> <li>• Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 18     | I/O      | P0_4      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• NFC detection pin, active-low</li> <li>• Out_Ind_1</li> </ul>  |
| 19     | I/O      | P1_5      | Configurable control or indication pin (Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• NFC detection pin</li> <li>• Slide switch detector, active-high</li> <li>• Out_Ind_1</li> <li>• Multi-speaker Master/Slave mode control (FW dependent)</li> </ul>  |
| 20     | I        | HCI_RXD   | HCI UART data input   |
| 21     | O        | HCI_TXD   | HCI UART data output  |
| 22     | P        | CODEC_VO  | LDO output for codec power  |
| 23     | P        | LDO31_VIN | LDO input; connect to SYS_PWR (pin # 29)  |



TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS (CONTINUED)

| Pin No | Pin Type | Name      | Description  |
|--------|----------|-----------|--|
| 24     | P        | LDO31_VO  | 3V LDO output, for VDD_IO power, do not calibrate  |
| 25     | P        | ADAP_IN   | 5V power adaptor input   |
| 26     | P        | BAT_IN    | Battery input. Voltage range: 3.2V to 4.2V   |
| 27     | I        | AMB_DET   | Analog input for ambient temperature detection   |
| 28     | P        | SAR_VDD   | SAR 1.8V input; connect to BK_O pin  |
| 29     | P        | SYS_PWR   | Power output which come from BAT_IN or ADAP_IN   |
| 30     | P        | BK_VDD    | 1.8V buck VDD Power Input; connect to SYS_PWR pin  |
| 31     | P        | BK_LX     | 1.8V buck PWM/PFM output   |
| 32     | P        | BK_O      | 1.8V buck feedback input   |
| 33     | I        | MFB       | 1. Multi-function button and power-on key<br>2. UART RX_IND, active-high   |
| 34     | I        | LED3      | LED driver 3   |
| 35     | I        | LED2      | LED driver 2   |
| 36     | I        | LED1      | LED driver 1   |
| 37     | I/O      | P3_7      | Configurable control or indication pin<br>(Internally pulled up if configured as an input)<br>UART TX_IND, active-low  |
| 38     | I/O      | P3_5      | Configurable control or indication pin<br>(Internally pulled up if configured as an input)   |
| 39     | I/O      | P0_0      | Configurable control or indication pin<br>(Internally pulled up if configured as an input)<br>Slide switch detector, active-high   |
| 40     | I/O      | P0_3      | Configurable control or indication pin<br>(Internally pulled up if configured as an input) <ul style="list-style-type: none"> <li>• REV key, active-low.</li> <li>• Buzzer signal output</li> <li>• Out_Ind_2</li> <li>• Class 1 Rx Control signal of external RF T/R switch, active-high</li> </ul>   |
| 41     | I        | EAN       | System configuration pin along with the P2_0 and P2_4 pins, used to set the IS2062/64 SoC in any one of the following modes: <ul style="list-style-type: none"> <li>• Application mode (for normal operation)</li> <li>• Test mode (to change EEPROM values)</li> <li>• Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 42     | P        | AVDD_USB  | USB power input; connect to LDO31_VO pin   |
| 43     | I/O      | DM        | Differential data-minus USB  |
| 44     | I/O      | DP        | Differential data-positive USB   |
| 45     | P        | CLDO_O    | 1.2V core LDO output   |
| 46     | P        | PMIC_IN   | 1.8V power input for internal blocks; connect to BK_O (pin # 32)   |
| 47     | P        | RFLDO_O   | 1.28V RF LDO output  |
| 48     | P        | VBG       | Bandgap output reference for decoupling interference   |
| 49     | P        | ULPC_VSUS | ULPC 1.2V output power, maximum loading 1 mA   |
| 50     | I        | XO_N      | 16 MHz crystal input negative  |
| 51     | I        | XO_P      | 16 MHz crystal input positive  |

# IS2062/64

**TABLE 1-3: IS2064 SOC PIN DESCRIPTIONS (CONTINUED)**

| Pin No | Pin Type | Name   | Description   |
|--------|----------|--------|---|
| 52     | P        | VCC_RF | RF power input for both synthesizer and Tx/Rx block   |
| 53     | I/O      | RTX    | RF path (transmit/receive)  |
| 54     | I/O      | P3_1   | Configurable control or indication pin (Internally pulled up if configured as an input) REV key when Class 1 RF (default), active-low   |
| 55     | I/O      | P3_3   | Configurable control or indication pin (Internally pulled up if configured as an input) FWD key when class 1 RF (default), active-low   |
| 56     | I/O      | P3_6   | Configurable control or indication pin (Internally pulled up if configured as an input) Multi-SPK Master/Slave mode control (FW dependent)  |
| 57     | I/O      | P0_2   | Configurable control or indication pin (Internally pulled up if configured as an input) Play/Pause key as the default setting   |
| 58     | I/O      | P2_0   | System configuration pin along with the EAN and P2_4 pins can be used to set the SoC in any one of the following modes: <ul style="list-style-type: none"> <li>• Application mode (for normal operation),</li> <li>• Test mode (to change EEPROM values), and</li> <li>• Write Flash mode (to load a new firmware into the SoC), see <a href="#">Table 6-1</a></li> </ul> |
| 59     | I/O      | P2_7   | Configurable control or indication pin (Internally pulled up if configured as an input) Volume-up key (default)   |
| 60     | I/O      | P3_0   | Configurable control or indication pin (Internally pulled up if configured as an input) AUX-In detector   |
| 61     | I/O      | TFS0   | I <sup>2</sup> S interface: left/right clock  |
| 62     | I/O      | P0_5   | Configurable control or indication pin (Internally pulled up if configured as an input) Volume down key (default)   |
| 63     | P        | VDD_IO | I/O power supply input (3.0V~3.6V); connect to LDO31_VO pin   |
| 64     | I/O      | DR0    | I <sup>2</sup> S interface: digital left/right data   |
| 65     | I/O      | RFS0   | I <sup>2</sup> S interface: left/right clock  |
| 66     | I/O      | SCLK0  | I <sup>2</sup> S interface: bit clock   |
| 67     | I/O      | DT0    | I <sup>2</sup> S interface: digital left/right data   |
| 68     | O        | AOHPR  | Headphone output, right channel   |
| 69-83  | P        | EP     | Exposed pads, Used as ground (GND) pins   |

**Legend:** I= Input pin      O= Output pin      I/O= Input/Output pin      P= Power pin

**Note:** These pins can be configured using the UI tool.

## 2.0 AUDIO

The input and output audios have different stages and each stage can be programmed to vary the gain response characteristics. For microphone, both single-end inputs and differential inputs are supported. To maintain a high quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors can be used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

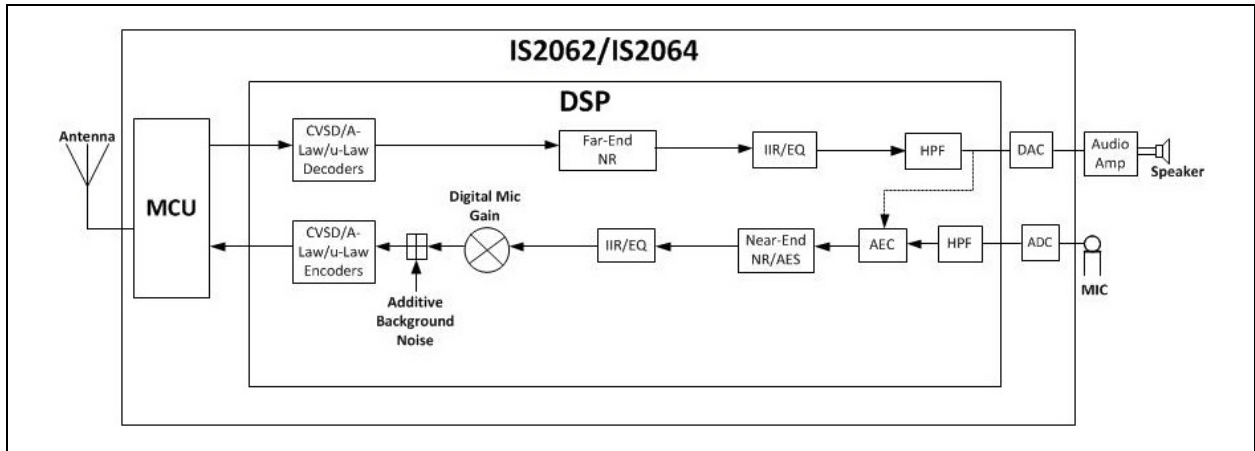
### 2.1 Digital Signal Processor

A Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction are in-built. To reduce nonlinear distortion and help echo cancellation, an outgoing signal level to

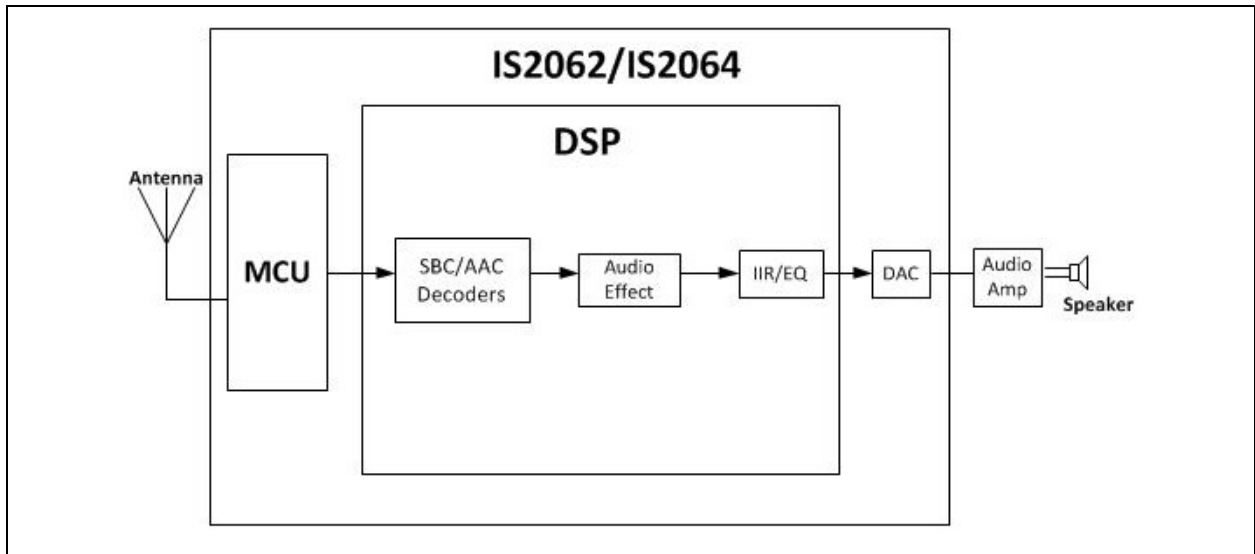
the speaker will exceed the threshold (and therefore likely to create echo). This may result in suppression of the signal. Adaptive filtering is also applied to track the echo path impulse in response to provide echo free and full-duplex user experience. The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by microphones and improves mutual understanding in communication. Advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are in-built. The audio effect algorithms are to improve the user's audio listening experience in terms of better quality audio after audio signal processing.

Figure 2-1 and Figure 2-2 illustrate the processing flow of speaker phone applications for speech and audio signal processing.

**FIGURE 2-1: SPEECH PROCESSING**



**FIGURE 2-2: AUDIO PROCESSING**



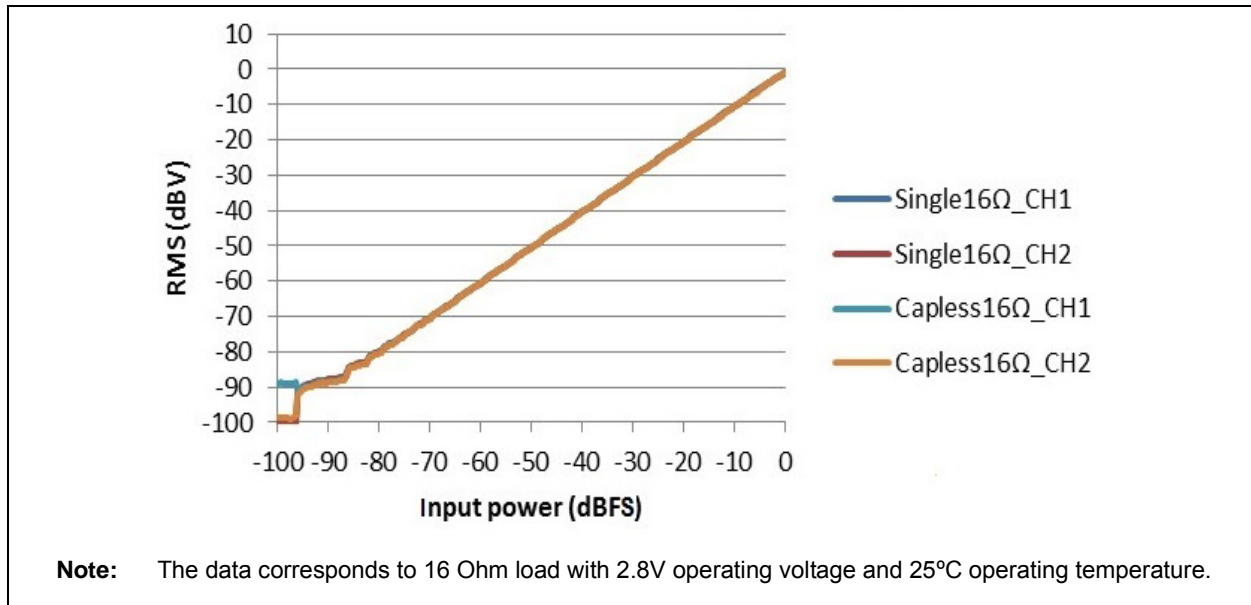
The DSP parameters can be configured using the DSP tool. For additional information on the DSP tool, refer to the "IS206X DSP Application Note".

**Note:** The DSP tool and IS206X DSP Application Note are available for download from the Microchip web site at: [www.microchip.com/IS2062](http://www.microchip.com/IS2062) and [www.microchip.com/IS2064](http://www.microchip.com/IS2064).

## 2.2 Codec

The built-in codec has a high signal-to-noise ratio (SNR) performance and it consist of an analog-to-digital converter (ADC), a digital-to-analog converter (DAC) and additional analog circuitry. Figure 2-3 through Figure 2-6 illustrate dynamic range and frequency response of the codec.

**FIGURE 2-3: CODEC DAC DYNAMIC RANGE**



**FIGURE 2-4: CODEC DAC THD+N VERSUS INPUT POWER**

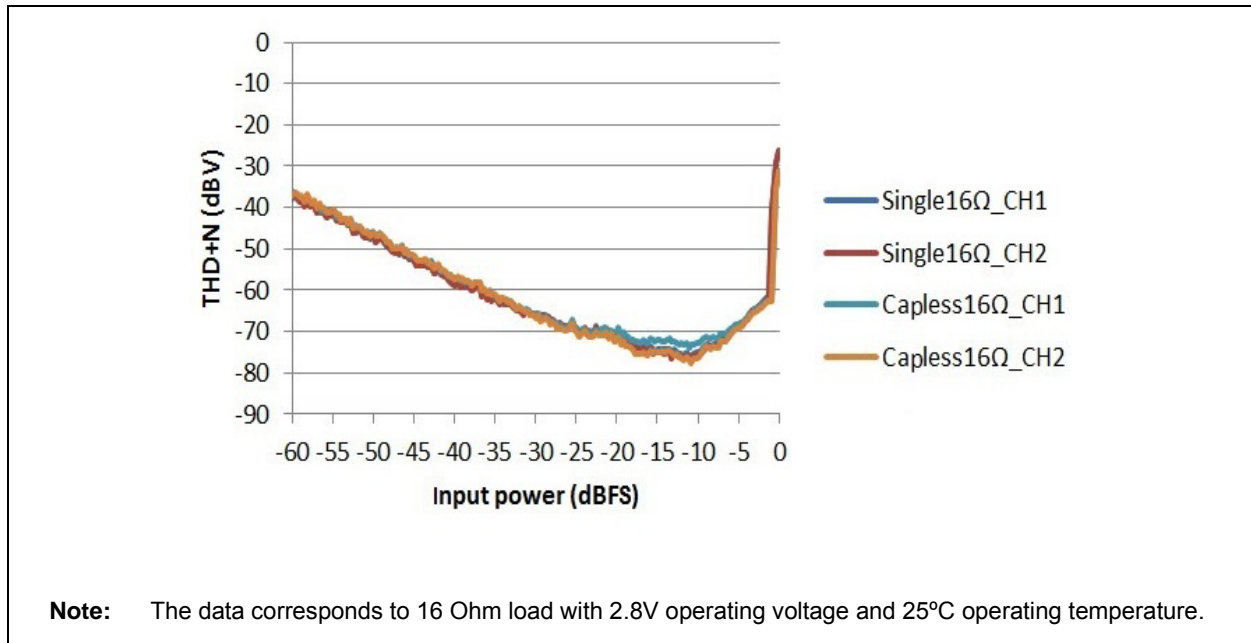


FIGURE 2-5: CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

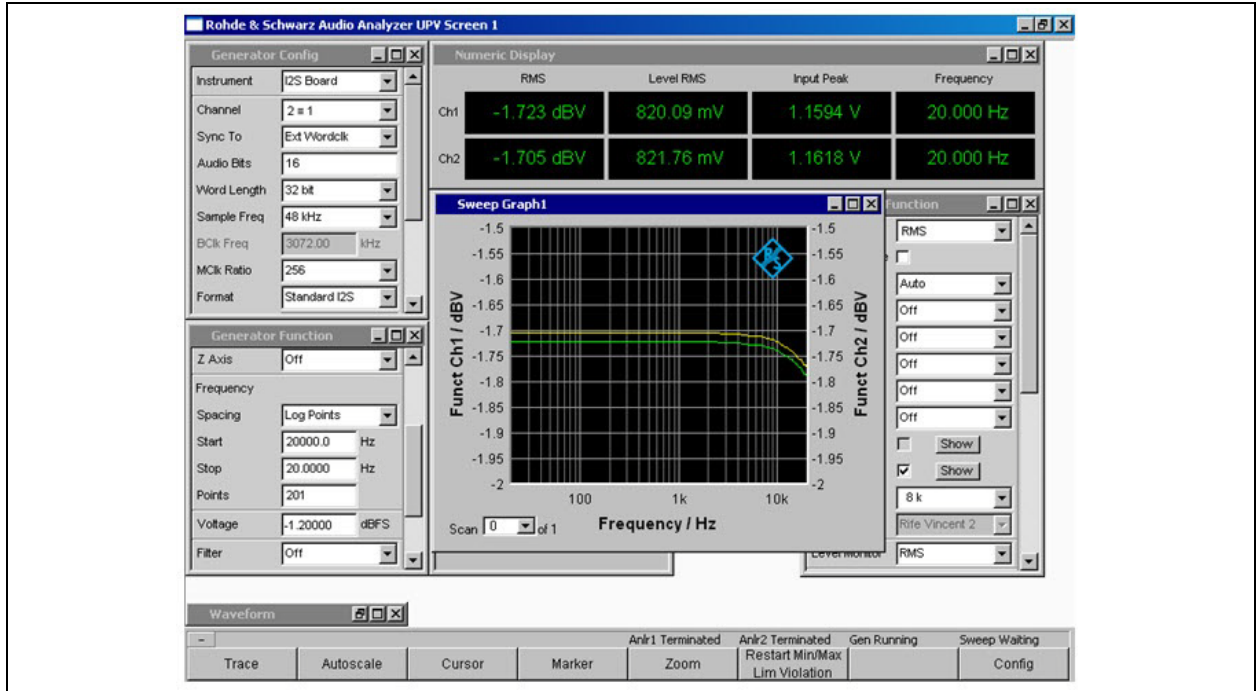
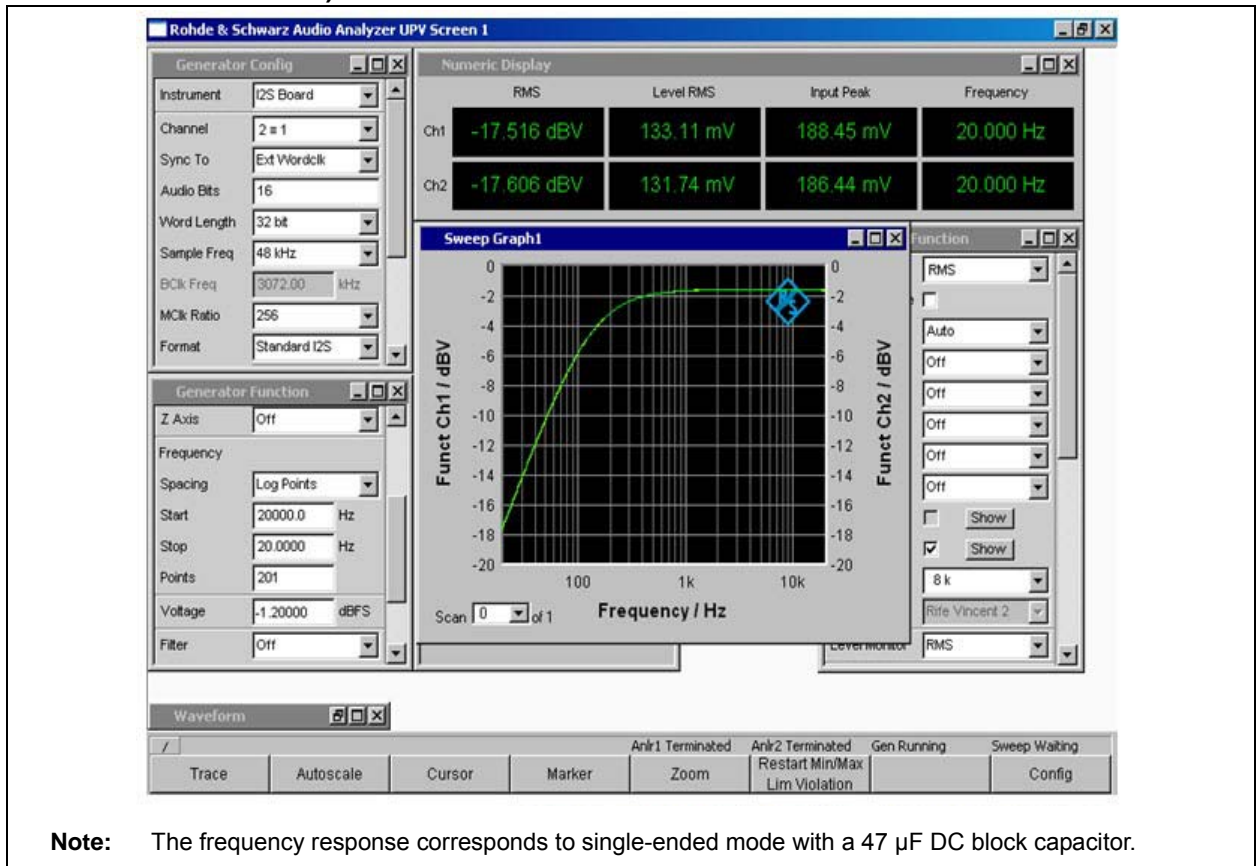


FIGURE 2-6: CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



## 2.3 Auxiliary Port

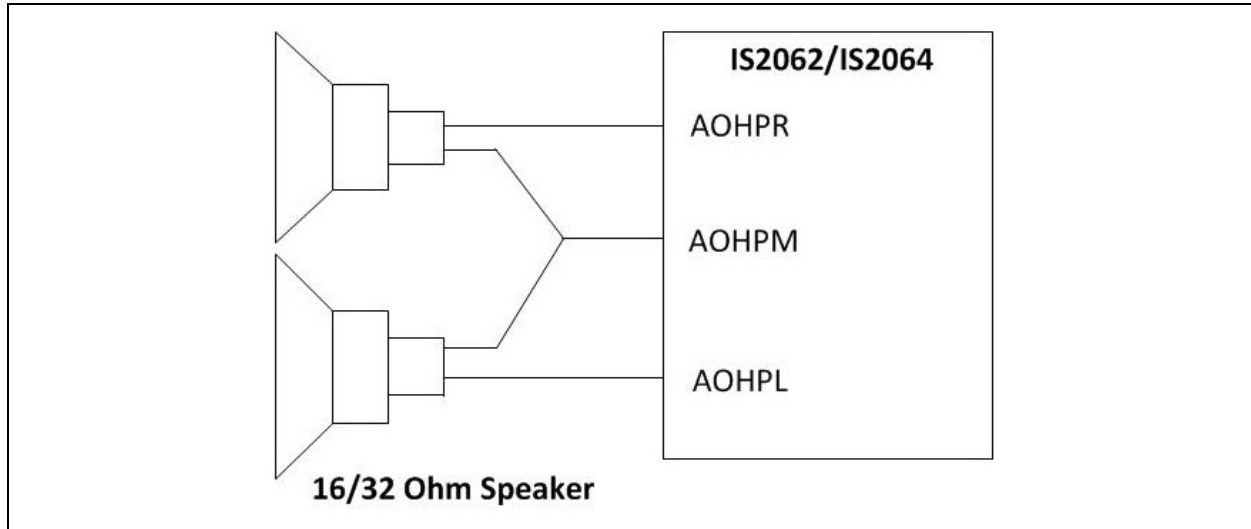
The IS2062/64 SoC supports one analog (line-in) signal from external audio source. The analog (line-in) signal can be processed by the DSP to generate different sound effects, multi-band dynamic range compression and audio widening, which can be setup by using the DSP tool.

## 2.4 Analog Speaker Output

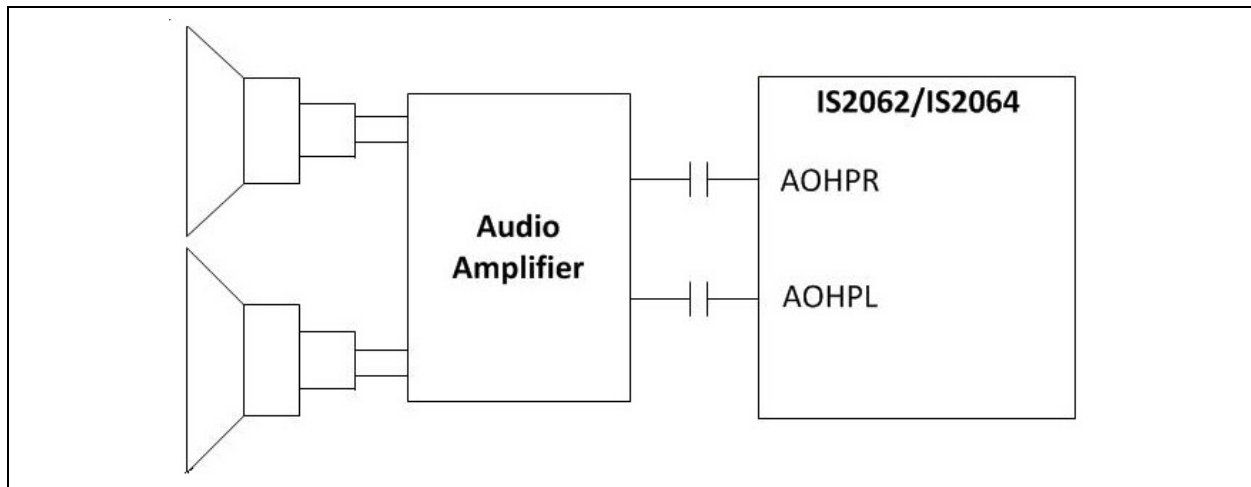
The IS2062/64 SoC supports the following speaker output modes:

- Capless mode — Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. [Figure 2-7](#) illustrates the analog speaker output Capless mode.
- Single-ended mode — Used for driving an external audio amplifier where a DC blocking capacitor is required. [Figure 2-8](#) illustrates the analog speaker output Single-Ended mode.

**FIGURE 2-7: ANALOG SPEAKER OUTPUT CAPLESS MODE**



**FIGURE 2-8: ANALOG SPEAKER OUTPUT SINGLE-ENDED MODE**



## 3.0 TRANSCIVER

The IS2062/64 SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock to synchronize with another device.

### 3.1 Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm. This is applied for Class 2 or Class 3 radios without an external RF PA.

The transmitter directly performs IQ conversion to minimize the frequency drift.

### 3.2 Receiver

The low-noise amplifier (LNA) operates with TR-combined mode for single port application. It can save a pin on package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into digital signal for de-modulator analysis. A channel filter has been integrated into receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability. The image rejection filter is used to reject image frequency for low-IF architecture. This filter for low-IF architecture is intended to reduce external Band Pass Filter (BPF) component for super heterodyne architecture.

Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

### 3.3 Synthesizer

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside, with a tunable internal LC tank that can reduce variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for synthesizer.

### 3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specification.

For Bluetooth 2.0 and above specifications, EDR has been introduced to provide data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the

payload part of EDR packets represents 2-bit or 3-bit. This is achieved by using two different modulations,  $\pi/4$  DQPSK and 8 DPSK.

### 3.5 Adaptive Frequency Hopping (AFH)

The IS2062/64 SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose the clear channel for transceiver Bluetooth signal.

NOTES:



## 4.0 MICROCONTROLLER

A microcontroller is built into an SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies where the firmware can dynamically adjust the trade-off between the computing power and the power consumption. In ROM version, the MCU firmware is hard-wired to minimize power consumption and to save the external Flash cost.

### 4.1 Memory

There are sufficient ROM and RAM to fulfill the requirement of processor, in which a synchronous single port RAM interface is used. The register bank, dedicated single port memory and Flash memory are connected to the processor bus. The processor coordinates all the link control procedures and data movement using a set of pointer registers.

### 4.2 External Reset

The IS2062/64 SoC provides a watchdog timer (WDT) to Reset the SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action can also be driven by an

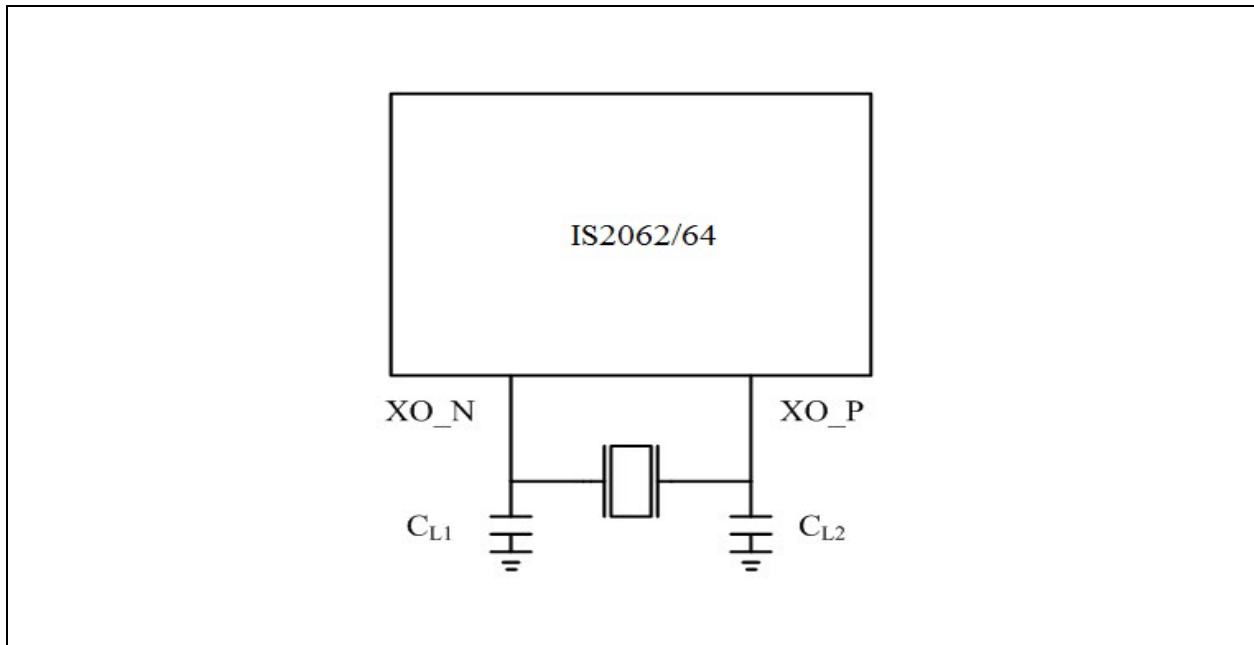
external Reset signal which is used to control the device externally by forcing it into a POR state. The RST\_N signal input is active-low and no connection is required in most of the applications.

### 4.3 Reference Clock

The IS2062/64 SoC is composed of an integrated crystal oscillation function that uses a 16 MHz,  $\pm 10$  ppm external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent loading capacitance in mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors ( $C_{trim}$ ).

The value of trimming capacitance is 200 fF ( $200 \times 10^{-15}$  F) per LSB at 5-bit word and the overall adjustable clock frequency is  $\pm 50$  kHz (based on crystal with load capacitance,  $C_L$  spec = 9 pF). Figure 4-1 illustrates the crystal connection of the IS2062/64 SoC with two capacitors.

**FIGURE 4-1: CRYSTAL CONNECTION**



NOTES:

## 5.0 POWER MANAGEMENT UNIT

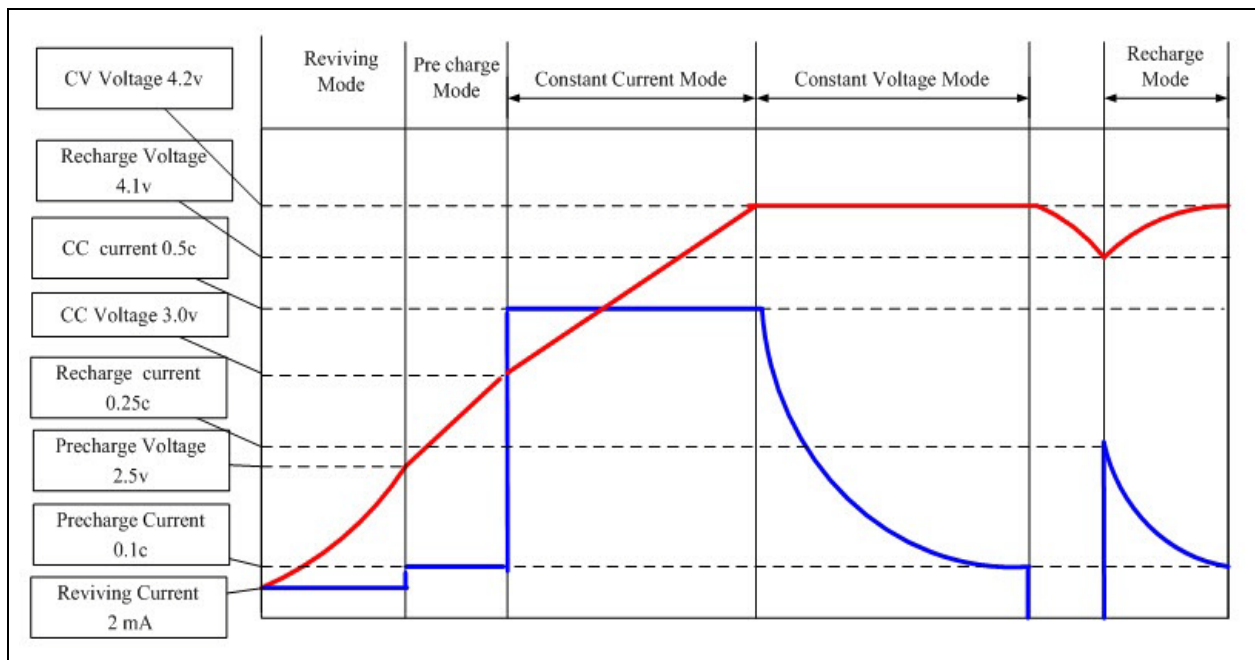
The IS2062/64 SoC has an integrated Power Management Unit (PMU). The main features of the PMU are a lithium-ion and lithium-polymer battery charger and voltage regulation. A power switch is used to switch over the power source between a battery and an adaptor. The PMU also provides current for driving LEDs.

## 5.1 Charging a Battery

The IS2062/64 SoC has a built-in battery charger which is optimized for lithium-ion and lithium-polymer batteries. The charger includes a current sensor for charging control, user programmable current regulator and high accuracy voltage regulator.

The charging current parameters are configured by using the UI tool. Whenever an adaptor is plugged-in, the charging circuit become activated. Reviving, pre-charging, constant current and constant voltage modes and re-charging functions are included. The maximum charging current is 350 mA. [Figure 5-1](#) illustrates the charging curve of a battery.

**FIGURE 5-1: BATTERY CHARGING CURVE**



## 5.2 Voltage Monitoring

A 10-bit, successive approximation ADC (SAR ADC) provides a dedicated channel for voltage level detection. The warning level can be programmed by using the UI tool. The ADC provides a granular resolution to enable the MCU to take control over the charging process.

## 5.3 LDO

A built-in Low-Dropout Regulator (LDO) is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control the power on/off procedure. The built-in programmable LDOs provide power for codec and digital I/O pads. Also, it is used to buffer the high input voltage from battery or adaptor. This LDO requires 1  $\mu$ F bypass capacitor.

## 5.4 Switching Regulator

The built-in programmable output voltage regulator can convert the battery voltage to RF and baseband core power supply. This converter has a high conversion efficiency and a fast transient response.

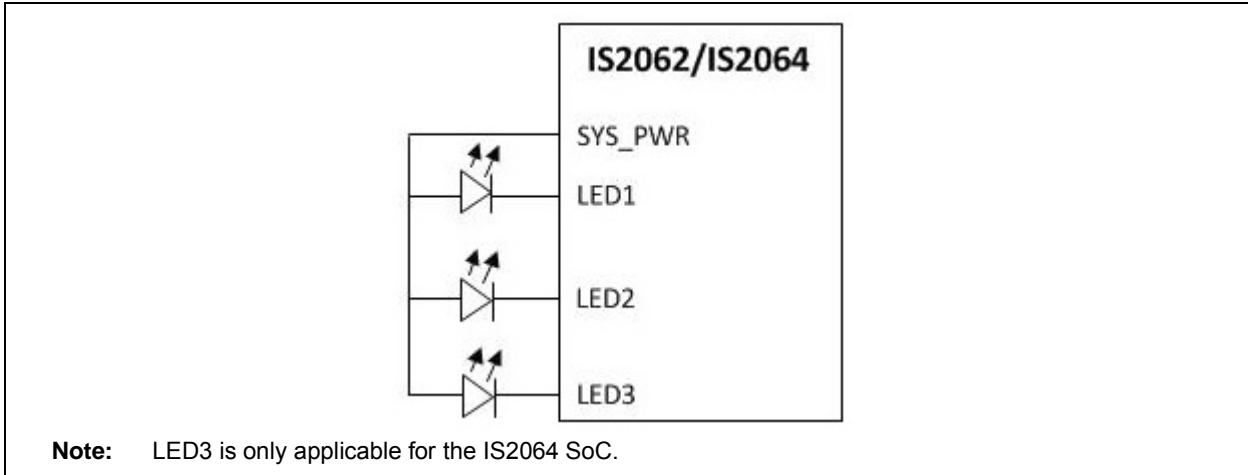
## 5.5 LED Driver

The IS2062 SoC has two LED drivers and the IS2064 SoC has three LED drivers. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED can be connected directly to the IS2062/64 SoC. The LED settings can be configured using the UI tool.

[Figure 5-2](#) illustrates the LED driver details.

# IS2062/64

FIGURE 5-2: LED DRIVER



## 5.6 Under Voltage Protection

When the SYS\_PWR pin voltage drops below 2.9V, the system will shut-down automatically.

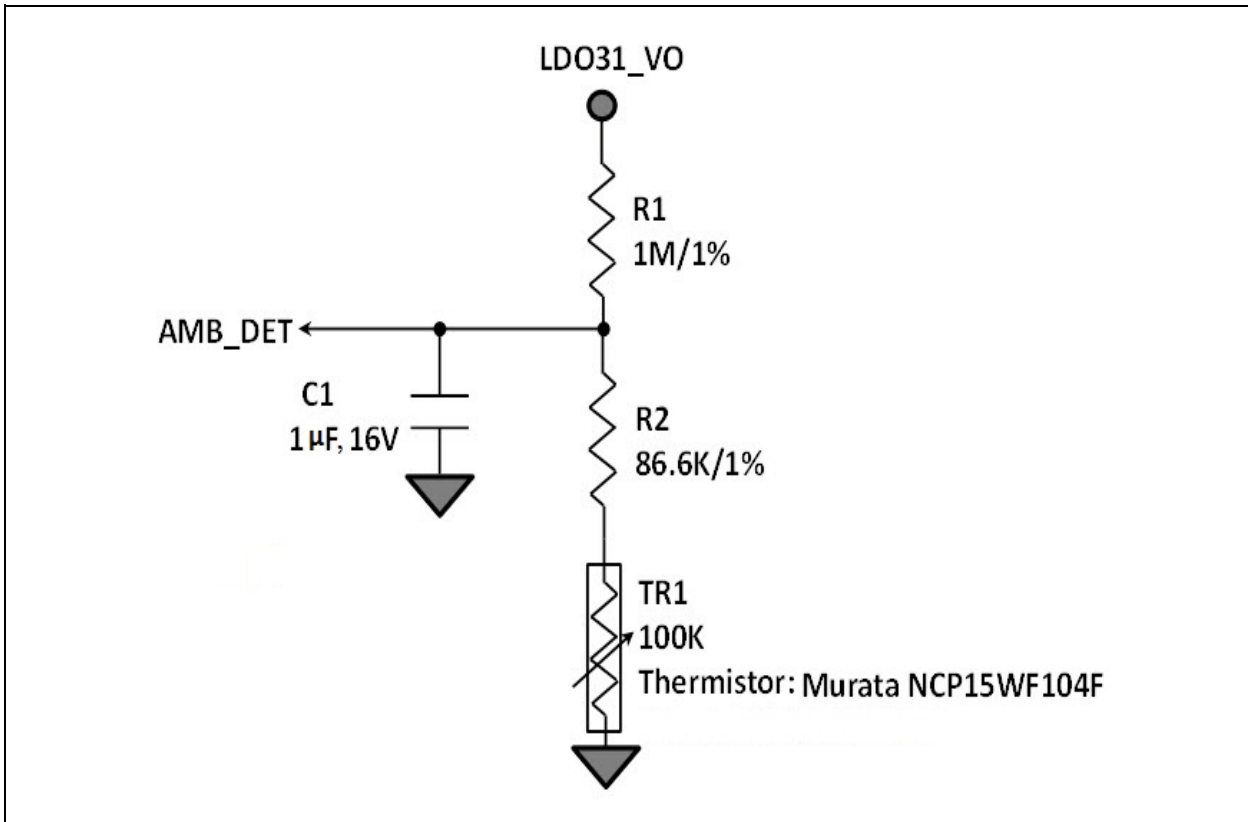
## 5.7 Ambient Detection

The IS2062/64 SoC has a built-in ADC for charger thermal protection.

Figure 5-3 illustrates the suggested circuit and thermistor, Murata NCP15WF104F. The charger thermal protection can avoid battery charge in restricted temperature range. The upper and lower limits for temperature values are configured by using the UI tool.

**Note:** Thermistor should be placed close to the battery in the user application for accurate temperature measurements and to enable thermal shutdown feature.

FIGURE 5-3: AMBIENT DETECTION



## 6.0 APPLICATION INFORMATION

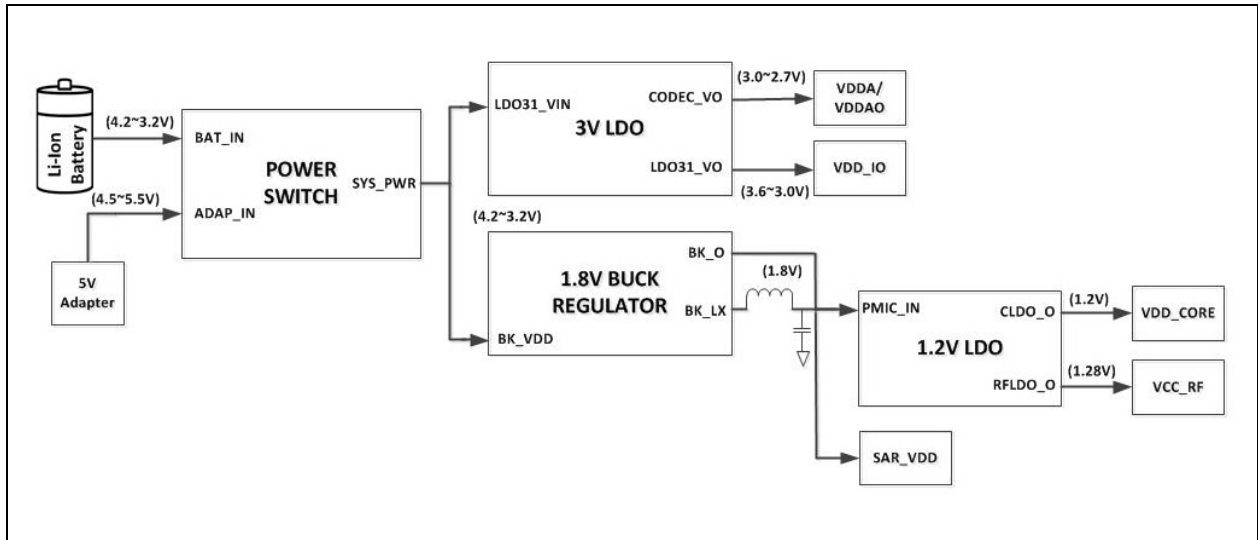
### 6.1 Power Supply

Figure 6-1 illustrates the connection from the BAT\_IN pin to any other voltage supply pins of the IS2062/64 SoC.

The IS2062/64 SoC is powered through the BAT\_IN input pin. If battery is not connected, an external power supply must be provided as an input to the ADAP\_IN pin.

**Note:** When external power supply is connected to the ADAP\_IN pin of the IS2062/64 SoC, the BAT\_IN pin can be left open if battery is not connected.

**FIGURE 6-1: POWER TREE DIAGRAM**

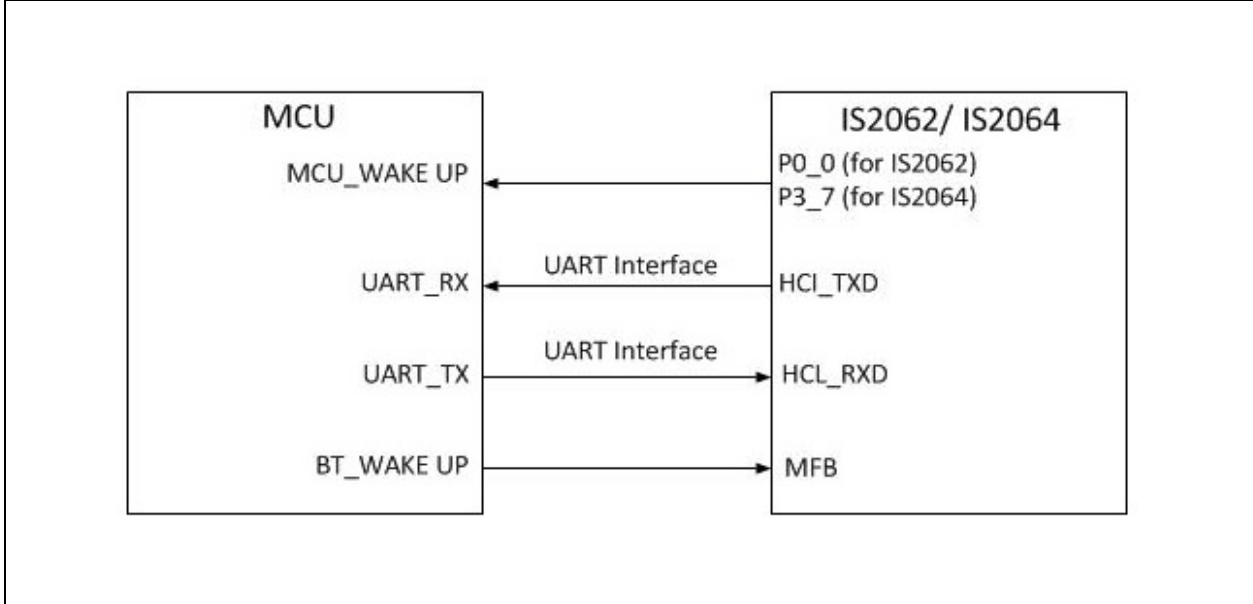


# IS2062/64

## 6.2 Host MCU Interface

Figure 6-2 illustrates the UART interface between the IS2062/64 SoC and MCU.

**FIGURE 6-2: HOST MCU INTERFACE OVER UART**

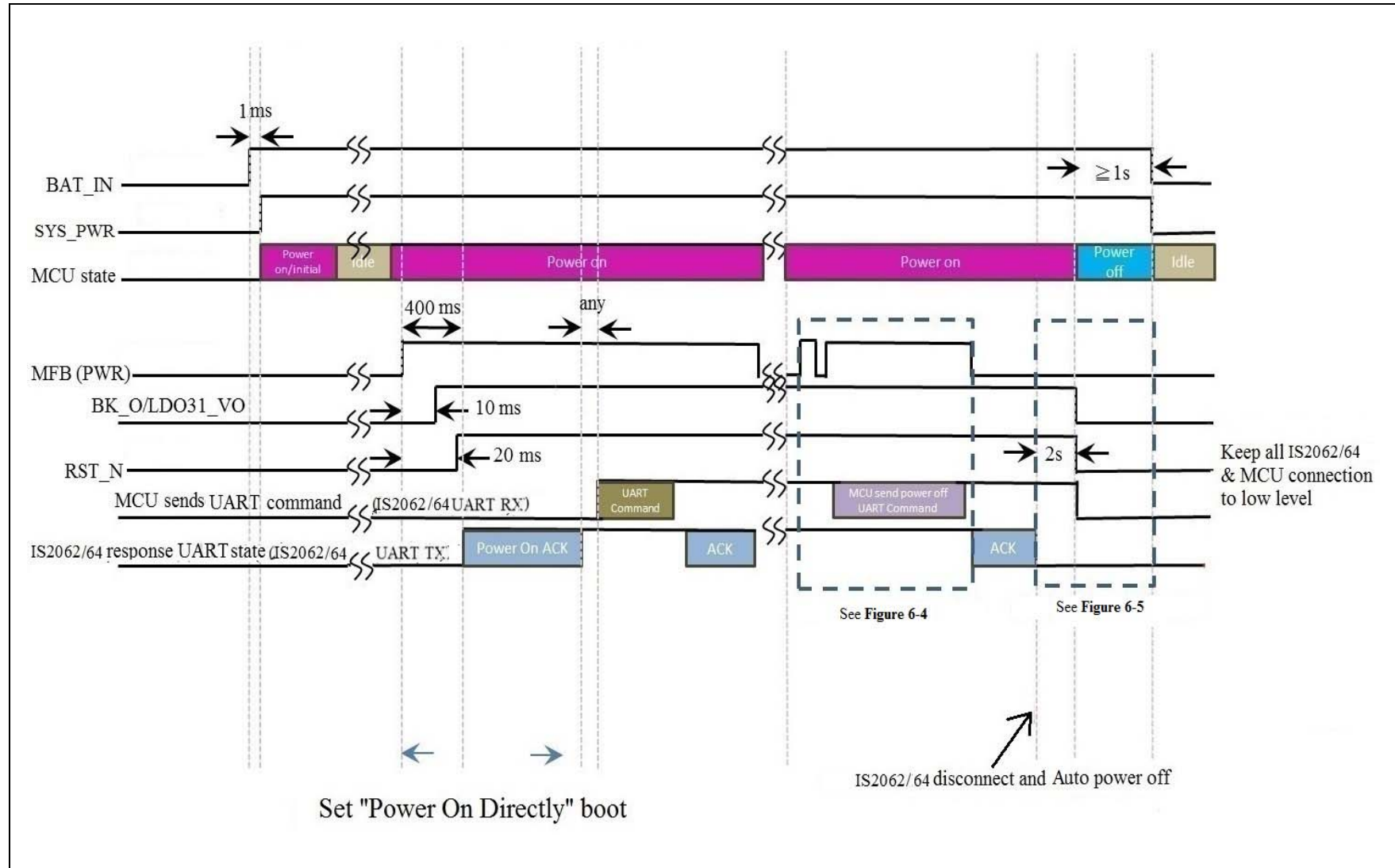


The MCU can control the IS2062/64 SoC over the UART interface and wakeup the SoC using the MFB pins, P0\_0 (IS2062) and P3\_7 (IS2064).

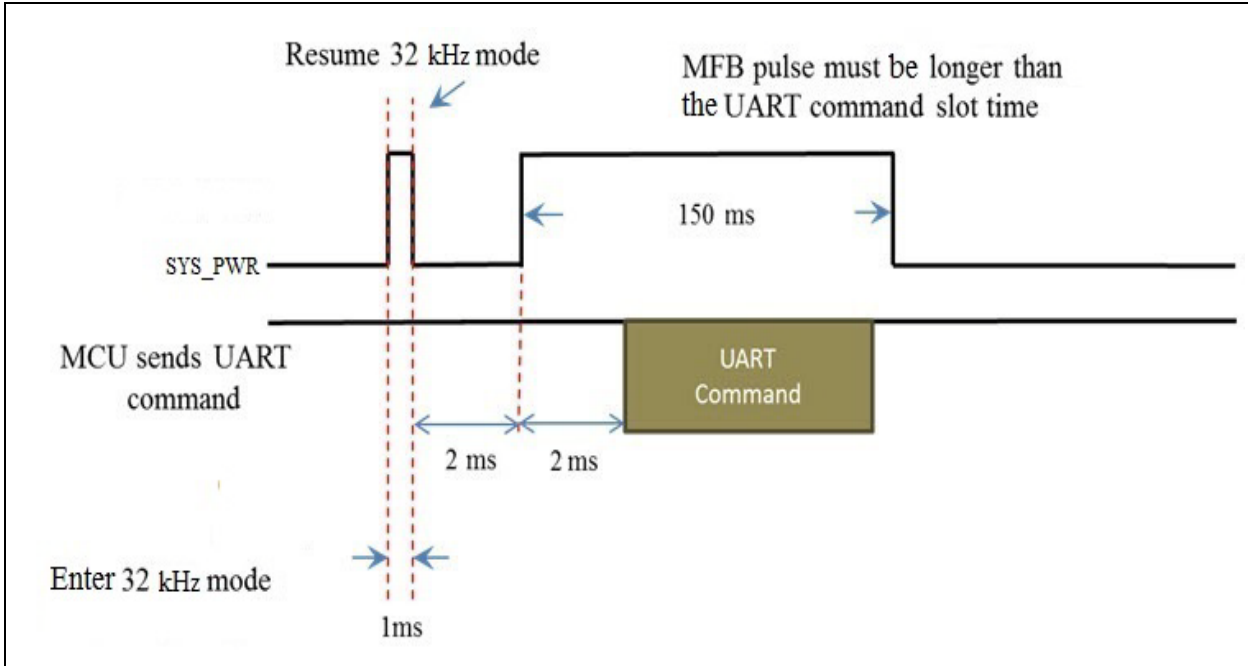
Refer to the "UART\_CommandSet" document for a list of functions the IS2062/64 SoC supports and how to use the UI tool to set up the system using the UART command, which is available for download from the Microchip web site at: [www.microchip.com/IS2062](http://www.microchip.com/IS2062) and [www.microchip.com/IS2064](http://www.microchip.com/IS2064).

Figure 6-3 through Figure 6-8 illustrate the various UART control signal timing sequences.

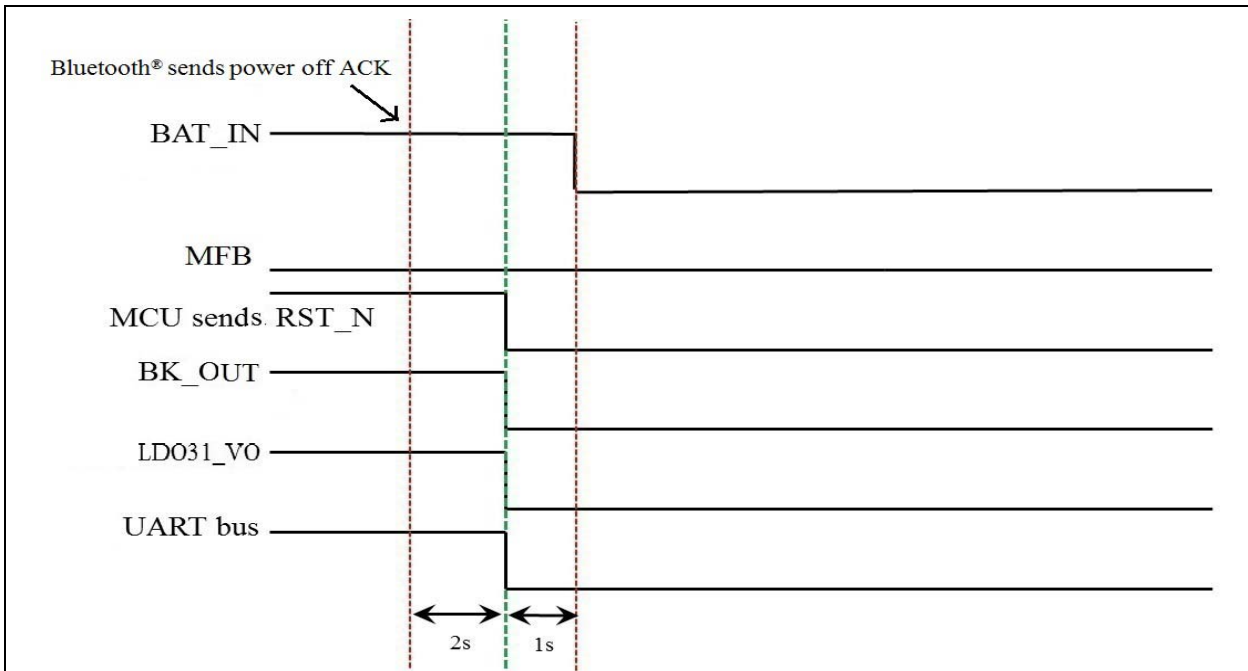
**FIGURE 6-3: POWER ON/OFF SEQUENCE**



**FIGURE 6-4: TIMING SEQUENCE OF RX INDICATION AFTER POWER ON**



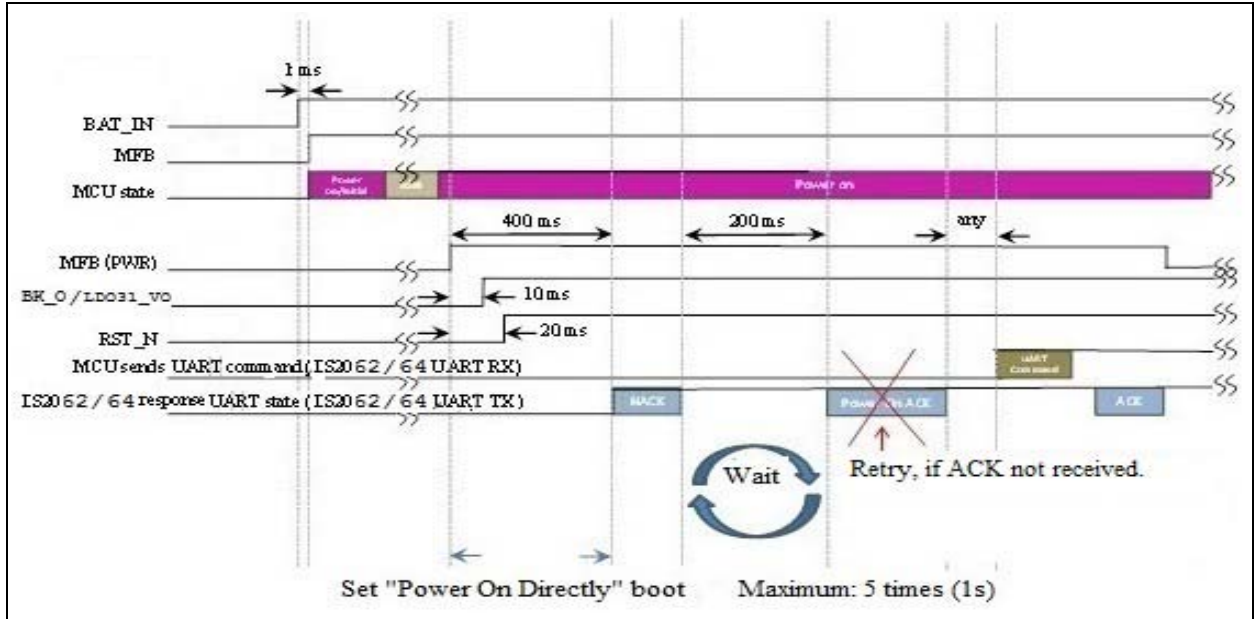
**FIGURE 6-5: TIMING SEQUENCE OF POWER OFF**



- Note 1:** EEPROM clock = 100 kHz.
- 2:** For a byte write,  $0.01 \text{ ms} \times 32 \text{ clock} \times 2 = 640 \mu\text{s}$ .
- 3:** It is recommended to have ramp-down time more than  $640 \mu\text{s}$  during power-off sequence to ensure safe operation of the device.



**FIGURE 6-6: TIMING SEQUENCE OF POWER ON (NACK)**



**FIGURE 6-7: RESET TIMING SEQUENCE IN CASE OF NO RESPONSE FROM SOC TO HOST MCU**

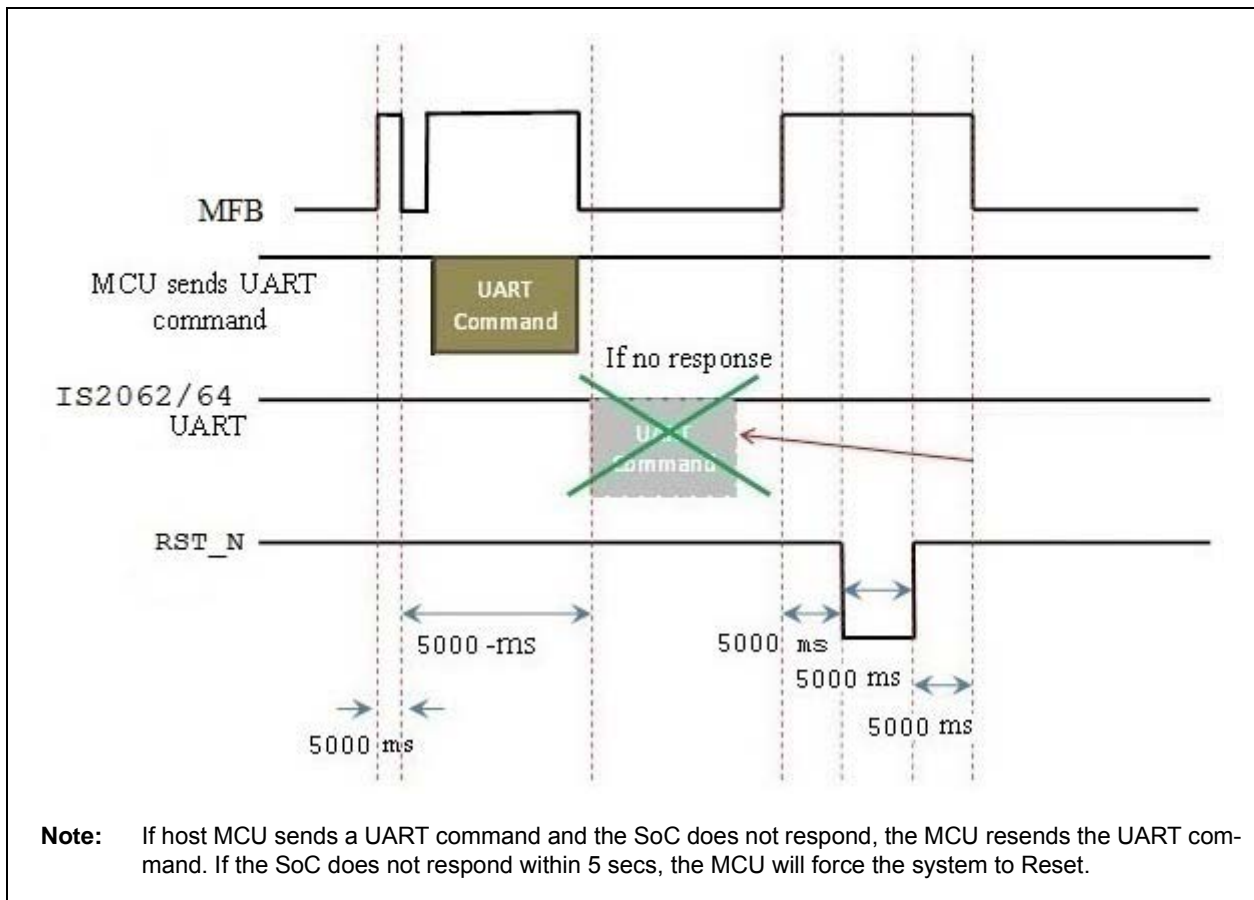
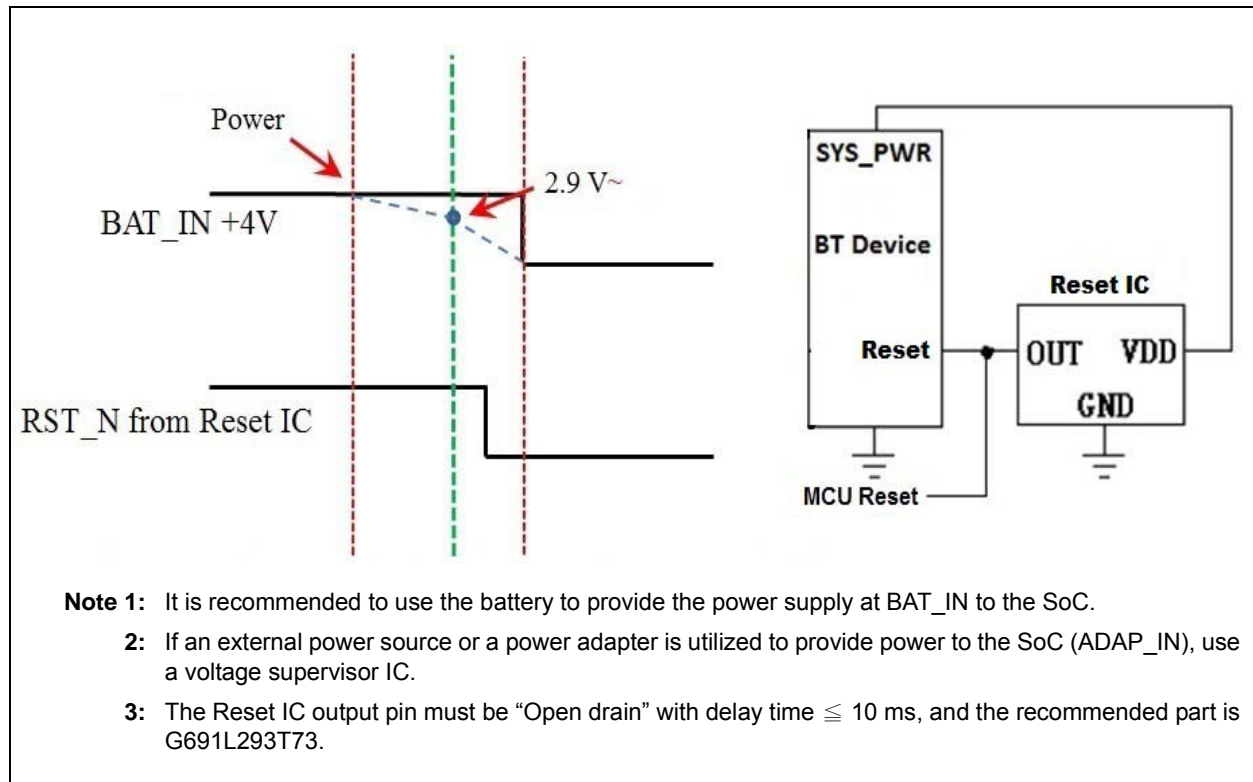


FIGURE 6-8: TIMING SEQUENCE OF POWER DROP PROTECTION



- Note 1:** It is recommended to use the battery to provide the power supply at BAT\_IN to the SoC.
- 2:** If an external power source or a power adapter is utilized to provide power to the SoC (ADAP\_IN), use a voltage supervisor IC.
- 3:** The Reset IC output pin must be "Open drain" with delay time  $\leq 10$  ms, and the recommended part is G691L293T73.

### 6.3 Configuring and Programming

Configuration and firmware programming modes are entered according to the system configuration I/O pins. Table 6-1 provides the system configuration settings. The P2\_0, P2\_4 and EAN pins have internal pull ups.

**TABLE 6-1: SYSTEM CONFIGURATION SETTINGS**

| P2_0 | P2_4 | EAN                             | Operating Mode              |
|------|------|---------------------------------|-----------------------------|
| High | High | Flash code: Low; ROM code: High | APP mode (Normal operation) |
| Low  | High | Flash code: Low; ROM code: High | Test mode (Write EEPROM)    |
| Low  | Low  | High                            | Write Flash                 |

# IS2062/64

## 6.4 General Purpose I/O Pins

The IS2062 SoC provides 10 GPIOs and the IS2064 SoC provides 15 GPIOs, and these GPIOs can be configured using the UI tool. [Table 6-2](#) through [Table 6-5](#) provide the GPIO configuration details of the IS2062/64 SoC.

The MFB pin must be configured as the power on/off key and the remaining pins can be configured for any one of the default functions as provided in [Table 6-2](#) and [Table 6-3](#).

**TABLE 6-2: IS2062 I/O PIN CONFIGURATION**

| I/O Pin Name | Default Functions |
|--------------|-------------------|
| MFB          | Power on/off      |
| P0_2         | Play/Pause        |
| P2_7         | Volume Up         |
| P0_5         | Volume Down       |
| P0_1         | FWD               |
| P0_3         | REV               |

**TABLE 6-3: IS2064 I/O PIN CONFIGURATION**

| I/O Pin Name | Default Functions |
|--------------|-------------------|
| MFB          | Power on/off      |
| P0_2         | Play/Pause        |
| P2_7         | Volume Up         |
| P0_5         | Volume Down       |
| P3_3         | FWD               |
| P3_1         | REV               |

Some pins can be configured to indicate or control the external devices. The most popular applications are NFC for easy pairing and Buzzer for indication and external audio amplifier for loud speaker.

**TABLE 6-4: IS2062 I/O PIN (FOR ADDITIONAL FUNCTIONS)**

| I/O Configurable Features | Functions           |
|---------------------------|---------------------|
| P1_5                      | Slide switch        |
| P0_4                      | NFC detect          |
| P0_4 / P1_5               | External AMP enable |

**TABLE 6-5: IS2064 I/O PIN FOR ADDED FUNCTIONS**

| I/O Configurable Features | Functions           |
|---------------------------|---------------------|
| P1_5                      | Slide switch        |
| P0_4                      | NFC detect          |
| P0_4 / P1_5               | External AMP enable |

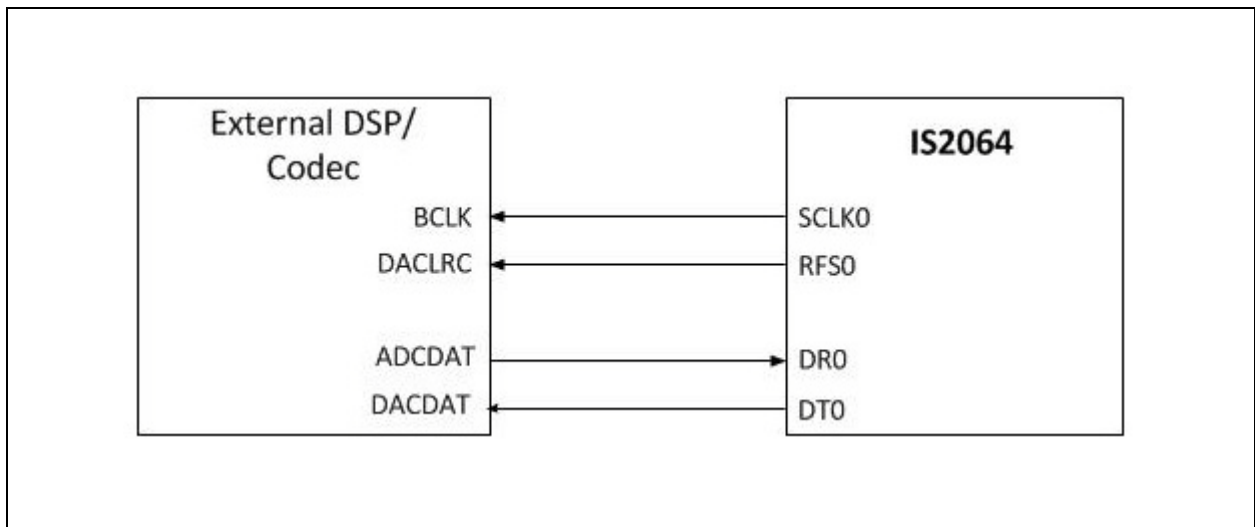
## 6.5 I<sup>2</sup>S Mode Application

The IS2064 SoC provides an I<sup>2</sup>S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I<sup>2</sup>S setting can be configured by using the UI and DSP tools. The external codec or DSP interfaces with these pins: SCLK0, RFS0, DR0, and DT0 (pin no. 3, 2, 1, and 4).

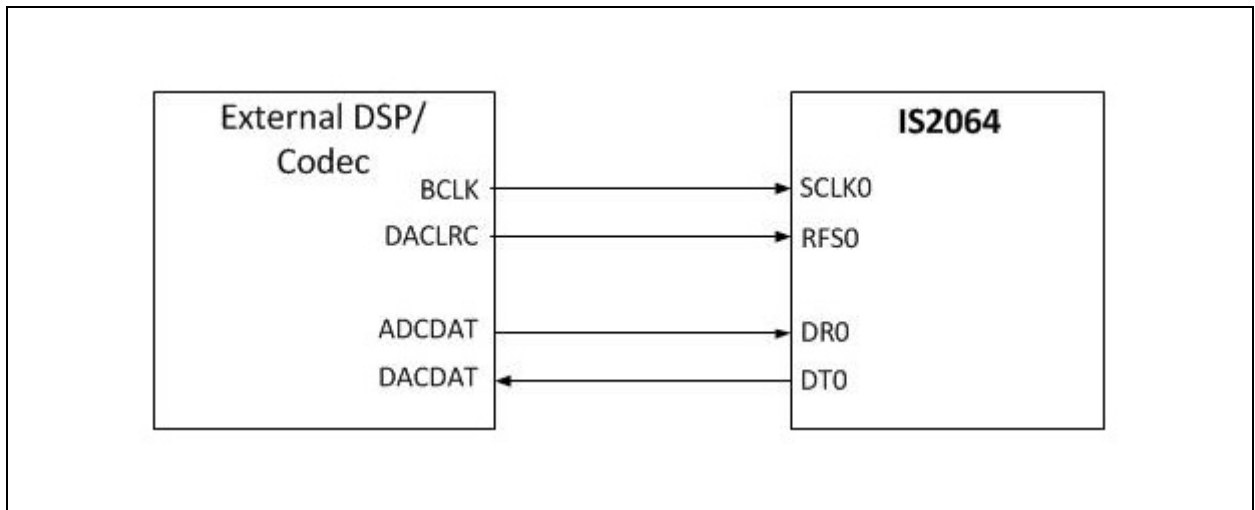
Figure 6-9 and Figure 6-10 illustrate the I<sup>2</sup>S signal connection between the IS2064 SoC and an external DSP. Use the DSP tool to configure the IS2064 SoC as Master/Slave.

For additional information on timing specifications, refer to [8.1 “Timing specifications”](#).

**FIGURE 6-9: IS2064 IN I<sup>2</sup>S MASTER MODE**



**FIGURE 6-10: IS2064 SLAVE MODE**



NOTES:

## 7.0 ANTENNA PLACEMENT RULE

Antenna placement affects the whole system performance of the Bluetooth integrated product. Antenna requires free space to radiate RF signals and it should not be surrounded by the GND plane.

Figure 7-1 illustrates a typical example of the antenna placement on the main application board with the GND plane.

**FIGURE 7-1: ANTENNA PLACEMENT EXAMPLES**

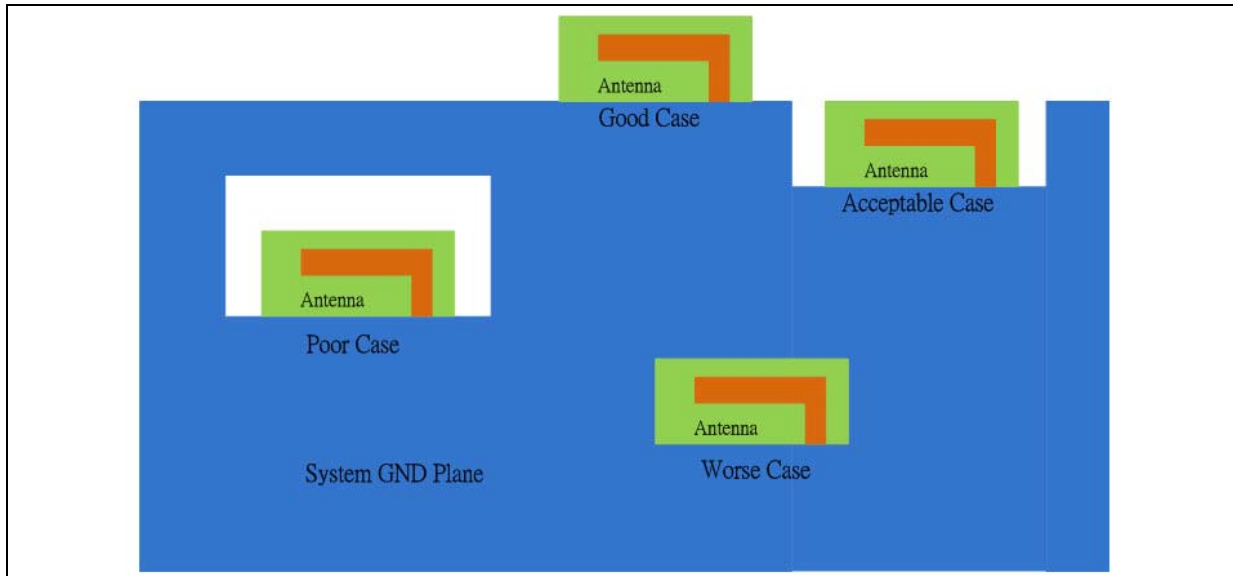
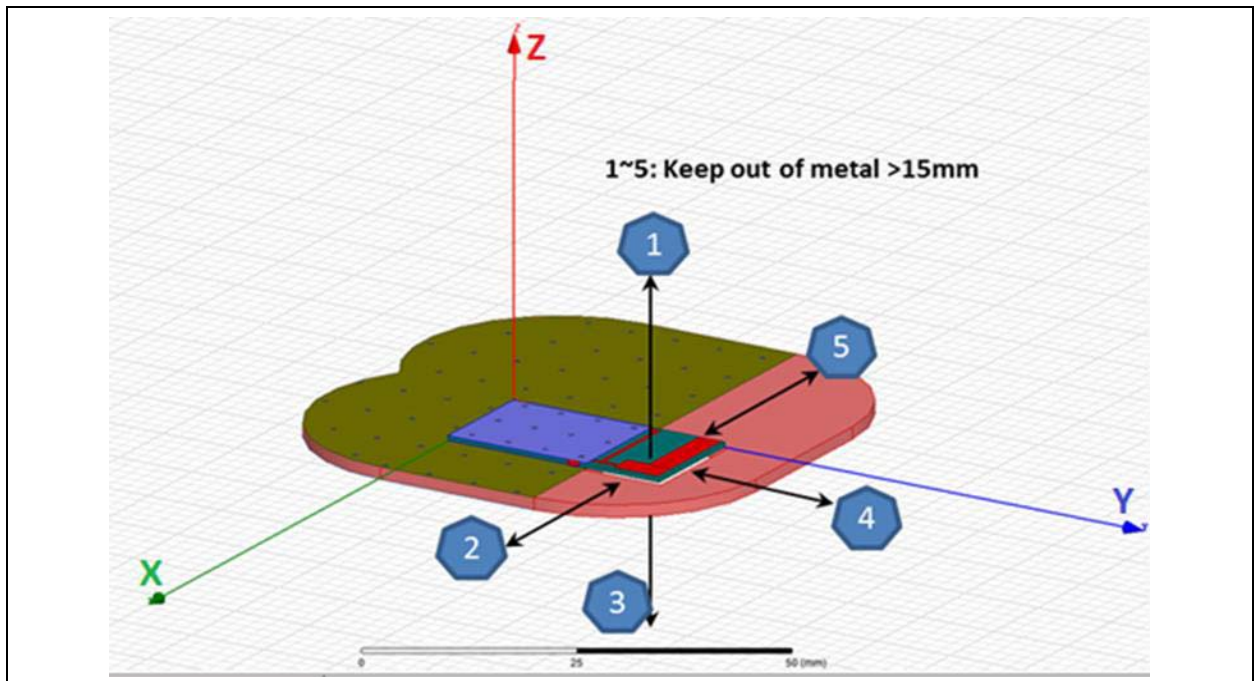


Figure 7-2 illustrates the keep-out area recommended for the antenna.

**FIGURE 7-2: KEEP OUT AREA RECOMMENDATION FOR ANTENNA**



For additional information on the antenna placement, refer to the specific antenna data sheet of the antenna manufacturer.

NOTES:



## 8.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS2062/64 stereo audio SoC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the IS2062/64 devices are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

### Absolute Maximum Ratings

|  |                 |
|--|-----------------|
| Ambient temperature under bias .....       | -20°C to +70°C  |
| Storage temperature .....                  | -65°C to +150°C |
| Digital core supply voltage VDD_CORE ..... | 0V to +1.35V    |
| RF supply voltage VCC_RF .....             | 0V to +1.35V    |
| SAR ADC supply voltage SAR_VDD .....       | 0V to +2.1V     |
| Codec supply voltage VDDA/VDDAO .....      | 0V to +3.3V     |
| I/O supply voltage VDD_IO .....            | 0V to +3.6V     |
| Buck supply voltage BK_VDD .....           | 0V to +4.3V     |
| Supply voltage LDO31_VIN .....             | 0V to +4.3V     |
| Battery input voltage BAT_IN .....         | 0V to +4.3V     |
| Adapter input voltage ADAP_IN .....        | 0V to +7V       |

**Note:** Stresses listed under “**Absolute Maximum Ratings**” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

# IS2062/64

Table 8-1 through Table 8-10 provide the recommended operating conditions and the electrical specifications of the IS2062/64 SoC.

**TABLE 8-1: RECOMMENDED OPERATING CONDITION**

| Symbol                 | Parameter                   | Min. | Typical | Max. | Unit |
|------------------------|-----------------------------|------|---------|------|------|
| VDD_CORE               | Digital core supply voltage | 1.14 | 1.2     | 1.26 | V    |
| VCC_RF                 | RF supply voltage           | 1.22 | 1.28    | 1.34 | V    |
| SAR_VDD                | SAR ADC supply voltage      | 1.62 | 1.8     | 1.98 | V    |
| VDDA/VDDAO             | Codec supply voltage        | 1.8  | 2.8     | 3.0  | V    |
| VDD_IO                 | I/O supply voltage          | 3.0  | 3.3     | —    | V    |
| BK_VDD                 | Buck supply voltage         | 3    | 3.8     | 4.25 | V    |
| LDO31_VIN              | Supply voltage              | 3    | 3.8     | 4.25 | V    |
| BAT_IN                 | Input voltage for battery   | 3.2  | 3.8     | 4.25 | V    |
| ADAP_IN                | Input voltage for adaptor   | 4.5  | 5       | 5.5  | V    |
| T <sub>OPERATION</sub> | Operation temperature       | -20  | +25     | +70  | °C   |

**Note:** The PMU output powers, BK\_O, CODEC\_VO, RFLDO\_O and CLDO\_O, can be programmed through the EEPROM parameters.

**TABLE 8-2: BUCK SWITCHING REGULATOR<sup>(2)</sup>**

| Parameter  | Min. | Typical | Max.  | Unit    |
|--|------|---------|-------|---------|
| Input Voltage  | 3.0  | 3.8     | 4.25  | V       |
| Output Voltage ( $I_{load} = 70\text{ mA}$ , $V_{in} = 4\text{V}$ )        | 1.7  | 1.8     | 2.05  | V       |
| Output Voltage Accuracy  | —    | ±5      | —     | %       |
| Output Voltage Adjustable Step   | —    | 50      | —     | mV/Step |
| Output Adjustment Range  | -0.1 | —       | +0.25 | V       |
| Average Load Current ( $I_{LOAD}$ )  | 120  | —       | —     | mA      |
| Conversion efficiency (BAT = 3.8V, $I_{load} = 50\text{ mA}$ )<br>(Note 2) | —    | 88      | —     | %       |
| Quiescent Current (PFM)  | —    | —       | 40    | µA      |
| Output Current (peak)  | 200  | —       | —     | mA      |
| Shutdown Current   | —    | —       | <1    | µA      |

**Note 1:** Test condition: Temperature +25 °C and wired inductor 10 µH.

**2:** These parameters are characterized, but not tested in manufacturing.

**TABLE 8-3: LOW DROP REGULATOR<sup>(1,2)</sup>**

| Parameter   | Min.     | Typical | Max. | Unit |
|---|----------|---------|------|------|
| Input Voltage   | 3.0      | 3.8     | 4.25 | V    |
| Output Voltage  | CODEC_VO | —       | 2.8  | V    |
|   | LDO31_VO | —       | 3.3  |      |
| Output Accuracy ( $V_{IN} = 3.7\text{V}$ , $I_{LOAD} = 100\text{ mA}$ , +27 °C) | —        | ±5      | —    | %    |
| Output current (average)  | —        | —       | 100  | mA   |
| Drop-out voltage<br>( $I_{load} = \text{maximum output current}$ )              | —        | —       | 300  | mV   |
| Quiescent Current<br>(excluding load, $I_{load} < 1\text{ mA}$ )                | —        | 45      | —    | µA   |
| Shutdown Current  | —        | —       | <1   | µA   |

**Note 1:** Test condition: Temperature +25 °C.

**2:** These parameters are characterized but not tested in manufacturing.

**TABLE 8-4: BATTERY CHARGER<sup>(1,3)</sup>**

| Parameter   | Min.  | Typical | Max. | Unit |
|---|---|---------|------|------|
| Input Voltage (ADAP_IN)   | 4.5   | 5.0     | 5.5  | V    |
| Supply current to charger only                                    | —   | 3       | 4.5  | mA   |
| Maximum Battery Fast Charge Current                               | Headroom > 0.7V<br>(ADAP_IN = 5V)                 | —       | 350  | mA   |
|   | Headroom = 0.3V~0.7V<br>(ADAP_IN = 4.5V) (Note 2) | —       | 175  | mA   |
| Trickle Charge Voltage Threshold                                  | —   | 3       | —    | V    |
| Battery Charge Termination Current,<br>(% of Fast Charge Current) | —   | 10      | —    | %    |

**Note 1:** Headroom =  $V_{ADAP\_IN} - V_{BAT}$ .

**2:** When  $V_{ADAP\_IN} - V_{BAT} > 2\text{V}$ , the maximum fast charge current is 175 mA for thermal protection.

**3:** These parameters are characterized but not tested in manufacturing.

# IS2062/64

**TABLE 8-5: LED DRIVER<sup>(1, 2)</sup>**

| Parameter                     | Min. | Typical | Max. | Unit |
|-------------------------------|------|---------|------|------|
| Open-drain Voltage            | —    | —       | 3.6  | V    |
| Programmable Current Range    | 0    | —       | 5.25 | mA   |
| Intensity Control             | —    | 16      | —    | step |
| Current Step                  | —    | 0.35    | —    | mA   |
| Power Down Open-drain Current | —    | —       | 1    | μA   |
| Shutdown Current              | —    | —       | 1    | μA   |

**Note 1:** Test condition: BK\_O = 1.8V with temperature +25 °C.

**2:** These parameters are characterized but not tested in manufacturing.

**TABLE 8-6: AUDIO CODEC DIGITAL TO ANALOG CONVERTER<sup>(4)</sup>**

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz

| Parameter (Condition)  | Min.       | Typical | Max. | Unit           |    |
|--|------------|---------|------|----------------|----|
| Output Sampling Rate   | —          | 128     | —    | f <sub>s</sub> |    |
| Resolution   | 16         | —       | 20   | Bit            |    |
| Output Sample Rate   | 8          | —       | 48   | kHz            |    |
| Signal to Noise Ratio ( <b>Note 1</b> )<br>(SNR @cap-less mode) for 48 kHz   | —          | 96      | —    | dB             |    |
| Signal to Noise Ratio ( <b>Note 1</b> )<br>(SNR @single-end mode) for 48 kHz | —          | 98      | —    | dB             |    |
| Digital Gain   | -54        | —       | 4.85 | dB             |    |
| Digital Gain Resolution  | —          | 2~6     | —    | dB             |    |
| Analog Gain  | -28        | —       | 3    | dB             |    |
| Analog Gain Resolution   | —          | 1       | —    | dB             |    |
| Output Voltage Full-scale Swing (AVDD = 2.8V)                                | 495        | 742.5   | —    | mV/rms         |    |
| Maximum Output Power (16 Ohm load)   | —          | 34.5    | —    | mW             |    |
| Maximum Output Power (32 Ohm load)   | —          | 17.2    | —    | mW             |    |
| Allowed Load   | Resistive  | —       | 16   | O.C. Ohm       |    |
|  | Capacitive | —       | —    | 500 pF         |    |
| THD+N (16 Ohm load) ( <b>Note 2</b> )  | —          | 0.05    | —    | %              |    |
| Signal to Noise Ratio (SNR @ 16 Ohm load) ( <b>Note 3</b> )                  | —          | —       | 98   | —              | dB |

**Note 1:** f<sub>in</sub>=1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load = 100 kOhm.

**2:** f<sub>in</sub> = 1 kHz, B/W = 20~20 kHz, A-weighted, -1dBFS signal, Load=16 Ohm.

**3:** f<sub>in</sub> = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 0.05%, 0dBFS signal, Load = 16 Ohm.

**4:** These parameters are characterized but not tested in manufacturing.

**TABLE 8-7: AUDIO CODEC ANALOG TO DIGITAL CONVERTER<sup>(2)</sup>**

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz

| Parameter (Condition)  | Min. | Typical | Max. | Unit   |
|--|------|---------|------|--------|
| Resolution   | —    | —       | 16   | Bit    |
| Output Sample Rate   | 8    | —       | 48   | kHz    |
| Signal to Noise Ratio (Note 1)<br>(SNR @MIC or Line-in mode) | —    | 92      | —    | dB     |
| Digital Gain   | -54  | —       | 4.85 | dB     |
| Digital Gain Resolution                                      | —    | 2~6     | —    | dB     |
| MIC Boost Gain   | —    | 20      | —    | dB     |
| Analog Gain  | —    | —       | 60   | dB     |
| Analog Gain Resolution                                       | —    | 2.0     | —    | dB     |
| Input full-scale at maximum gain (differential)              | —    | 4       | —    | mV/rms |
| Input full-scale at minimum gain (differential)              | —    | 800     | —    | mV/rms |
| 3 dB bandwidth   | —    | 20      | —    | kHz    |
| Microphone mode (input impedance)                            | —    | 24      | —    | kOhm   |
| THD+N (microphone input) at 30mVrms input                    | —    | 0.02    | —    | %      |

**Note 1:**  $f_{in}$ =1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 1%, 150 mVpp input.

**2:** These parameters are characterized but not tested in manufacturing.

**TABLE 8-8: TRANSMITTER SECTION FOR BDR AND EDR<sup>(1, 2)</sup>**

| Parameter               | Min. | Typical          | Max. | Bluetooth specification | Unit |
|-------------------------|------|------------------|------|-------------------------|------|
| Transmit power          | —    | 2 <sup>(3)</sup> | 4    | -6 to 4                 | dBm  |
| Relative transmit power | -4   | -1.8             | 1    | -4 to 1                 | dB   |

**Note 1:** The RF TX power is modulation value.

**2:** The RF Transmit power is calibrated during production using MP tool software and MT8852 Bluetooth Test equipment.

**3:** Test condition: VCC\_RF = 1.28V, temperature +25 °C.

**TABLE 8-9: RECEIVER SECTION FOR BDR AND EDR<sup>(1, 2)</sup>**

|                          | Modulation | Min. | Typical | Max. | Bluetooth specification | Unit |
|--------------------------|------------|------|---------|------|-------------------------|------|
| Sensitivity at 0.1% BER  | GFSK       | —    | -89     | —    | ≤-70                    | dBm  |
| Sensitivity at 0.01% BER | π/4 DQPSK  | —    | -90     | —    | ≤-70                    | dBm  |
|                          | 8 DPSK     | —    | -83     | —    | ≤-70                    | dBm  |

**Note 1:** Test condition: VCC\_RF = 1.28V, temperature +25 °C.

**2:** These parameters are characterized, but not tested in manufacturing.

**TABLE 8-10: SYSTEM CURRENT CONSUMPTION OF IS2062<sup>(1, 2)</sup>**

| System Status   | Typical | Max. | Unit |
|---|---------|------|------|
| System Off Mode   | —       | 10   | μA   |
| Stop Advertising (Samsung S5 (SM-G900I)/Android™ 4.4.2) |         |      |      |
| Standby Mode  | 0.57    | —    | mA   |
| Link Mode   | 0.5     | —    | mA   |
| ESCO Link   | 15.1    | —    | mA   |
| A2DP Link   | 14.3    | —    | mA   |
| Stop Advertising (iPhone® 6 / iOS 8.4)                  |         |      |      |
| Standby Mode  | 0.6     | —    | mA   |
| Link Mode   | 0.6     | —    | mA   |
| SCO Link  | 15.3    | —    | mA   |
| A2DP Link   | 15.4    | —    | mA   |

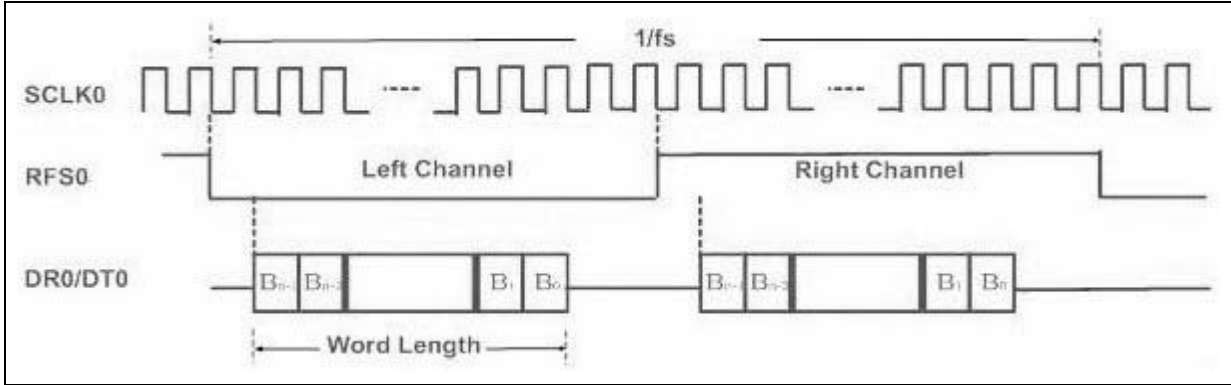
**Note 1:** Standby Mode: Power-on without Bluetooth link; Link Mode: With Bluetooth link in low-power mode.

**2:** Current consumption values are taken with the BM62 EVB as a test platform, BAT\_IN = 3.8V. Distance between smart phone and EVB is 30 cm. Speaker is without loading.

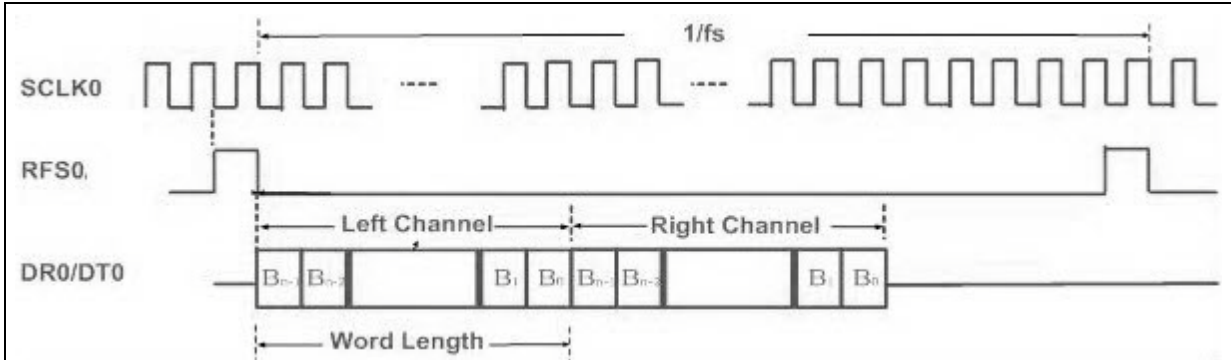
## 8.1 Timing specifications

Figure 8-1 and Figure 8-2 illustrate the clock and data timing specifications.

**FIGURE 8-1: TIMING FOR I<sup>2</sup>S MODES (MASTER/SLAVE)**



**FIGURE 8-2: TIMING FOR PCM MODES (MASTER/SLAVE)**



**Note 1:**  $f_s$ : 8, 16, 32, 44.1, 48, 88.2 and 96 kHz.

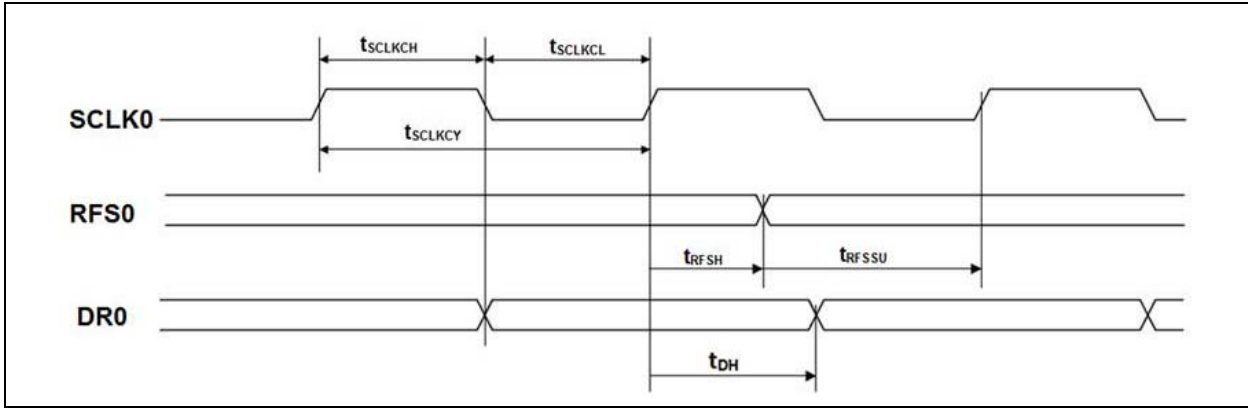
**Note 2:** SCLK0:  $64 \times f_s / 256 \times f_s$ .

**Note 3:** Word length: 16-bit and 24-bit.

# IS2062/64

Figure 8-3 illustrates the audio interface timing and Table 8-11 provides the audio interface timing specifications.

**FIGURE 8-3: AUDIO INTERFACE TIMING**



**TABLE 8-11: AUDIO INTERFACE TIMING SPECIFICATIONS**

| PARAMETER                             | SYMBOL       | MIN | TYP | MAX | UNIT |
|---------------------------------------|--------------|-----|-----|-----|------|
| SCLK0 Duty Ratio                      | $d_{SCLK}$   | —   | 50  | —   | %    |
| SCLK0 cycle time                      | $t_{SCLKCY}$ | 50  | —   | —   | ns   |
| SCLK0 pulse width high                | $t_{SCLKCH}$ | 20  | —   | —   | ns   |
| SCLK0 pulse width low                 | $t_{SCLKCL}$ | 20  | —   | —   | ns   |
| RFS0 set-up time to SCLK0 rising edge | $t_{RFSSU}$  | 10  | —   | —   | ns   |
| RFS0 hold time from SCLK0 rising edge | $t_{RFSH}$   | 10  | —   | —   | ns   |
| DR0 hold time from SCLK0 rising edge  | $t_{DH}$     | 10  | —   | —   | ns   |

**Note:** Test Conditions: Slave Mode,  $f_s = 48$  kHz, 24-bit data and SLK0 period =  $256 f_s$ .

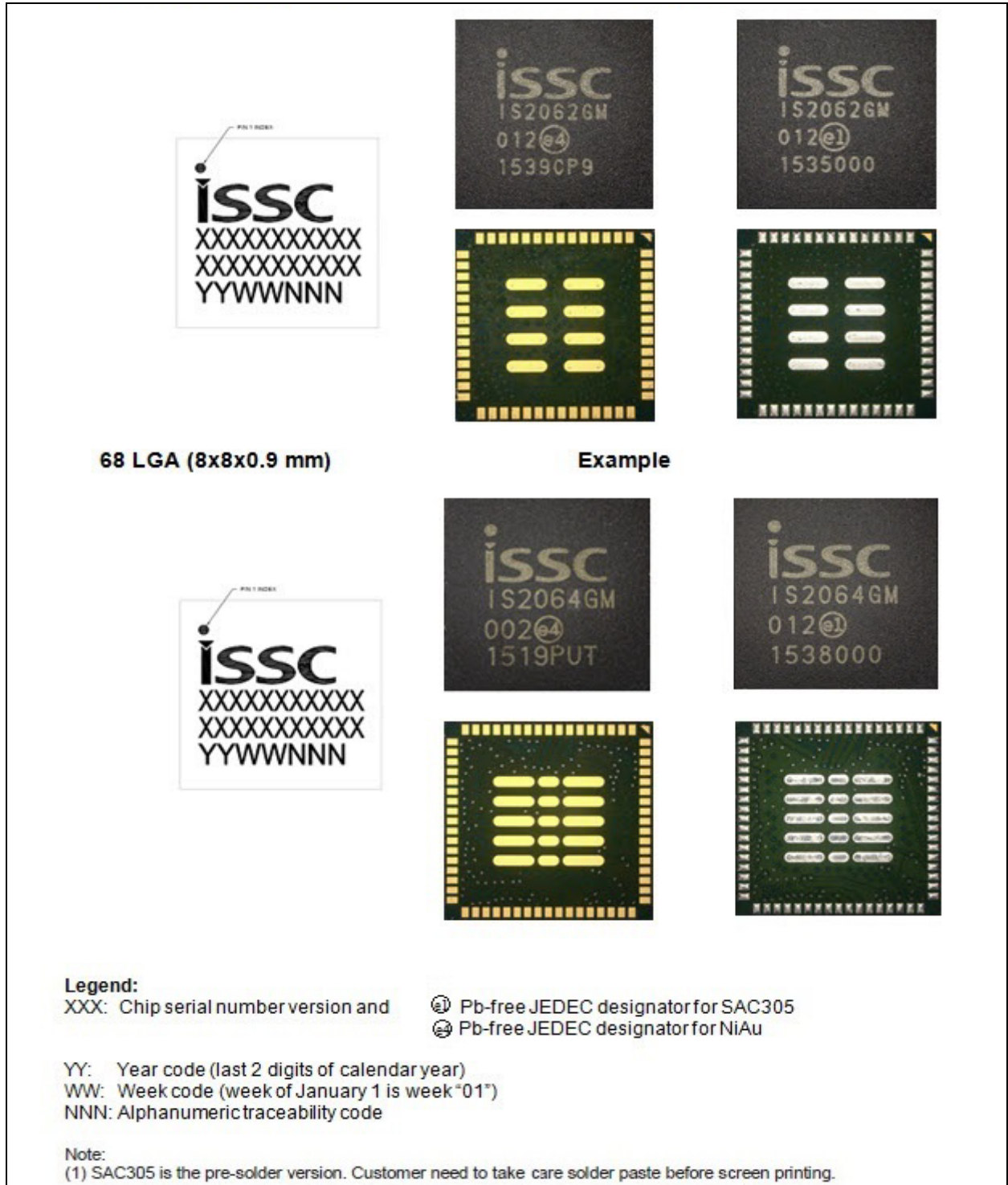


## 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information

Figure 9-1 illustrates the package marking information of the IS2062/64 SoC.

**FIGURE 9-1: PACKAGE MARKING INFORMATION**



## 9.2 Package Details

Figure 9-2 and Figure 9-3 illustrate the package details of the IS2062 SoC.

**FIGURE 9-2: IS2062 - NIAU PACKAGE DETAILS**

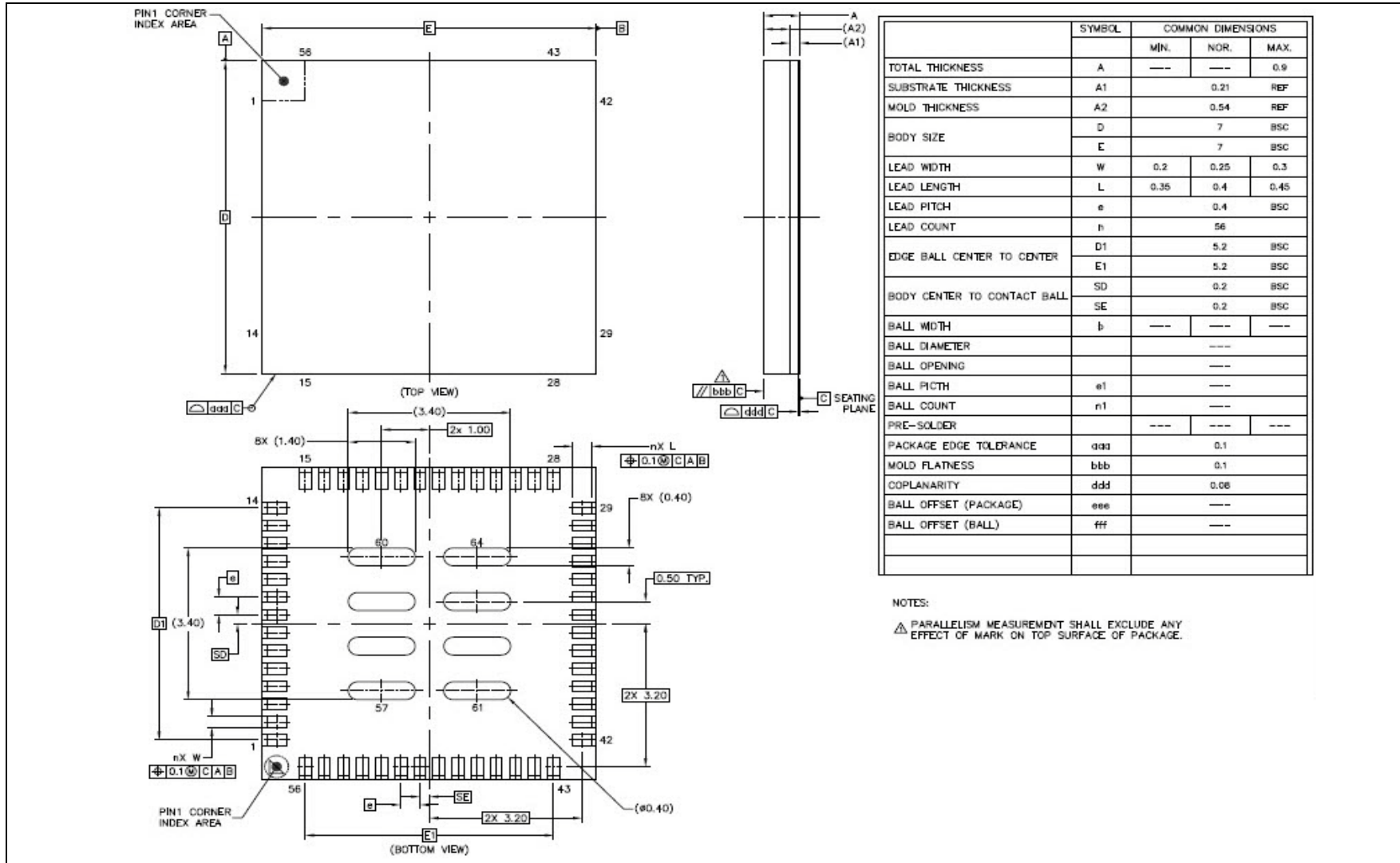
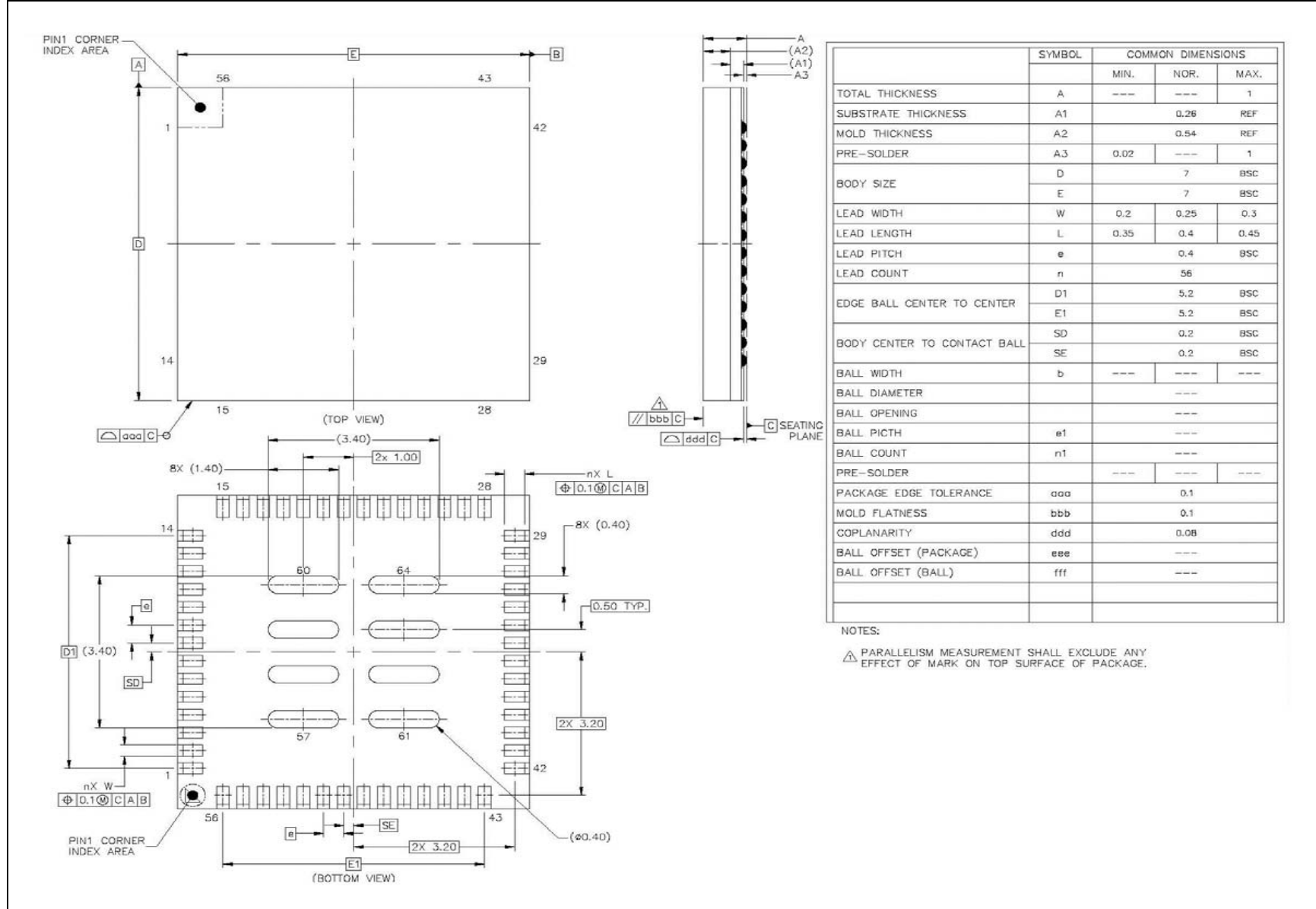


FIGURE 9-3: IS2062 - SAC305 PACKAGE DETAILS

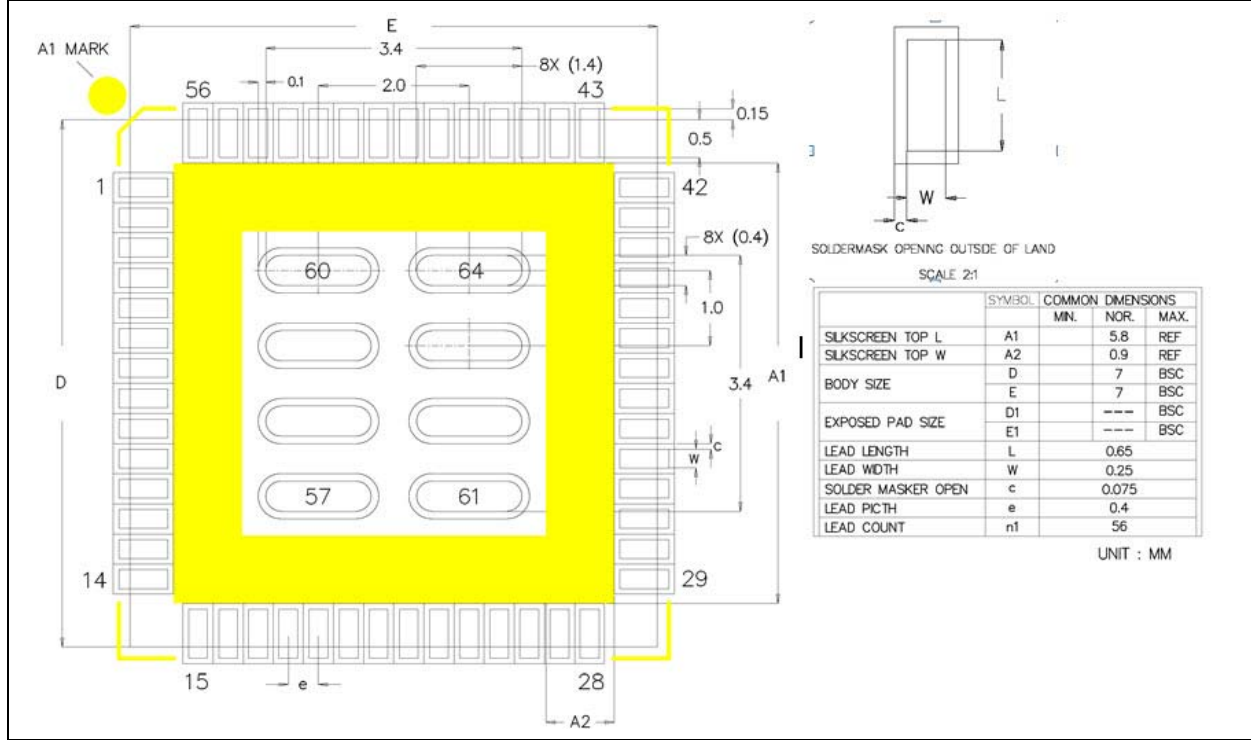


# IS2062/64

## 9.3 Footprint Dimensions

Figure 9-4 illustrates the footprint dimensions of the IS2062 SoC.

**FIGURE 9-4: IS2062 FOOTPRINT DIMENSIONS**



### 9.4 Package Details

Figure 9-5 and Figure 9-6 illustrate the package details of the IS2064 SoC.

**FIGURE 9-5: IS2064 -NIAU PACKAGE DETAILS**

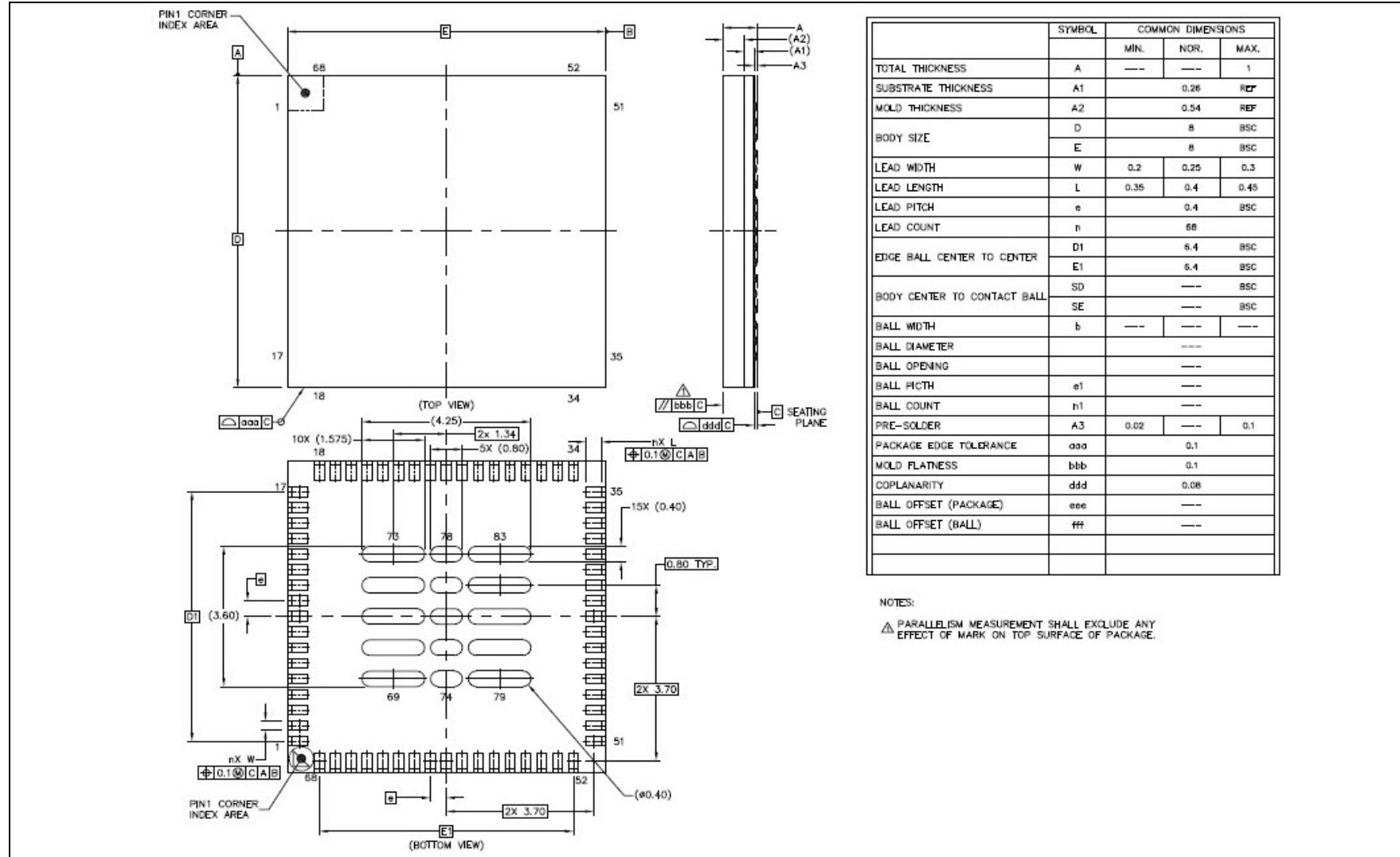
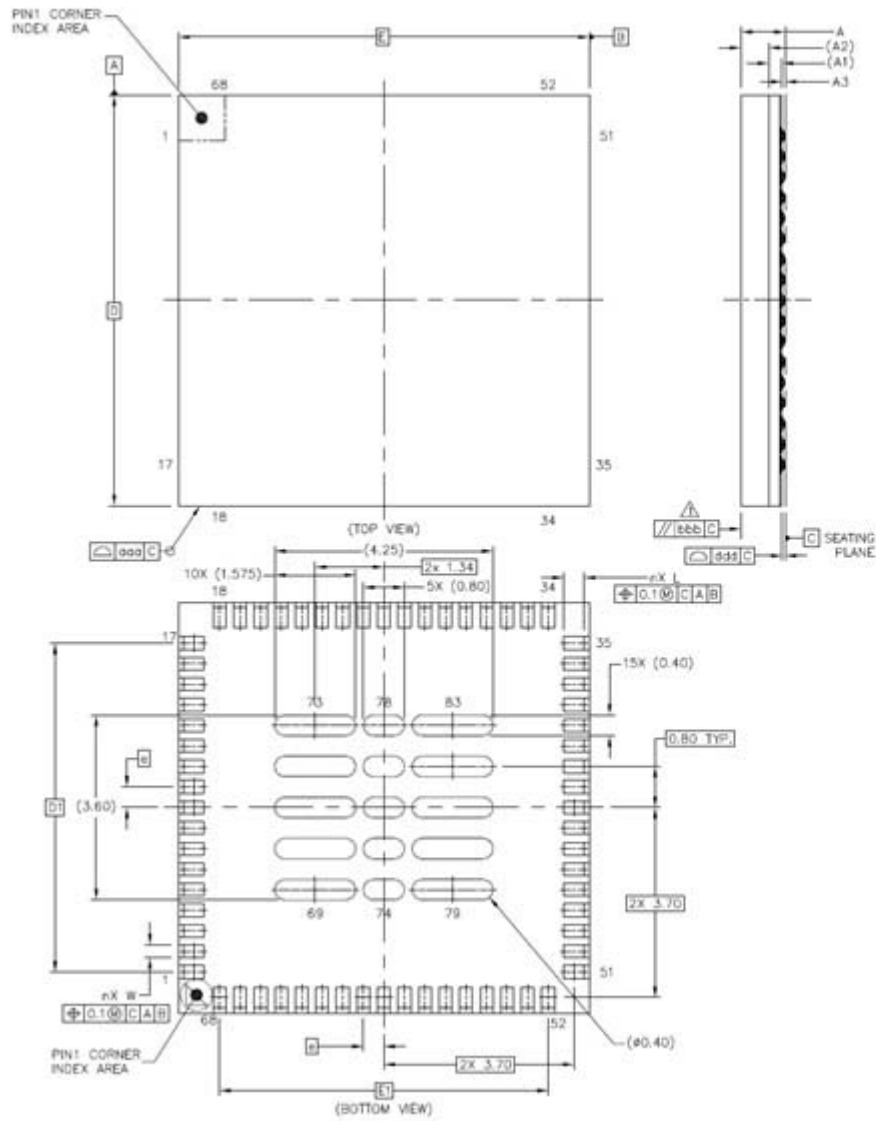


FIGURE 9-6: IS2064 - SAC305 PACKAGE DETAILS



|                             | SYMBOL | COMMON DIMENSIONS |      |      |
|-----------------------------|--------|-------------------|------|------|
|                             |        | MIN.              | NDR. | MAX. |
| TOTAL THICKNESS             | A      | ---               | ---  | 1    |
| SUBSTRATE THICKNESS         | A1     |                   | 0.26 | REF  |
| MOLD THICKNESS              | A2     |                   | 0.54 | REF  |
| BODY SIZE                   | D      |                   | 8    | BSC  |
|                             | E      |                   | 8    | BSC  |
| LEAD WIDTH                  | W      | 0.2               | 0.25 | 0.3  |
| LEAD LENGTH                 | L      | 0.35              | 0.4  | 0.45 |
| LEAD PITCH                  | e      |                   | 0.4  | BSC  |
| LEAD COUNT                  | n      |                   | 68   |      |
| EDGE BALL CENTER TO CENTER  | D1     |                   | 6.4  | BSC  |
|                             | E1     |                   | 6.4  | BSC  |
| BODY CENTER TO CONTACT BALL | SD     |                   | ---  | BSC  |
|                             | SE     |                   | ---  | BSC  |
| BALL WIDTH                  | b      | ---               | ---  | ---  |
| BALL DIAMETER               |        |                   | ---  |      |
| BALL OPENING                |        |                   | ---  |      |
| BALL PITCH                  | e1     |                   | ---  |      |
| BALL COUNT                  | n1     |                   | ---  |      |
| PRE-SOLDER                  | A3     | 0.02              | ---  | 0.1  |
| PACKAGE EDGE TOLERANCE      | aaa    |                   | 0.1  |      |
| MOLD FLATNESS               | bbb    |                   | 0.1  |      |
| COPLANARITY                 | ddd    |                   | 0.08 |      |
| BALL OFFSET (PACKAGE)       | eee    |                   | ---  |      |
| BALL OFFSET (BALL)          | fff    |                   | ---  |      |

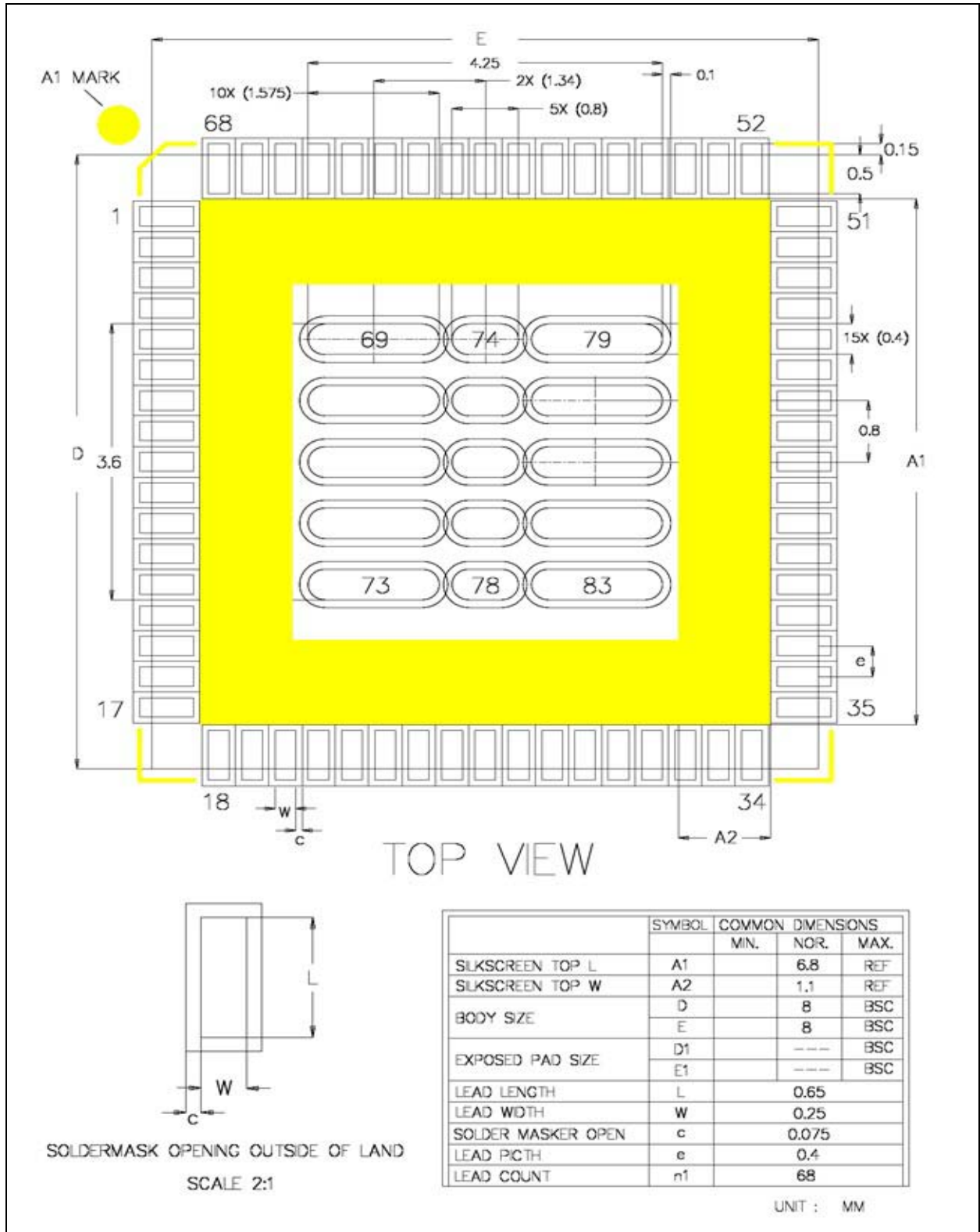
NOTES:

△ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

## 9.5 Footprint Dimensions

Figure 9-7 illustrates the footprint dimensions of the IS2064 SoC.

**FIGURE 9-7: IS2064 FOOTPRINT DIMENSIONS**



NOTES:



## 10.0 REFLOW PROFILE AND STORAGE CONDITION

Figure 10-1 and Figure 10-2 illustrate reflow profiles and stencil information of the IS2062/64 SoC.

### 10.1 Stencil of SMT Assembly Suggestion

#### 10.1.1 STENCIL TYPE & THICKNESS

- Laser cutting
- Stainless steel
- Thickness: 0.5 mm Pitch, thickness more than 0.15 mm

#### 10.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

- Aspect ratio (width/thickness) more than 1.5
- Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB
  - Oval-shape opening is used to get the optimum paste release
  - Rounded corners to minimize clogging
  - Positive taper walls (5° tapering) with bottom opening larger than the top

#### 10.1.3 APERTURE DESIGN FOR THERMAL PAD

- Small multiple openings are used instead of one big opening, see Figure 10-1
- 60~80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with bottom opening larger than the top, see Figure 10-2

FIGURE 10-1: REFLOW PROFILE APERTURE DESIGN

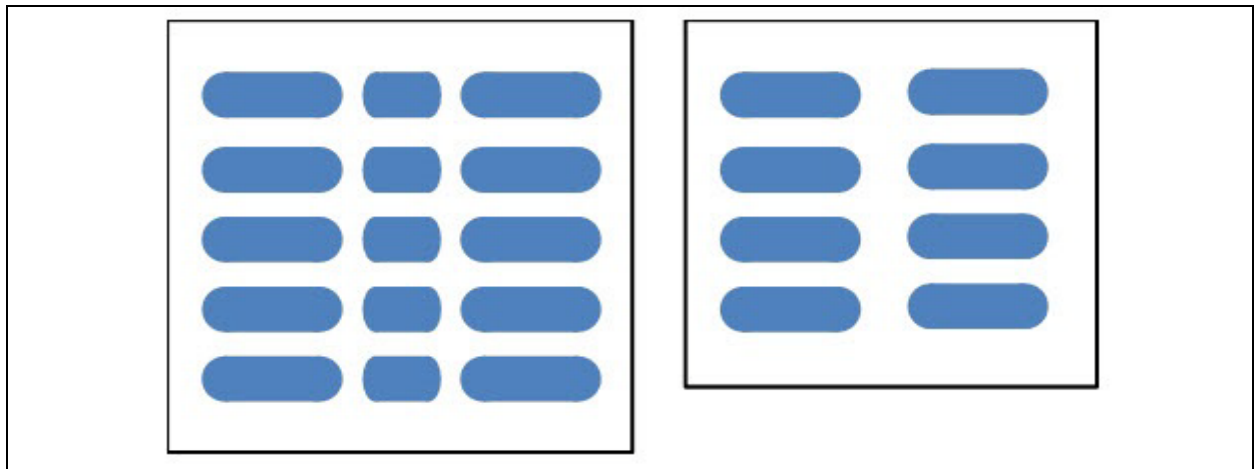
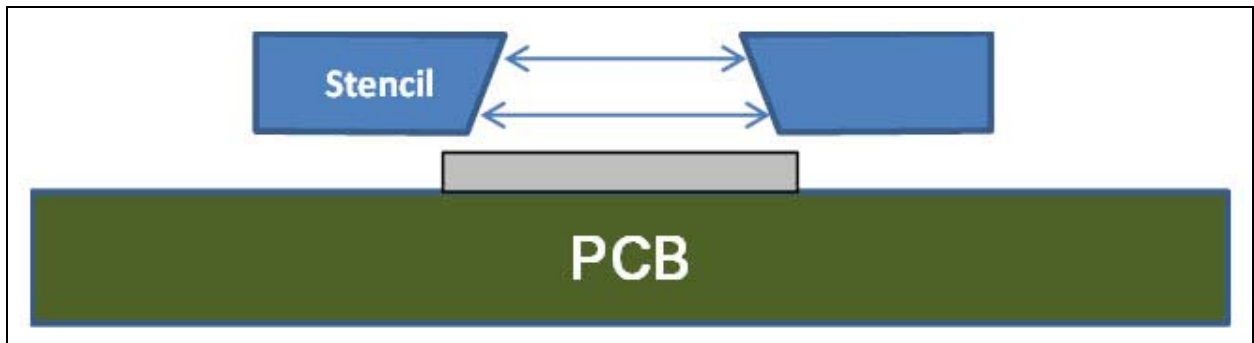


FIGURE 10-2: STENCIL TYPE

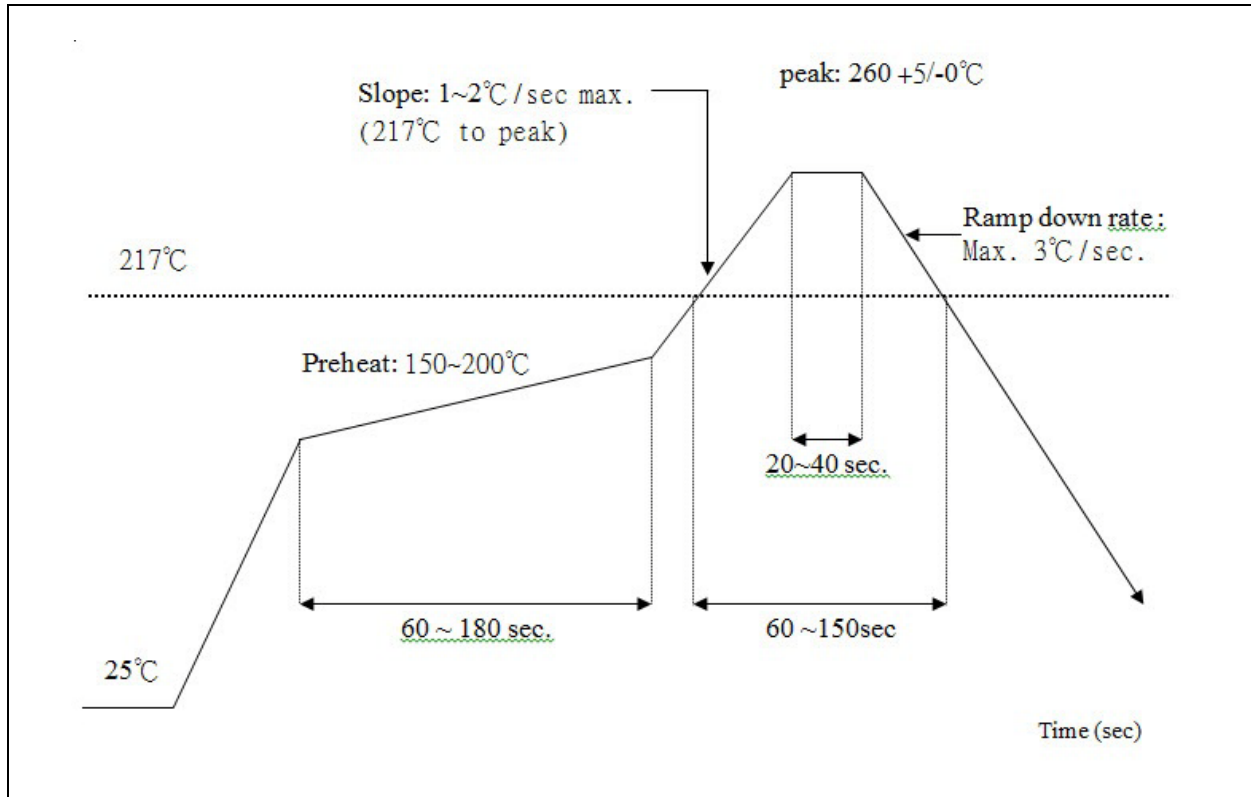


## 10.2 Reflow Condition

Figure 10-3 illustrates the reflow profile and the following are its specific features:

- Standard condition: IPC/JEDEC J-STD-020
- Preheat: 150~200 °C ~60~180 seconds
- Average ramp-up rate (+217 °C to peak): 1~2 °C/sec max
- Temperature maintain above 217: 60~150 seconds
- Time within +5°C of actual peak temperature: 20 ~ 40 seconds
- Peak temperature: 260 +5/-0 °C
- Ramp-down rate (peak to +217°C): +3°C/sec. max
- Time +25 °C to peak temperature: 8 minutes max
- Cycle interval: 5 minutes

**FIGURE 10-3: REFLOW PROFILE**




## 10.3 Storage Condition

Users must follow these specific storage conditions for the IS2062/64 SoC.

- Calculated shelf life in the sealed bag: 24 months at <40 °C and <90% Relative Humidity (RH)
- Once the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <30 °C /60% RH.

Figure 10-4 shows the IS2062/64 SoC bag labeling details.

**FIGURE 10-4: IS2062/64 SoC STORAGE CONDITIONS**

|  |   |   |
|--|---|---|
|   | <p><b>Caution</b><br/>This bag contains<br/><b>MOISTURE-SENSITIVE DEVICES</b></p> | <p>LEVEL<br/><b>3</b></p> <p><small>If blank, see adjacent bar code label</small></p> |
| <p>1. Calculated shelf life in sealed bag : <b>24</b> months at &lt; 40°C and &lt;90% relative humidity (RH)</p>   |   |   |
| <p>2. Peak package body temperature: _____ °C<br/><small>If blank, see adjacent bar code label</small></p>   |   |   |
| <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be</p> <p>a) Mounted within: <b>168</b> hours of factory conditions<br/><small>If blank, see adjacent bar code label</small><br/>≤30°C/60% RH, or</p> <p>b) Stored per J-STD-033</p> |   |   |
| <p>4. Devices require bake, before mounting, if:</p> <p>a) Humidity Indicator Card reads &gt; 10% for level 2a - 5a devices or &gt; 60% for level 2 devices when read at 23± 5°C</p> <p>b) 3a or 3b are not met.</p>   |   |   |
| <p>5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.</p>  |   |   |
| <p>Bag Seal Date: _____<br/><small>If blank, see adjacent bar code label</small></p>   |   |   |
| <p><b>Note: Level and body temperature defined by IPC/JEDEC J-STD-020</b></p>  |   |   |

NOTES:

## 11.0 ORDERING INFORMATION

Table 11-1 provides the ordering information of the IS2062/64 SoC.

**TABLE 11-1: ORDERING INFORMATION**

| Device | Bluetooth Version  | Package                       | Part Number  |
|--------|--|-------------------------------|--------------|
| IS2062 | Bluetooth 4.2, BDR/EDR/BLE SoC with integrated 2 mic and stereo speaker output                                     | 7 x 7 x 0.9 mm, 56LGA package | IS2062GM-012 |
| IS2064 | Bluetooth 4.2, BDR/EDR/BLE, with integrated 1 mic and stereo speaker output and I <sup>2</sup> S digital interface | 8 x 8 x 0.9 mm, 68LGA package | IS2064GM-012 |

**Note:** The IS2062/64 SoC can be purchased through a Microchip representative, Go to <http://www.microchip.com/> for ordering information.

NOTES:

## APPENDIX A: REFERENCE CIRCUIT

Figure A-1 through Figure A-5 illustrate the IS2062 reference schematics for a stereo headset application.

FIGURE A-1: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

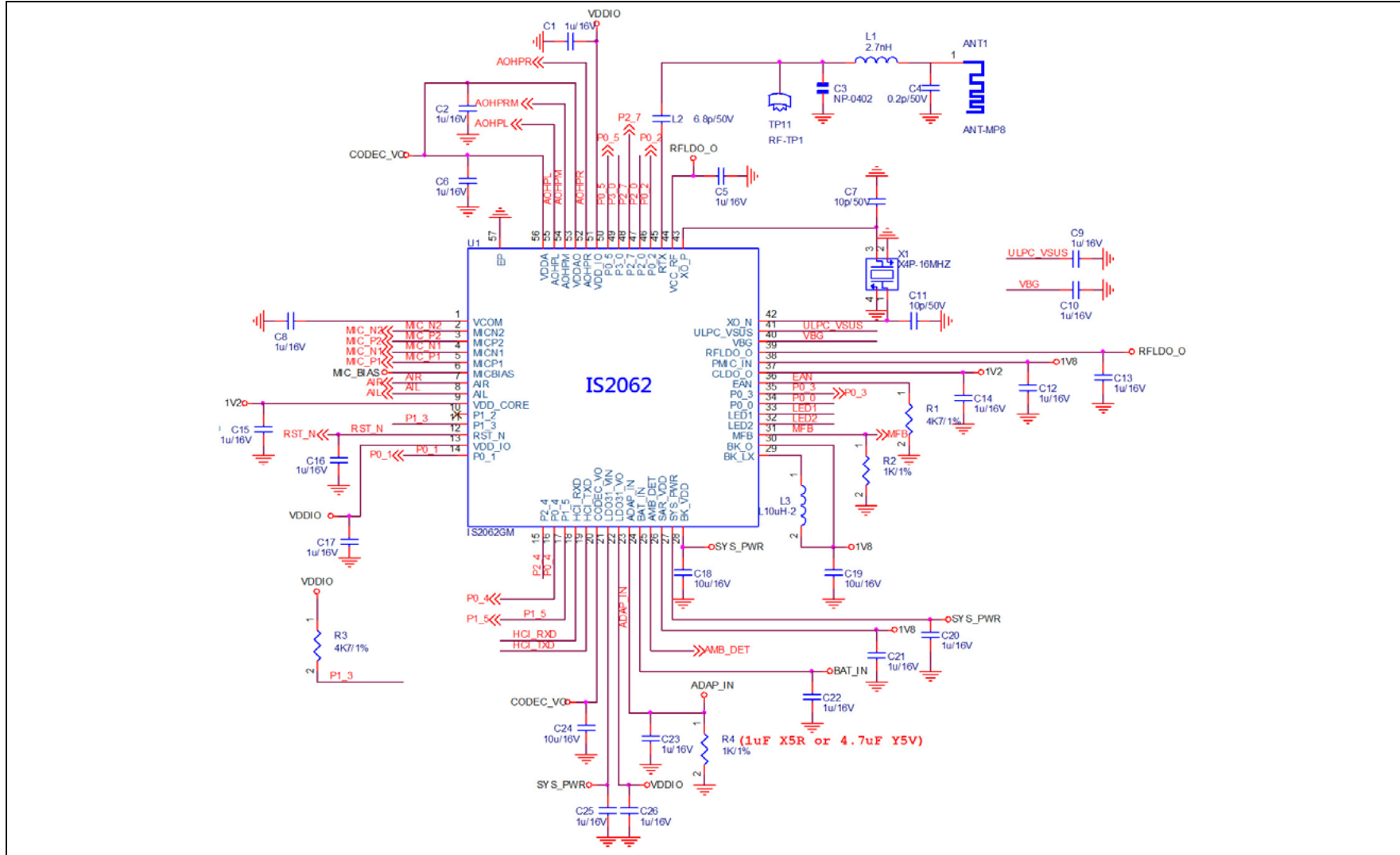


FIGURE A-2: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

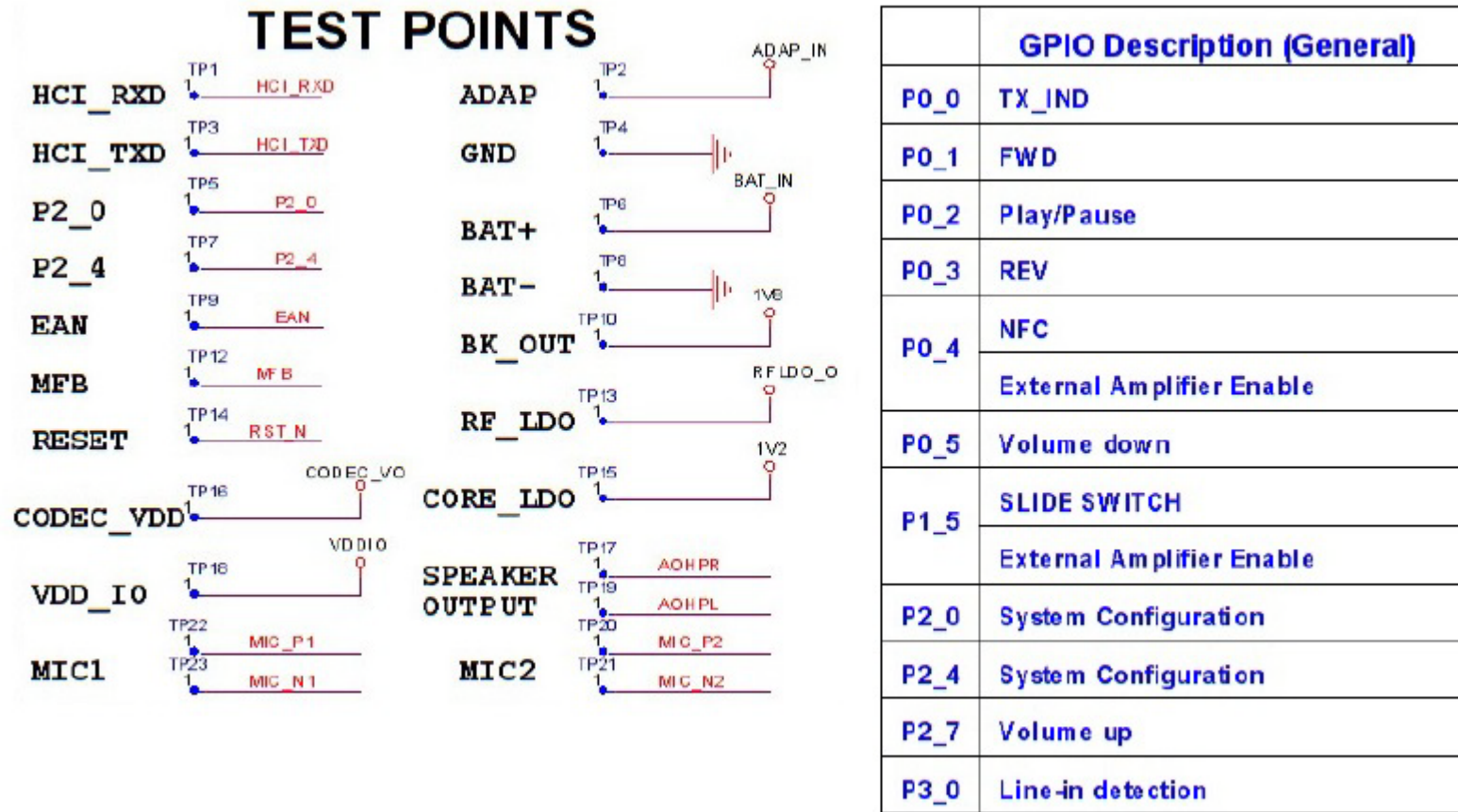
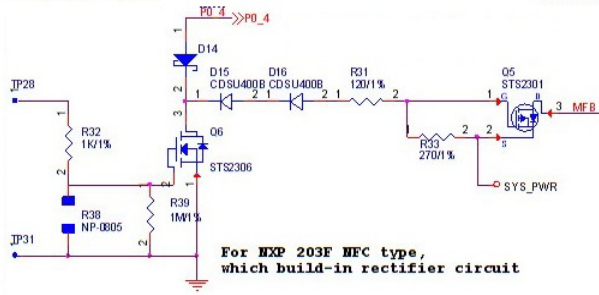


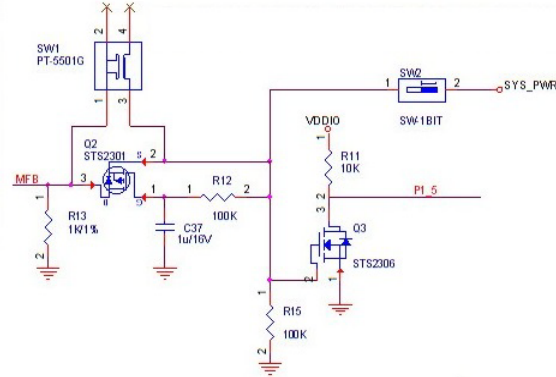


FIGURE A-3: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

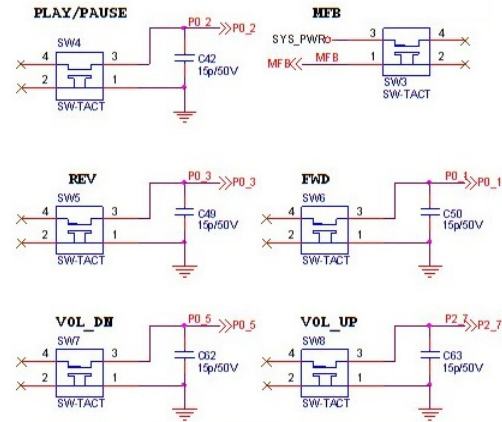
**NFC(OPTIONAL)**



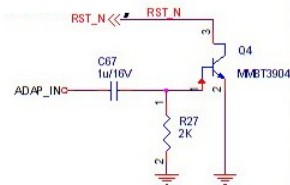
**SLIDE SWITCH(OPTIONAL)**



**SWITCH**



**Reset (OPTIONAL)**



**AMB DET**

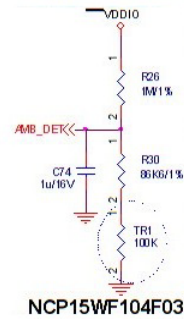
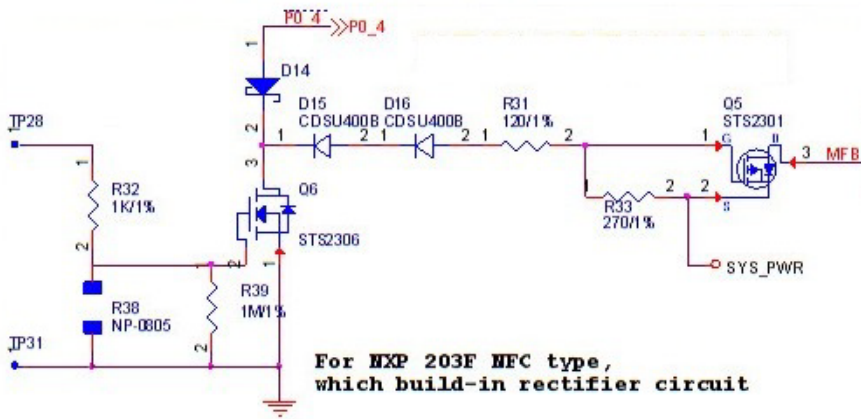
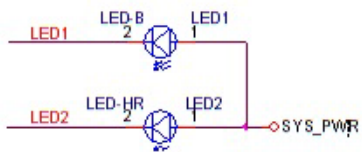


FIGURE A-4: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET

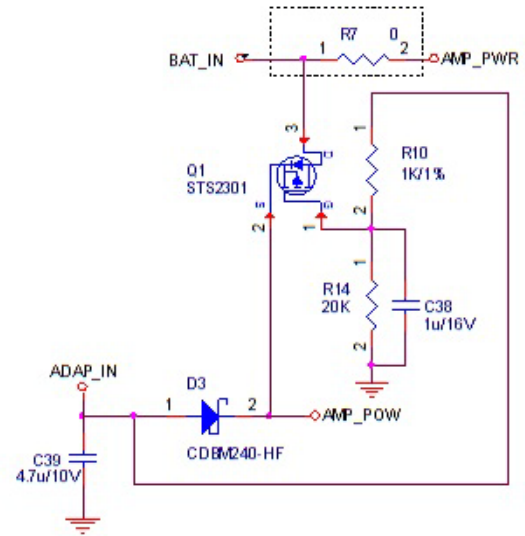
### NFC(OPTIONAL)



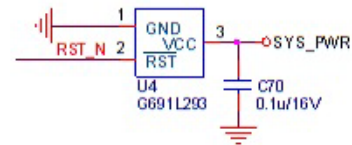
### LED



### EXT POWER TREE (OPTIONAL)



### Reset IC(OPTIONAL)



**FIGURE A-5: IS2062 REFERENCE CIRCUIT FOR STEREO HEADSET**

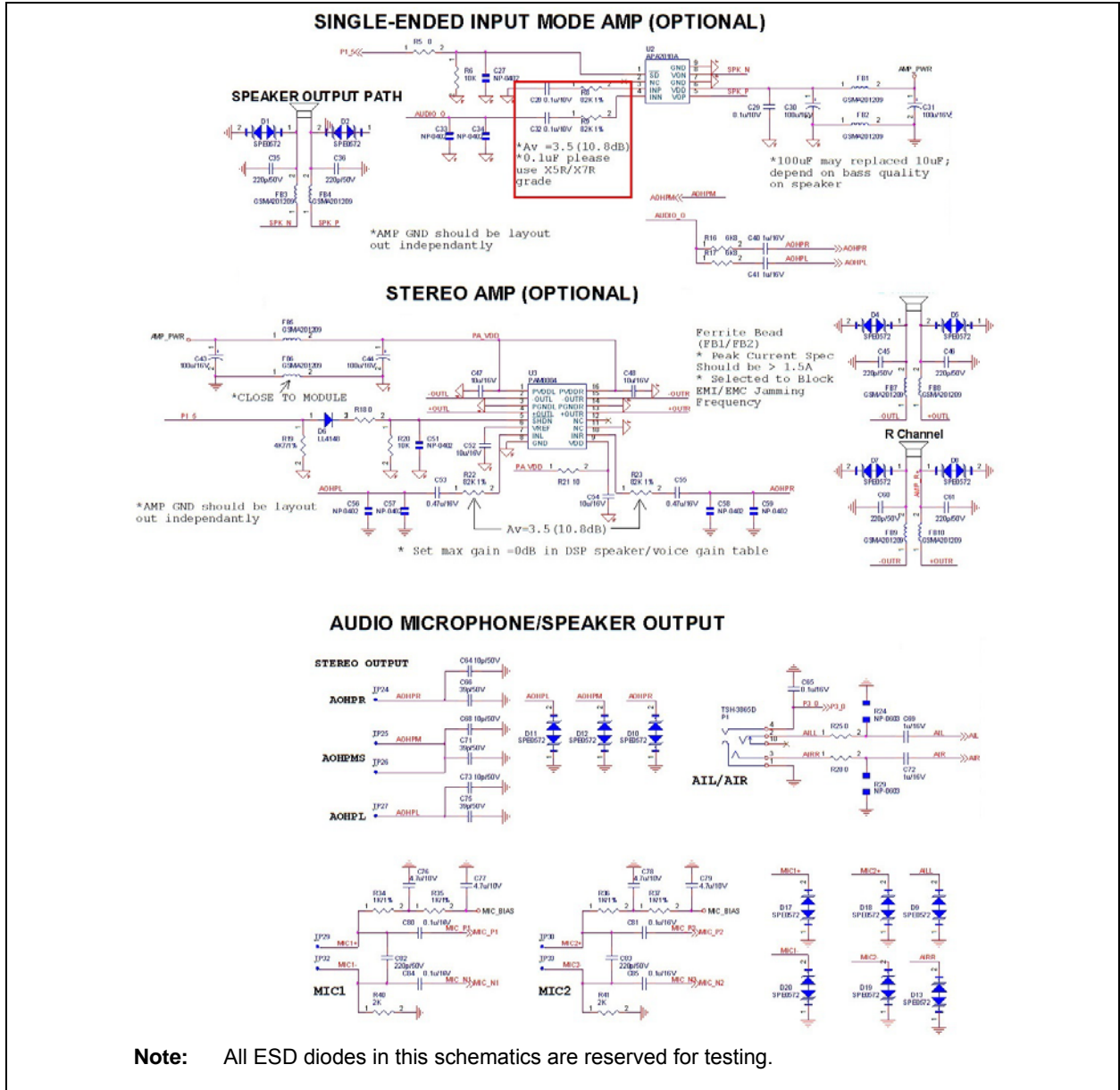


Figure A-6 through Figure A-9 illustrate the IS2064 reference schematic for a stereo headset application.

FIGURE A-6: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET

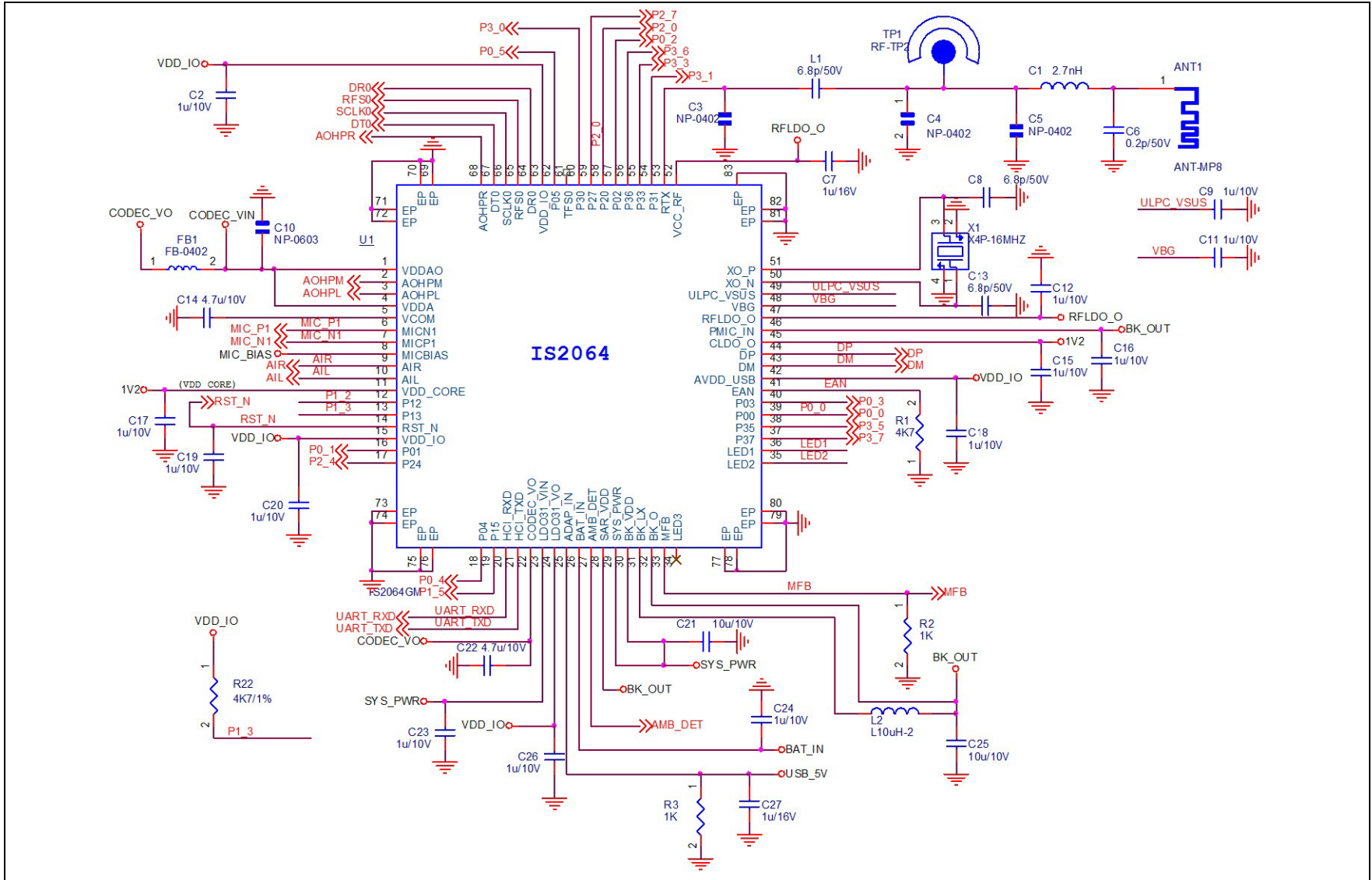
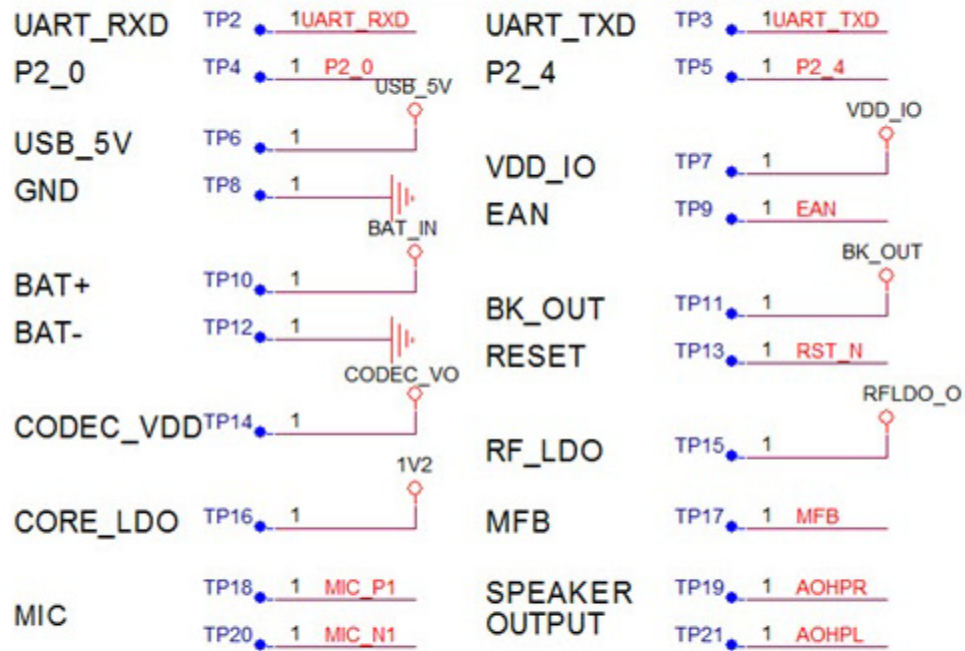


FIGURE A-7: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET

## TEST POINTS



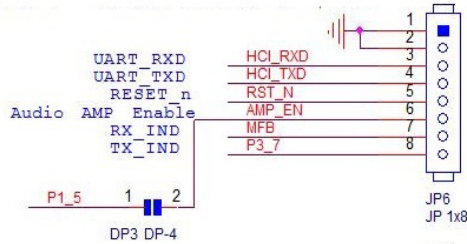
## GPIO DESCRIPTION

|      |                       |
|------|-----------------------|
| MFB  | UART_RX_IND; MFB      |
| P0_0 | SLIDE SWITCH          |
| P0_2 | PLAY/PAUSE            |
| P0_4 | AMP_EN/NFC            |
| P0_5 | VOL-                  |
| P2_7 | VOL+                  |
| P3_0 | AUX IN Detection      |
| P3_7 | UART_TX_IND           |
| P1_5 | AMP_EN/SLIDE SWITCH   |
|      | Single/Double setting |
| P3_6 | Single/Double setting |
| P2_0 | System Configuration  |
| EAN  | System Configuration  |

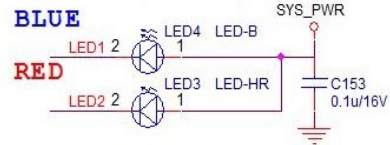


FIGURE A-8: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET

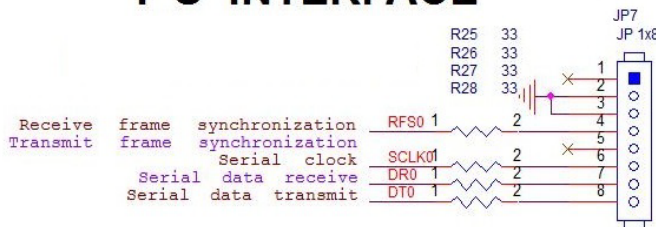
## UART CONTROL (OPTIONAL)



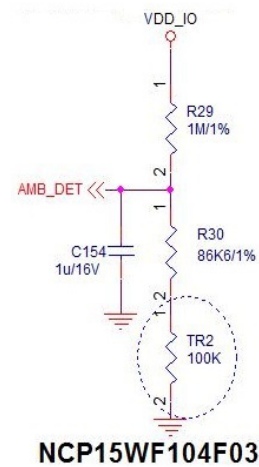
## LED



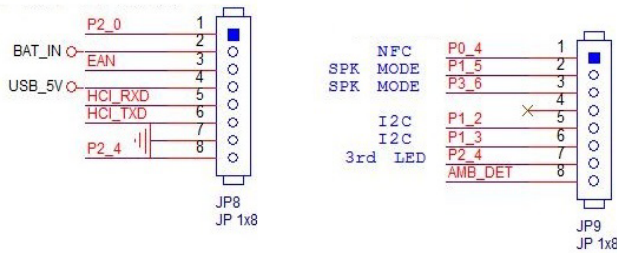
## I<sup>2</sup>S INTERFACE



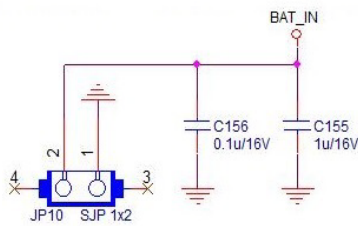
## AMB\_DET



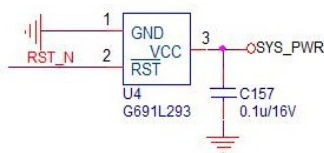
## RESERVE FOR DEBUG



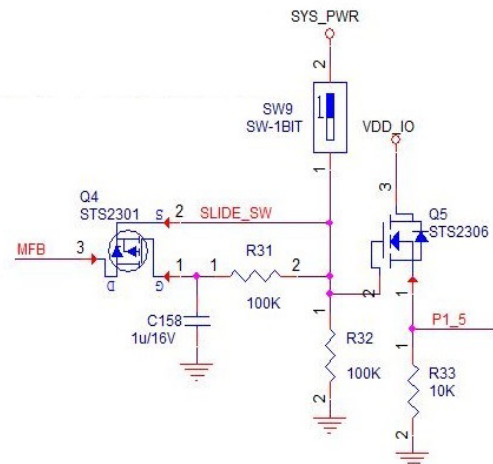
## BATTERY CONNECTOR



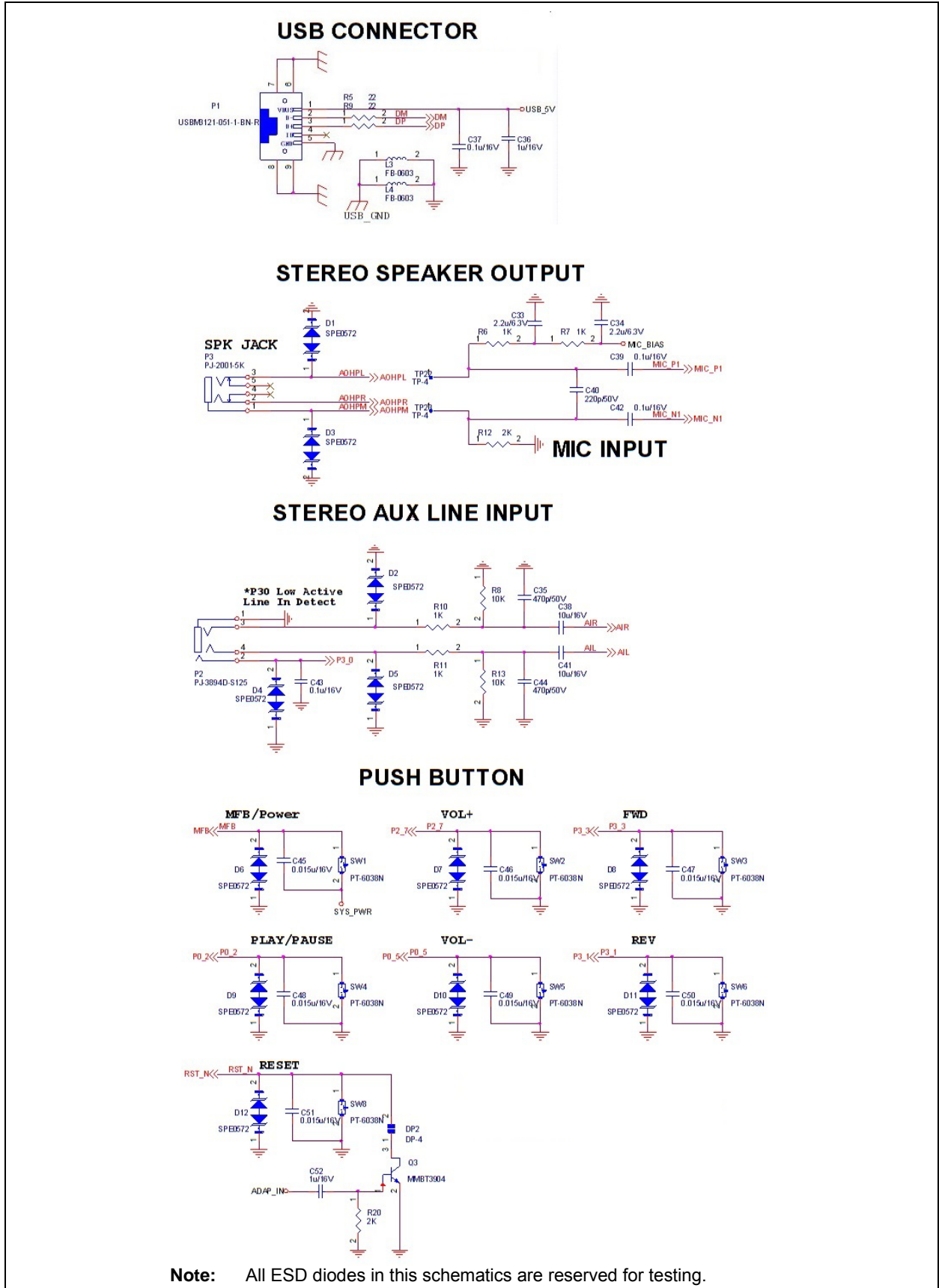
## RESET IC (OPTIONAL)



## SLIDE SWITCH



**FIGURE A-9: IS2064 REFERENCE CIRCUIT FOR STEREO HEADSET**



NOTES:



## APPENDIX B: REVISION HISTORY

### Revision A (May 2016)

This is the initial released version of this document.

NOTES:

## THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at [www.microchip.com](http://www.microchip.com). This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

## CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip's customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at [www.microchip.com](http://www.microchip.com). Under "Support", click on "Customer Change Notification" and follow the registration instructions.

## CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: <http://microchip.com/support>.

NOTES:

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

---

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
= ISO/TS 16949 =**

**Trademarks**

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, KeeLoq logo, Klear, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, RightTouch logo, REAL ICE, Ripple Blocker, Serial Quad I/O, SQL, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-0584-9



# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110

**Canada - Toronto**  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon

**Hong Kong**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Dongguan**  
Tel: 86-769-8702-9880

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

### ASIA/PACIFIC

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7828

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**  
Tel: 49-2129-3766400

**Germany - Karlsruhe**  
Tel: 49-721-625370

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Venice**  
Tel: 39-049-7625286

**Netherlands - Druen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Poland - Warsaw**  
Tel: 48-22-3325737

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820

07/14/15