IS2063

Bluetooth® 4.2 Stereo Audio SoC

Features

- Qualified for Bluetooth v4.2 specifications
- Supports HFP 1.6, HSP 1.2, A2DP 1.3, SPP 1.2 and AVRCP 1.6
- Supports Bluetooth 4.2 dual-mode (BR/EDR/BLE) (FW dependent):
  - Generic access service
  - Device information service
  - Proprietary services for data communication
  - Apple Notification Center Service (ANCS)
- Supports high resolution up to 24-bit, 96 kHz audio data format
- I^2S digital audio, microphone, analog audio and AUX-In
- Supports one microphone input
- UART, GPIOs and LEDs
- Supports firmware field upgrade
- Battery charging

Baseband Features

- 16 MHz main clock input
- Built-in Flash memory for programing
- Connects simultaneously two hosts (smartphone and tablet) with HFP/A2DP profiles
- Adaptive Frequency Hopping (AFH)

Audio Codec

- Sub-band coding (SBC) and optional Advanced Audio Coding (AAC) decoding
- 20-bit DAC with 98 dB SNR
- 16-bit ADC with 92 dB SNR
- Supports up to 24-bit, 96 kHz I^2S digital audio

RF Features

- Class 2 output power (+2 dBm typical)
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Combined Tx/Rx RF terminal simplifies external matching and reduces external antenna switches
- Tx/Rx RF switch for Class 2 or Class 3 applications
- Integrated synthesizer requires no external voltage-controlled oscillator (VCO), varactor diode, resonator and loop filter
- Crystal oscillator with built-in digital trimming compensates for temperature or process variations

DSP Audio Processing

- 32-bit DSP core
- Supports 64 kbps A-Law, μ-Law PCM format/Continuous Variable Slope Delta (CVSD) Modulation for Synchronous Connection-Oriented (SCO) channel operation
- Supports 8/16 kHz noise suppression
- Supports 8/16 kHz echo cancellation
- Supports Modified Sub-Band Coding (MSBC) decoder for wide band speech
- Built-in High Definition Clean Audio (HCA) algorithms for both narrow band and wide band speech processing
- Packet loss concealment (PLC)
- Built-in audio effect algorithms to enhance audio streaming
- Supports Serial Copy Management System (SCMS-T) content protection

Packages

Type	LGA
Pin count	68
Contact/Lead pitch	0.4
Dimensions	8 x 8 x 0.9

Note: All dimensions are in millimeters (mm) unless specified.

Peripherals

- High-speed HCI-UART interface (supports up to 921,600 bps)
- Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
- Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO)
- Built-in ADC for battery monitoring and voltage sensor
- An AUX-In port for external audio input
- Three LED drivers

Operating Condition

- Operating voltage: 3.2V to 4.2V
- Temperature range: -20°C to +70°C

Applications

- Soundbars and Subwoofers
- Speaker phones
- Headsets and headphones

Description

The IS2063 is a stereo audio SoC qualified for Bluetooth v4.2 with Enhanced Data Rate (EDR). It integrates a 32-bit DSP co-processor and a codec which is dedicated for voice and audio applications. For voice applications, the CVSD encoding/decoding, 8K/16K noise reduction and echo cancellation are implemented. For audio applications, the SBC and AAC Low-Complexity (AAC-LC) decoding functions are used.

The IS2063 SoC features a 20-bit audio DAC in addition to an I^2S digital audio interface that supports up to 24-bit, 96 kHz data formats. The system optimization includes an integrated battery voltage sensor, a battery charger, a switching regulator and LDOs.

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NOTES:

1.0 DEVICE OVERVIEW

The IS2063 SoC integrates a Bluetooth 4.2 radio transceiver, a Power Management Unit (PMU), a Microcontroller (MCU), an audio codec, a crystal and a 32-bit DSP. The IS2063 SoC can be configured using the UI tool.

Note:	The UI tool is a Windows-based utility tool, which is available for download from the Microchip web site at: www.microchip.com/IS2063.

Figure 1-1 illustrates a typical block diagram of the IS2063 SoC.

FIGURE 1-1: IS2063 SOC BLOCK DIAGRAM

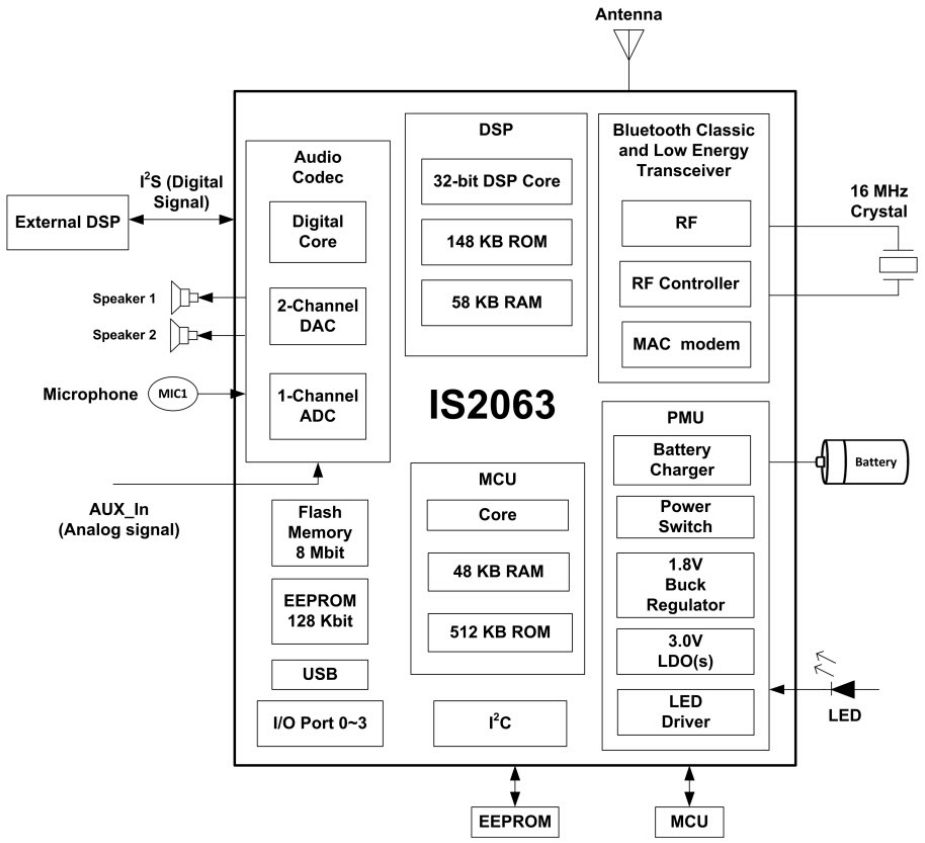


Table 1-1 provides the key features of the IS2063 SoC.

TABLE 1-1: IS2063 KEY FEATURES

Feature	IS2063
Application	Multi-speaker/Soundbar/Subwoofer
Stereo/mono	Stereo
Pin count	68
Dimensions (mm^2)	8 x 8
Audio DAC output	2 channel
DAC (single-ended) SNR at 2.8V (dB)	-98
DAC (capless) SNR at 2.8V (dB)	-96
ADC SNR at 2.8V (dB)	-92
I^2S digital interface	Yes
Analog AUX-In	Yes
Mono microphone	1
External audio amplifier interface	Yes
UART	Yes
LED driver	3
Internal DC-DC step-down regulator	Yes
DC 5V adapter input	Yes
Battery charger (350 mA max.)	Yes
ADC for thermal charger protection	No
Undervoltage protection (UVP)	No
GPIO	15
Button support	6
NFC (triggered by external NFC)	Yes
EEPROM	128K
Customized voice prompt	No
Multitone	Yes
DSP sound effect	Yes
BLE	Yes
Bluetooth profiles	
HFP	1.6
AVRCP	1.6
A2DP	1.3
HSP	1.2
SPP	1.2

Figure 1-2 illustrates the pin diagram of the IS2063 SoC.

FIGURE 1-2: IS2063 SOC PIN DIAGRAM

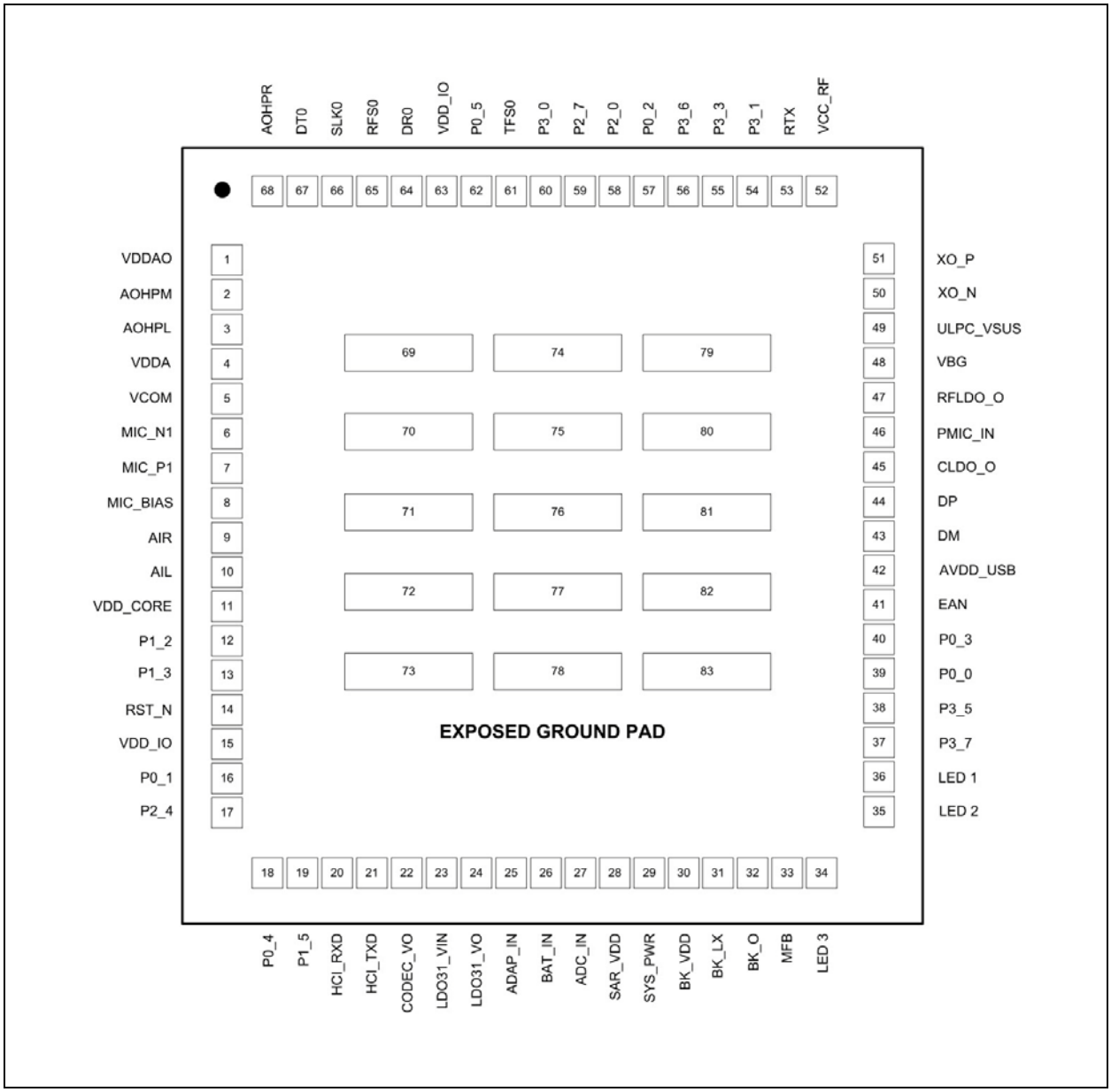


Table 1-2 provides the pin description of the IS2063 SoC. Users can configure these pins using the UI tool.

TABLE 1-2: IS2063 SOC PIN DESCRIPTION

Pin No	Pin Type	Name	Description
1	P	VDDAO	Power supply (3.3V) dedicated to codec output amplifiers; connect to the CODEC_VO pin
2	O	AOHPM	Headphone common mode output/sense input
3	O	AOHPL	Left channel analog headphone output
4	P	VDDA	Power supply (3.3V) or reference voltage for external codec; connect to CODEC_VO pin
5	P	VCOM	Internal biasing voltage for codec, connect a 4.7 µF capacitor to ground
6	I	MIC_N1	MIC1 mono differential analog negative input
7	I	MIC_P1	MIC1 mono differential analog positive input
8	P	MIC_BIAS	Electric microphone biasing voltage
9	I	AIR	Right channel, single-ended analog input
10	I	AIL	Left channel, single-ended analog input
11	P	VDD_CORE	Core 1.2V power input; connect to CLDO_O pin; connect to GND through a 1 µF (X5R/X7R) capacitor
12	O	P1_2	I^2C SCL (EEPROM clock)
13	I/O	P1_3	I^2C SDA (EEPROM data SDA)
14	I	RST_N	System reset (active-low)
15	P	VDD_IO	I/O power supply input (3.3V); connect to LDO31_VO (pin # 24); connect to GND through a 1 µF (X5R/X7R) capacitor
16	I/O	P0_1	Configurable control or indication pin (Internally pulled up if configured as an input) • Class1 Tx control signal for external RF T/R switch, active-high
17	I	P2_4	System configuration pin along with P2_0 and EAN pins can be used to set the IS2063 SoC in any one of these modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
18	I/O	P0_4	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin, active-low • Out_Ind_1
19	I/O	P1_5	Configurable control or indication pin (Internally pulled up if configured as an input) • NFC detection pin, active-low • Slide switch detector, active-high • Out_Ind_1 • Multi-SPK Master/Slave mode control (FW dependent)
20	I	HCI_RXD	HCI UART data input
21	O	HCI_TXD	HCI UART data output

Pin No	Pin Type	Name	Description
22	P	CODEC_VO	LDO output for codec power
23	P	LDO31_VIN	LDO input, connect to SYS_PWR (pin # 29)
24	P	LDO31_VO	3V LDO output, for VDD_IO power, do not calibrate
25	P	ADAP_IN	5V power adapter input
26	P	BAT_IN	Battery input, voltage range: 3.2V to 4.2V
27	I	ADC_IN	Analog input
28	P	SAR_VDD	SAR 1.8V input; connect to BK_O pin
29	P	SYS_PWR	System power output from BAT_IN or ADAP_IN
30	P	BK_VDD	1.8V buck VDD power input; connect to SYS_PWR pin
31	P	BK_LX	1.8V buck PWM/PFM output
32	P	BK_O	1.8V buck feedback input
33	I	MFB	• Multi-Function Button and power-on key • UART RX IND, active-high
34	I	LED3	LED driver 3
35	I	LED2	LED driver 2
36	I	LED1	LED driver 1
37	I/O	P3_7	Configurable control or indication pin (Internally pulled up if configured as an input) UART TX_IND, active-low
38	I/O	P3_5	Configurable control or indication pin (Internally pulled down if configured as an input)
39	I/O	P0_0	Configurable control or indication pin (Internally pulled up if configured as an input) • Slide switch detector, active-high
40	I/O	P0_3	Configurable control or indication pin (Internally pulled up, if configured as an input)
41	I	EAN	External address-bus negative System configuration pin along with P2_0 and P2_4 pins, used to set the IS2063 SoC in any one of the following three modes: • Application mode (for normal operation), • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1
42	P	AVDD_USB	USB power input; connect to LDO31_VO pin
43	I/O	DM	Differential data-minus USB
44	I/O	DP	Differential data-plus USB
45	P	CLDO_O	1.2V core LDO output
46	P	PMIC_IN	PMU power input
47	P	RFLDO_O	1.28V RF LDO output
48	P	VBG	Bandgap output reference for decoupling interference
49	P	ULPC_VSUS	ULPC 1.2V output power, maximum loading 1 mA
50	I	XO_N	16 MHz crystal input negative
51	I	XO_P	16 MHz crystal input positive
52	P	VCC_RF	RF power input (1.28V) for both synthesizer and Tx/Rx block
53	I/O	RTX	RF path (transmit/receive)

Pin No	Pin Type	Name	Description
54	I/O	P3_1	Configurable control or indication pin (Internally pulled up if configured as an input) • REV key (default), active-low
55	I/O	P3_3	Configurable control or indication pin (Internally pulled up if configured as an input) • FWD key (default), active-low
56	I/O	P3_6	Configurable control or indication pin (Internally pulled up if configured as an input) • Multi-SPK Master/Slave mode control (FW dependent)
57	I/O	P0_2	Configurable control or indication pin (Internally pulled up if configured as an input) Play/Pause key (default)
58	I/O	P2_0	System configuration pin along with the EAN and P2_4 pins, used to set the IS2063 SoC in any one of the following modes: • Application mode (for normal operation), • Test mode (to change EEPROM values), and • Write Flash mode (to load a new firmware into the SoC), see Table 6-1 • Pulse/PWM signal output
59	I/O	P2_7	Configurable control or indication pin (Internally pulled up if configured as an input) Volume up key (default), active-low
60	I/O	P3_0	Configurable control or indication pin (Internally pulled up if configured as an input) AUX-In detector, active-low
61	I/O	TFS0	I^2S interface: left/right clock
62	I/O	P0_5	Configurable control or indication pin (Internally pulled up if configured as an input) Volume down key (default), active-low
63	P	VDD_IO	I/O power supply input (3.3V); connect to LDO31_VO pin
64	I/O	DR0	I^2S interface: digital left/right data
65	I/O	RFS0	I^2S interface: left/right clock
66	I/O	SCLK0	I^2S interface: bit clock
67	I/O	DT0	I^2S interface: digital left/right data
68	O	AOHPR	Headphone output, right channel
69-83	P	EP	Exposed pads, Used as ground (GND) pins

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin

Note: All I/O pins can be configured using the UI tool.

2.0 AUDIO

The input and output audios have different stages and each stage can be programmed to vary the gain response characteristics. For microphones, both single-ended inputs and differential inputs are supported. To maintain a high quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors can be used at both positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction are in-built. To reduce nonlinear distortion and to help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. Adaptive filtering is also applied to track the echo path impulse in response to provide echo free and full-duplex user experience.

The embedded noise reduction algorithm helps to extract clean speech signals from the noisy inputs captured by the microphones and improves mutual understanding in communication. The advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are in-built. The audio effect algorithms improve the user's audio listening experience in terms of better quality after audio signal processing.

Figure 2-1 and Figure 2-2 illustrate the processing flow of speaker-phone applications for speech and audio signal processing.

FIGURE 2-1: SPEECH PROCESSING

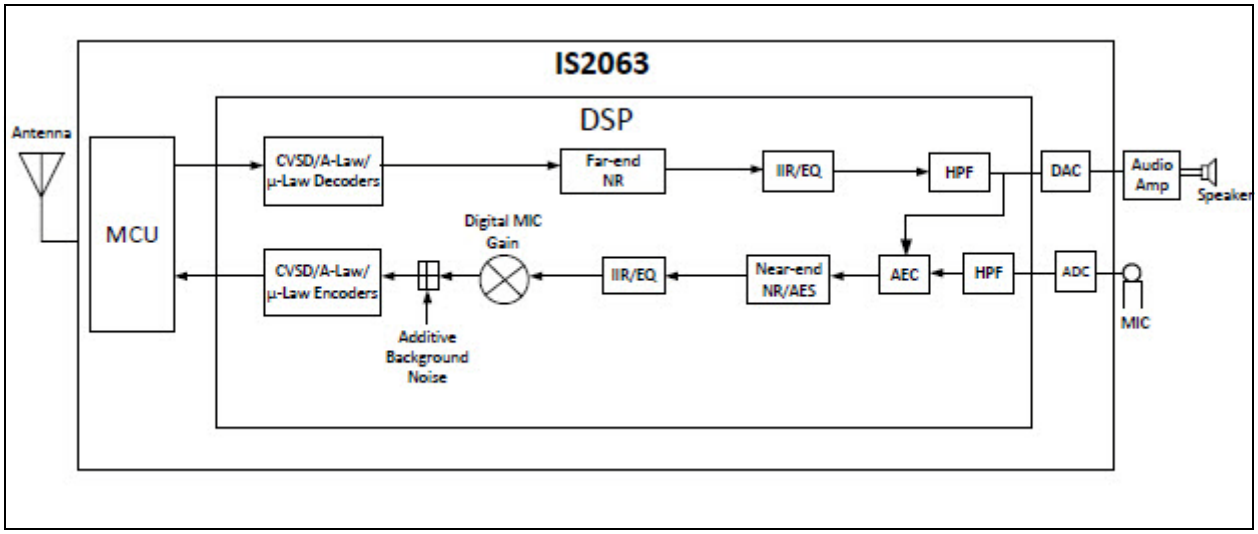
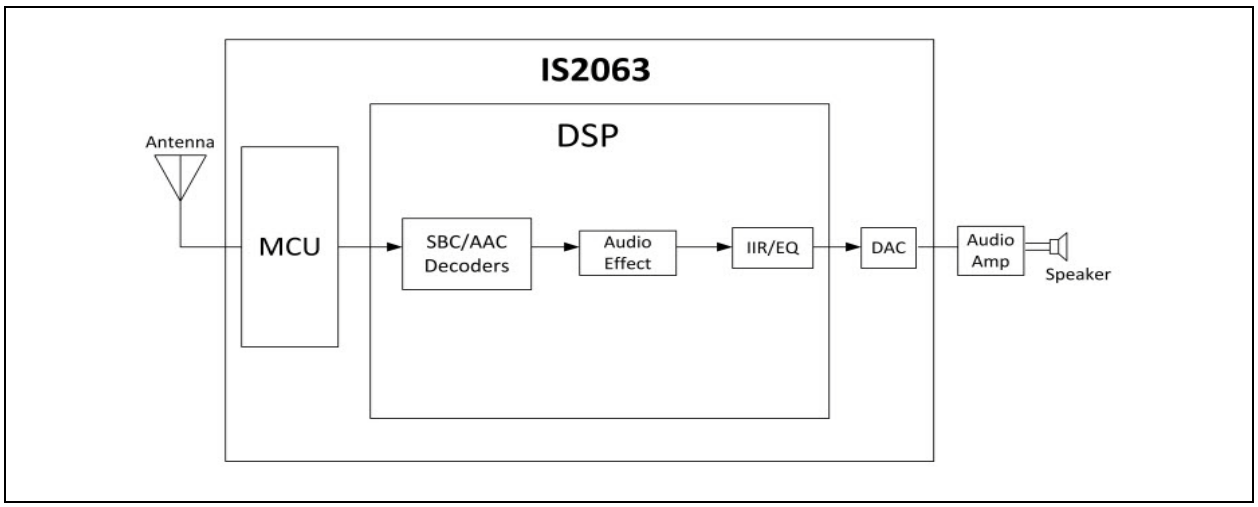


FIGURE 2-2: AUDIO PROCESSING



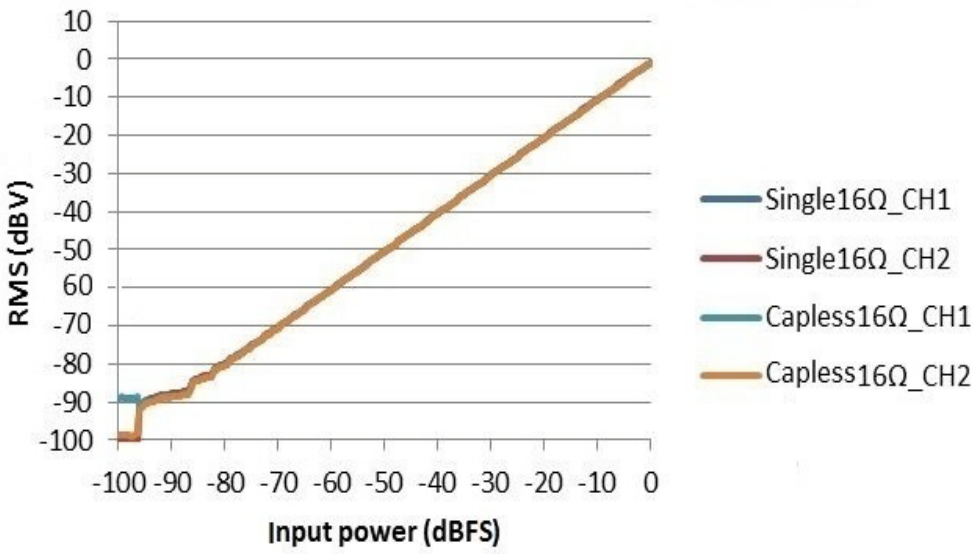
The DSP parameters can be configured using the DSP tool. For additional information on the DSP tool, refer to *"IS206X DSP Application Note"*.

Note:	The DSP tool and "*IS206X DSP Application Note*" are available for download from the Microchip web site at: www.microchip.com/IS2063.

2.2 Codec

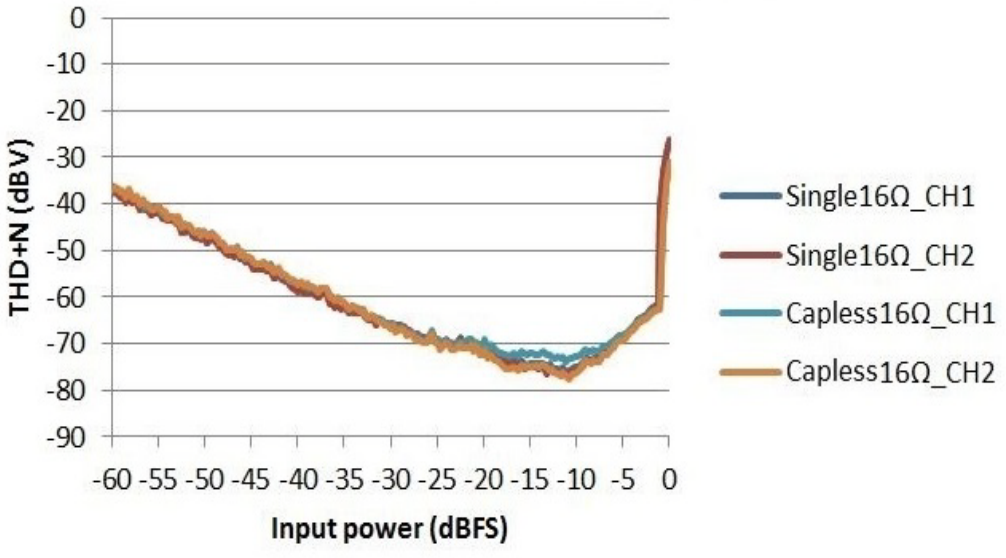
The built-in codec has a high signal-to-noise ratio (SNR) performance and it consists of an ADC, a DAC and an additional analog circuitry. Figure 2-3 through Figure 2-6 illustrate the dynamic range and frequency response of the codec.

FIGURE 2-3: CODEC DAC DYNAMIC RANGE



Note: The data corresponds to the 16 ohm load with 2.8V operating voltage and +25ºC operating temperature.

FIGURE 2-4: CODEC DAC THD+N VERSUS INPUT POWER



Note: The data corresponds to the 16 ohm load with 2.8V operating voltage and +25ºC operating temperature.

FIGURE 2-5: CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

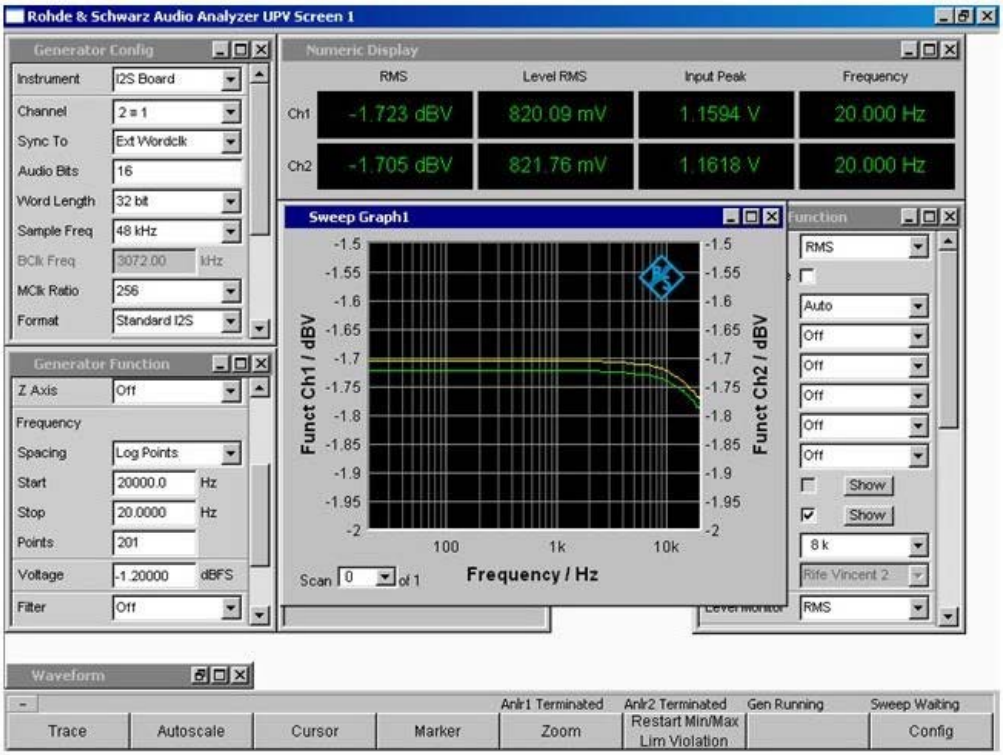
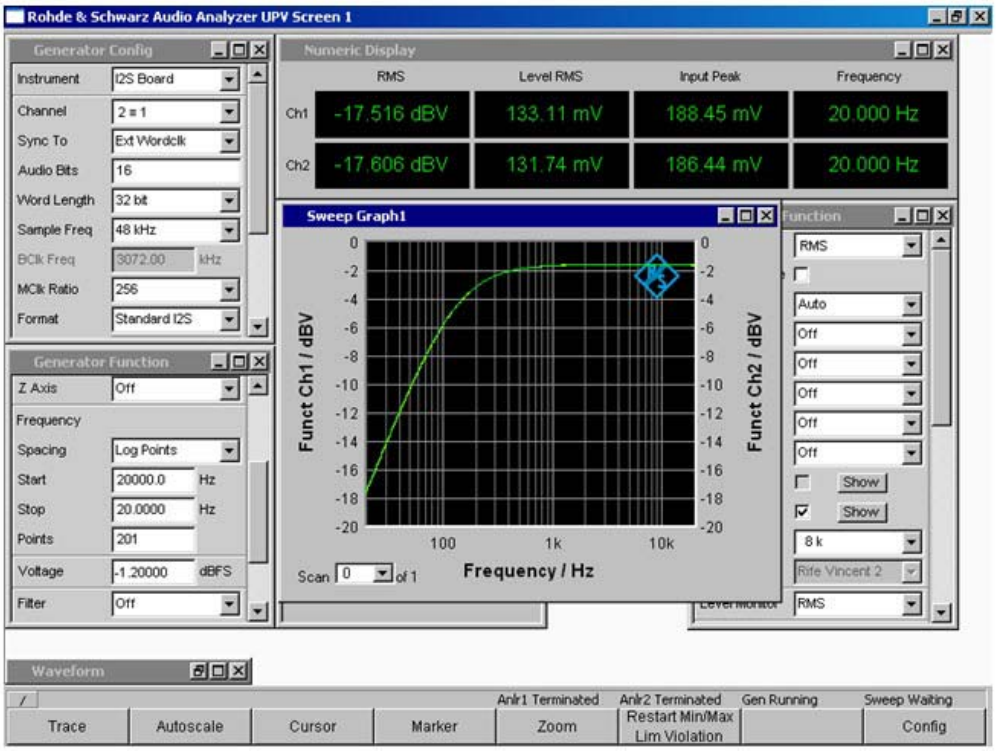


FIGURE 2-6: CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



Note: The DAC frequency response corresponds to single-ended mode with a 47 µF DC block capacitor.

2.3 Auxiliary Port

The IS2063 SoC supports analog (line-in) signals from the external audio source. The analog (line-in) signal can be processed by the DSP to generate different sound effects (Multi-band dynamic range compression and audio widening), which can be setup by using the DSP tool.

2.4 Analog Speaker Output

The IS2063 SoC supports the following speaker output modes.

- Capless mode — Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. Figure 2-7 illustrates the capless mode.
- Single-ended mode — Used for driving an external audio amplifier where a DC blocking capacitor is required. Figure 2-8 illustrates the single-ended mode.

FIGURE 2-7: ANALOG SPEAKER OUTPUT CAPLESS MODE

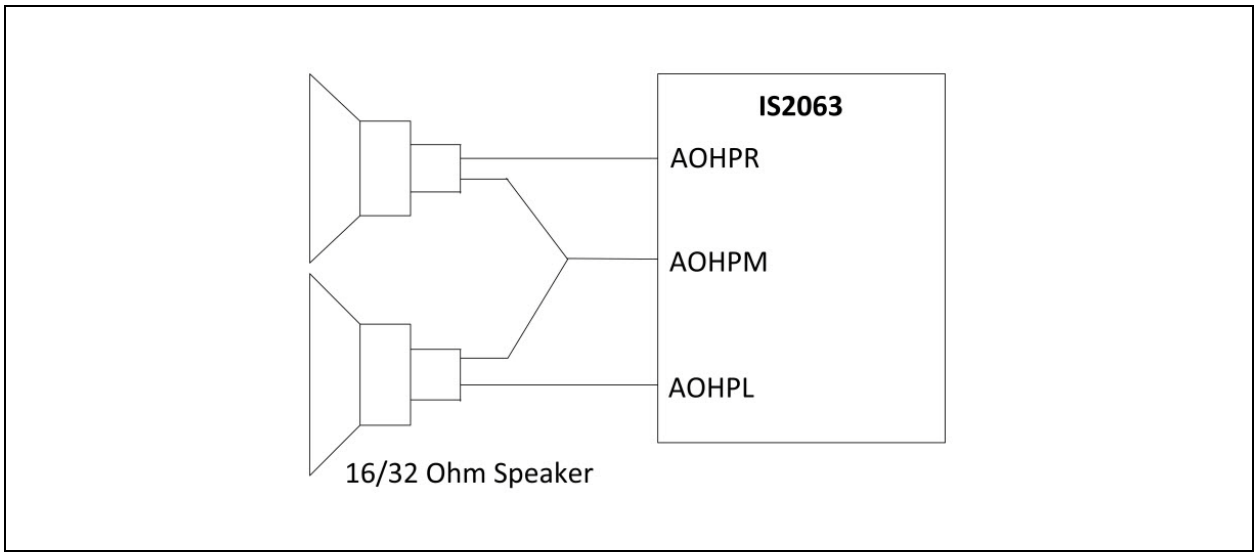
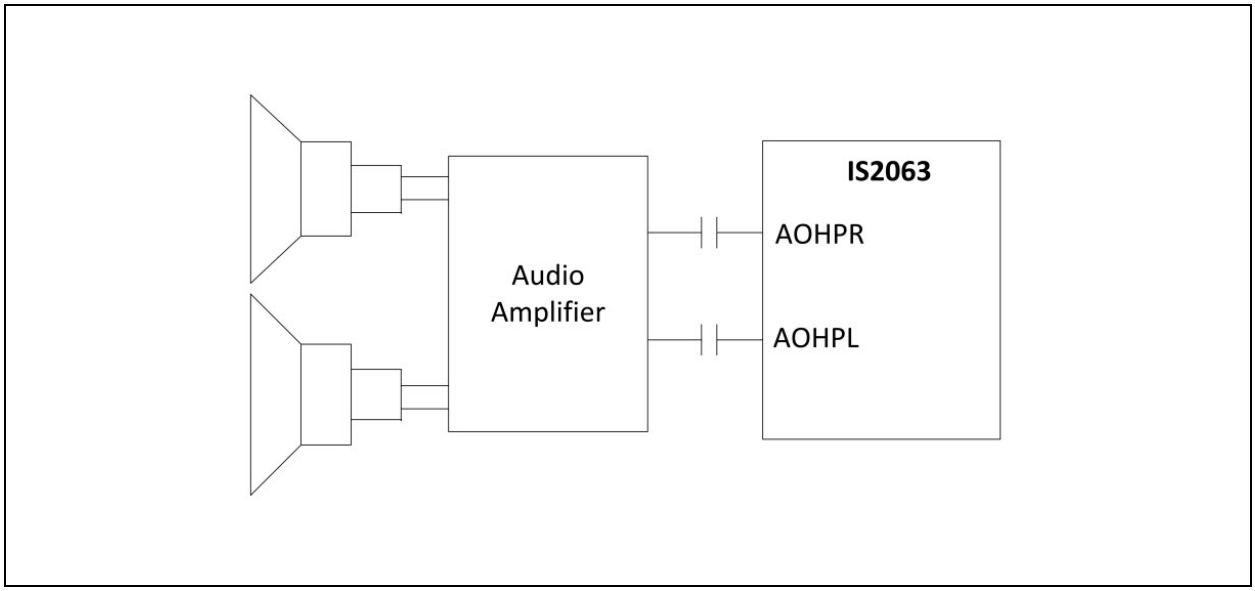


FIGURE 2-8: ANALOG SPEAKER OUTPUT SINGLE-ENDED MODE



3.0 TRANSCEIVER

The IS2063 SoC is designed and optimized for Bluetooth 2.4 GHz systems. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronizing with another device.

3.1 Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm. This is applied into Class 2 or Class 3 radios without an external RF PA. The transmitter performs the IQ conversion to minimize the frequency drift.

3.2 Receiver

The low-noise amplifier (LNA) operates with TR-combined mode for the single port application. It can save the pin on the package without having an external Tx/Rx switch.

The ADC is used to sample the input analog signal and convert it into a digital signal for demodulator analysis. A channel filter is integrated into the receiver channel before the ADC to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for the low-IF architecture, and it also intended to reduce the external Band Pass Filter (BPF) component for a super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

Synthesizer generates a clock for radio transceiver operation. The VCO inside, with a tunable internal LC tank, can reduce any variation for components. A crystal oscillator with an internal digital trimming circuit provides a stable clock for the synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on the Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specifications.

For Bluetooth 2.0 and above specifications, EDR is introduced to provide the data rates of 1/2/3 Mbps. For baseband, both BDR and EDR utilize the same
1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of the EDR packet represents 2 or 3 bits. This is achieved by using two different modulations, $\pi/4$ DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping (AFH)

The IS2063 SoC has an AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose a clear channel for transceiver Bluetooth signal.

NOTES:

4.0 MICROCONTROLLER

Microcontroller is built into the SoC to execute the Bluetooth protocols. It operates from 16 MHz to higher frequencies where the firmware can dynamically adjust the trade-off between the computing power and the power consumption. In ROM version, the MCU firmware is hard-wired to minimize the power consumption for the firmware execution and to save the external Flash cost.

4.1 Memory

There are sufficient ROM and RAM to fulfill the processor requirements, in which a synchronous single-port RAM interface is used. The register bank, dedicated single port memory, and Flash memory are connected to the processor bus. The processor coordinates with all link control procedures and the data movement happens using a set of pointer registers.

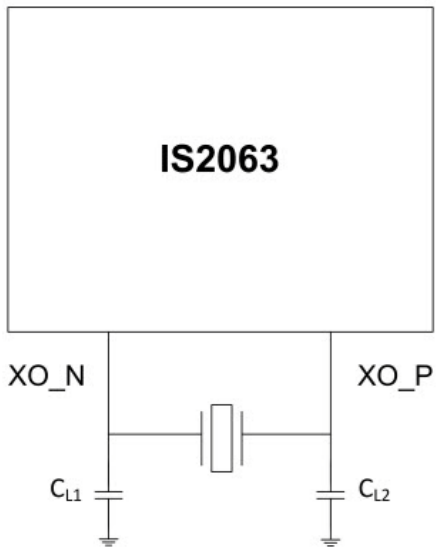
4.2 External Reset

The IS2063 SoC provides a watchdog timer (WDT) to reset the SoC. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action can also be driven by an external Reset signal which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most of the applications.

4.3 Reference Clock

The IS2063 SoC is composed of an integrated crystal oscillation function that uses a 16 MHz ±10 ppm external crystal and two specified loading capacitors to provide a high quality system reference timer source. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent loading capacitance in mass production. Frequency trim is achieved by adjusting the crystal loading capacitance through the on-chip trim capacitors (C_{trim}).
The value of trimming capacitance is 200 fF ($200x10^{-15}$ F) per LSb at 5-bit word and the overall adjustable clock frequency is ±40 kHz (based on crystal with load capacitance, C_L spec = 9 pF). Figure 4-1 illustrates the crystal connection of the IS2063 SoC with two capacitors.

FIGURE 4-1: CRYSTAL CONNECTION



Note 1: C_{trim}= 200 fF * (1~31); C_{int} ~ 3 pF.

2: $C_L = [C_{L1} \times C_{L2})/(C_{L1}+C_{L2})]+(C_{trim}/2)+C_{int}$ (Set trim value as 16, then C_{trim}= 3.2 pF).

3: For 16 MHz crystal, in which C_L= 9 pF, we can get C_{L1} = C_{L2} = 9.1 pF).

4: For C_L selection, refer to the data sheet of the crystal.

NOTES:

5.0 POWER MANAGEMENT UNIT

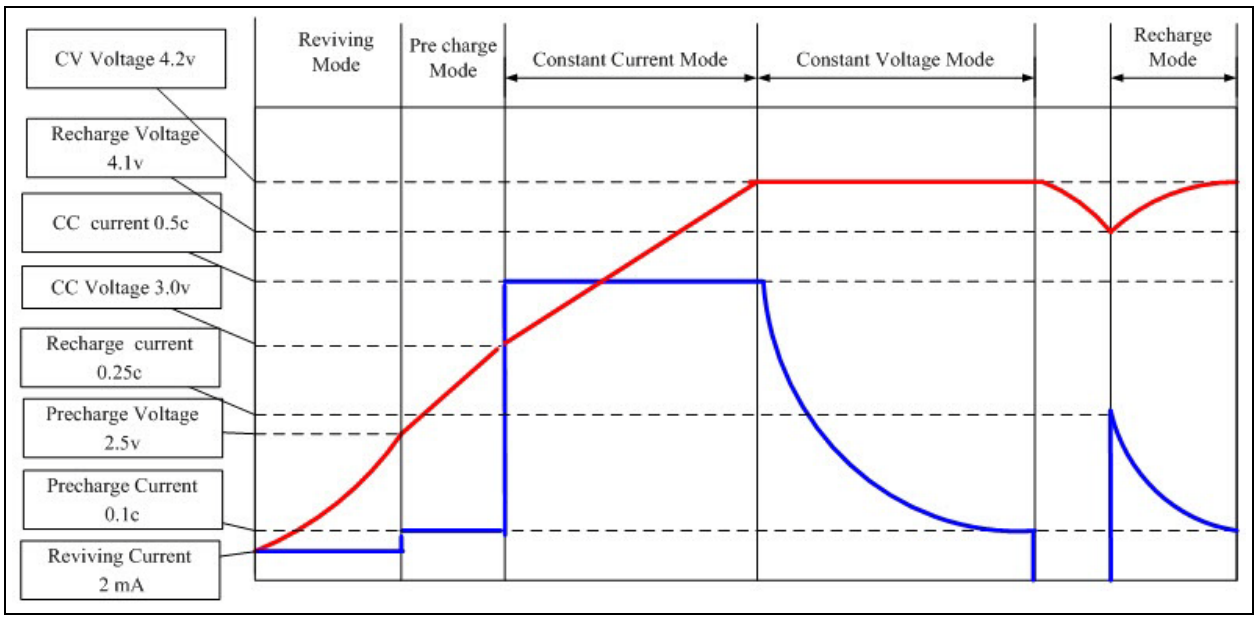
The IS2063 SoC has an integrated Power Management Unit (PMU). The main features of the PMU are a lithium-ion and lithium-polymer battery charger and a voltage regulator. A power switch is used to switch over the power source between the battery and an adapter. Also, the PMU provides current for driving three LEDs.

5.1 Charging a Battery

The IS2063 SoC has a built-in battery charger which is optimized for lithium-ion and lithium-polymer batteries. The battery charger includes a current sensor for charging control, user programmable current regulator and high accuracy voltage regulator.

The charging current parameters are configured using the UI tool. Whenever the adapter is plugged-in, the charging circuit becomes activated. Reviving, pre-charging, constant current and constant voltage modes and re-charging functions are included. The maximum charging current is 350 mA. Figure 5-1 illustrates the charging curve of a battery.

FIGURE 5-1: CHARGING CURVE



5.2 Voltage Monitoring

The 10-bit successive approximation register ADC (SAR ADC) provides a dedicated channel for battery voltage level detection. The warning level can be programmed using the UI tool. The ADC provides a granular resolution to enable the MCU to take control over the charging process.

5.3 LDO

The built-in Low-Dropout Regulator (LDO) is used to convert the battery or adapter power for power supply. It also integrates hardware architecture to control the power on/off procedure. The built-in programmable LDOs provide power for codec and digital I/O pads. Also, it is used to buffer the high input voltage from battery or adapter. This LDO requires 1 µF bypass capacitor.

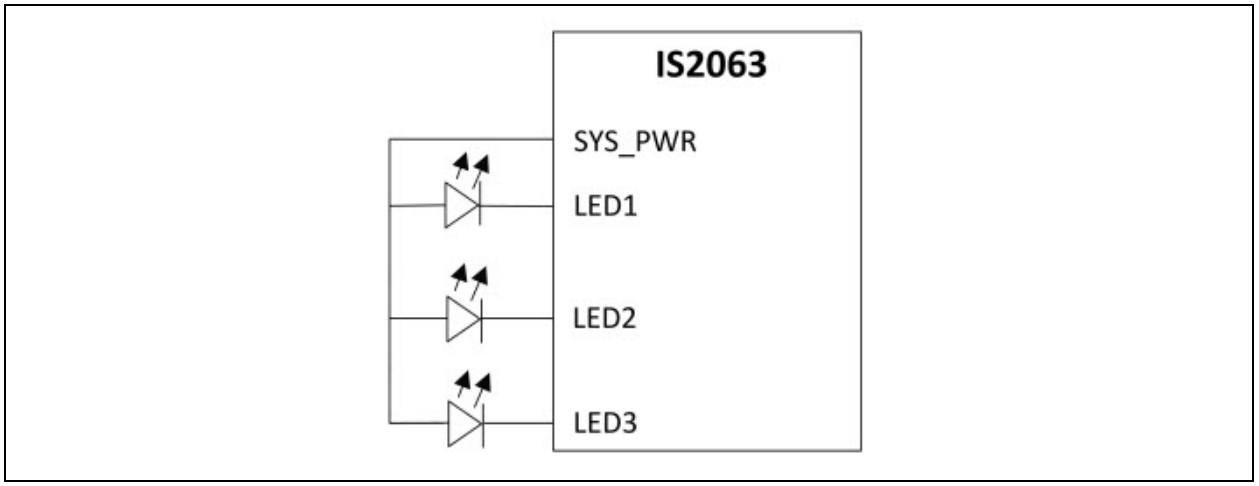
5.4 Switching Regulator

The built-in programmable output voltage regulator can convert the battery voltage to RF and baseband core power supply. This converter has a high conversion efficiency and a fast transient response.

5.5 LED Driver

The IS2063 SoC has three LED drivers to control the LEDs. The LED drivers provide enough sink current (16-step control and 0.35 mA for each step) and the LED can be connected to the IS2063 SoC. The LED settings can be configured using the UI tool. Figure 5-2 illustrates the LED drivers in the IS2063 SoC.

FIGURE 5-2: LED DRIVER



5.6 Under Voltage Protection

When the voltage of the SYS_PWR pin drops below the voltage level of 2.9V, the system will shut-down automatically.

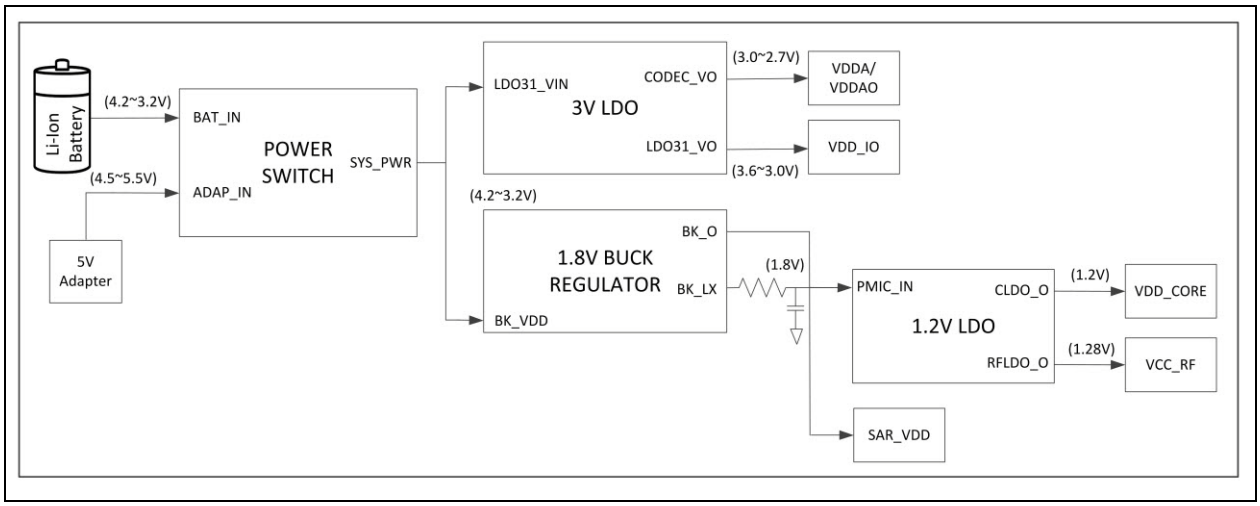
6.0 APPLICATION INFORMATION

6.1 Power Supply

Figure 6-1 illustrates the PCB connection from the BAT_IN pin to other voltage supply pins of the IS2063 SoC. The IS2063 SoC is powered through the BAT_IN input pin. If battery is not connected, an external power supply must be provided as an input to the ADAP_IN pin.

Note:	When an external power supply is connected to the ADAP_IN pin, the BAT_IN pin can be left open if battery is not connected.

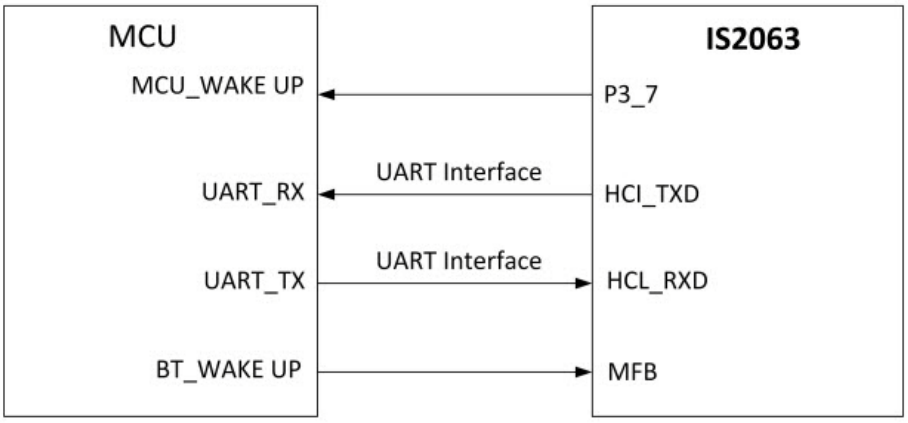
FIGURE 6-1: POWER TREE DIAGRAM



6.2 Host MCU Interface

Figure 6-2 illustrates the UART interface between the IS2063 SoC and an external MCU.

FIGURE 6-2: HOST MCU INTERFACE OVER UART



The MCU can control the IS2063 SoC over the UART interface and wake-up the IS2063 SoC using the MFB pins. The P3_7 pin can be used to wake-up the host MCU.

Refer to the "*UART_CommandSet*" document for a list of functions the IS2063 SoC supports and how to use the UI tool to set up the system using the UART command.

Note:	The *"UART_CommandSet"* document is available for download from Microchip web site at: www.microchip.com/IS2063.

Figure 6-3 through Figure 6-7 illustrate the timing sequences of various UART control signals.

FIGURE 6-3: POWER ON/OFF SEQUENCE

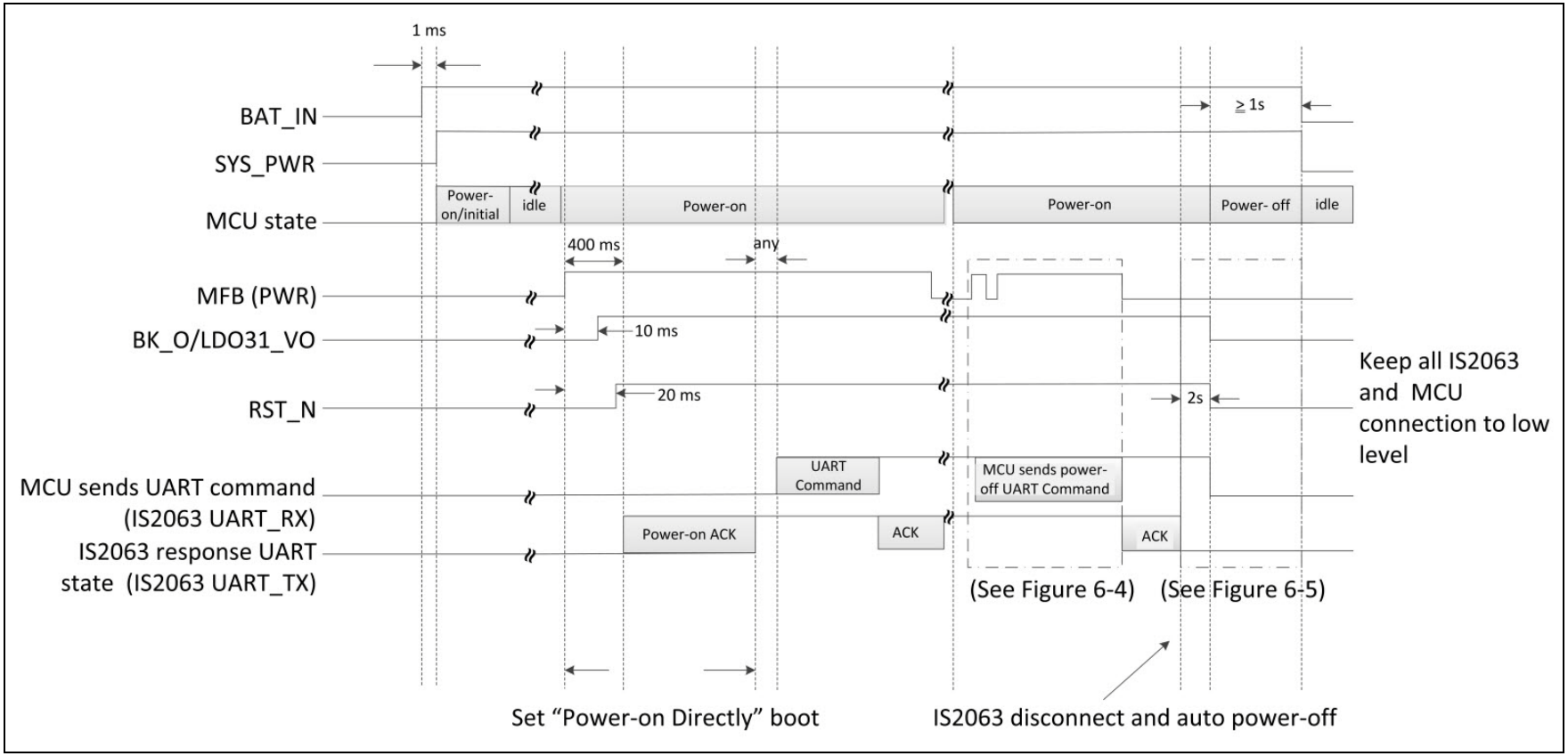


FIGURE 6-4: RX TIMING SEQUENCE (POWER-ON STATE)

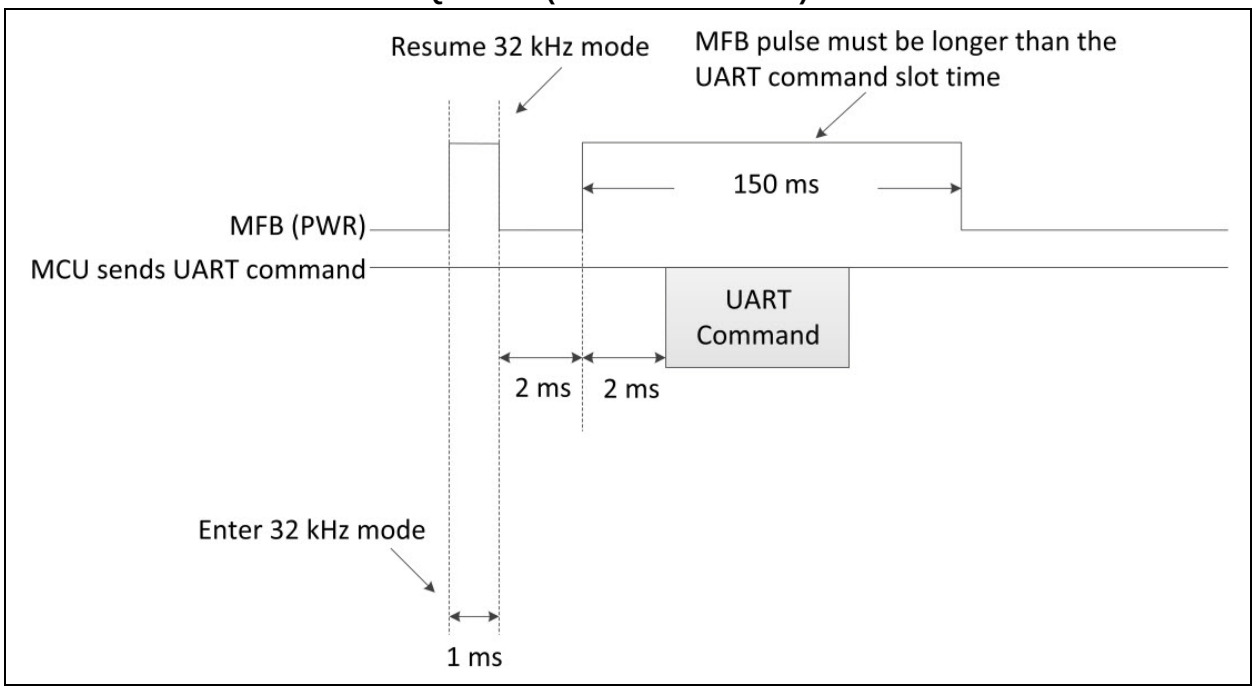
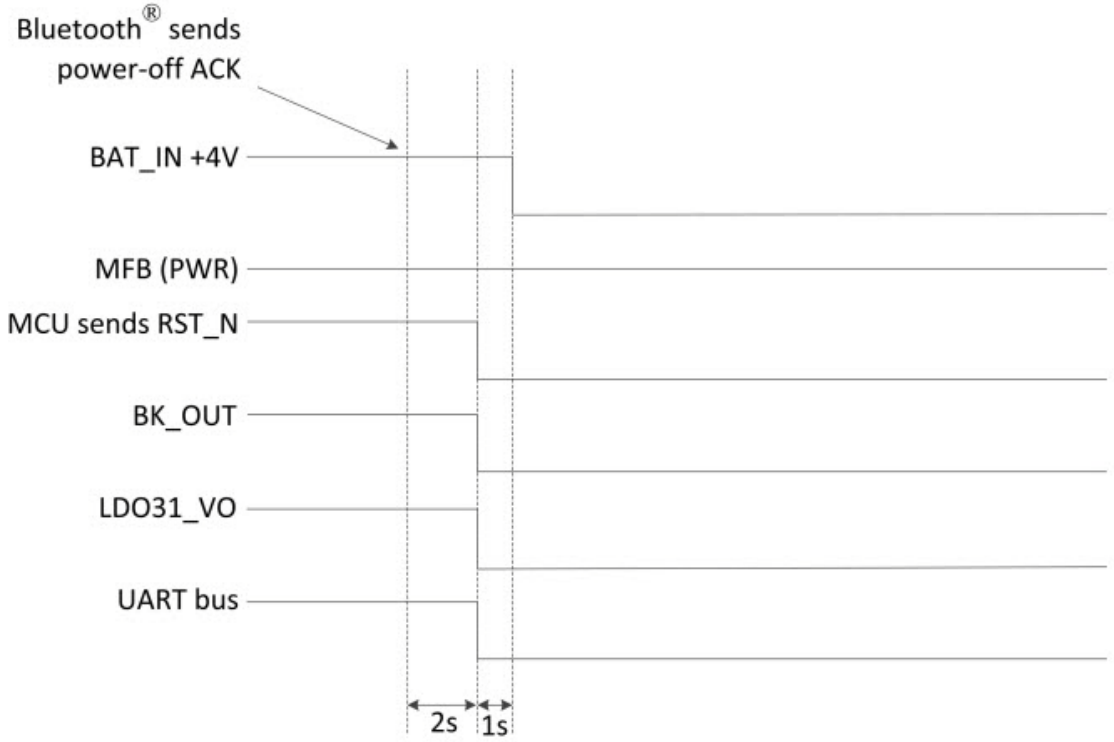


FIGURE 6-5: TIMING SEQUENCE (POWER-OFF STATE)



Note 1: EEPROM clock = 100 kHz.

2: For a byte write, 0.01 ms x 32 clock x 2 = 640 µs.

3: It is recommended to have a ramp-down time more than 640 µs during the power-off sequence to ensure a safe operation of the device.

FIGURE 6-6: TIMING SEQUENCE OF POWER-ON (NACK)

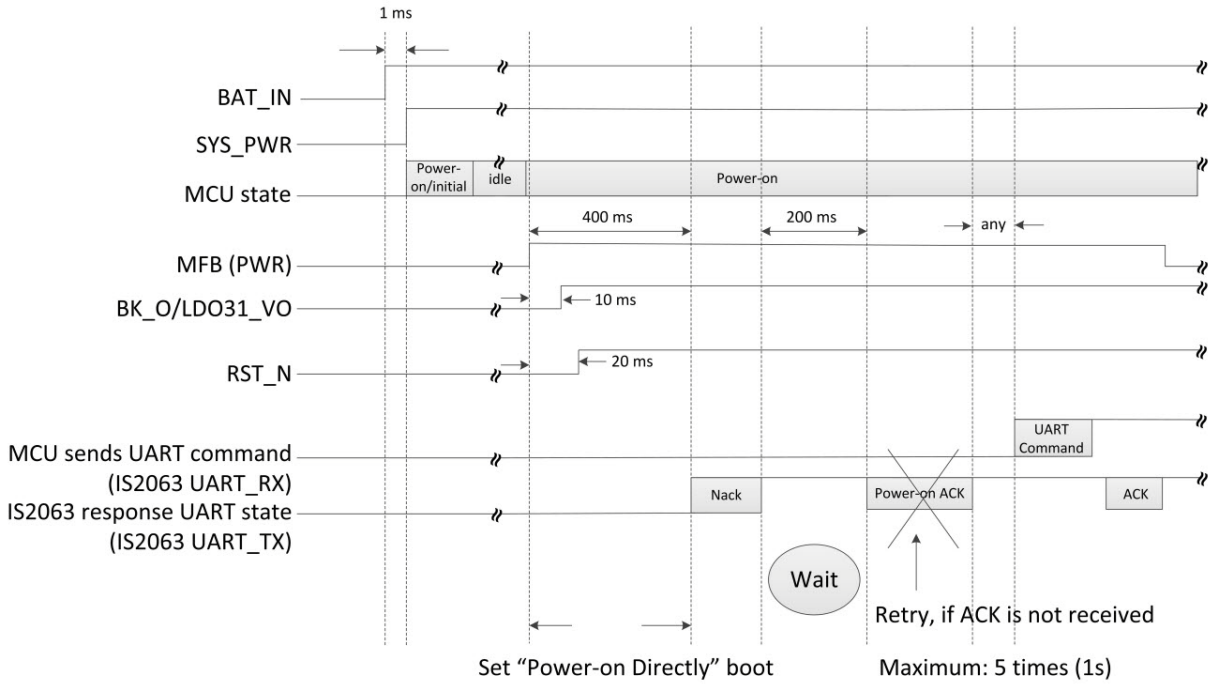
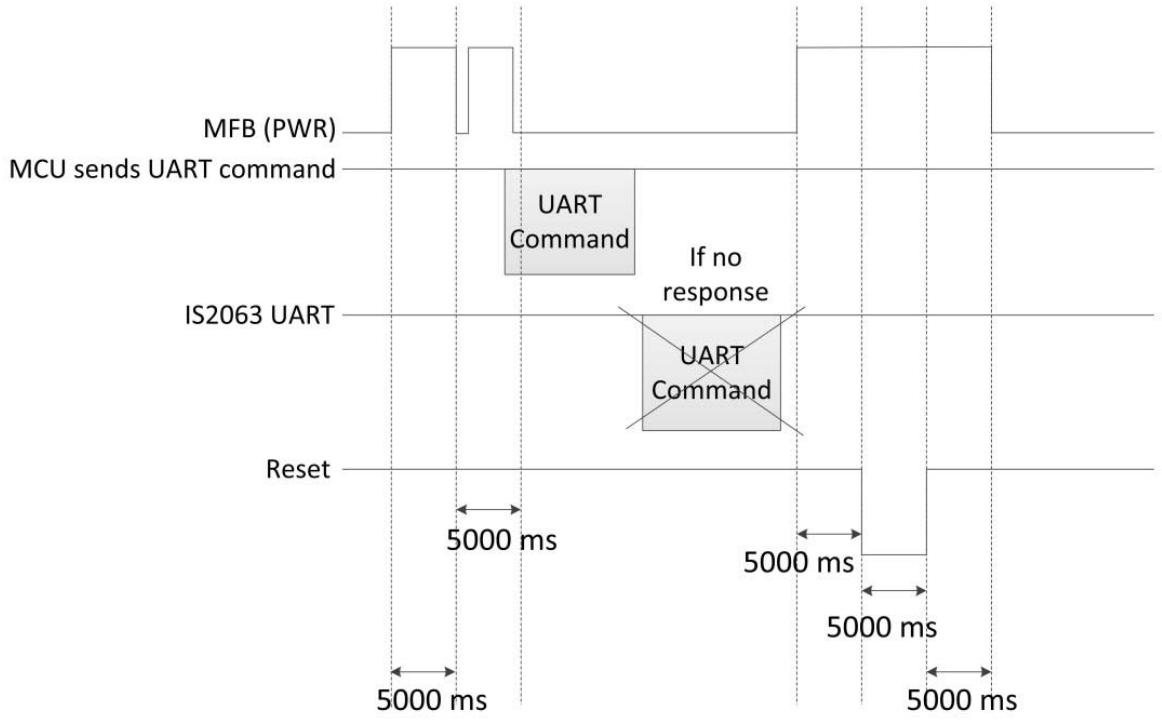


FIGURE 6-7: RESET TIMING SEQUENCE IN NO RESPONSE FROM SOC TO HOST MCU



Note: When the host MCU sends a UART command and the IS2063 SoC does not respond, the MCU resends the UART command. If the SoC does not respond within 5 secs, the MCU will force the system to Reset.

6.3 Configuration and Programming

Configuration and firmware programming modes are entered according to the system configuration I/O pins. Table 6-1 provides the system configuration settings. The P2_0, P2_4 and EAN pins have internal pull up.

TABLE 6-1: SYSTEM CONFIGURATION SETTINGS

P2_0	P2_4	EAN	Operating Mode
High	High	Flash code: Low; ROM code: High	APP mode (Normal operation)
Low	High	Flash code: Low; ROM code: High	Test mode (Write EEPROM)
Low	Low	High	Write Flash

6.4 General Purpose I/O Pins

The IS2063 SoC provides 10 GPIOs and these GPIOs can be configured using the UI tool. Table 6-2 and Table 6-3 provide the GPIO configuration details of the IS2063 SoC. The MFB pin must be configured as the power on/off key and the remaining pins can be configured for any one of the default functions as provided in Table 6-2 and Table 6-3.

TABLE 6-2: IS2063 I/O PIN CONFIGURATION

I/O pin name	Default Functions
MFB	Power on/off
P0_2	Play/Pause
P2_7	Volume up
P0_5	Volume down
P3_3	FWD
P3_1	REV

Some pins can be configured to indicate or control the external devices. The most popular applications are NFC for easy pairing and Buzzer for indication and external audio amplifier for loud speaker.

TABLE 6-3: IS2063 I/O PIN (FOR ADDITIONAL FUNCTIONS)

I/O Configurable Features	Functions
P0_0/P1_5	Slide switch
P0_4	NFC detect
P0_0/P0_4	External AMP enable

6.5 I²S Mode Application

The IS2063 SoC provides an I²S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I²S setting can be configured using the UI and DSP tools.

Note: The DSP and UI tools are available for download from the Microchip web site at: www.microchip.com/IS2063.

The external codec or DSP interfaces with these pins: SCLK0, RFS0, DR0 and DT0 (pin nos. 3, 2, 1, and 4 respectively). Figure 6-8 and Figure 6-9 illustrate the I²S connection between the IS2063 SoC and an external DSP. Use the DSP tool to configure the IS2063 SoC as a master/slave.

For additional information on timing specifications, refer to **8.1 "Timing specifications"**.

FIGURE 6-8: IS2063 IN I²S MASTER MODE

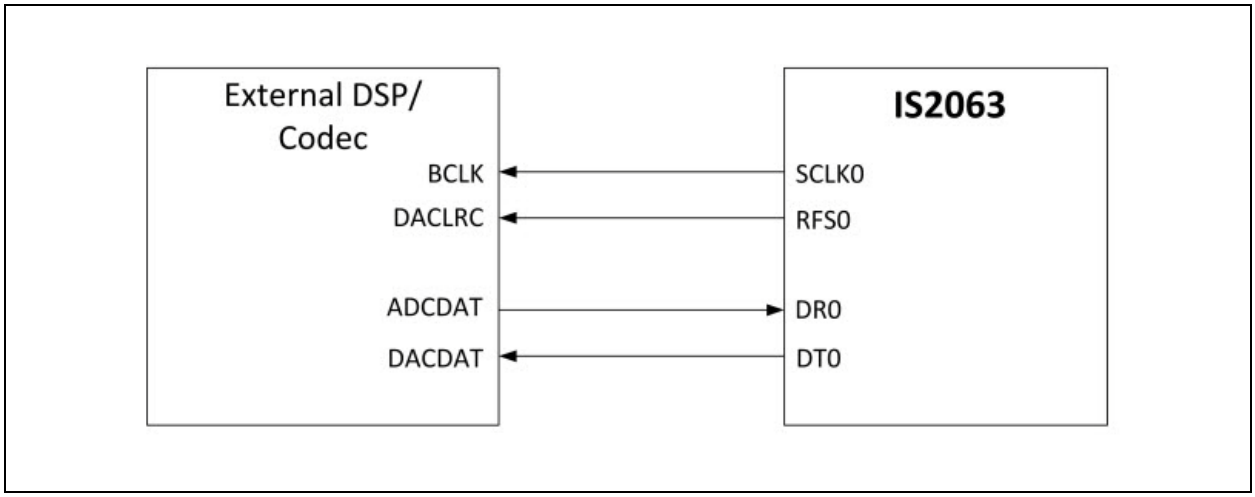
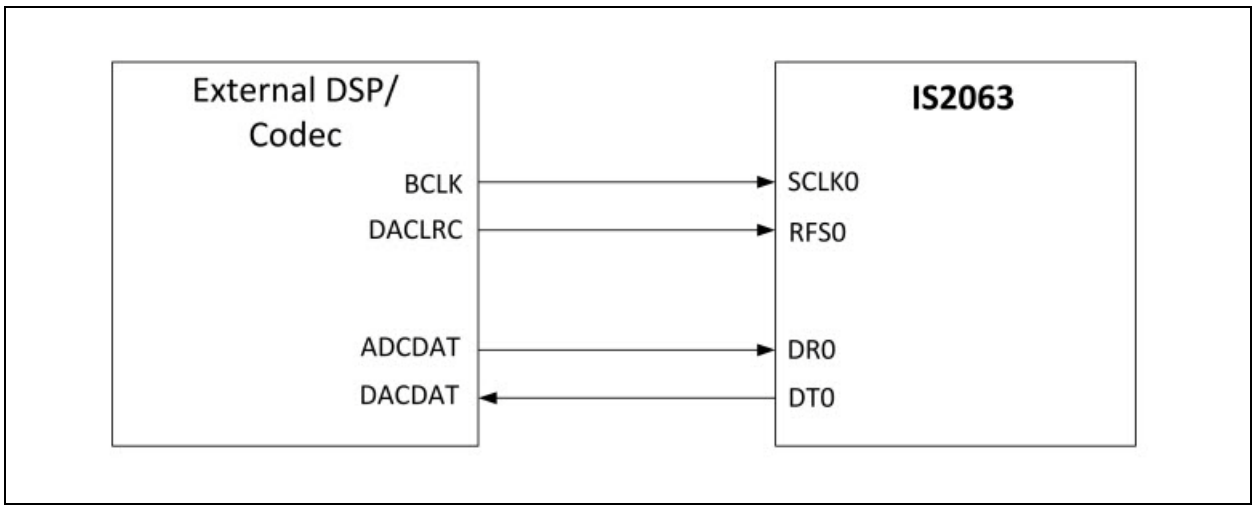


FIGURE 6-9: IS2063 IN I²S SLAVE MODE



NOTES:

7.0 ANTENNA PLACEMENT RULE

For Bluetooth-enabled products, the antenna placement affects the overall performance of the system. The antenna requires free space to radiate RF signals and it should not be surrounded by the ground plane.

Figure 7-1 illustrates a typical example of good and poor antenna placement on the main application board with the ground plane.

FIGURE 7-1: ANTENNA PLACEMENT EXAMPLES

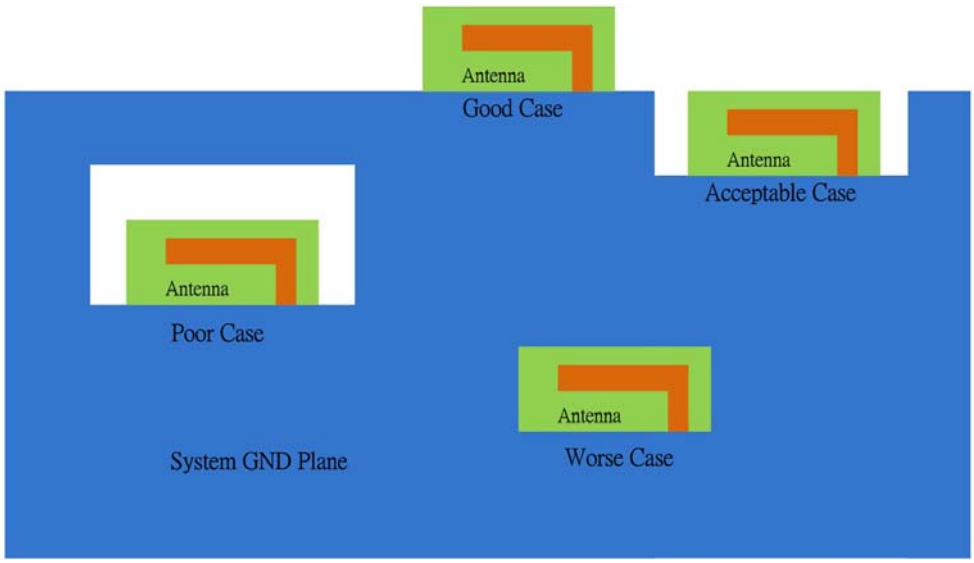
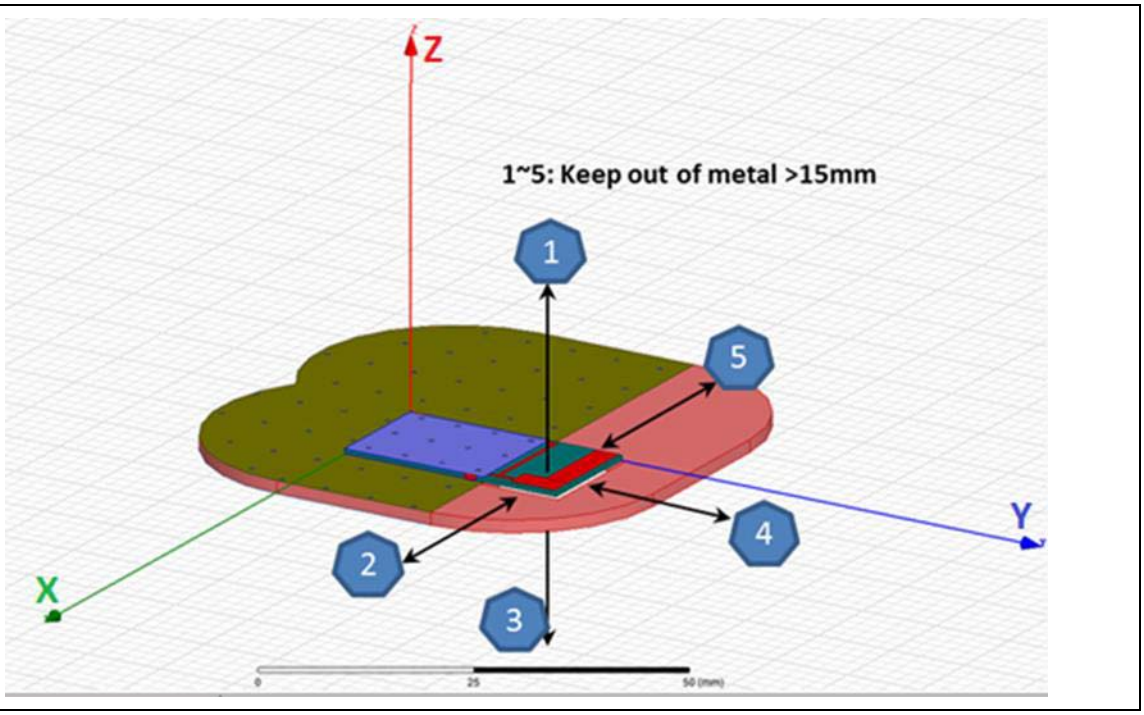


Figure 7-2 illustrates the recommended keep-out area for the PCB antenna.

FIGURE 7-2: KEEP OUT AREA RECOMMENDED FOR PCB ANTENNA



For additional information on the antenna placement, refer to the specific antenna data sheet of the antenna manufacturer.

NOTES:

8.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the IS2063 Stereo Audio SoC electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the IS2063 device are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

Ambient temperature under bias ..... -20°C to +70°C
Storage temperature ..... -65°C to +150°C
Digital core supply voltage VDD_CORE ..... 0V to +1.35V
RF supply voltage VCC_RF ..... 0V to +1.35V
SAR ADC supply voltage SAR_VDD ..... 0V to +2.1V
Codec supply voltage VDDA/VDDAO ..... 0V to +3.3V
Buck supply voltage BK_VDD ..... 0V to +4.3V
Supply voltage LDO31_VIN ..... 0V to +4.3V
Battery input voltage BAT_IN ..... 0V to +4.3V
Adapter input voltage ADAP_IN ..... 0V to +7V

Note: Stresses listed under "**Absolute Maximum Ratings**" may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8-1 through Table 8-9 provide the recommended operating conditions and the electrical specifications of the IS2063 SoC.

TABLE 8-1: RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typical	Max.	Unit
VDD_CORE	Digital core supply voltage	1.14	1.2	1.26	V
VCC_RF	RF supply voltage	1.22	1.28	1.34	V
SAR_VDD	SAR ADC supply voltage	1.62	1.8	1.98	V
VDDA/VDDAO	Codec supply voltage	1.8	2.8	3.0	V
VDD_IO	I/O supply voltage	3.0	3.3	3.6	V
BK_VDD	Buck supply voltage	3	3.8	4.25	V
LDO31_VIN	Supply voltage	3	3.8	4.25	V
BAT_IN	Input voltage for battery	3.2	3.8	4.25	V
ADAP_IN	Input voltage for adapter	4.5	5	5.5	V
$T_{OPERATION}$	Operation temperature	-20	+25	+70	ºC

Note: The PMU output powers, BK_O, CODEC_VO, RFLDO_O and CLDO_O, can be programmed through the EEPROM parameters.

TABLE 8-2: BUCK REGULATOR(2)

Parameter	Min.	Typical	Max.	Unit
Input Voltage	3.0	3.8	4.25	V
Output Voltage (I_{load} = 70 mA, V_{in} = 4V)	1.7	1.8	2.05	V
Output Voltage Accuracy	–	±5	–	%
Output Voltage Adjustable Step	–	50	–	mV/Step
Output Adjustment Range	-0.1	–	+0.25	V
Average Load Current (I_{LOAD})	120	–	–	mA
Conversion efficiency (BAT = 3.8V, I_{load} = 50 mA)	–	88(1)	–	%
Quiescent Current (PFM)	–	–	40	µA
Output Current (peak)	200	–	–	mA
Shutdown Current	–	–	<1	µA

Note 1: Test condition: Temperature +25 ºC and wired inductor 10 µH.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-3: LOW DROP REGULATOR(1,2)

Parameter		Min.	Typical	Max.	Unit
Input Voltage		3.0	3.8	4.25	V
Output Voltage	CODEC_VO	–	2.8	–	V
	LDO31_VO	–	3.3	–	
Output Accuracy (V_{IN} = 3.7V, I_{LOAD} = 100 mA, +27 ºC)		–	±5	–	%
Output current (average)		–	–	100	mA
Drop-out voltage (I_{load} = maximum output current)		–	–	300	mV
Quiescent Current (excluding load, I_{load} < 1 mA)		–	45	–	µA
Shutdown Current		–	–	<1	µA

Note 1: Test condition: Temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-4: BATTERY CHARGER(1,3)

Parameter		Min.	Typical	Max.	Unit
Input Voltage (ADAP_IN)		4.5	5.0	5.5	V
Supply current to charger only		–	3	4.5	mA
Maximum Battery Fast Charge Current	Headroom > 0.7V (ADAP_IN = 5V)	–	350	–	mA
	Headroom = 0.3V~0.7V (ADAP_IN = 4.5V) **(Note 2)**	–	175	–	mA
Trickle Charge Voltage Threshold		–	3	–	V
Battery Charge Termination Current, (% of Fast Charge Current)		–	10	–	%

Note 1: Headroom = V_{ADAP_IN} - V_{BAT}.

2: When V_{ADAP_IN} - V_{BAT} > 2V, the maximum fast charge current is 175 mA for thermal protection.

3: These parameters are characterized but not tested in manufacturing.

TABLE 8-5: LED DRIVER(1,2)

Parameter	Min.	Typical	Max.	Unit
Open-drain Voltage	–	–	3.6	V
Programmable Current Range	0	–	5.25	mA
Intensity Control	–	16	–	step
Current Step	–	0.35	–	mA
Power Down Open-drain Current	–	–	1	µA
Shutdown Current	–	–	1	µA

Note 1: Test condition: BK_O = 1.8V, temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-6: AUDIO CODEC DIGITAL TO ANALOG CONVERTER(4)

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz					
Parameter (Condition)		**Min.**	**Typical**	**Max.**	**Unit**
Output Sampling Rate		–	128	–	f_s
Resolution		16	–	20	Bit
Output Sample Rate		8	–	48	kHz
Signal to Noise Ratio **(Note 1)** (SNR @capless mode) for 48 kHz		–	96	–	dB
Signal to Noise Ratio **(Note 1)** (SNR @single-ended mode) for 48 kHz		–	98	–	dB
Digital Gain		-54	–	4.85	dB
Digital Gain Resolution		–	2~6	–	dB
Analog Gain		-28	–	3	dB
Analog Gain Resolution		–	1	–	dB
Output Voltage Full-scale Swing (AVDD = 2.8V)		495	742.5	–	mV/rms
Maximum Output Power (16 Ohm load)		–	34.5	–	mW
Maximum Output Power (32 Ohm load)		–	17.2	–	mW
Allowed Load	Resistive	–	16	O.C.	Ohm
	Capacitive	–	–	500	pF
THD+N (16 Ohm load) **(Note 2)**		–	0.05	–	%
Signal to Noise Ratio (SNR @ 16 Ohm load) **(Note 3)**	–	–	98	–	dB

Note 1: f_{in}=1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load = 100 kOhm.

2: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, -1dBFS signal, Load = 16 Ohm.

3: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 0.05%, 0dBFS signal, Load = 16 Ohm.

4: These parameters are characterized but not tested in manufacturing.

TABLE 8-7: AUDIO CODEC ANALOG TO DIGITAL CONVERTER(2)

T = +25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz				
Parameter (Condition)	**Min.**	**Typical**	**Max.**	**Unit**
Resolution	–	–	16	Bit
Output Sample Rate	8	–	48	kHz
Signal to Noise Ratio **(Note 1)** (SNR @MIC or Line-in mode)	–	92	–	dB
Digital Gain	-54	–	4.85	dB
Digital Gain Resolution	–	2~6	–	dB
MIC Boost Gain	–	20	–	dB
Analog Gain	–	–	60	dB
Analog Gain Resolution	–	2.0	–	dB
Input full-scale at maximum gain (differential)	–	4	–	mV/rms
Input full-scale at minimum gain (differential)	–	800	–	mV/rms
3 dB bandwidth	–	20	–	kHz
Microphone mode (input impedance)	–	24	–	kOhm
THD+N (microphone input) at 30mVrms input	–	0.02	–	%

Note 1: f_{in}=1 kHz, B/W=20~20 kHz, A-weighted, THD+N < 1%, 150 mV_{pp} input.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-8: TRANSMITTER SECTION FOR BDR AND EDR(1,2)

Parameter	**Min.**	**Typical**	**Max.**	**Bluetooth specification**	**Unit**
Maximum RF Transmit power	–	2(3)	–	-6 to 4	dBm
EDR/BDR Relative transmit power	-4	-1.8	1	-4 to 1	dB

Note 1: The RF TX power is modulation value.

2: The RF Transmit power is calibrated during production using MP tool and MT8852 Bluetooth Test equipment.

3: Test condition: VCC_RF = 1.28V, temperature +25 ºC.

TABLE 8-9: RECEIVER SECTION FOR BDR AND EDR(1,2)

	Modulation	**Min.**	**Typical**	**Max.**	**Bluetooth specification**	**Unit**
Sensitivity at 0.1% BER	GFSK	–	-89	–	≤-70	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	–	-90	–	≤-70	dBm
	8 DPSK	–	-83	–	≤-70	dBm

Note 1: Test condition: VCC_RF = 1.28V, temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

8.1 Timing specifications

Figure 8-1 and Figure 8-2 illustrate the timing diagram of the IS2063 SoC in I^2S and PCM modes.

FIGURE 8-1: TIMING DIAGRAM FOR I^2S MODES (MASTER/SLAVE)

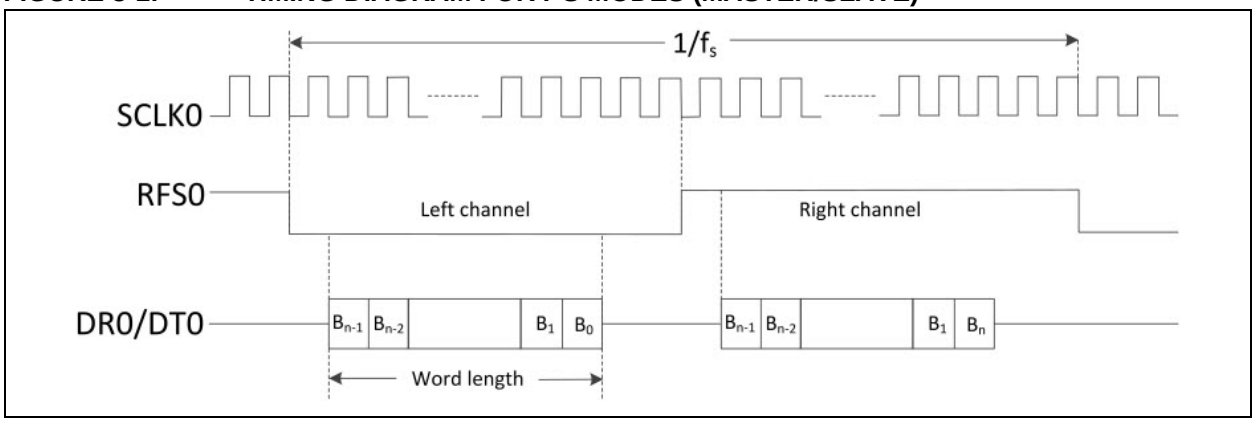
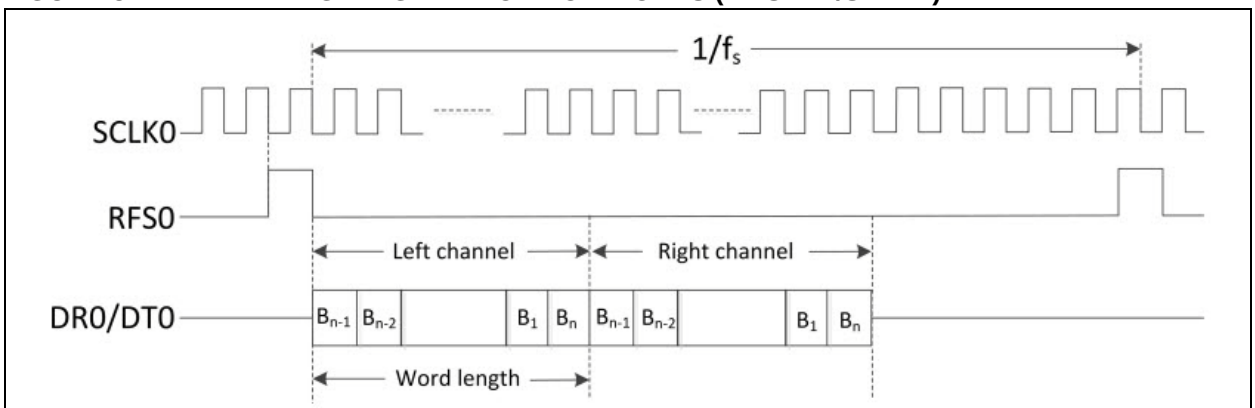


FIGURE 8-2: TIMING DIAGRAM FOR PCM MODES (MASTER/SLAVE)



Note 1: f_s: 8,16, 32, 44.1, 48, 88.2 and 96 kHz.

2: SCLK0: $64*f_s/256*f_s$.

3: Word length: 16-bit and 24-bit.

Figure 8-3 illustrates the audio interface timing diagram and Table 8-10 provides the audio interface timing specifications.

FIGURE 8-3: AUDIO INTERFACE TIMING

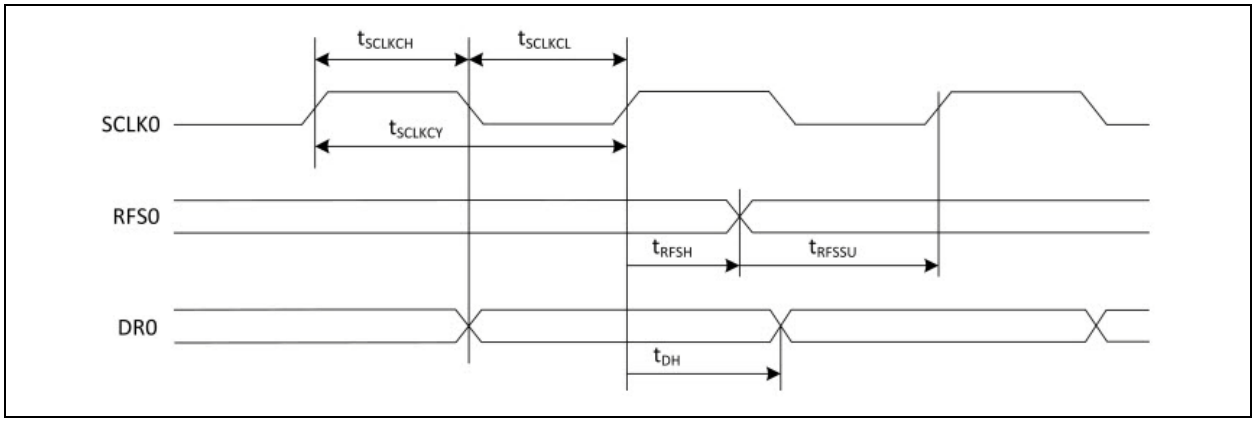


TABLE 8-10: AUDIO INTERFACE TIMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT
SCLK0 duty ratio	d_{SCLK}	–	50	–	%
SCLK0 cycle time	t_{SCLKCY}	50	–	–	ns
SCLK0 pulse width high	t_{SCLKCH}	20	–	–	ns
SCLK0 pulse width low	t_{SCLKCL}	20	–	–	ns
RFS0 set-up time to SCLK0 rising edge	t_{RFSSU}	10	–	–	ns
RFS0 hold time from SCLK0 rising edge	t_{RFSH}	10	–	–	ns
DR0 hold time from SCLK0 rising edge	t_{DH}	10	–	–	ns

Note: Test Conditions: Slave Mode, f_s = 48 kHz, 24-bit data and SCLK0 period = 256 f_s.

NOTES:

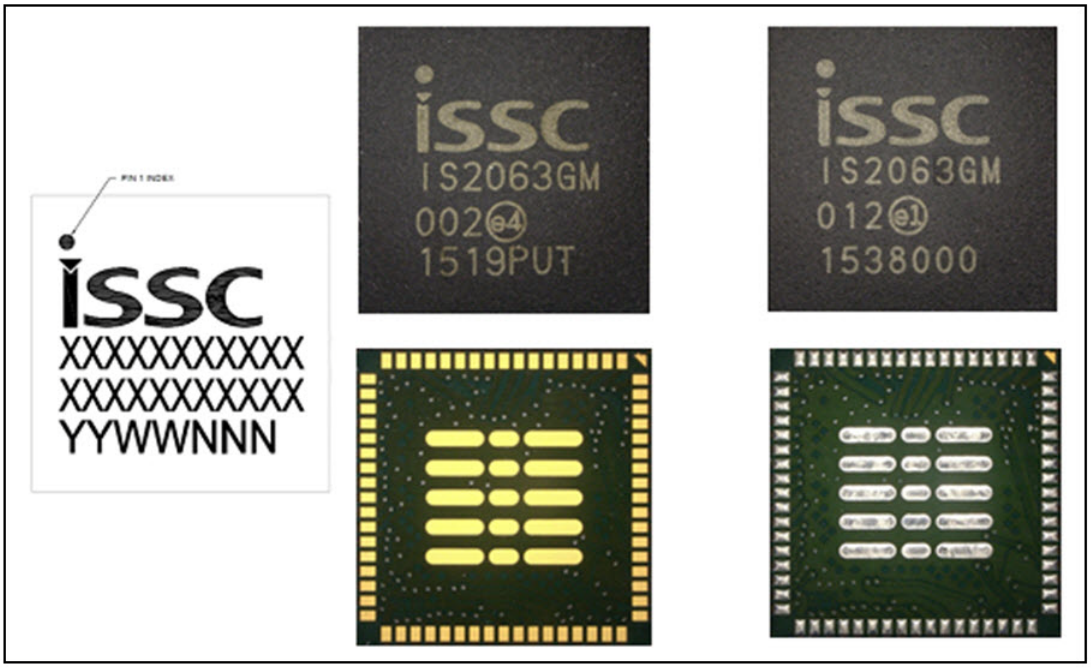
9.0 PACKAGE INFORMATION

9.1 Package Marking Information

Figure 9-1 illustrates the package marking information of the IS2063 SoC.

FIGURE 9-1: PACKAGE MARKING INFORMATION

68 LGA (8x8x0.9 mm) Example



Legend:
XXX: Chip serial number version and
(e1) Pb-free JEDEC designator for SAC305(*1)
(e4) Pb-free JEDEC designator for NiAu

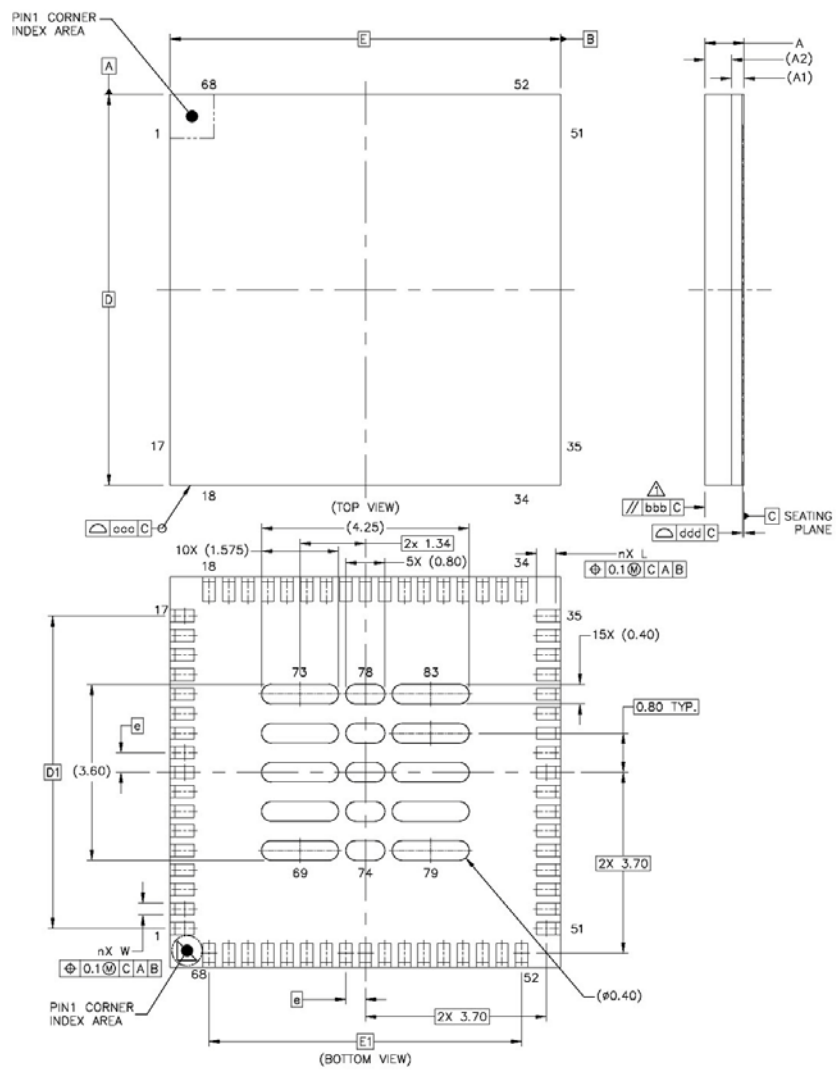
YY: Year code (last 2 digits of calendar year)
WW: Week code (week of January 1 is week "01")
NNN: Alphanumeric traceability code

Note:
(1) SAC305 is the pre-solder version. Customer need to take care solder paste before screen printing.

9.2 Package Details

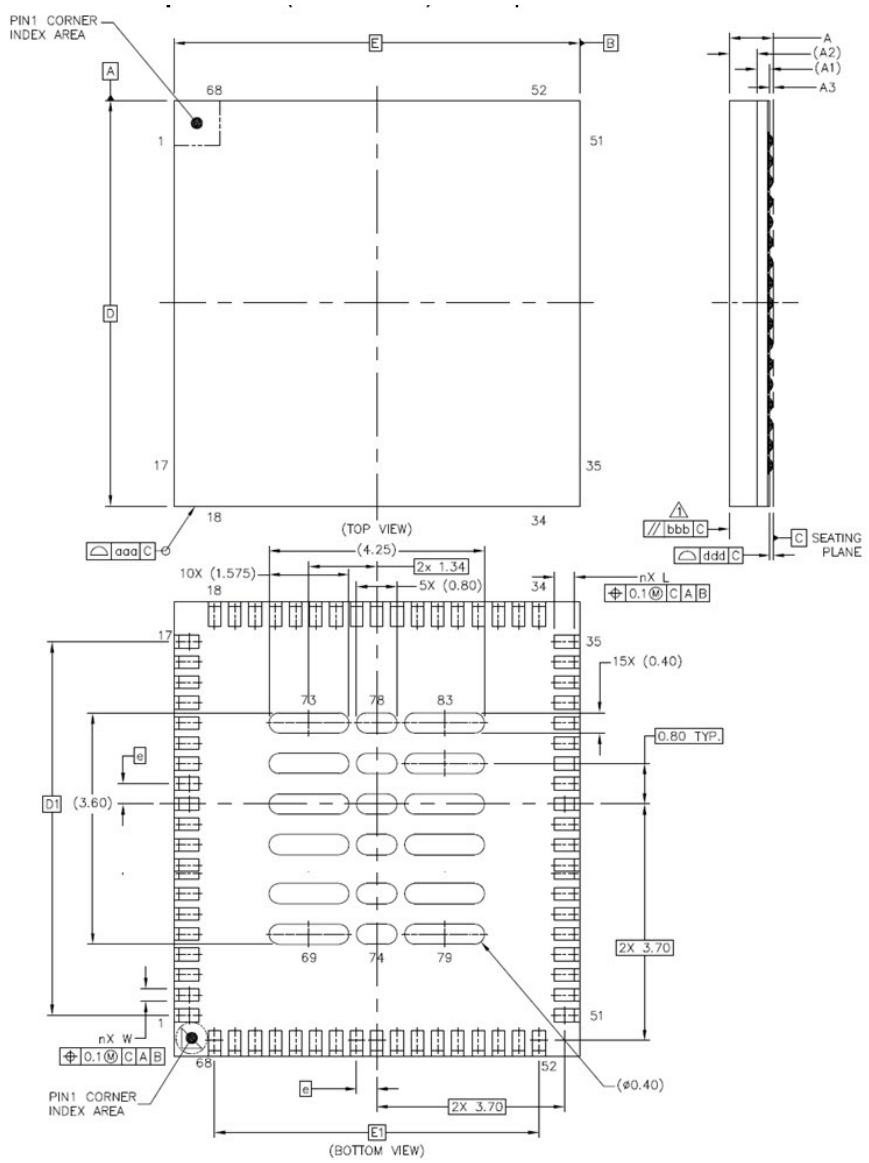
Figure 9-2 and Figure 9-3 illustrate the package details of the IS2063 SoC.

FIGURE 9-2: IS2063 - NIAU PACKAGE DETAILS



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.9
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		8	BSC
	E		8	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		68	
EDGE BALL CENTER TO CENTER	D1		6.4	BSC
	E1		6.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PITCH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

FIGURE 9-3: IS2063 - SAC305 PACKAGE DETAILS



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1
SUBSTRATE THICKNESS	A1		0.26	REF
MOLD THICKNESS	A2		0.54	REF
BODY SIZE	D		8	BSC
	E		8	BSC
LEAD WIDTH	W	0.2	0.25	0.3
LEAD LENGTH	L	0.35	0.4	0.45
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		68	
EDGE BALL CENTER TO CENTER	D1		6.4	BSC
	E1		6.4	BSC
BODY CENTER TO CONTACT BALL	SD		---	BSC
	SE		---	BSC
BALL WIDTH	b	---	---	---
BALL DIAMETER			---	
BALL OPENING			---	
BALL PICTH	e1		---	
BALL COUNT	n1		---	
PRE-SOLDER	A3	0.02	---	0.1
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

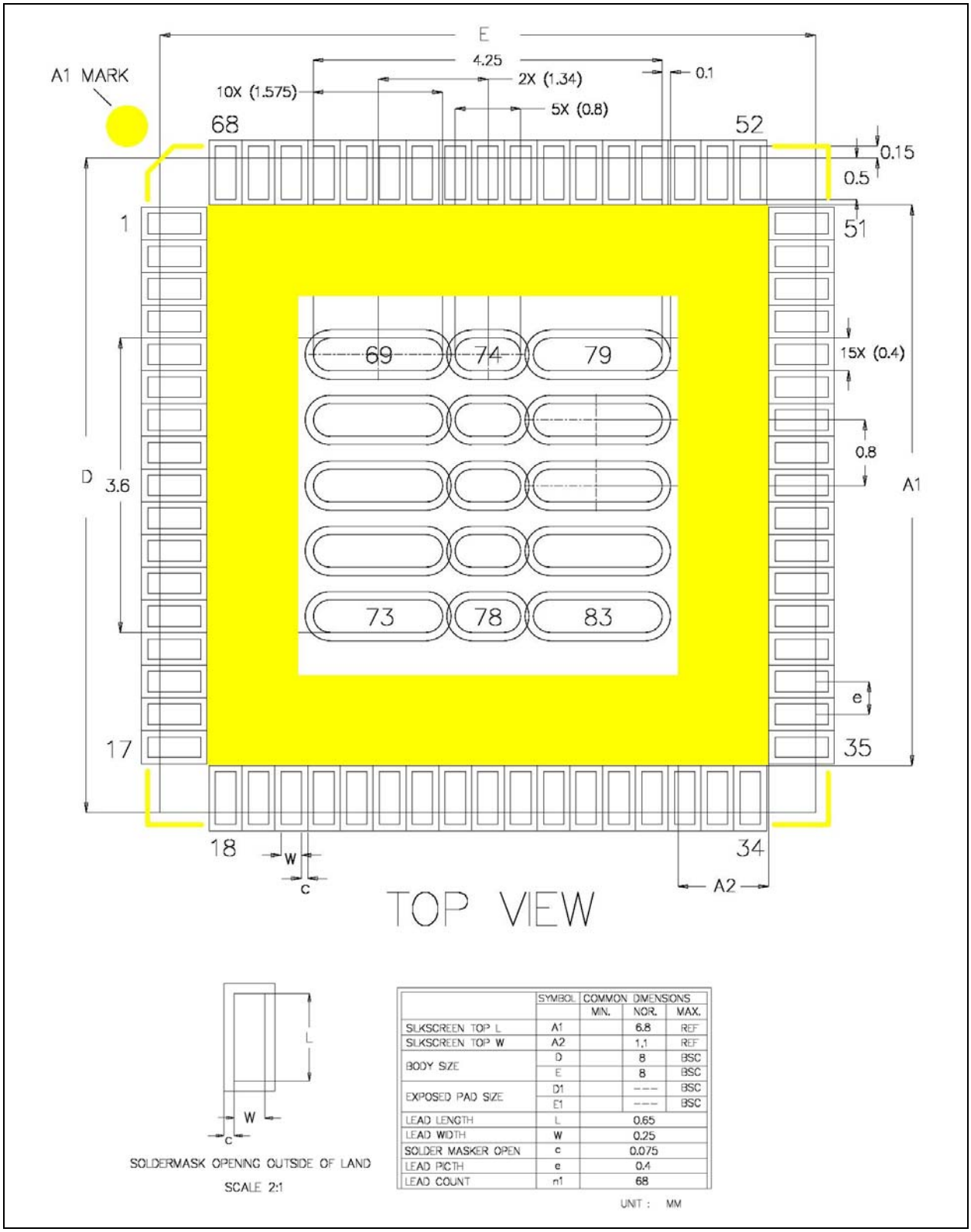
NOTES:

⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

9.3 Footprint Dimensions

Figure 9-4 illustrates the footprint dimensions of the IS2063 SoC.

FIGURE 9-4: IS2063 FOOTPRINT DIMENSIONS



	SYMBOL	COMMON DIMENSONS		
		MIN.	NOR.	MAX.
SILKSCREEN TOP L	A1		6.8	REF
SILKSCREEN TOP W	A2		1.1	REF
BODY SIZE	D		8	BSC
	E		8	BSC
EXPOSED PAD SIZE	D1		---	BSC
	E1		---	BSC
LEAD LENGTH	L		0.65	
LEAD WIDTH	W		0.25	
SOLDER MASKER OPEN	c		0.075	
LEAD PICTH	e		0.4	
LEAD COUNT	n1		68	

UNIT : MM

10.0 REFLOW PROFILE AND STORAGE CONDITION

Figure 10-1 and Figure 10-2 illustrate the reflow profiles and stencil information of the IS2063 SoC.

10.1 Stencil of SMT Assembly Suggestion

10.1.1 STENCIL TYPE AND THICKNESS

- Laser cutting
- Stainless steel
- Thickness: 0.5 mm pitch, thickness more than 0.15 mm

10.1.2 APERTURE SIZE AND SHAPE FOR TERMINAL PAD

- Aspect ratio (width/thickness) is more than 1.5
- Aperture shape
  - The stencil aperture is designed to match the pad size on the PCB
  - Oval-shape opening is used to get the optimum paste release
  - Rounded corners to minimize the clogging
  - Positive taper walls (5° tapering) with the bottom opening larger than the top opening

10.1.3 APERTURE DESIGN FOR THERMAL PAD

- Small multiple openings are used instead of one big opening, refer Figure 10-1
- 60 to 80% solder paste coverage
- Rounded corners to minimize clogging
- Positive taper walls (5° tapering) with the bottom opening larger than the top opening, see Figure 10-2

FIGURE 10-1: REFLOW PROFILE APERTURE DESIGN

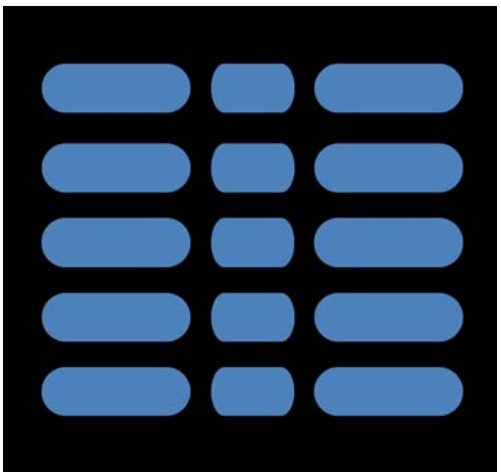
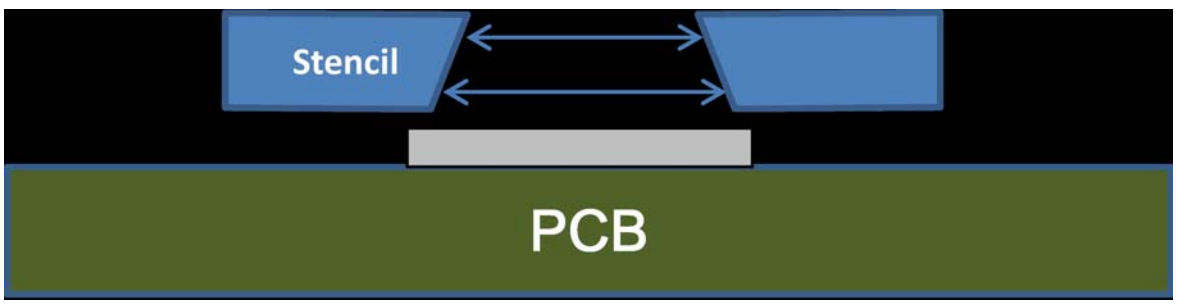


FIGURE 10-2: STENCIL TYPE

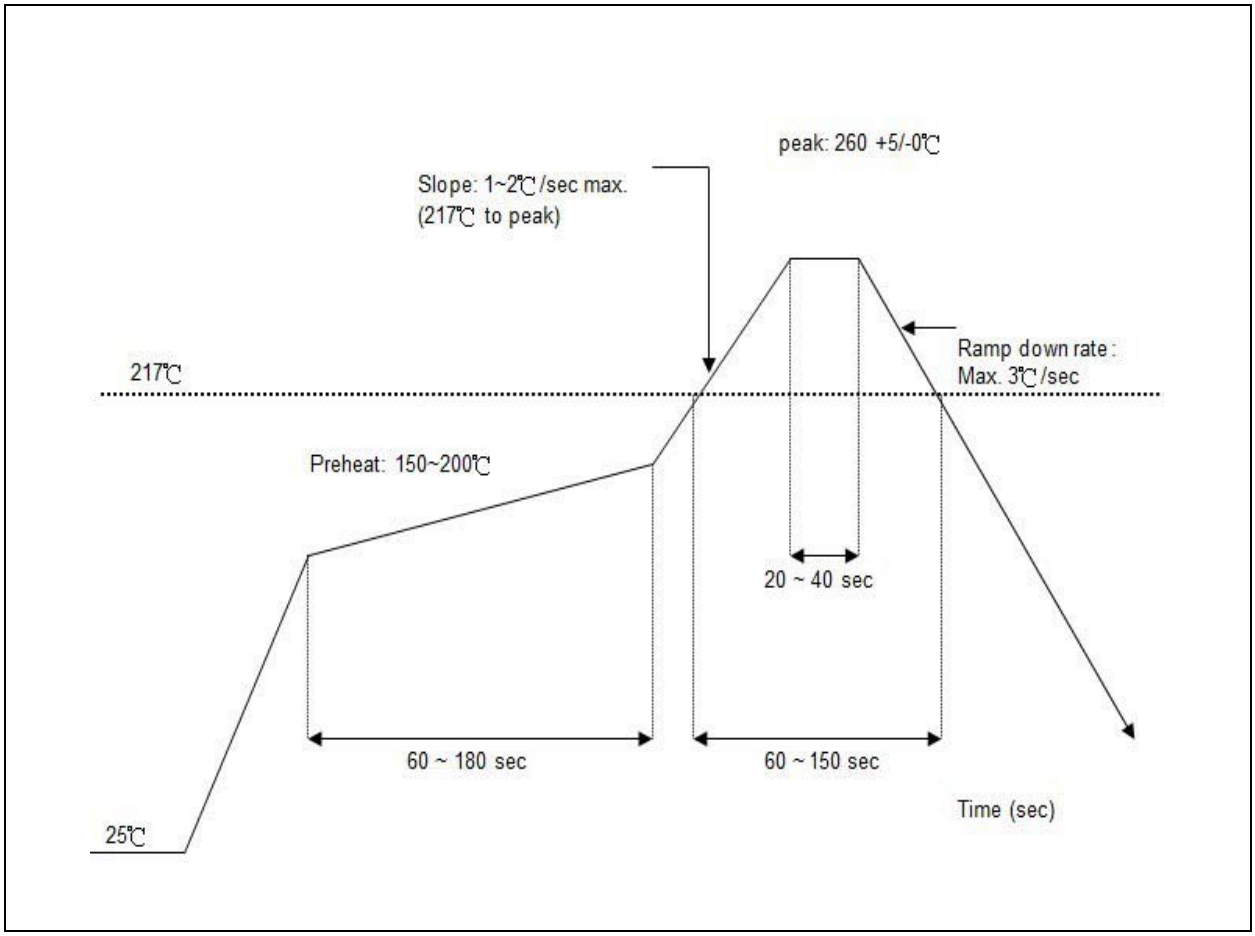


10.2 Reflow Condition

Figure 10-3 illustrates the reflow profile and the following are its specific features:

- Standard condition: IPC/JEDEC J-STD-020
- Preheat: 150~200 ℃ ~60~180 seconds
- Average ramp-up rate (+217 ℃ to peak): 1~2 ℃ /sec max
- Temperature maintained above 217: 60~150 seconds
- Time within +5℃ of actual peak temperature: 20 ~ 40 seconds
- Peak temperature: 260 +5/-0 ℃
- Ramp-down rate (peak to +217℃): +3℃/sec. max
- Time +25 ℃ to peak temperature: 8 minutes max
- Cycle interval: 5 minutes

FIGURE 10-3: REFLOW PROFILE



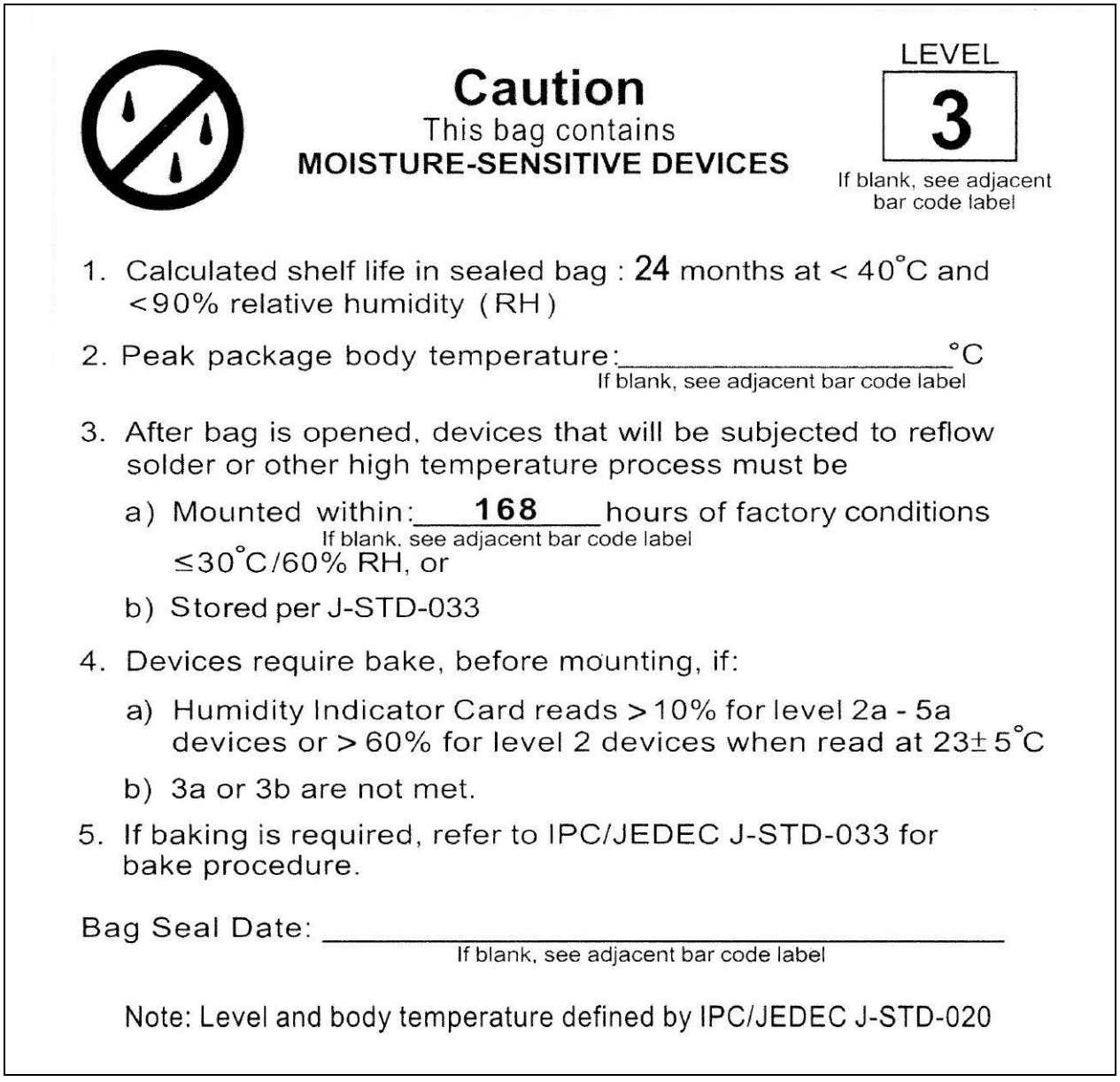
10.3 Storage Condition

Users must follow these specific storage conditions for the IS2063 SoC.

- Calculated shelf life in the sealed bag: 24 months at <40 ℃ and <90% relative humidity (RH).
- Once the bag is opened, devices that are subjected to reflow solder or other high temperature process must be mounted within 168 hours of factory conditions, that is <30 ℃ /60% RH.

Figure 10-4 illustrates the IS2063 SoC bag labeling details.

FIGURE 10-4: IS2063 SOC STORAGE CONDITIONS



NOTES:

11.0 ORDERING INFORMATION

Table 11-1 provides the ordering information of the IS2063 SoC.

TABLE 11-1: ORDERING INFORMATION

Device	Bluetooth Version	Package	Part Number
IS2063	Bluetooth 4.2, BDR/EDR/BLE SoC with integrated 1 microphone and stereo speaker output, and I^2S digital interface	8 x 8 x 0.9 mm, 68-LGA package	IS2063GM

Note: The IS2063 SoC can be purchased through a Microchip representative. Go to http://www.microchip.com/ for the ordering information.

NOTES:

APPENDIX A: REFERENCE CIRCUIT

Figure A-1 through Figure A-4 illustrate the IS2063 reference schematics for the stereo headset application.

FIGURE A-1: IS2063 REFERENCE CIRCUIT FOR STEREO HEADSET

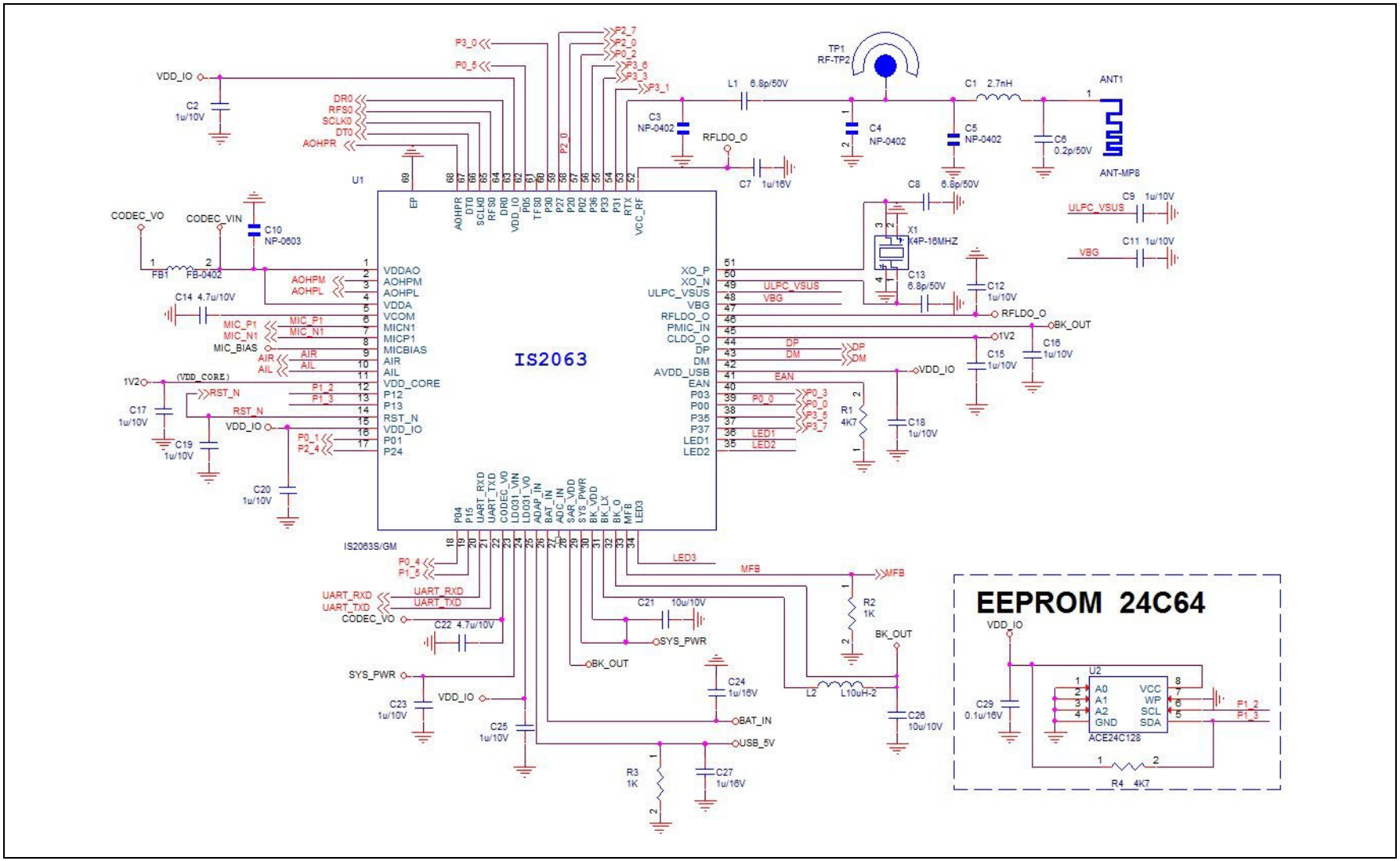
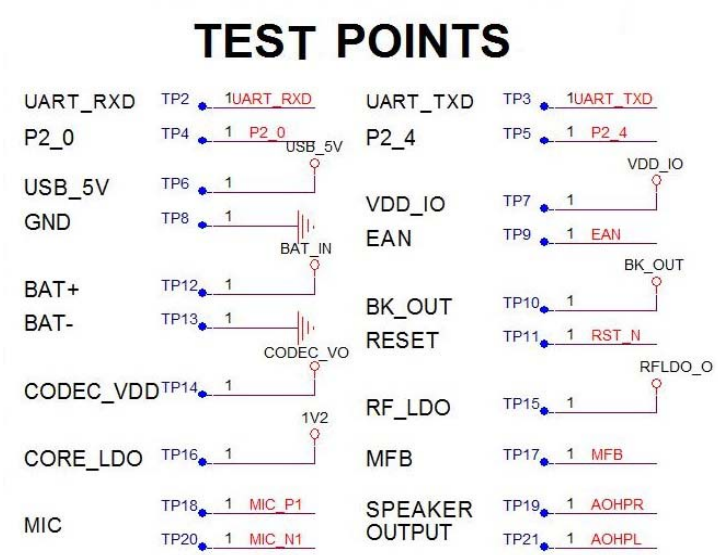


FIGURE A-2: IS2063 REFERENCE CIRCUIT FOR STEREO HEADSET



GPIO DESCRIPTION

MFB	UART_RX_IND; MFB
P0_0	SLIDE SWITCH
P0_2	PLAY/PAUSE
P0_4	AMP_EN/NFC
P0_5	VOL-
P2_7	VOL+
P0_3	REV
P0_1	FWD
P3_0	AUX IN Detection
P3_7	UART_TX_IND
P1_5	AMP_EN/SLIDE SWITCH
	Multi-SPK Master/Slave mode control
P3_6	Multi-SPK Master/Slave mode control
P2_0	System Configuration
EAN	System Configuration

FIGURE A-3: IS2063 REFERENCE CIRCUIT FOR STEREO HEADSET

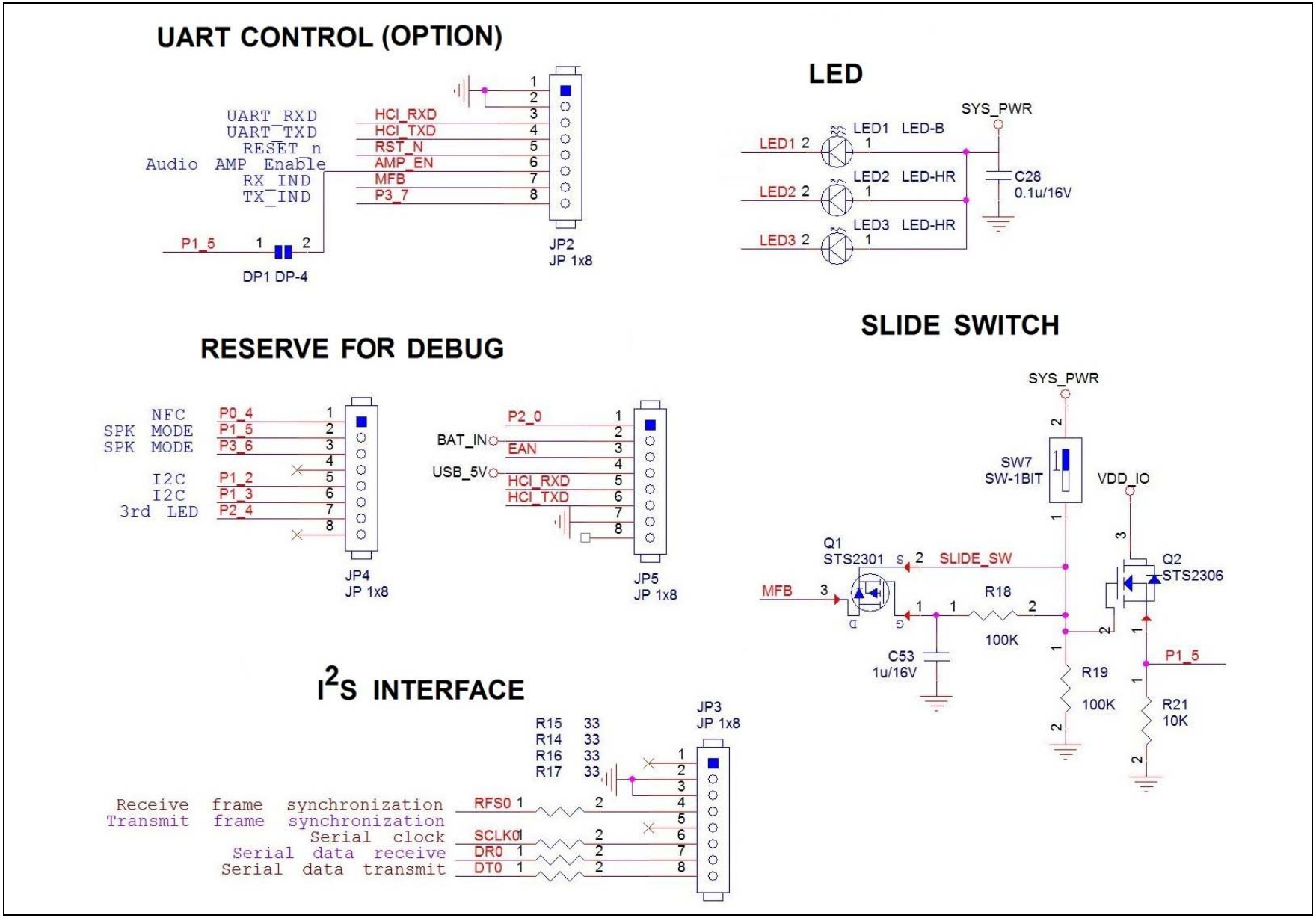
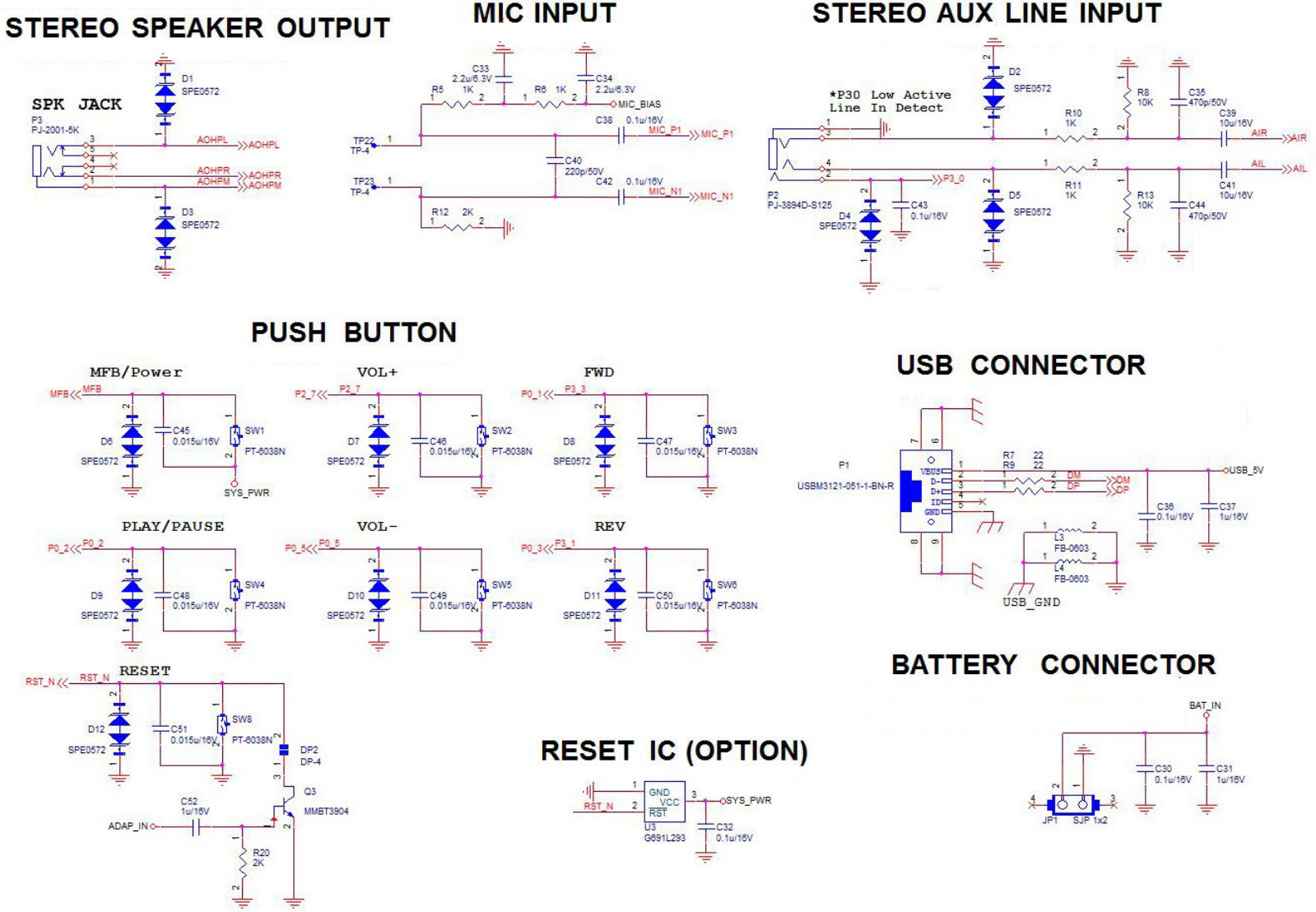


FIGURE A-4: IS2063 REFERENCE CIRCUIT FOR STEREO HEADSET



Note: All ESD diodes in this schematics are reserved for the testing.

APPENDIX B: REVISION HISTORY

Revision A (June 2016)

This is the initial released version of this document.

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