



IS39LV512 / IS39LV010 / IS39LV040 512 Kbit / 1Mbit / 4Mbit 3.0 Volt-only CMOS Flash Memory

FEATURES

- **Single Power Supply Operation**
 - Low voltage range: 2.70 V - 3.60 V
- **Memory Organization**
 - IS39LV512: 64K x 8 (512 Kbit)
 - IS39LV010: 128K x 8 (1 Mbit)
 - IS39LV040: 512K x 8 (4 Mbit)
- **High Performance Read**
 - 70 ns access time
- **Cost Effective Sector/Block Architecture**
 - Uniform 4 Kbyte sectors
 - Uniform 64 Kbyte blocks (sector group - except IS39LV512)
- **Data# Polling and Toggle Bit Features**
- **Hardware Data Protection**
- **Automatic Erase and Byte Program**
 - Build-in automatic program verification
 - Typical 16 μ s/byte programming time
 - Typical 55 ms sector/block/chip erase time
- **Low Power Consumption**
 - Typical 4 mA active read current
 - Typical 8 mA program/erase current
 - Typical 0.1 μ A CMOS standby current
- **High Product Endurance**
 - Guarantee 100,000 program/erase cycles per single sector (preliminary)
 - Minimum 20 years data retention
- **Industrial Standard Pin-out and Packaging**
 - 32-pin (8 mm x 14 mm) VSOP
 - 32-pin PLCC
 - Optional lead-free (Pb-free) package
- **Operation temperature range**
 - IS39LV512/010 -40°C~+85°C
 - IS39LV040 0°C~+85°C

GENERAL DESCRIPTION

The IS39LV512/010/040 are 512 Kbit/1 Mbit/4 Mbit 3.0 Volt-only Flash Memories. These devices are designed to use a single low voltage, range from 2.70 Volt to 3.60 Volt, power supply to perform read, erase and program operations. The 12.0 Volt V_{PP} power supply for program and erase operations are not required. The devices can be programmed in standard EPROM programmers as well.

The memory array of IS39LV512 is divided into uniform 4 Kbyte sectors for data or code storage. The memory arrays of IS39LV010/040 are divided into uniform 4 Kbyte sectors or uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). The sector or block erase feature allows users to flexibly erase a memory area as small as 4 Kbyte or as large as 64 Kbyte by one single erase operation without affecting the data in others. The chip erase feature allows the whole memory array to be erased in one single erase operation. The devices can be programmed on a byte-by-byte basis after performing the erase operation.

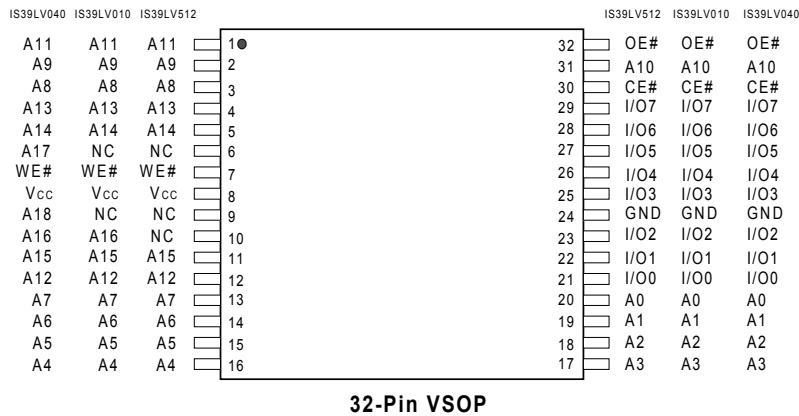
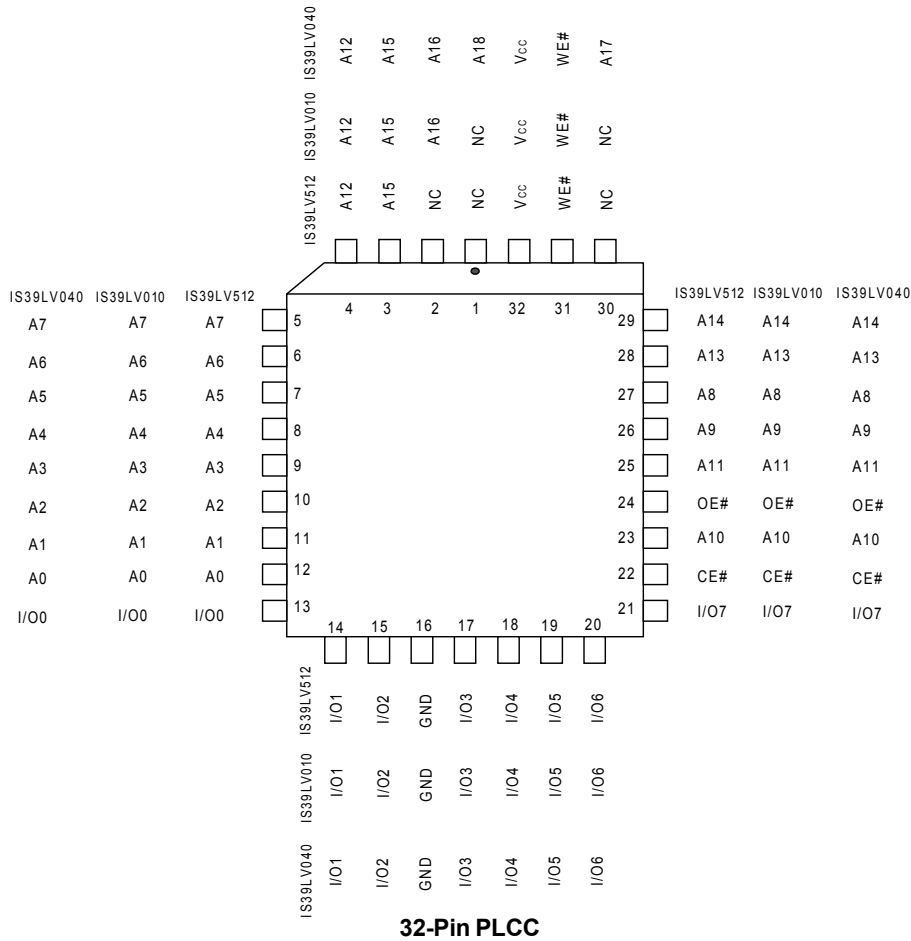
The devices have a standard microprocessor interface as well as a JEDEC standard pin-out/command set. The program operation is executed by issuing the program command code into command register. The internal control logic automatically handles the programming voltage ramp-up and timing. The erase operation is executed by issuing the chip erase, block, or sector erase command code into command register. The internal control logic automatically handles the erase voltage ramp-up and timing. The preprogramming on the array which has not been programmed is not required before an erase operation. The devices offer Data# Polling and Toggle Bit functions, the progress or completion of program and erase operations can be detected by reading the Data# Polling on I/O7 or the Toggle Bit on I/O6.

The IS39LV512/010/040 are manufactured on pFLASH™'s advanced nonvolatile CMOS technology. The devices are offered in 32-pin VSOP and PLCC packages with 70 ns access time.



IS39LV512 / IS39LV010 / IS39LV040

CONNECTION DIAGRAMS

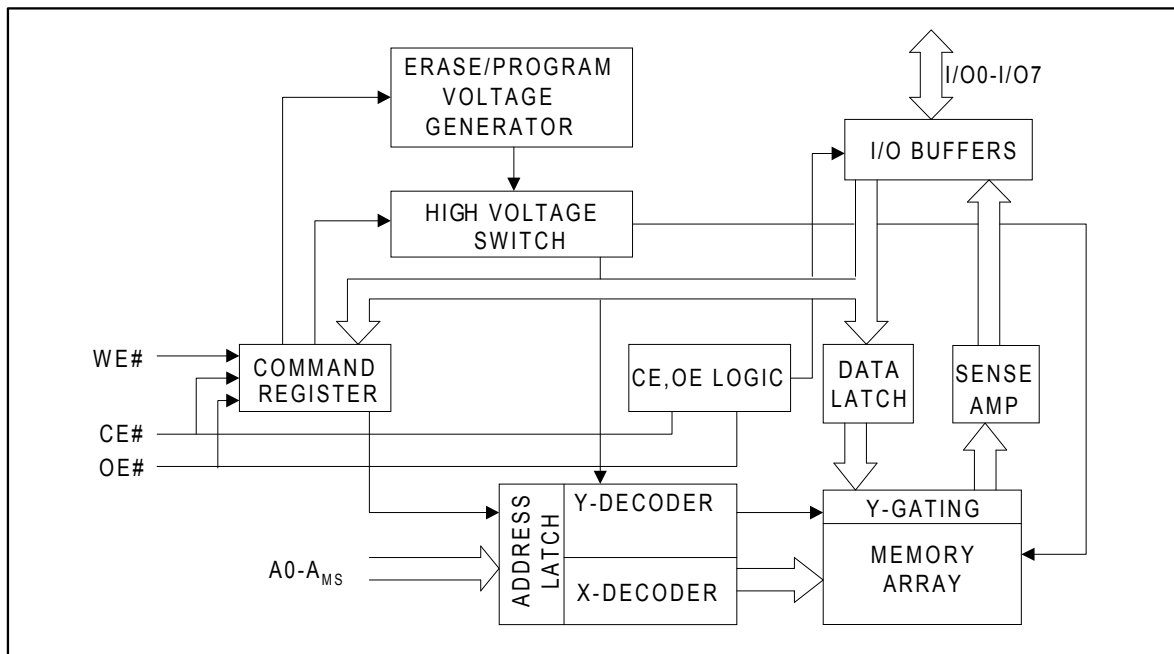


**PIN DESCRIPTIONS**

| SYMBOL | TYPE | DESCRIPTION |
|-------------------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A0 - A _{MS} ⁽¹⁾ | INPUT | Address Inputs: For memory addresses input. Addresses are internally latched on the falling edge of WE# during a write cycle. |
| CE# | INPUT | Chip Enable: CE# goes low activates the device's internal circuitries for device operation. CE# goes high deselects the device and switches into standby mode to reduce the power consumption. |
| WE# | INPUT | Write Enable: Activate the device for write operation. WE# is active low. |
| OE# | INPUT | Output Enable: Control the device's output buffers during a read cycle. OE# is active low. |
| I/O0 - I/O7 | INPUT/ OUTPUT | Data Inputs/Outputs: Input command/data during a write cycle or output data during a read cycle. The I/O pins float to tri-state when OE# are disabled. |
| VCC | | Device Power Supply |
| GND | | Ground |
| NC | | No Connection |

Note:

1. A_{MS} is the most significant address where A_{MS} = A15 for IS39LV512, A16 for IS39LV010, and A18 for IS39LV040.

BLOCK DIAGRAM

DEVICE OPERATION
READ OPERATION

The access of IS39LV512/010/040 are similar to EPROM. To read data, three control functions must be satisfied:

- CE# is the chip enable and should be pulled low (V_{IL}).
- OE# is the output enable and should be pulled low (V_{IL}).
- WE# is the write enable and should remain high (V_{IH}).

PRODUCT IDENTIFICATION

The product identification mode can be used to identify the manufacturer and the device through hardware or software read ID operation. See Table 1 for pFLASH™ Manufacturer ID and Device ID. The hardware ID mode is activated by applying a 12.0 Volt on A9 pin, typically used by an external programmer for selecting the right programming algorithm for the devices. Refer to Table 2 for Bus Operation Modes. The software ID mode is activated by a three-bus-cycle command. See Table 3 for Software Command Definition.

BYTE PROGRAMMING

The programming is a four-bus-cycle operation and the data is programmed into the devices (to a logical “0”) on a byte-by-byte basis. See Table 3 for Software Command Definition. A program operation is activated by writing the three-byte command sequence followed by program address and one byte of program data into the devices. The addresses are latched on the falling edge of WE# or CE# whichever occurs later, and the data are latched on the rising edge of WE# or CE# whichever occurs first. The internal control logic automatically handles the internal programming voltages and timing.

A data “0” can not be programmed back to a “1”. Only erase operation can convert the “0”s to “1”s. The Data# Polling on I/O7 or Toggle Bit on I/O6 can be used to detect the progress or completion of a program cycle.



DEVICE OPERATION (CONTINUED)

CHIP ERASE

The entire memory array can be erased through a chip erase operation. Pre-programs the devices are not required prior to a chip erase operation. Chip erase starts immediately after a six-bus-cycle chip erase command sequence. All commands will be ignored once the chip erase operation has started. The devices will return to standby mode after the completion of chip erase.

SECTOR AND BLOCK ERASE

The memory array of IS39LV512/010/040 are organized into uniform 4 Kbyte sectors. A sector erase operation allows to erase any individual sector without affecting the data in others. The memory array of IS39LV010/040, excluding IS39LV512, are also organized into uniform 64 Kbyte blocks (sector group - consists of sixteen adjacent sectors). A block erase operation allows to erase any individual block. The sector or block erase operation is similar to chip erase.

I/O7 DATA# POLLING

The IS39LV512/010/040 provide a Data# Polling feature to indicate the progress or completion of a program and erase cycles. During a program cycle, an attempt to read the devices will result in the complement of the last loaded data on I/O7. Once the program operation is completed, the true data of the last loaded data is valid on all outputs. During a sector, block, or chip erase cycle, an attempt to read the device will result a “0” on I/O7. After the erase operation is completed, an attempt to read the device will result a “1” on I/O7.

I/O6 TOGGLE BIT

The IS39LV512/010/040 also provide a Toggle Bit feature to detect the progress or completion of a program and erase cycles. During a program or erase cycle, an attempt to read data from the device will result a toggling between “1” and “0” on I/O6. When the program or erase operation is complete, I/O6 will stop toggling and valid data will be read. Toggle bit may be accessed at any time during a program or erase cycle.

HARDWARE DATA PROTECTION

Hardware data protection protects the devices from unintentional erase or program operation. It is performed in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8 V (typical), the write operation is inhibited. (b) Write inhibit: holding any of the signal OE# low, CE# high, or WE# high inhibits a write cycle. (c) Noise filter: pulses of less than 5 ns (typical) on the WE# or CE# input will not initiate a write operation.

Table 1. Product Identification

| Product Identification | Data |
|------------------------|------|
| Manufacturer ID | 9Dh |
| Device ID: | |
| IS39LV512 | 1Bh |
| IS39LV010 | 1Ch |
| IS39LV040 | 3Eh |



SECTOR/BLOCK ADDRESS TABLE

| Memory Density | | | Block | Block Size (Kbytes) | Sector | Sector Size (Kbytes) | Address Range |
|----------------|--------|--------|------------------------|---------------------|-----------------|----------------------|-----------------|
| 512Kbit | 1 Mbit | 4 Mbit | Block 0 ⁽²⁾ | 64 | Sector 0 | 4 | 00000h - 00FFFh |
| | | | | | Sector 1 | 4 | 01000h - 01FFFh |
| | | | | | : | : | : |
| | | | | | Sector 15 | 4 | 0F000h - 0FFFFh |
| | | | Block 1 | 64 | Sector 16 | 4 | 10000h - 10FFFh |
| | | | | | Sector 17 | 4 | 11000h - 11FFFh |
| | | | | | : | : | : |
| | | | | | Sector 31 | 4 | 1F000h - 1FFFFh |
| | | | Block 2 | 64 | " | " | 20000h - 2FFFFh |
| | | | Block 3 | 64 | " | " | 30000h - 3FFFFh |
| | | | Block 4 | 64 | " | " | 40000h - 4FFFFh |
| | | | Block 5 | 64 | " | " | 50000h - 5FFFFh |
| Block 6 | 64 | | " | " | 60000h - 6FFFFh | | |
| Block 7 | 64 | | " | " | 70000h - 7FFFFh | | |

Notes:

1. A Block is a 64 Kbyte sector group which consists of sixteen adjacent sectors of 4 Kbyte each.
2. Block erase feature is available for IS39LV010/040 only. The chip erase command should be used to erase the Block 0 for the IS39LV512.

**OPERATING MODES**

Table 2. Bus Operation Modes

| Mode | CE# | OE# | WE# | ADDRESS | I/O |
|---------------------------------|-----------------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------|------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | X (1) | D _{OUT} |
| Write | V _{IL} | V _{IH} | V _{IL} | X | D _{IN} |
| Standby | V _{IH} | X | X | X | High Z |
| Output Disable | X | V _{IH} | X | X | High Z |
| Product Identification Hardware | V _{IL} | V _{IL} | V _{IH} | A2 - A _{MS} ⁽²⁾ = X, A9 = V _H ⁽³⁾ , A1 = V _{IL} , A0 = V _{IL} | Manufacturer ID |
| | | | | A2 - A _{MS} ⁽²⁾ = X, A9 = V _H ⁽³⁾ , A1 = V _{IL} , A0 = V _{IH} | Device I |

Notes:

1. X can be V_{IL}, V_{IH} or addresses.
2. A_{MS} = Most significant address;
A_{MS} = A15 for IS39LV512, A16 for IS39LV010, and
A18 for IS39LV040.
3. V_H = 12.0 V ± 0.5 V.

COMMAND DEFINITION
Table 3. Software Command Definition

| Command Sequence | Bus Cycle | 1st Bus Cycle Addr Data | 2nd Bus Cycle Addr Data | 3rd Bus Cycle Addr Data | 4th Bus Cycle Addr Data | 5th Bus Cycle Addr Data | 6th Bus Cycle Addr Data |
|--------------------------------|-----------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| Read | 1 | Addr D _{OUT} | | | | | |
| Chip Erase | 6 | 555h AAh | 2AAh 55h | 555h 80h | 555h AAh | 2AAh 55h | 555h 10h |
| Sector Erase | 6 | 555h AAh | 2AAh 55h | 555h 80h | 555h AAh | 2AAh 55h | SA ⁽¹⁾ 30h |
| Block Erase | 6 | 555h AAh | 2AAh 55h | 555h 80h | 555h AAh | 2AAh 55h | BA ⁽²⁾ 50h |
| Byte Program | 4 | 555h AAh | 2AAh 55h | 555h A0h | Addr D _{IN} | | |
| Product ID Entry | 3 | 555h AAh | 2AAh 55h | 555h 90h | | | |
| Product ID Exit ⁽³⁾ | 3 | 555h AAh | 2AAh 55h | 555h F0h | | | |
| Product ID Exit ⁽³⁾ | 1 | XXXh F0h | | | | | |

Notes:

1. SA = Sector address of the sector to be erased.
2. BA = Block address of the block to be erased.
3. Either one of the Product ID Exit command can be used.

DEVICE OPERATIONS FLOWCHARTS

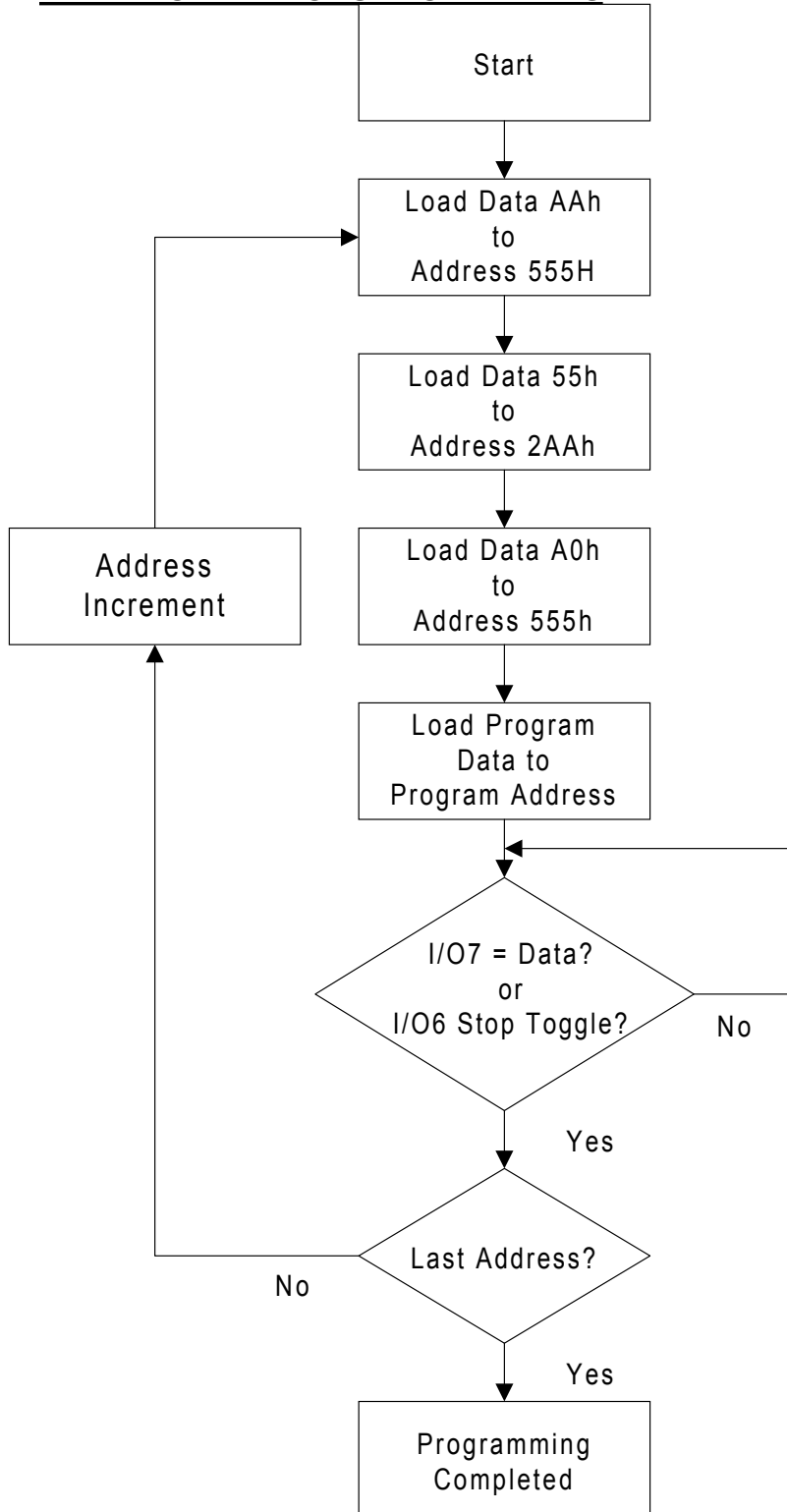
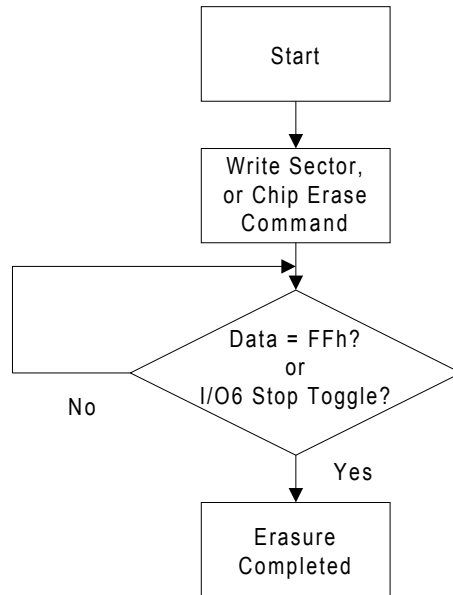
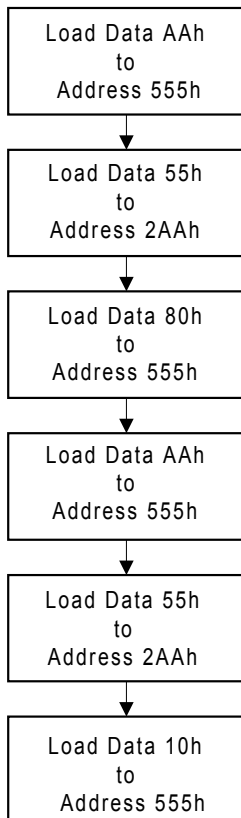


Chart 1. Automatic Programming Flowchart

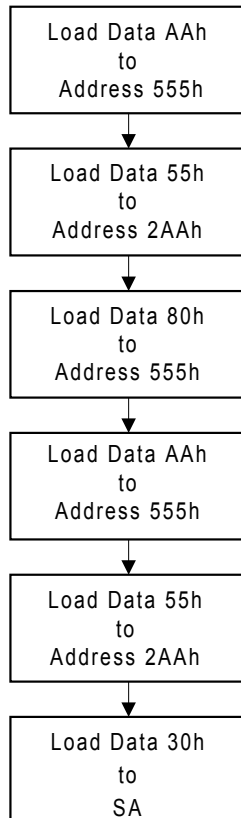
DEVICE OPERATIONS FLOWCHARTS (CONTINUED)



CHIP ERASE COMMAND



SECTOR ERASE COMMAND



BLOCK ERASE COMMAND

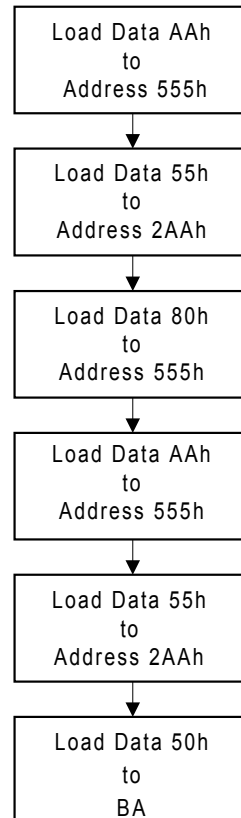
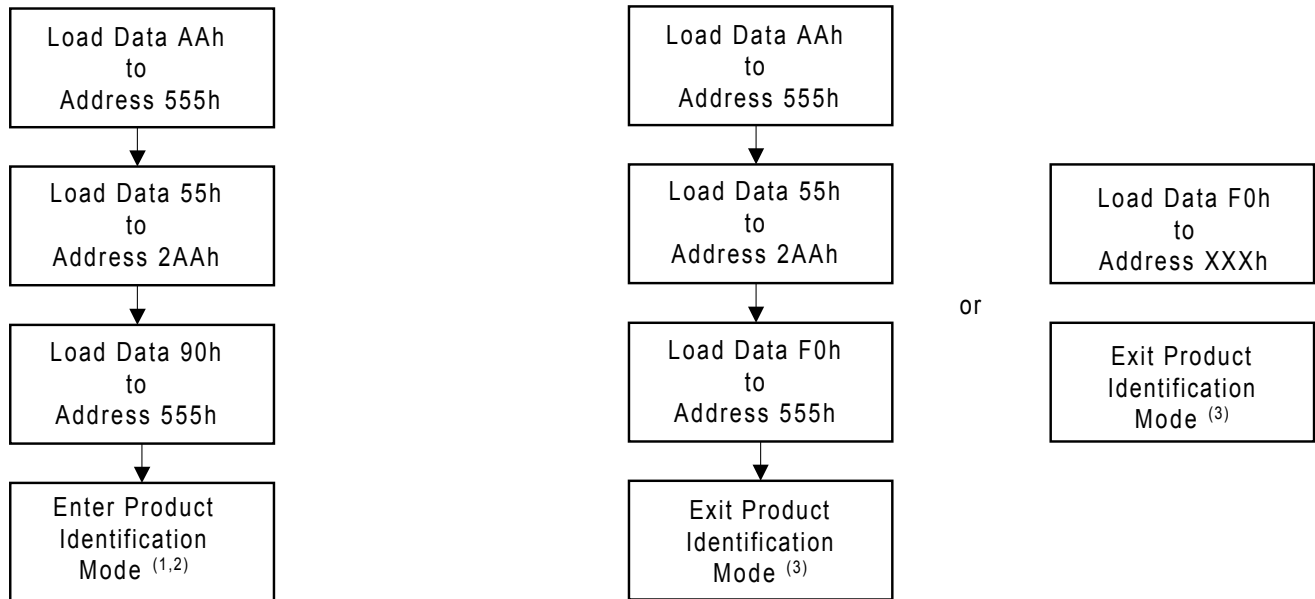


Chart 2. Automatic Erase Flowchart

DEVICE OPERATIONS FLOWCHARTS (CONTINUED)



Notes:

1. The device will enter Product Identification mode after executing the Product ID Entry command.
2. Under Product Identification mode, the Manufacturer ID and Device ID of devices can be read at address X0000h and X0001h where X = Don't Care.
3. The device returns to standby operation.

Chart 3. Software Product Identification Entry/Exit Flowchart

**ABSOLUTE MAXIMUM RATINGS** ⁽¹⁾

| | |
|--------------------------------------------------------------------|----------------------|
| Temperature Under Bias | -65°C to +125°C |
| Storage Temperature | -65°C to +125°C |
| Surface Mount Lead Soldering Temperature | 240°C 3 Seconds |
| Input Voltage with Respect to Ground on All Pins except A9 pin (2) | -0.5V to VCC + 0.5 V |
| Input Voltage with Respect to Ground on A9 pin (3) | -0.5V to +13.0 V |
| All Output Voltage with Respect to Ground | -0.5V to VCC + 0.5 V |
| VCC (2) | -0.5V to +6.0 V |

Notes:

1. Stresses under those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. The functional operation of the device or any other conditions under those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended periods may affect device reliability.
2. Maximum DC voltage on input or I/O pins are $V_{CC} + 0.5V$. During voltage transitioning period, input or I/O pins may overshoot to $V_{CC} + 2.0V$ for a period of time up to 20 ns. Minimum DC voltage on input or I/O pins are -0.5V. During voltage transitioning period, input or I/O pins may undershoot GND to -2.0V for a period of time up to 20 ns.
3. Maximum DC voltage on A9 pin is +13.0 V. During voltage transitioning period, A9 pin may overshoot to +14.0 V for a period of time up to 20 ns. Minimum DC voltage on A9 pin is -0.5V. During voltage transitioning period, A9 pin may undershoot GND to -2.0V for a period of time up to 20 ns.

DC AND AC OPERATING RANGE

| Part Number | IS39LV512/010 | IS39LV040 |
|-----------------------|-----------------|-----------------|
| Operating Temperature | -40° to +85°C | 0° to +85°C |
| Vcc Power Supply | 2.70 V - 3.60 V | 2.70 V - 3.60 V |

**DC CHARACTERISTICS**

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------|---------------------------|---------------------------------------------------------------------|-----------------------|------|-----------------------|-------|
| ILI | Input Load Current | V _{IN} = 0 V to V _{CC} | | | 1 | mA |
| ILO | Output Leakage Current | V _{I/O} = 0 V to V _{CC} | | | 1 | mA |
| ISB1 | VCC Standby Current CMOS | CE#, OE# = V _{CC} - 0.3 V | | 0.1 | 5 | mA |
| ISB2 | VCC Standby Current TTL | CE# = V _{IH} to V _{CC} | | 0.05 | 3 | mA |
| ICC1 | VCC Active Read Current | f = 5 MHz; I _{OUT} = 0 mA | | 4 | 15 | mA |
| ICC2(1) | VCC Program/Erase Current | | | 8 | 20 | mA |
| VIL | Input Low Voltage | | -0.5 | | 0.8 | V |
| VIH | Input High Voltage | | 0.7 V _{CC} | | V _{CC} + 0.3 | V |
| VOL | Output Low Voltage | I _{OL} = 2.1 mA; V _{CC} = V _{CCmin} | | | 0.45 | V |
| VOH | Output High Voltage | I _{OH} = -100 mA; V _{CC} = V _{CC min} | V _{CC} - 0.2 | | | V |

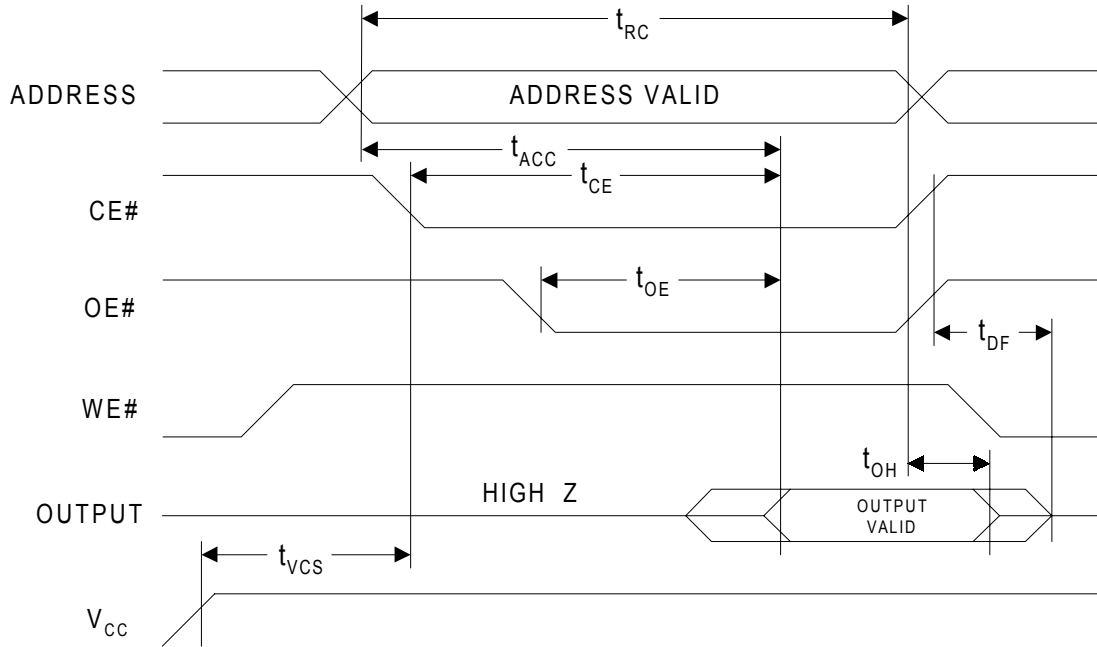
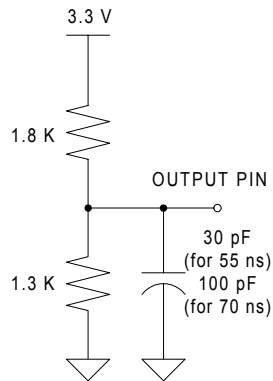
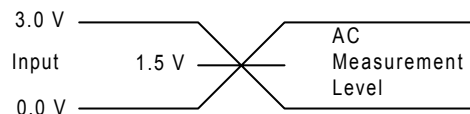
Note: 1. Characterized but not 100% tested.



AC CHARACTERISTICS

READ OPERATIONS CHARACTERISTICS

| Symbol | Parameter | IS39LV512/010/040 | | Units |
|---------------|----------------------------------------------------------------|--------------------------|----|--------------|
| tRC | Read Cycle Time | 70 | | ns |
| tACC | Address to Output Delay | | 70 | ns |
| tCE | CE# to Output Delay | | 70 | ns |
| tOE | OE# to Output Delay | | 35 | ns |
| tDF | CE# or OE# to Output High Z | 0 | 25 | ns |
| tOH | Output Hold from OE#, CE# or Address, whichever occurred first | 0 | | ns |
| tVCS | VCC Set-up Time | 50 | | ms |

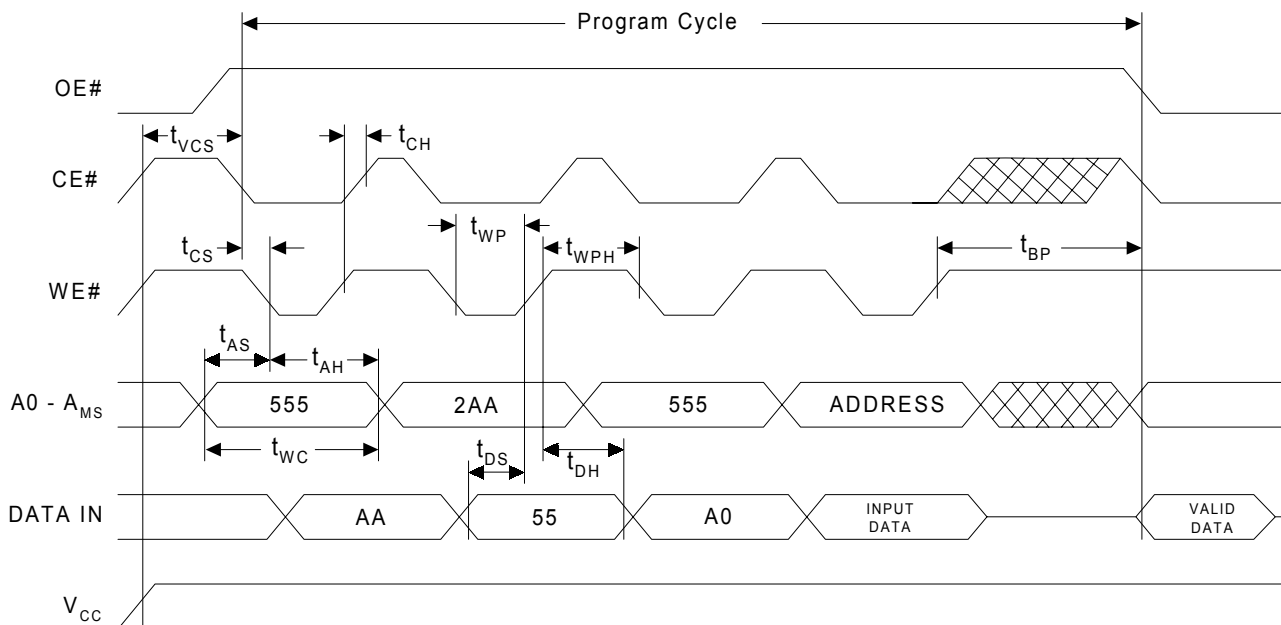
AC CHARACTERISTICS (CONTINUED)
READ OPERATIONS AC WAVEFORMS

OUTPUT TEST LOAD

INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

PIN CAPACITANCE (f = 1 MHz, T = 25°C)

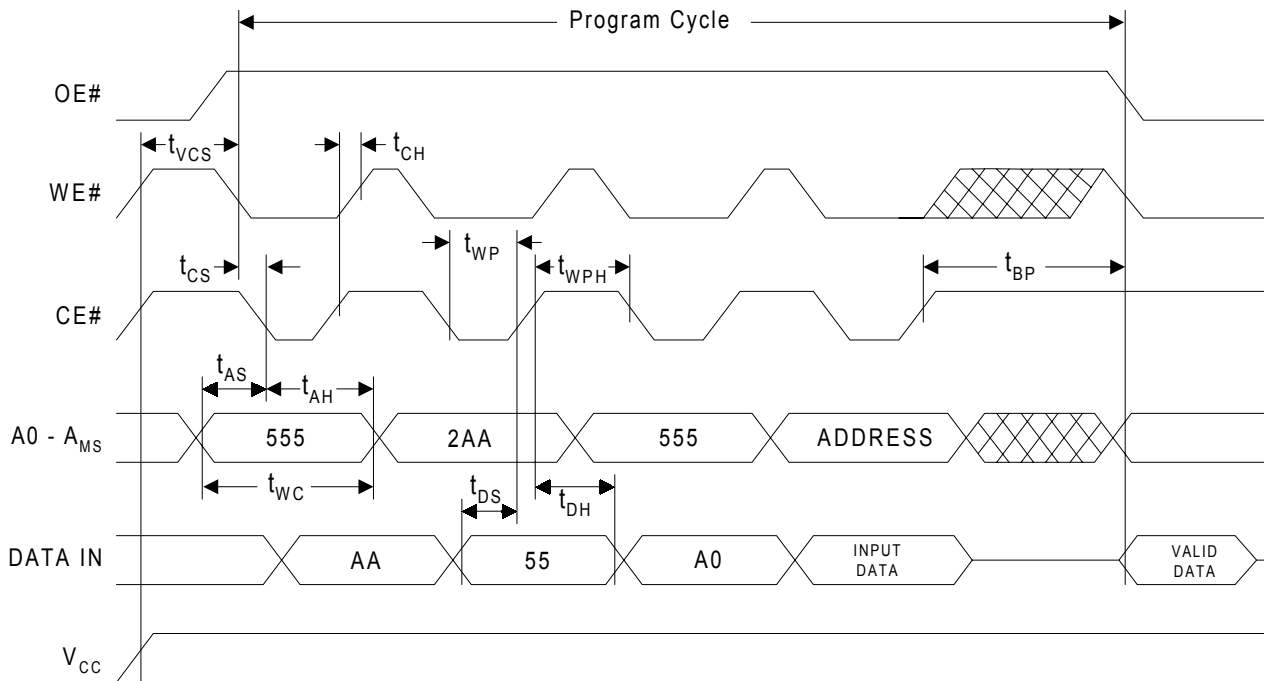
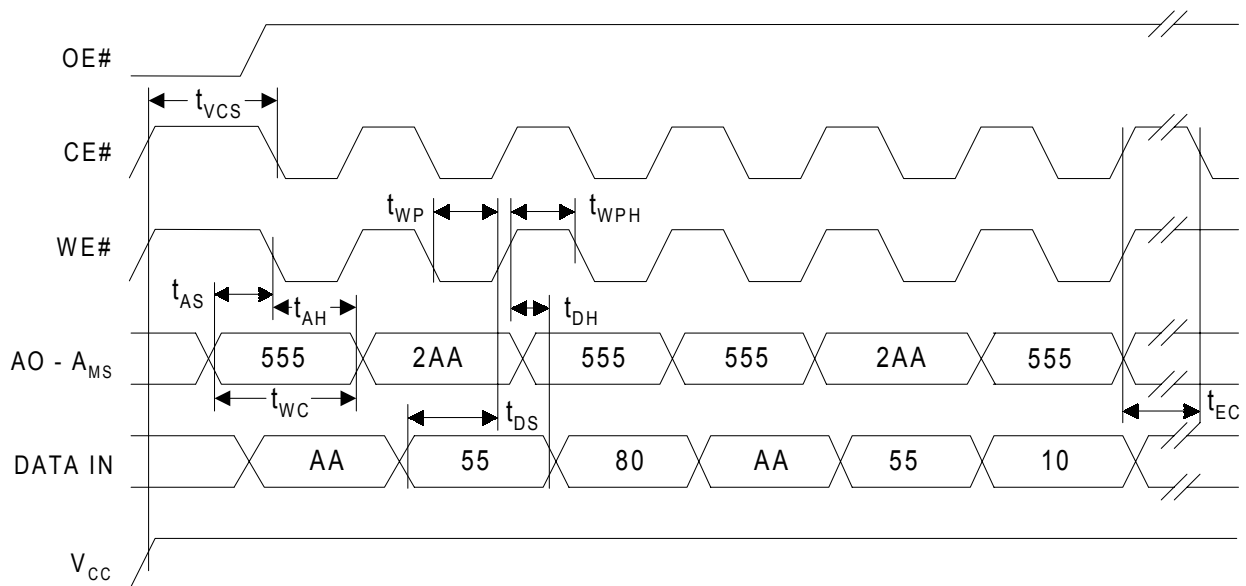
| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|-----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0 V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0 V$ |

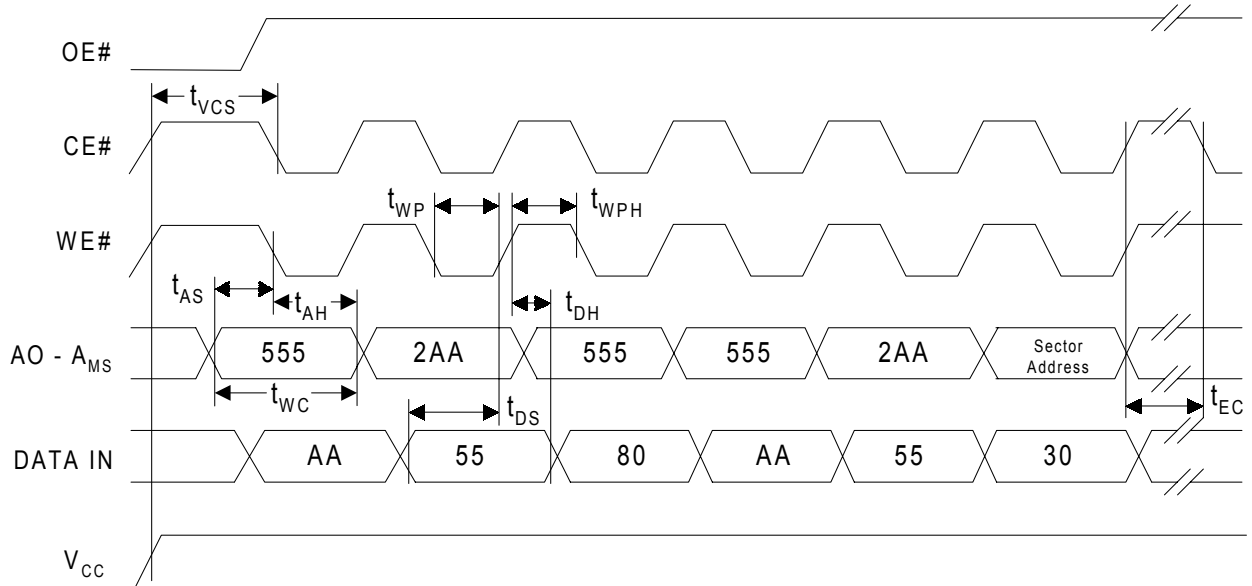
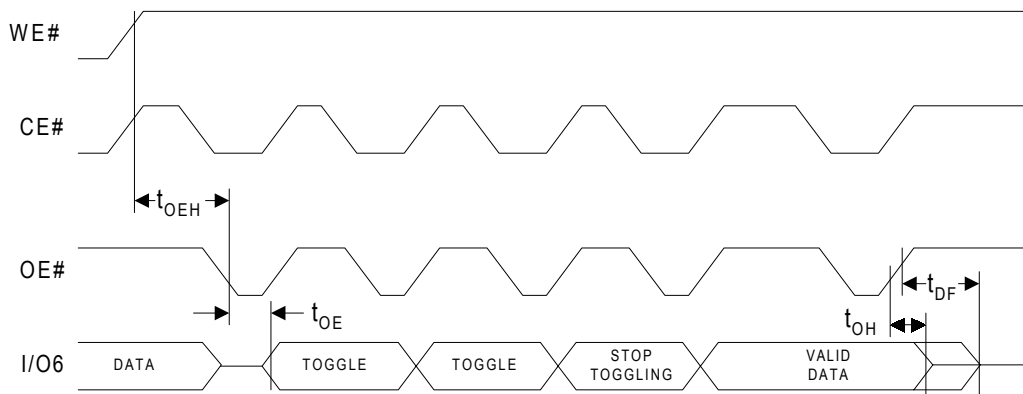
Note: These parameters are characterized but not 100% tested.

AC CHARACTERISTICS (CONTINUED)
WRITE (PROGRAM/ERASE) OPERATIONS CHARACTERISTICS

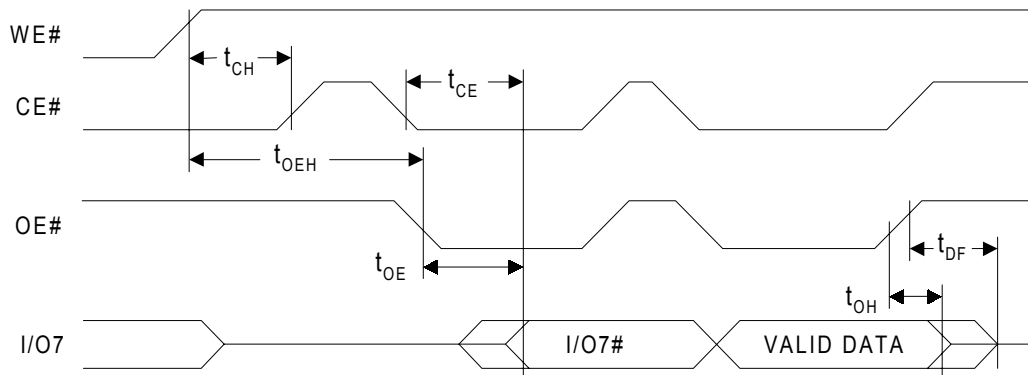
| Symbol | Parameter | IS39LV512/010/040 | | Units |
|-------------------|--------------------------|-------------------|-----|-------|
| | | Min | Max | |
| t _{WC} | Write Cycle Time | 70 | | ns |
| t _{AS} | Address Set-up Time | 0 | | ns |
| t _{AH} | Address Hold Time | 30 | | ns |
| t _{CS} | CE# and WE# Set-up Time | 0 | | ns |
| t _{CH} | CE# and WE# Hold Time | 0 | | ns |
| t _{OE#H} | OE# High Hold Time | 10 | | ns |
| t _{DS} | Data Set-up Time | 40 | | ns |
| t _{DH} | Data Hold Time | 0 | | ns |
| t _{WP} | Write Pulse Width | 35 | | ns |
| t _{WPH} | Write Pulse Width High | 20 | | ns |
| t _{BP} | Byte Programming Time | | 40 | ms |
| t _{EC} | Chip or Block Erase Time | | 100 | ms |
| t _{VCS} | VCC Set-up Time | 50 | | ms |

PROGRAM OPERATIONS AC WAVEFORMS - WE# CONTROLLED


AC CHARACTERISTICS (CONTINUED)

CHIP ERASE OPERATIONS AC WAVEFORMS


AC CHARACTERISTICS (CONTINUED)
SECTOR OR BLOCK ERASE OPERATIONS AC WAVEFORMS

TOGGLE BIT AC WAVEFORMS


Note: Toggling CE#, OE#, or both OE# and CE# will operate Toggle Bit.

AC CHARACTERISTICS (CONTINUED)
DATA# POLLING AC WAVEFORMS


Note: Toggling CE#, OE#, or both OE# and CE# will operate Data# Polling.

PROGRAM/ERASE PERFORMANCE

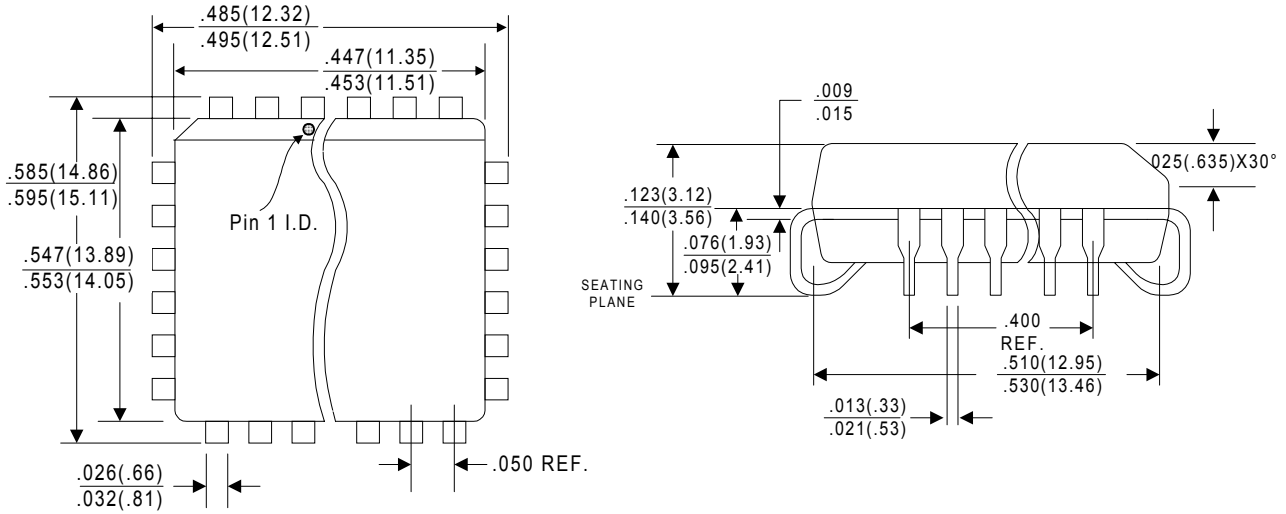
| Parameter | Unit | Typ | Max | Remarks |
|-----------------------|------|-----|-----|-----------------------------------------------------------|
| Sector Erase Time | ms | 55 | 100 | From writing erase command to erase completion |
| Block Erase Time | ms | 55 | 100 | From writing erase command to erase completion |
| Chip Erase Time | ms | 55 | 100 | From writing erase command to erase completion |
| Byte Programming Time | ms | 16 | 20 | Excludes the time of four-cycle program command execution |

Note: 1. These parameters are characterized but not 100% tested.
 2. Preliminary specification only and will be formalized after cycling qualification test.

PACKAGE TYPE INFORMATION

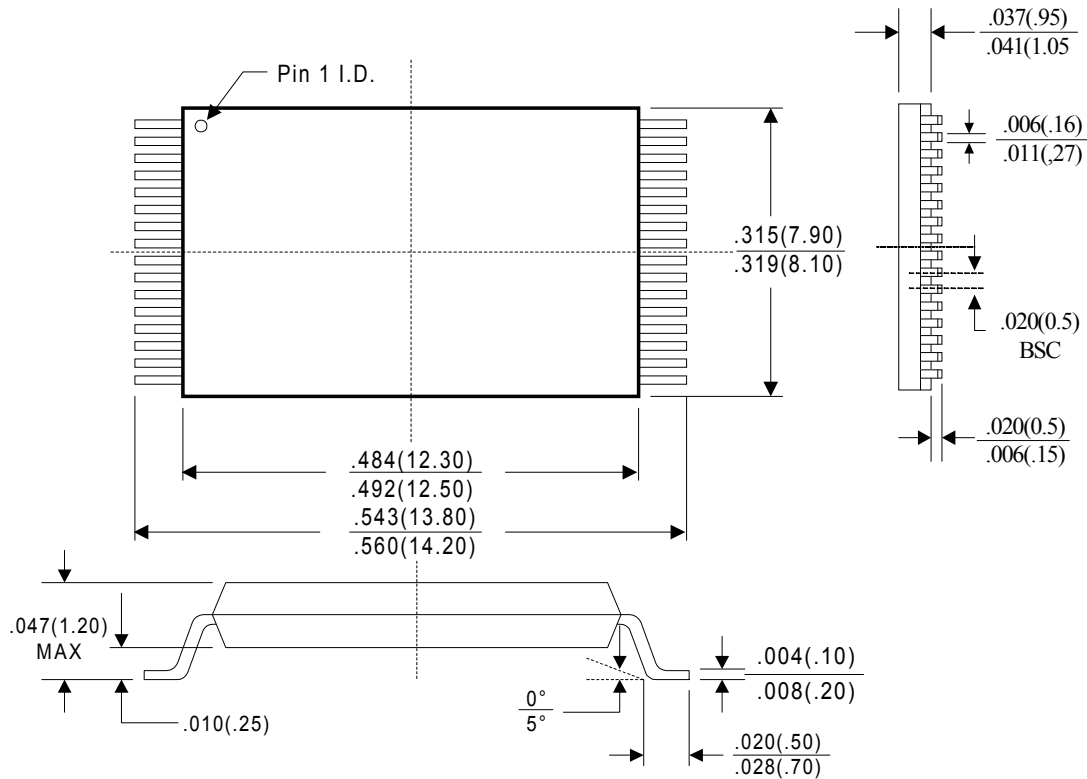
PLCC

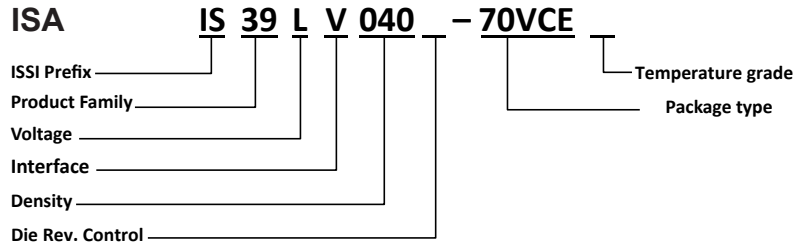
32-Pin Plastic Leaded Chip Carrier Dimensions in Inches (Millimeters)



VSOP

32-Pin Thin Small Outline Package (VSOP - 8 mm x 14 mm)(measure in millimeters)





Flash Product Family

ISA = 29/39

ISA Operating Voltage Range

G/L = 2.70-3.60V

Die Rev. Control

Blank = First Rev.

ISA Interface

V = ISA x8
L = ISA x8/x16

Density

025 = 256Kb
512 = 512Kb
010 = 1Mb
020 = 2Mb
040 = 4Mb
080 = 8Mb
016 = 16Mb
032 = 32Mb
064 = 64Mb
128 = 128Mb
256 = 256Mb

Package Type

JE = 48 pin TSSOP
JT = 56 pin TSSOP
70JCE = 32 pin PLCC
70VCE = 32 pin VSOP (8x14mm)
JH = 48 ball (BGA 6x8mm) (Call Factory)
JI = 64 ball (BGA 11x13mm) (Call Factory)
JS = WLCSP (Call Factory)
JW = KGD (Call Factory)

Lead-Free Package

E/L = Lead-Free

Temperature Grade

E = Extended grade (-40C to +105C)
A1 = Automotive grade (-40C to +85C)
A2 = Automotive grade(-40C to +105C)
A3 = Automotive grade(-40C to +125C)
Blank = Refer to datasheet



ORDERING INFORMATION

| Density | Frequency (MHz) | Order Part Number | Package |
|---------|-----------------|-------------------|-------------|
| 512K | 100 | IS39LV512-70JCE | 32-pin PLCC |
| | | IS39LV512-70VCE | 32-pin VSOP |
| 1M | 100 | IS39LV010-70JCE | 32-pin PLCC |
| | | IS39LV010-70VCE | 32-pin VSOP |
| 4M | 100 | IS39LV040-70JCE | 32-pin PLCC |
| | | IS39LV040-70VCE | 32-pin VSOP |