IS61SP12832

128K x 32 SYNCHRONOUS PIPELINED STATIC RAM

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Pentium™ or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Common data inputs and data outputs
- JEDEC 100-Pin LQFP and 119-pin PBGA package
- Single +3.3V, +10%, –5% power supply
- Power-down snooze mode

DESCRIPTION

The *ICSI* IS61SP12832 is a high-speed, low-power synchronous static RAM designed to provide a burstable, high-performance, secondary cache for the Pentium™, 680X0™, and PowerPC™ microprocessors. It is organized as 131,072 words by 32 bits, fabricated with *ICSI*'s advanced CMOS technology. The device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be from one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQa, $\overline{BW2}$ controls DQb, $\overline{BW3}$ controls DQc, $\overline{BW4}$ controls DQd, conditioned by $\overline{BWE}$ being LOW. A LOW on $\overline{GW}$ input would cause all bytes to be written.

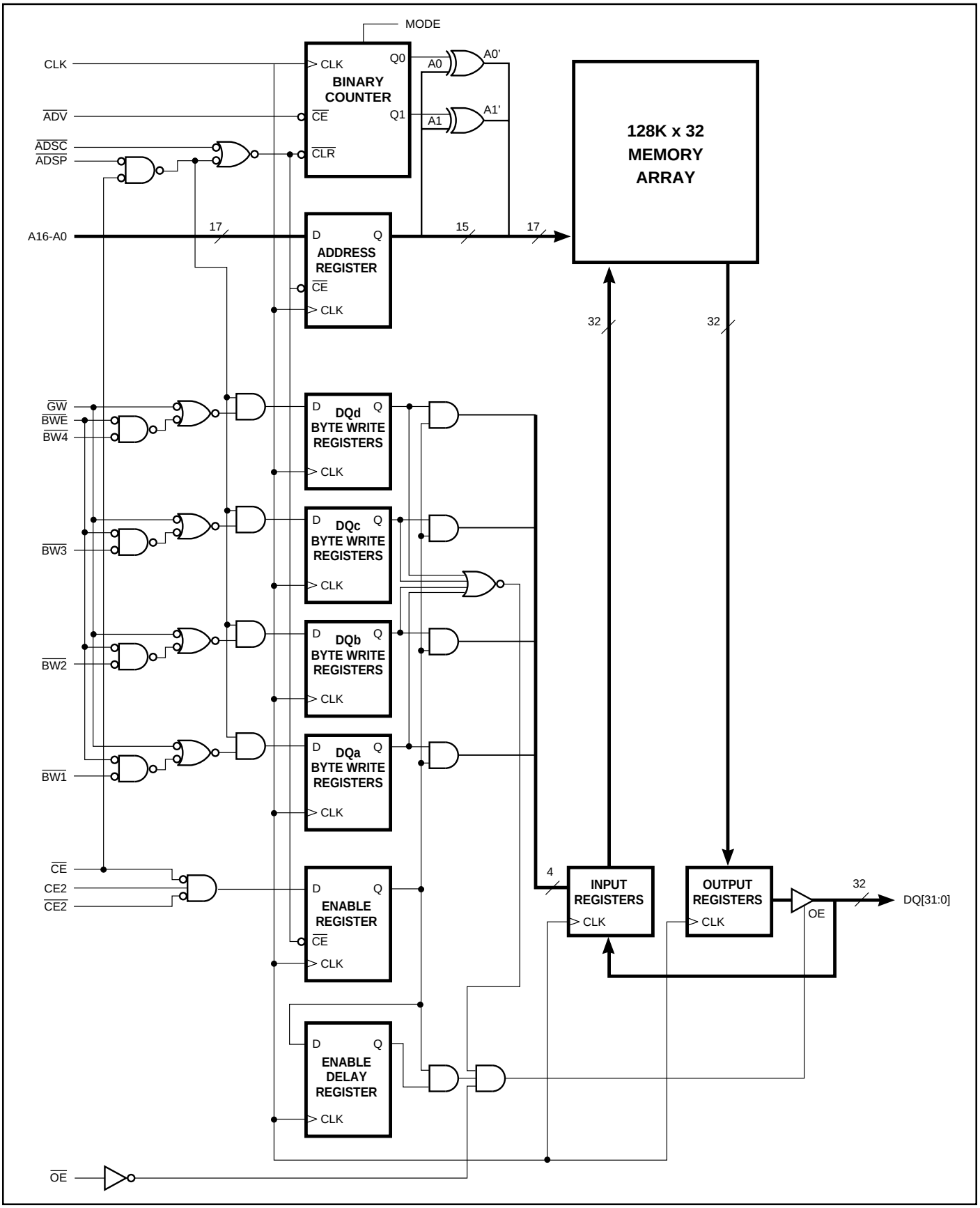
Bursts can be initiated with either $\overline{ADSP}$ (Address Status Processor) or $\overline{ADSC}$ (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally by the IS61SP12832 and controlled by the $\overline{ADV}$ (burst address advance) input pin.

The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

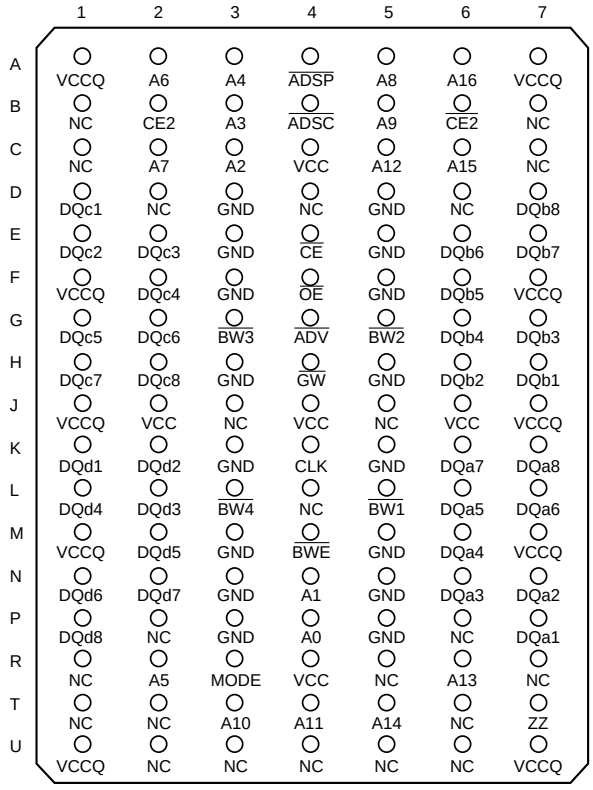
Symbol	Parameter	-166	-150	-133	-117	-5	Units
t_{KQ}	Clock Access Time	3.5	3.8	4	4	5	ns
t_{KC}	Cycle Time	6	6.7	7.5	8.5	10	ns
	Frenquency	166	150	133	117	100	MHz

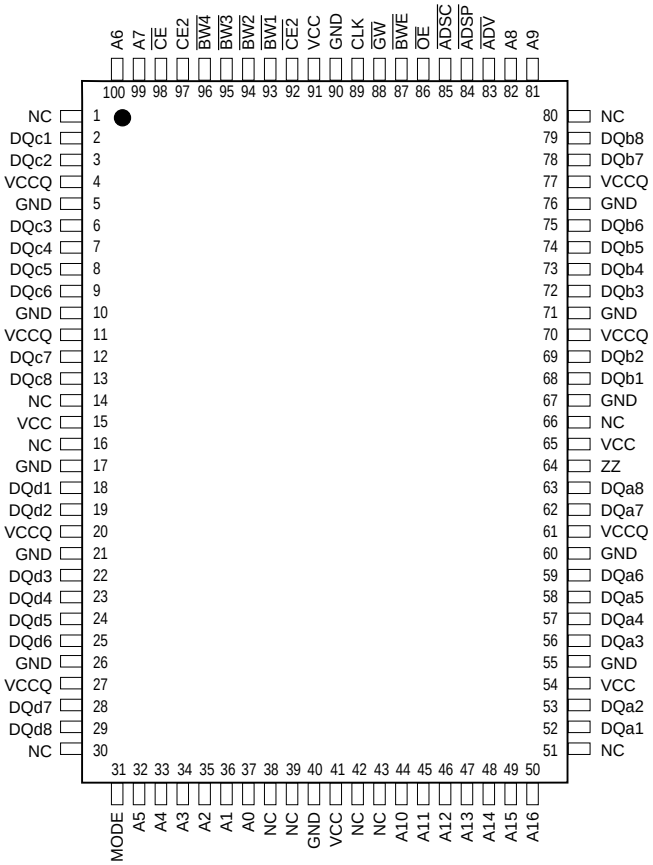
BLOCK DIAGRAM



PIN CONFIGURATION

119-pin PBGA (Top View) and 100-Pin LQFP





PIN DESCRIPTIONS

A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
A2-A16	Synchronous Address Inputs
CLK	Synchronous Clock
$\overline{ADSP}$	Synchronous Processor Address Status
$\overline{ADSC}$	Synchronous Controller Address Status
$\overline{ADV}$	Synchronous Burst Address Advance
$\overline{BW1}$-$\overline{BW4}$	Synchronous Byte Write Enable
$\overline{BWE}$	Synchronous Byte Write Enable

$\overline{GW}$	Synchronous Global Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
MODE	Burst Sequence Mode Selection
V_{CC}	+3.3V Power Supply
GND	Ground
V_{CCQ}	Isolated Output Buffer Supply: +3.3V
ZZ	Snooze Enable
GND_Q	Isolated Output Buffer Ground

TRUTH TABLE

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	DQ
Deselected, Power-down	None	H	X	X	X	L	X	X	X	High-Z
Deselected, Power-down	None	L	X	H	L	X	X	X	X	High-Z
Deselected, Power-down	None	L	L	X	L	X	X	X	X	High-Z
Deselected, Power-down	None	X	X	H	H	L	X	X	X	High-Z
Deselected, Power-down	None	X	0	X	H	L	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	L	X	X	X	X	High-Z
Read Cycle, Begin Burst	External	L	H	L	H	0	X	Read	X	High-Z
Write Cycle, Begin Burst	External	L	H	L	H	L	X	Write	X	High-Z
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	X	X	X	H	H	L	Read	H	High-Z
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	L	Q
Read Cycle, Continue Burst	Next	H	X	X	X	H	L	Read	H	High-Z
Write Cycle, Continue Burst	Next	X	X	X	H	H	L	Write	X	High-Z
Write Cycle, Continue Burst	Next	H	X	X	X	H	L	Write	X	High-Z
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	X	X	X	H	H	H	Read	H	High-Z
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	L	Q
Read Cycle, Suspend Burst	Current	H	X	X	X	H	H	Read	H	High-Z
Write Cycle, Suspend Burst	Current	X	X	X	H	H	H	Write	X	High-Z
Write Cycle, Suspend Burst	Current	H	X	X	X	H	H	Write	X	High-Z

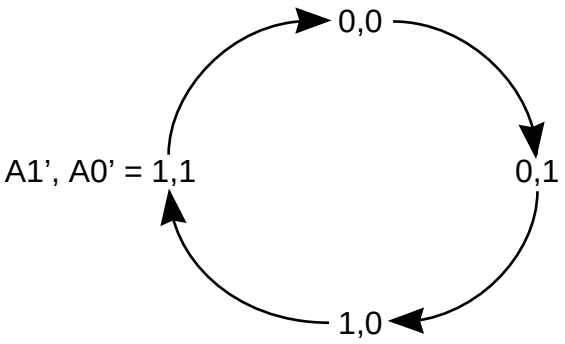
PARTIAL TRUTH TABLE

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	$\overline{BW4}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte 1	H	L	L	H	H	H
Write All Bytes	H	L	L	L	L	L
Write All Bytes	L	X	X	X	X	X

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{CCQ} or No Connect)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND_Q)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–55 to +150	°C
P_D	Power Dissipation	1.6	W
I_{OUT}	Output Current (per I/O)	100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins	–0.5 to V_{CCQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs	–0.5 to V_{CC} + 0.5	V
V_{CC}	Voltage on Vcc Supply Relatiive to GND	–0.5 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	3.3V, +10%, –5%
Industrial	–40°C to +85°C	3.3V, +10%, –5%

DC ELECTRICAL CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CCQ} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.8	V
I_{LI}	Input Leakage Current	GND < V_{IN} < V_{CCQ}[2]	Com. Ind.	–2 –5	2 5	µA
I_{LO}	Output Leakage Current	GND < V_{OUT} < V_{CCQ}, $\overline{OE}$ = V_{IH}	Com. Ind.	–2 –5	2 5	µA

POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		-166 Typ.	-166 Max.	-150 Typ.	-150 Max.	-133 Typ.	-133 Max.	-117 Typ.	-117 Max	-5 Typ.	-5 Max.	Unit
I_{CC}	AC Operating Supply Current	Device Selected, All Inputs = V_{IL} or V_{IH} $\overline{OE}$ = V_{IH}, Vcc = Max. Cycle Time > t_{KC} min.	Com. Ind.	200 —	230 —	190 200	220 230	180 190	210 220	175 185	205 215	170 180	200 210	mA mA
I_{SB}	Standby Current	Device Deselected, Vcc = Max., All Inputs = V_{IH} or V_{IL} CLK Cycle Time > t_{KC} min.	Com. Ind.	45 —	70 —	45 50	70 80	45 50	70 80	45 50	65 75	45 50	65 75	mA mA
I_{ZZ}	Power-down Mode Current	ZZ = V_{CCQ} Clock Running All Inputs < GND + 0.2V or > Vcc – 0.2V	Com. Ind.	— —	5 15	— —	5 15	— —	5 15	— —	5 15	— —	5 15	mA mA

Notes:
1. The MODE pin has an internal pullup. This pin may be a No Connect, tied to GND, or tied to V_{CCQ}.
2. The MODE pin should be tied to Vcc or GND. It exhibits ±10 µA maximum leakage current when tied to < GND + 0.2V or > Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

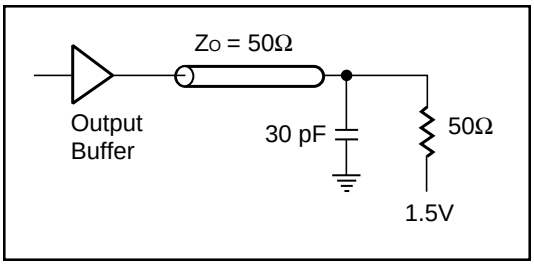


Figure 1

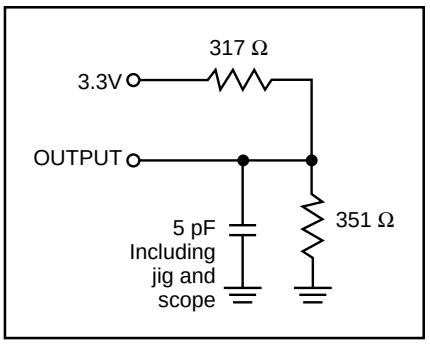


Figure 2

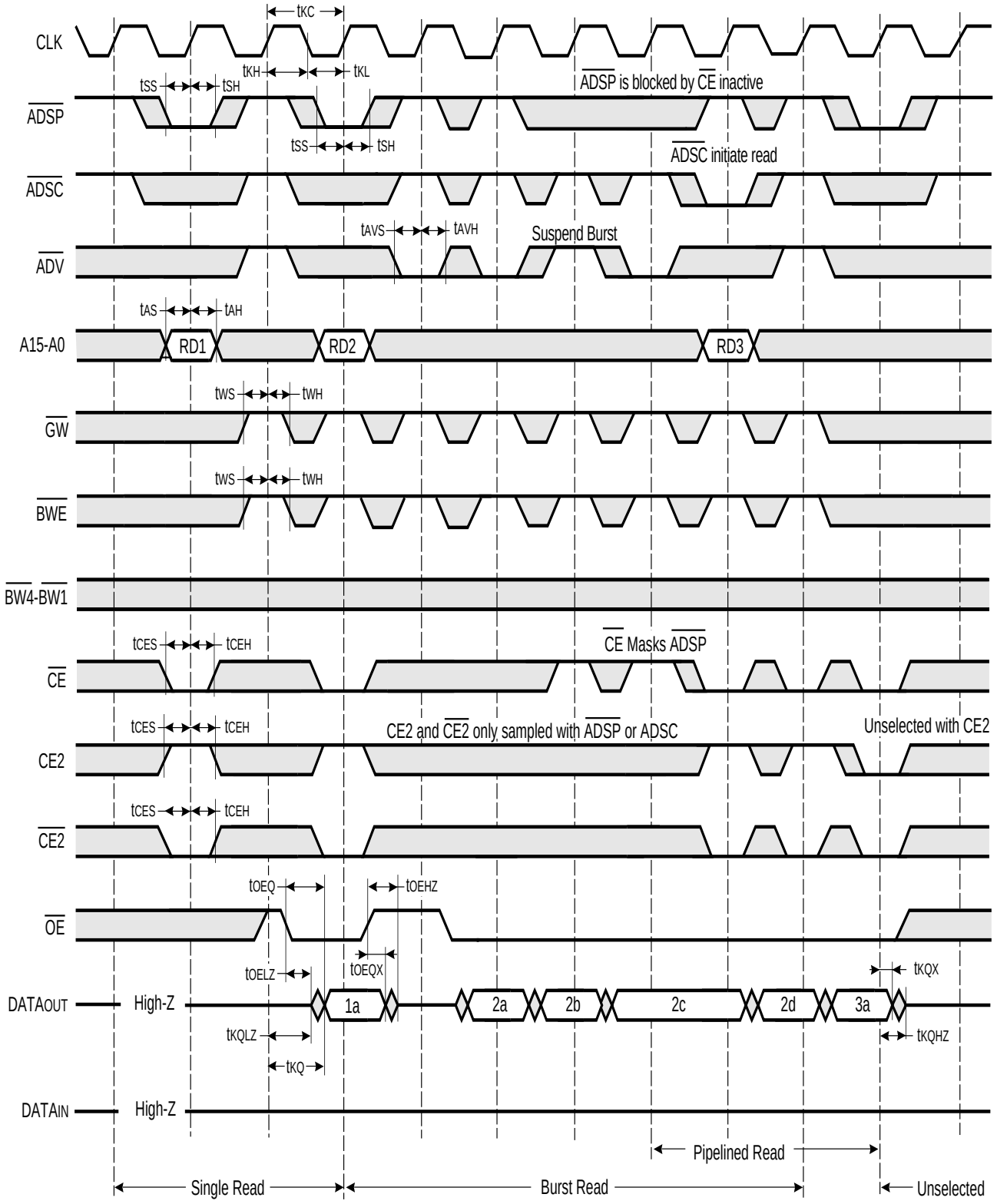
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}	Clock Frequency	—	166	—	150	—	133	—	117	—	100	MHz
t_{KC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t_{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{KQ}	Clock Access Time	—	3.5	—	3.8	—	4	—	4	—	5	ns
t_{KQX}[1]	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	1.5	—	2.5	—	ns
t_{KQLZ}[1,2]	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{KQHZ}[1,2]	Clock High to Output High-Z	1.5	6	1.5	6.7	1.5	7.5	1.5	8.5	1.5	10	ns
t_{OEQ}	Output Enable to Output Valid	—	3.5	—	3.5	—	3.8	—	4	—	5	ns
t_{OEQX}[1]	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	0	—	ns
t_{OELZ}[1,2]	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{OEHZ}[1,2]	Output Disable to Output High-Z	2	3.5	2	3.5	2	3.8	2	4	2	5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns

Note:

1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

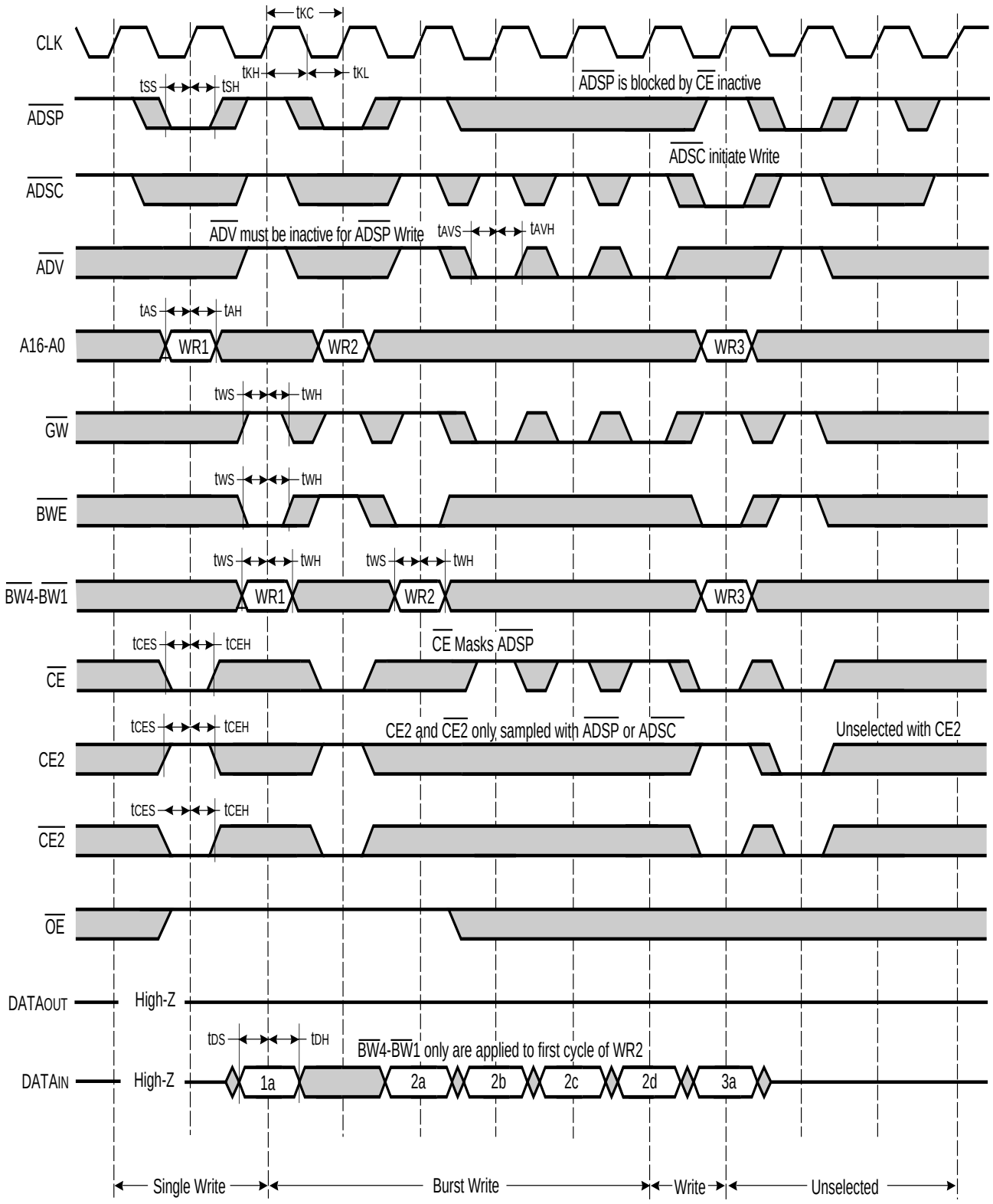
READ/WRITE CYCLE TIMING



WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{KC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t_{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{WS}	Write Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{DS}	Data In Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AVS}	Address Advance Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{DH}	Data In Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{AVH}	Address Advance Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns

WRITE CYCLE TIMING

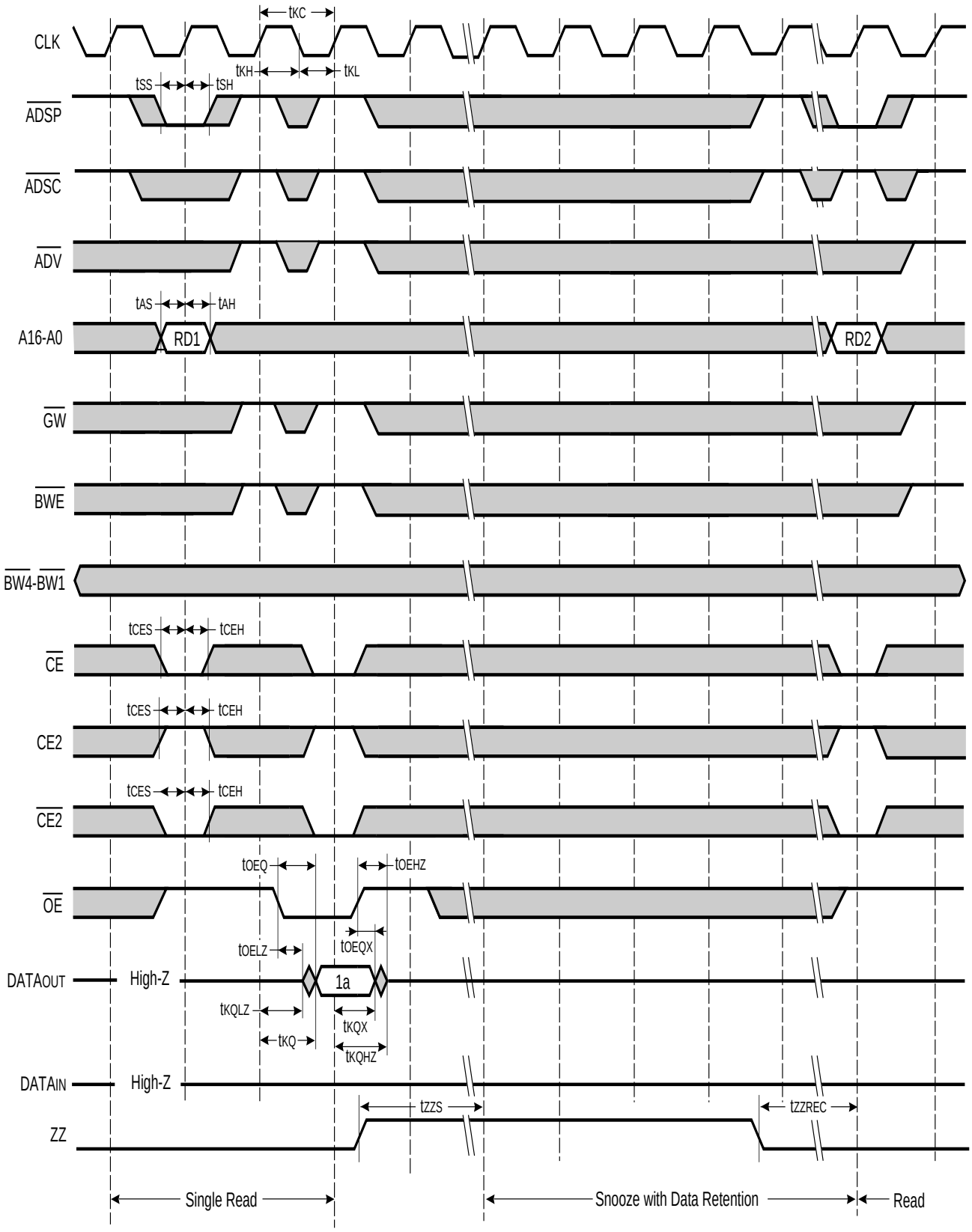


SNOOZE AND RECOVERY CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	-166		-150		-133		-117		-5		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{KC}	Cycle Time	6	—	6.7	—	7.5	—	8.5	—	10	—	ns
t_{KH}	Clock High Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{KL}	Clock Low Time	2.4	—	2.6	—	2.8	—	3.4	—	4	—	ns
t_{KQ}	Clock Access Time	—	3.5	—	3.8	—	4	—	4	—	5	ns
t_{KQX}(1)	Clock High to Output Invalid	1.5	—	1.5	—	1.5	—	2	—	2.5	—	ns
t_{KQLZ}(1,2)	Clock High to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{KQHZ}(1,2)	Clock High to Output High-Z	1.5	3.6	1.5	6.7	1.5	7.5	1.5	8.5	1.5	10	ns
t_{OEQ}	Output Enable to Output Valid	—	3.5	—	3.5	—	3.9	—	4	—	5	ns
t_{OEQX}(1)	Output Disable to Output Invalid	0	—	0	—	0	—	0	—	0	—	ns
t_{OELZ}(1,2)	Output Enable to Output Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t_{OEHZ}(1,2)	Output Disable to Output High-Z	2	3.5	2	3.5	2	3.8	2	4	2	5	ns
t_{AS}	Address Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{SS}	Address Status Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{CES}	Chip Enable Setup Time	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{SH}	Address Status Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
t_{ZZS}	ZZ Standby	2	—	2	—	2	—	2	—	2	—	cyc
t_{ZZREC}	ZZ Recovery	2	—	2	—	2	—	2	—	2	—	cyc

Notes:
1. Guaranteed but not 100% tested. This parameter is periodically sampled.
2. Tested with load in Figure 2.

SNOOZE AND RECOVERY CYCLE TIMING



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Speed	Order Part Number	Package
166 MHz	IS61SP12832-166TQ IS61SP12832-166B	14x20x1.4mm LQFP 14*22mm PBGA
150 MHz	IS61SP12832-150TQ IS61SP12832-150B	14*20*1.4mm LQFP 14*22mm PBGA
133 MHz	IS61SP12832-133TQ IS61SP12832-133B	14*20*1.4mm LQFP 14*22mm PBGA
117 MHz	IS61SP12832-117TQ IS61SP12832-117B	14*20*1.4mm LQFP 14*22mm PBGA
5 ns	IS61SP12832-5TQ IS61SP12832-5B	14*20*1.4mm LQFP 14*22mm PBGA

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