Data Sheet | September 30, 2011 | FN7456.3

1GHz Triple Multiplexing Amplifiers

The ISL59424, ISL59445 are 1GHz bandwidth multiplexing amplifiers designed primarily for video input switching. These MUX-amps exhibit a fixed gain of 1 and also feature a high speed three-state to enable the output of multiple devices to be wired together. All logic inputs have pull-downs to ground and may be left floating. The $\overline{EN}$ pin, when pulled high, sets the ISL59424, ISL59445 in to low current mode-consuming just 15mW. An added feature in the ISL59424 is a latch enable function ($\overline{LE}$) that allows independent logic control using a common logic bus. When $\overline{LE}$ is high the last logic state is preserved.

TABLE 1. CHANNEL SELECT LOGIC TABLE ISL59424

S0	$\overline{ENABLE}$	HIZ	$\overline{LE}$	OUTPUT
0	0	0	0	INO (A, B, C)
1	0	0	0	IN1 (A, B, C)
X	1	X	X	Power Down
X	0	1	X	High Z
X	0	0	1	Last S0 State Preserved

TABLE 2. CHANNEL SELECT LOGIC TABLE ISL59445

S1	S0	$\overline{ENABLE}$	HIZ	OUTPUT
0	0	0	0	IN0 (A, B, C)
0	1	0	0	IN1 (A, B, C)
1	0	0	0	IN2 (A, B, C)
1	1	0	0	IN3 (A, B, C)
X	X	1	X	Power Down
X	X	0	1	High Z

Features

- Triple 2:1 and 4:1 Multiplexers for RGB
- Internally Set Gain-of-1
- High Speed Three-state Outputs (HIZ)
- Power-down Mode ($\overline{EN}$)
- Latch Enable (ISL59424)
- ±5V Operation
- ±1200 V/µsec Slew Rate
- 1GHz Bandwidth
- Latched Select Pin (ISL59424)
- Pb-Free (RoHS Compliant)

Applications

- HDTV/DTV Analog Inputs
- Video Projectors
- Computer Monitors
- Set-top Boxes
- Security Video
- Broadcast Video Equipment

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59424IRZ	59424 IRZ	24 Ld QFN	MDP0046
ISL59424IRZ-T13	59424 IRZ	24 Ld QFN	MDP0046
ISL59424IRZ-T7	59424 IRZ	24 Ld QFN	MDP0046
ISL59445IRZ	59445 IRZ	32 Ld QFN	L32.5x6A
ISL59445IRZ-T13	59445 IRZ	32 Ld QFN	L32.5x6A
ISL59445IRZ-T7	59445 IRZ	32 Ld QFN	L32.5x6A
ISL59445IRZ-EVAL	Evaluation Board		

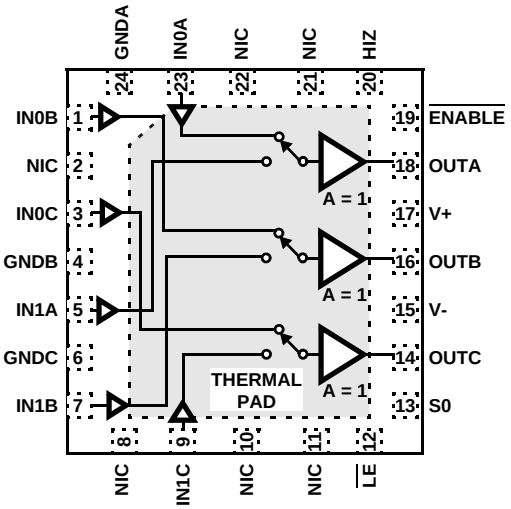
NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL59424 and ISL59445. For more information on MSL please see techbrief TB363.
4. 32 LD QFN Exposed Pad Size 2.48 x 3.40mm.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2005, 2010. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

Pinouts

ISL59424
(24-LD QFN)
TOP VIEW

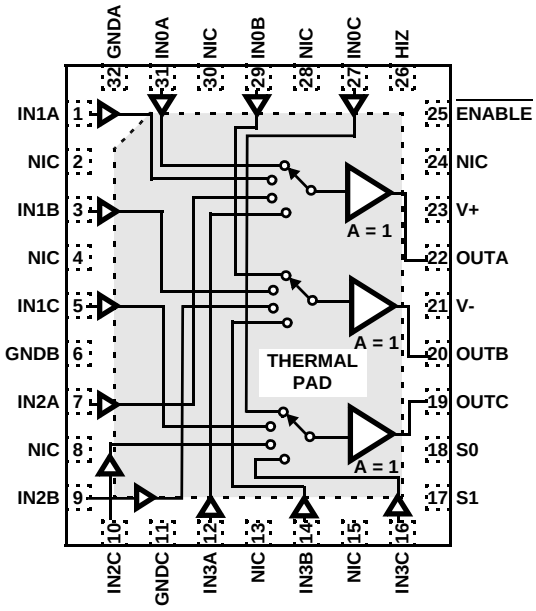


THERMAL PAD INTERNALLY CONNECTED TO V-. PAD MUST BE TIED TO V-

LATCHED ON HIGH $\overline{LE}$

NIC = NO INTERNAL CONNECTION

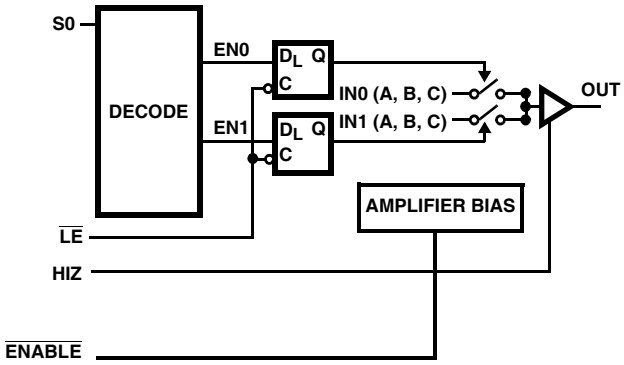
ISL59445
(32-LD QFN)
TOP VIEW



THERMAL PAD INTERNALLY CONNECTED TO V-. PAD MUST BE TIED TO V-

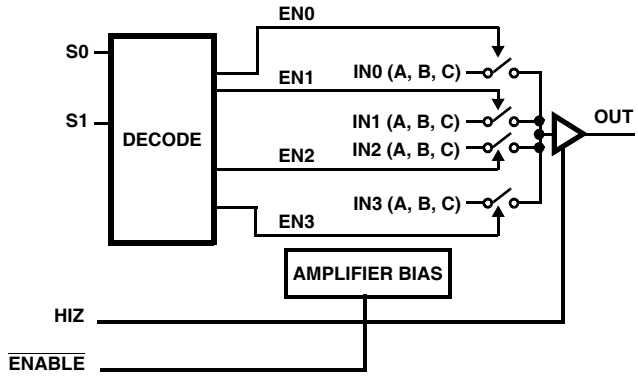
NIC = NO INTERNAL CONNECTION

Functional Diagram ISL59424



A LOGIC HIGH ON $\overline{LE}$ WILL LATCH THE LAST S0 STATE. THIS LOGIC STATE IS PRESERVED WHEN CYCLING HIZ OR ENABLE FUNCTIONS.

Functional Diagram ISL59445



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V+ to V-) 11V
Input Voltage . . . . . V- -0.5V, V+ +0.5V
Supply Turn-On Slew Rate 1V/µs
Digital & Analog Input Current (Note 5) 50mA
Output Current (Continuous) 50mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2500V
Machine Model 300V

Thermal Information

Thermal Resistance (Typical, Notes 6, 7)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN	46	10
32 Ld QFN	46	10

Storage Temperature Range . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -40°C to +85°C
Operating Junction Temperature . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, V_{IN} = $1V_{P-P}$ & R_L = 500Ω to GND unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
I_S Enabled	Enabled Supply Current (ISL59424)	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low, I_S+	35	39	43	mA
		No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low, I_S-	-40	-36	-32	mA
	Enabled Supply Current (ISL59445)	No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low, I_S+	47	53	60	mA
		No load, V_{IN} = 0V, $\overline{\text{Enable}}$ Low, I_S-	-57	-50	-44	mA
+I_S Disabled	Disabled Supply Current	$\overline{\text{Enable}}$ High, I_S+	2	3	4	mA
		$\overline{\text{Enable}}$ High, I_S-	-50	0	-	µA
I_b	Input Bias Current	V_{IN} = 0	-3.4	-2.2	-1.4	µA
I_{TRI}	Bias current into output, HIZ mode	ISL59424 - V_{OUT} = +5V	8	15	22	µA
		ISL59445 - V_{OUT} = 0V	-35	0	35	µA
V_{OUT}	Positive and Negative Output Swing	V_{IN} = ±3.5V	±3.2	±3.4	-	V
I_{OUT}	Output Current	R_L = 10Ω to GND	±80	±130	-	mA
V_{OS}	Offset Voltage		-13	3	13	mV
R_{OUT}	HIZ Output Resistance	HIZ = Logic High	-	1.0	-	MΩ
R_{OUT}	Enabled Output Resistance	HIZ = Logic Low	-	0.2	-	Ω
R_{IN}	Input Resistance	V_{IN} = ±3.5V	-	10	-	MΩ
A_{CL} or A_V	Voltage Gain	V_{IN} = ±1.5V	0.98	0.99	1.0	V/V
LOGIC						
V_{IH}	Input High Voltage (Logic Inputs)		2	-	-	V
V_{IL}	Input Low Voltage (Logic Inputs)		-	-	0.8	V
I_{IH}	Input High Current (Logic Inputs)	V_H = 5V	235	270	320	µA
I_{IL}	Input Low Current (Logic Inputs)	V_L = 0V	-	1	3	µA
AC GENERAL						
PSRR	Power Supply Rejection Ratio (ISL59424)	DC, PSRR V+ and V- combined	60	73	-	dB
	Power Supply Rejection Ratio (ISL59445)	DC, PSRR V+ and V- combined	50	57	-	dB

Electrical Specifications V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, V_{IN} = $1V_{P-P}$ & R_L = 500Ω to GND unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
ISO	Channel Isolation (ISL59424)	f = 10MHz, C_L = 0.5pF, V_{IN} = -6dBm	-	80	-	dB
	Channel Isolation (ISL59445)		-	75	-	dB
Xtalk	Channel Cross Talk (ISL59424)	f = 10MHz, C_L = 0.5pF, V_{IN} = -6dBm	-	75	-	dB
	Channel Cross Talk (ISL59445)		-	70	-	-
dG	Differential Gain Error	NTC-7, R_L = 150, C_L = 0.5pF	-	0.02	-	%
dP	Differential Phase Error	NTC-7, R_L = 150, C_L = 0.5pF	-	0.02	-	°
BW	-3dB Bandwidth	C_L = 0.5pF	-	1000	-	MHz
FBW	0.1dB Bandwidth	C_L = 0.5pF	-	130	-	MHz
	0.1dB Bandwidth	CL = 1.5pF	-	200	-	MHz
SWITCHING CHARACTERISTICS						
SR	Slew Rate	25% to 75%, R_L = 150Ω, Input Enabled, C_L= 1.5pF, V_{IN} = ±1V	-	±1200	-	V/µs
V_{GLITCH} ISL58424	Channel-to-Channel Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	40	-	mV_{P-P}
	$\overline{\text{Enable}}$ Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	300	-	mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	200	-	mV_{P-P}
V_{GLITCH} ISL59445	Channel-to-Channel Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	20	-	mV_{P-P}
	$\overline{\text{Enable}}$ Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	200	-	mV_{P-P}
	HIZ Switching Glitch	V_{IN} = 0V, C_L = 0.5pF	-	200	-	mV_{P-P}
t_{SW-L-H}	Channel Switching Time Low-to-High	1.2V logic threshold to 10% movement of analog output	-	15	-	ns
t_{SW-H-L}	Channel Switching Time High-to-Low	1.2V logic threshold to 10% movement of analog output	-	15	-	ns
tr	Rise Time	10% to 90%	-	600	-	ps
tf	Fall Time	10% to 10%	-	800	-	ps
tpd	Propagation Delay	10% to 10%	-	600	-	ps
t_S	0.1% Settling Time	Step = 1V	-	6	-	ns
t_{LH}	Latch Enable HoldTime	$\overline{\text{LE}}$ = 0V	-	10	-	ns

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified.

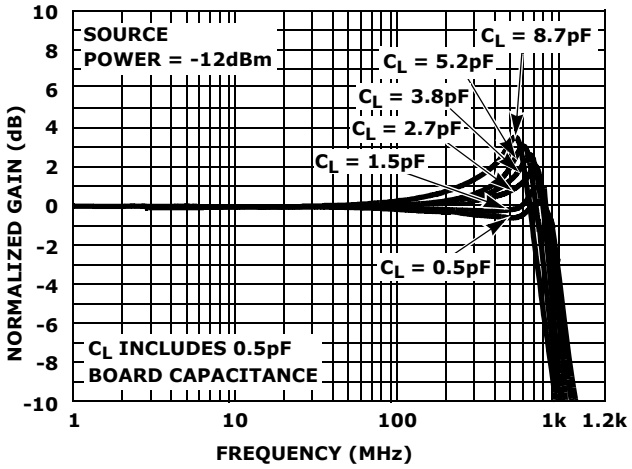


FIGURE 1. GAIN vs FREQUENCY vs C_L

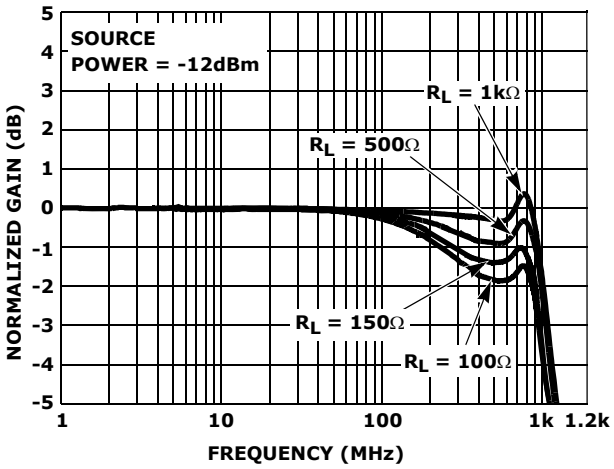


FIGURE 2. GAIN vs FREQUENCY vs R_L

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified. **(Continued)**

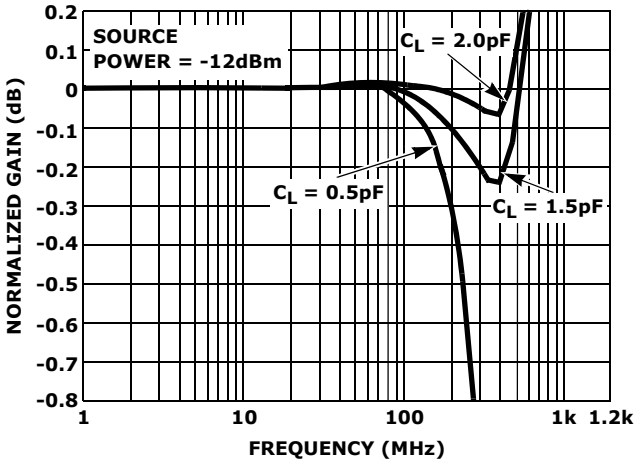


FIGURE 3. 0.1dB GAIN vs FREQUENCY

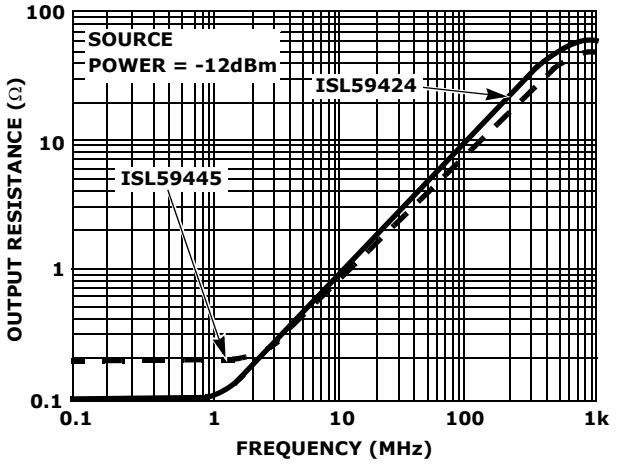


FIGURE 4. R_{OUT} vs FREQUENCY

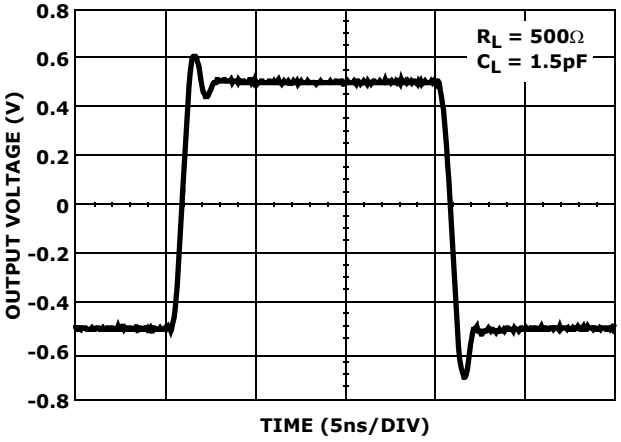


FIGURE 5. ISL59424 TRANSIENT RESPONSE

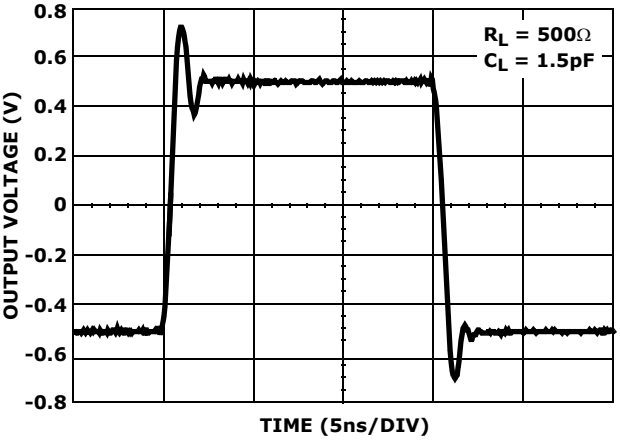


FIGURE 6. ISL59445 TRANSIENT RESPONSE

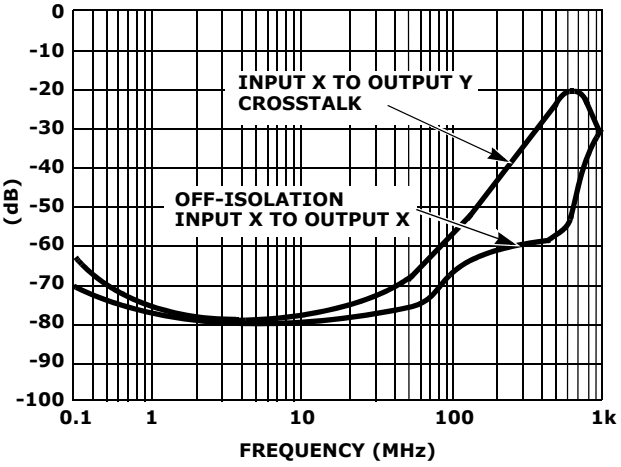


FIGURE 7. ISL59424 CROSSTALK AND OFF-ISOLATION

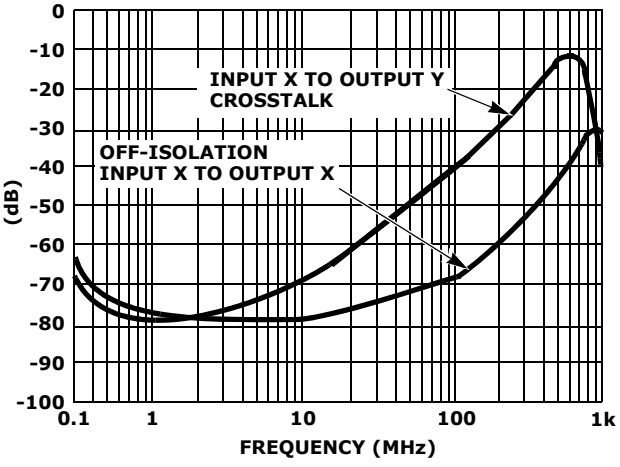


FIGURE 8. ISL59445 CROSSTALK AND OFF-ISOLATION

Typical Performance Curves V_S = ±5V, R_L = 500Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

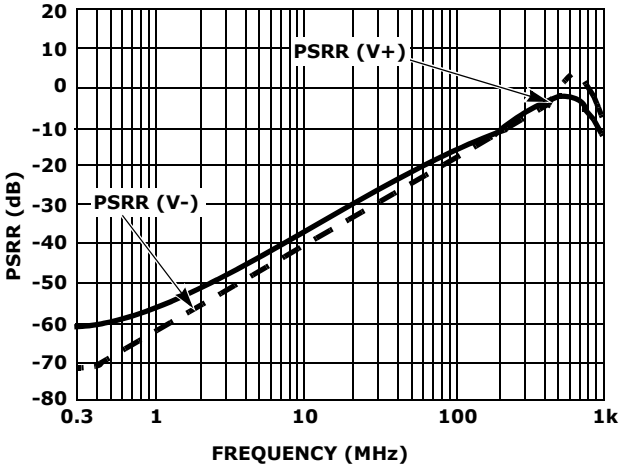


FIGURE 9. ISL59424 PSRR CHANNELS A, B, C

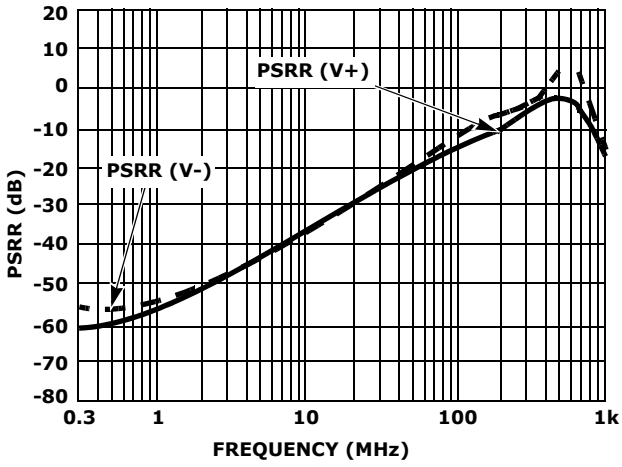


FIGURE 10. ISL59445 PSRR CHANNELS A, B, C

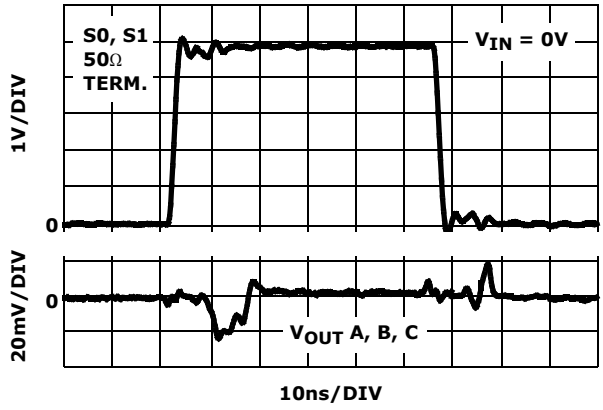


FIGURE 11. CHANNEL-TO-CHANNEL SWITCHING GLITCH V_{IN} = 0V

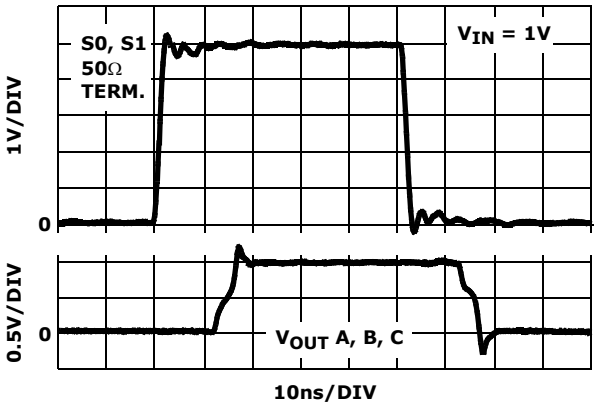


FIGURE 12. CHANNEL-TO-CHANNEL TRANSIENT RESPONSE V_{IN} = 1V

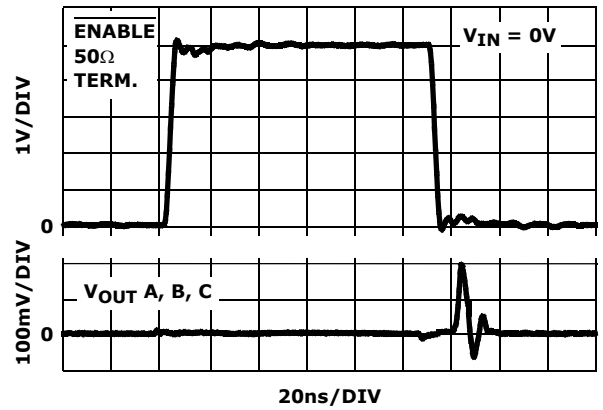


FIGURE 13. $\overline{\text{ENABLE}}$ SWITCHING GLITCH V_{IN} = 0V

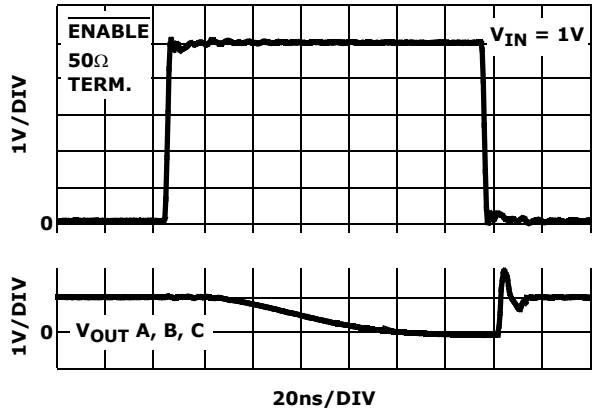


FIGURE 14. $\overline{\text{ENABLE}}$ TRANSIENT RESPONSE V_{IN} = 1V

Typical Performance Curves $V_S = \pm5V$, $R_L = 500\Omega$ to GND, $T_A = +25°C$, unless otherwise specified. **(Continued)**

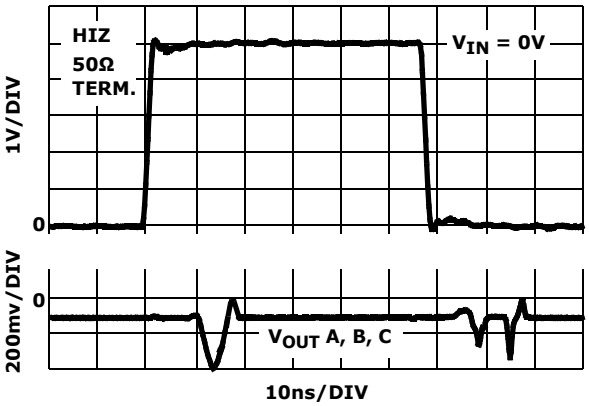


FIGURE 15. HIZ SWITCHING GLITCH V_{IN} = 0V

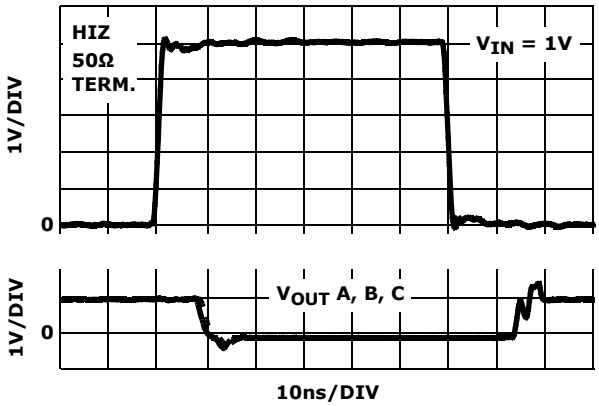


FIGURE 16. HIZ TRANSIENT RESPONSE V_{IN} = 1V

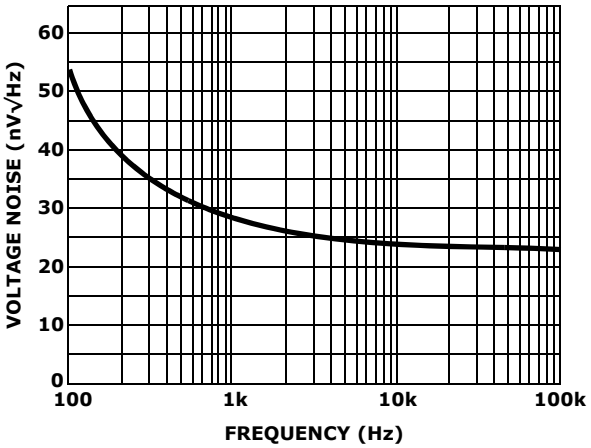
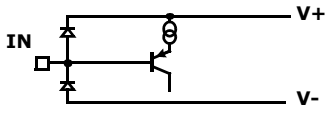


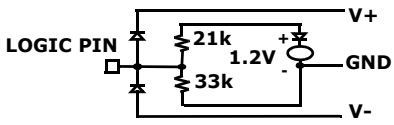
FIGURE 17. INPUT NOISE vs FREQUENCY (OUTPUT A, B, C)

Pin Descriptions

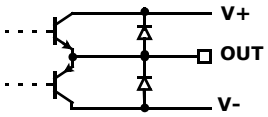
ISL59445 (32-LD QFN)	ISL59424 (24-LD QFN)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
1	5	IN1A	Circuit 1	Channel 1 input for output amplifier "A"
2, 4, 8, 13, 15, 24, 28, 30	2, 8, 10, 11, 21, 22	NIC	-	**N**ot **I**nternally **C**onnected; it is recommended these pins be tied to ground to minimize crosstalk.
3	7	IN1B	Circuit 1	Channel 1 input for output amplifier "B"
5	9	IN1C	Circuit 1	Channel 1 input for output amplifier "C"
6	4	GNDB	Circuit 4	Ground pin for output amplifier “B”
7		IN2A	Circuit 1	Channel 2 input for output amplifier "A"
9		IN2B	Circuit 1	Channel 2 input for output amplifier "B"
10		IN2C	Circuit 1	Channel 2 input for output amplifier "C"
11	6	GNDC	Circuit 4	Ground pin for output amplifier “C”
12		IN3A	Circuit 1	Channel 3 input for output amplifier "A"
14		IN3B	Circuit 1	Channel 3 input for output amplifier "B"
16		IN3C	Circuit 1	Channel 3 input for output amplifier "C"
17		S1	Circuit 2	Channel selection pin MSB (binary logic code)
18	13	S0	Circuit 2	Channel selection pin. LSB (binary logic code)
19	14	OUTC	Circuit 3	Output of amplifier “C”
20	16	OUTB	Circuit 3	Output of amplifier “B”
21	15	V-	Circuit 4	Negative power supply
22	18	OUTA	Circuit 3	Output of amplifier “A”
23	17	V+	Circuit 4	Positive power supply
25	19	$\overline{\text{ENABLE}}$	Circuit 2	Device enable (active low). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic High on this pin puts device into power-down mode. In power-down mode only logic circuitry is active. All logic states are preserved post power-down. This state is not recommended for logic control where more than one MUX-amp share the same video output line.
	12	$\overline{\text{LE}}$	Circuit 2	Device latch enable on the ISL59424. A logic high on $\overline{\text{LE}}$ will latch the last (S0, S1) logic state. HIZ and $\overline{\text{ENABLE}}$ functions are not latched with the $\overline{\text{LE}}$ pin.
26	20	HIZ	Circuit 2	Output disable (active high). Internal pull-down resistor ensures the device will be active with no connection to this pin. A logic high, puts the outputs in a high impedance state. Use this state to control logic when more than one MUX-amp share the same video output line.
27	3	IN0C	Circuit 1	Channel 0 for output amplifier "C"
29	1	IN0B	Circuit 1	Channel 0 for output amplifier "B"
31	23	IN0A	Circuit 1	Channel 0 for output amplifier "A"
32	24	GNDA	Circuit 4	Ground pin for output amplifier “A”



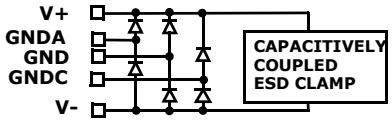
CIRCUIT 1



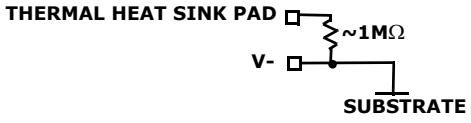
CIRCUIT 2



CIRCUIT 3



CIRCUIT 4



AC Test Circuits

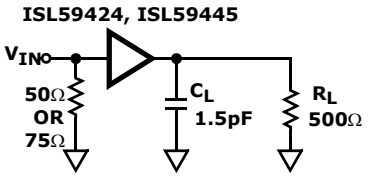


FIGURE 18A. TEST CIRCUIT WITH OPTIMAL OUTPUT LOAD

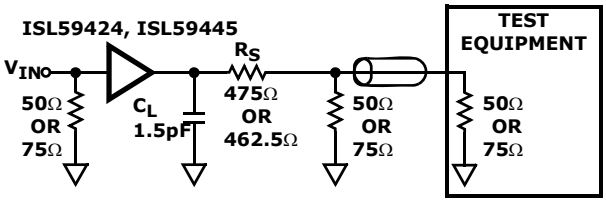


FIGURE 18B. TEST CIRCUIT FOR MEASURING WITH 50Ω OR 75Ω INPUT TERMINATED EQUIPMENT

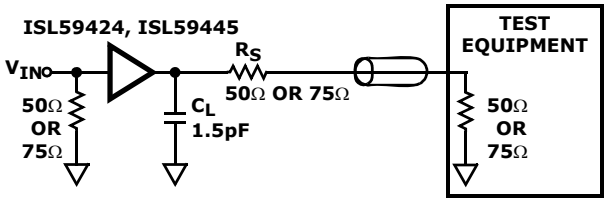


FIGURE 18C. BACKLOADED TEST CIRCUIT FOR VIDEO CABLE APPLICATION. BANDWIDTH AND LINEARITY FOR R_L LESS THAN 500Ω WILL BE DEGRADED.

FIGURE 18. TEST CIRCUITS

Figure 18A illustrates the optimum output load for testing AC performance. Figure 18B illustrates the optimum output load when connecting to 50Ω input terminated equipment.

Application Information

General

The ISL59424, ISL59445 are triple 2:1 and 4:1 muxes that are ideal for the matrix element of high performance switchers and routers. The ISL59424, ISL59445 are optimized to drive a 1.5pF in parallel with a 500Ω load. The capacitance can be split between the PCB capacitance an and external load capacitance. Their low input capacitance and high input resistance provide excellent 50Ω or 75Ω terminations.

Ground Connections

For the best isolation and crosstalk rejection, all GND pins and NIC pins must connect to the GND plane.

Control Signals

S0, S1, $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ - These pins are binary coded, TTL/CMOS compatible control inputs. The S0, S1 pins select which one of the inputs connect to the output. All three amplifiers are switched simultaneously from their respective inputs. The $\overline{\text{ENABLE}}$, $\overline{\text{LE}}$, HIZ pins are used to disable the part to save power, latch in the last logic state and three-state the output amplifiers, respectively. For control signal rise and fall times less than 10ns the use of termination resistors close to the part should be considered to minimize transients coupled to the output.

Power-Up Considerations

The ESD protection circuits use internal diodes from all pins the V+ and V- supplies. In addition, a dV/dT- triggered clamp is connected between the V+ and V- pins, as shown in the Equivalent Circuits 1 through 4 section of the “Pin Descriptions” on page 8. The dV/dT triggered clamp imposes a maximum supply turn-on slew rate of 1V/µs. Damaging currents can flow for power supply rates-of-rise in excess of 1V/µs, such as during hot plugging. Under these conditions, additional methods should be employed to ensure the rate of rise is not exceeded.

Consideration must be given to the order in which power is applied to the V+ and V- pins, as well as analog and logic input pins. Schottky diodes (Motorola MBR0550T or equivalent) connected from V+ to ground and V- to ground (Figure 19) will shunt damaging currents away from the internal V+ and V- ESD diodes in the event that the V+ supply is applied to the device before the V- supply.

If positive voltages are applied to the logic or analog video input pins before V+ is applied, current will flow through the internal ESD diodes to the V+ pin. The presence of large decoupling capacitors and the loading effect of other circuits connected to V+, can result in damaging currents through the ESD diodes and other active circuits within the device. Therefore, adequate current limiting on the digital and analog inputs is needed to prevent damage during the time the voltages on these inputs are more positive than V+.

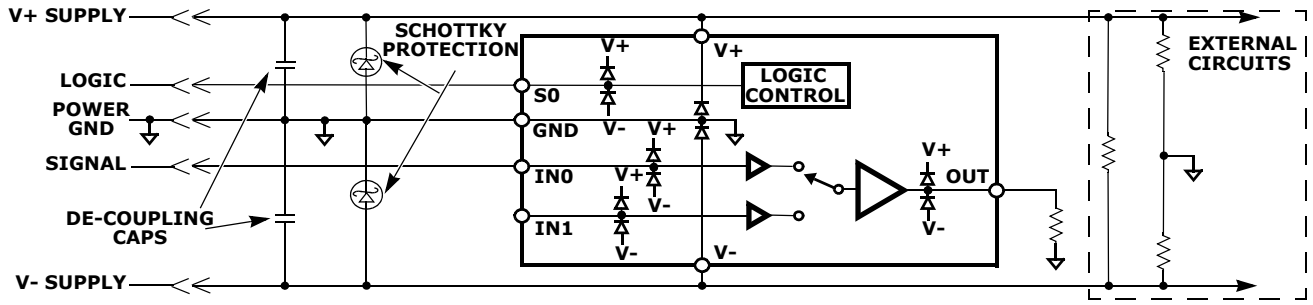


FIGURE 19. SCHOTTKY PROTECTION CIRCUIT

HIZ State

An internal pull-down resistor connected to the HIZ pin ensures the device will be active with no connection to the HIZ pin. The HIZ state is established within approximately 15ns (Figure 16) by placing a logic high (>2V) on the HIZ pin. If the HIZ state is selected, the output is a high impedance 1.4MΩ with approximately 1.5pF in parallel with a 10µA bias current from the output. Use this state to control the logic when more than one mux shares a common output.

In the HIZ state the output is three-stated, and maintains its high Z even in the presence of high slew rates. The supply current during this state is basically the same as the active state.

$\overline{\text{ENABLE}}$ and Power Down States

The enable pin is active low. An internal pull-down resistor ensures the device will be active with no connection to the $\overline{\text{ENABLE}}$ pin. The Power Down state is established within approximately 100ns (Figure 14), if a logic high (>2V) is placed on the $\overline{\text{ENABLE}}$ pin. In the Power Down state, the output has no leakage but has a large variable capacitance (on the order of 15pF), and is capable of being back-driven. Under this condition, large incoming slew rates can cause fault currents of tens of mA. **Do not use this state as a logic control for applications driving more than one mux on a common output.**

$\overline{\text{LE}}$ State

The ISL59424 is equipped with a Latch Enable pin. A logic high (>2V) on the $\overline{\text{LE}}$ pin latches the last logic state. This logic state is preserved when cycling HIZ or $\overline{\text{ENABLE}}$ functions.

Limiting the Output Current

No output short circuit current limit exists on these parts. All applications need to limit the output current to less than 50mA. Adequate thermal heat sinking of the parts is also required.

Application Example

Figure 19 illustrates the use of the ISL59445, two ISL84517 SPST switches and one NC7ST00P5X NAND gate to mux 3 different component video signals and one RGB video signal. The SPDT switches provide the sync signal for the RGB video and disconnects the sync signal for the component signal.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. The following are recommendations to achieve optimum high frequency performance from your PC board.

- The use of low inductance components such as chip resistors and chip capacitors is strongly recommended.
- Minimize signal trace lengths. Trace inductance and capacitance can easily limit circuit performance. Avoid sharp corners, use rounded corners when possible. Vias in the signal lines add inductance at high frequency and should be avoided. PCB traces greater than 1" begin to exhibit transmission line characteristics with signal rise/fall times of 1ns or less. High frequency performance may be degraded for traces greater than one inch, unless strip line are used.
- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches.
- Maximize use of AC de-coupled PCB layers. All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines). Avoid vias in the signal I/O lines.
- Use proper value and location of termination resistors. Termination resistors should be as close to the device as possible.
- When testing use good quality connectors and cables, matching cable types and keeping cable lengths to a minimum.
- Minimum of 2 power supply de-coupling capacitors are recommended (1000pF, 0.01µF) as close to the devices as possible - Avoid vias between the capacitor and the device because vias add unwanted inductance. Larger caps can be farther away. When vias are required in a layout, they should be routed as far away from the device as possible.

- The NIC pins are placed on both sides of the input pins. These pins are not internally connected to the die. It is recommended these pins be tied to ground to minimize crosstalk.

The QFN Package Requires Additional PCB Layout Rules for the Thermal Pad

The thermal pad is electrically connected to V- supply through the high resistance IC substrate. Its primary function is to provide heat sinking for the IC. However, because of the connection to the V- supply through the substrate, the thermal pad must be tied to the V- supply to prevent unwanted current flow to the thermal pad. Do **not** tie this pin to GND. Connecting this pin to GND could result in large back biased currents flowing between GND and V-. The ISL59445 uses the package with pad dimensions of D2 = 2.48mm and E2 = 3.4mm.

Maximum AC performance is achieved if the thermal pad is attached to a dedicated de-coupled layer in a multi-layered PC board. In cases where a dedicated layer is not possible, AC performance may be reduced at upper frequencies.

The thermal pad requirements are proportional to power dissipation and ambient temperature. A dedicated layer eliminates the need for individual thermal pad area. When a dedicated layer is not possible a 1” x 1” pad area is sufficient for the ISL59445 that is dissipating 0.5W in +50°C ambient. Pad area requirements should be evaluated on a case by case basis.

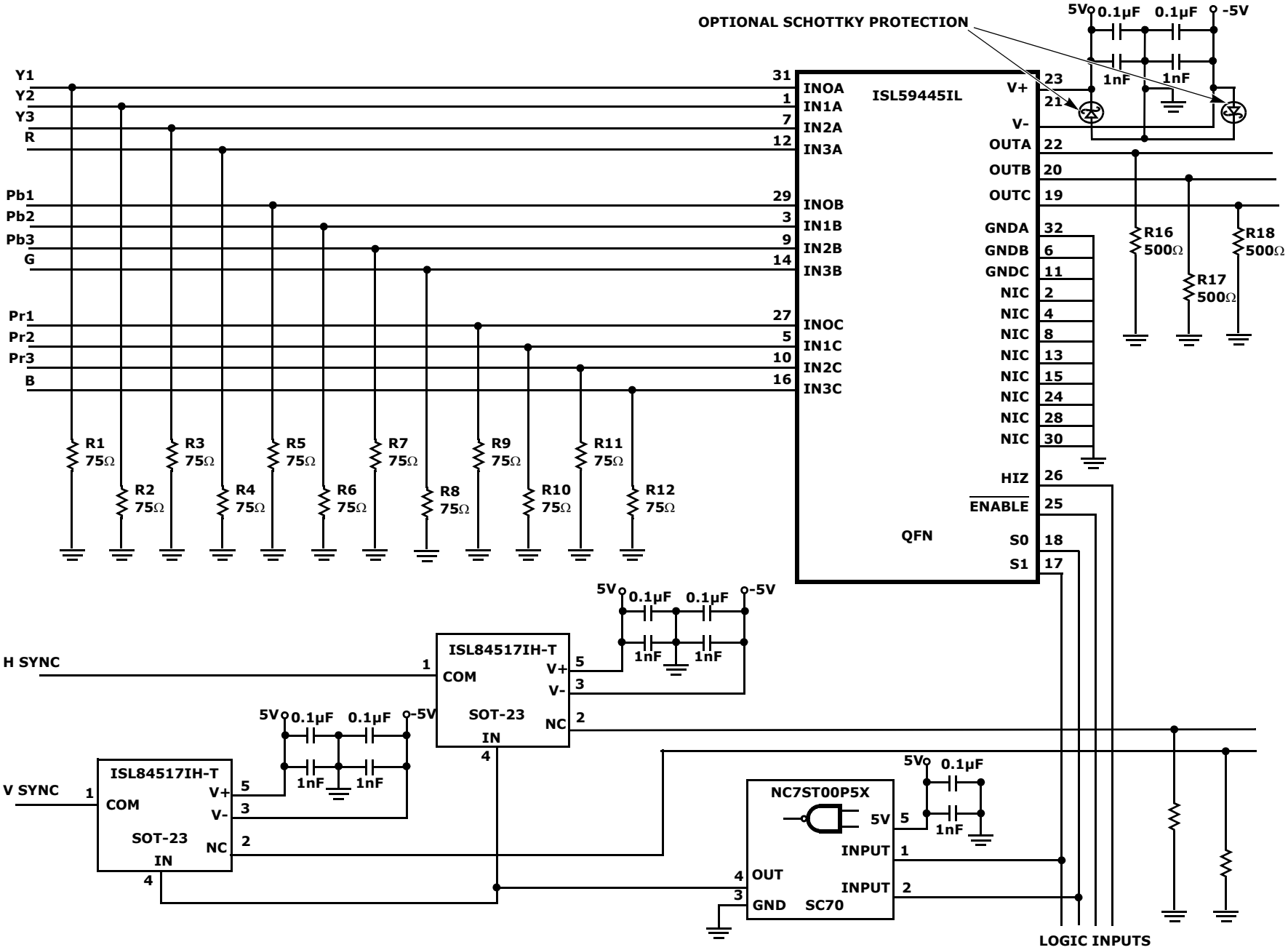
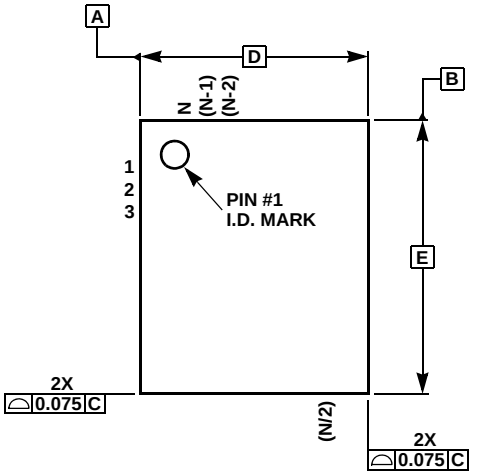
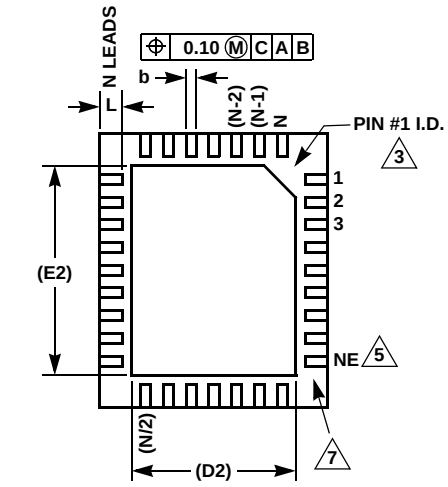


FIGURE 20. APPLICATION SHOWING THREE YPBPR CHANNELS AND ONE RGB+HV CHANNEL

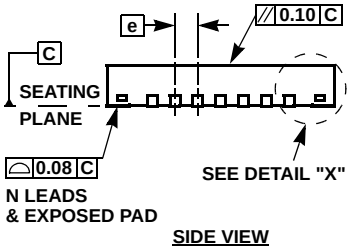
QFN (Quad Flat No-Lead) Package Family



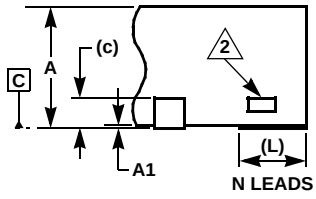
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

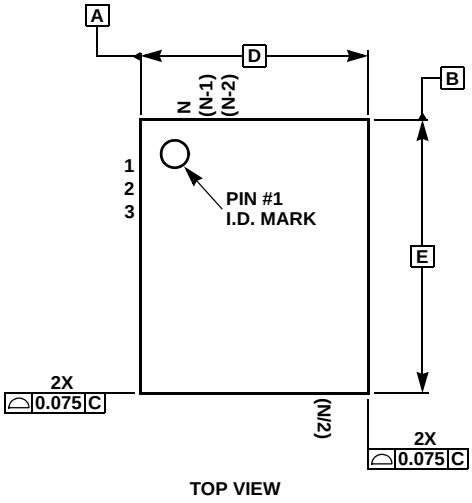
SYMBOL	MILLIMETERS					TOLERANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 11 2/07

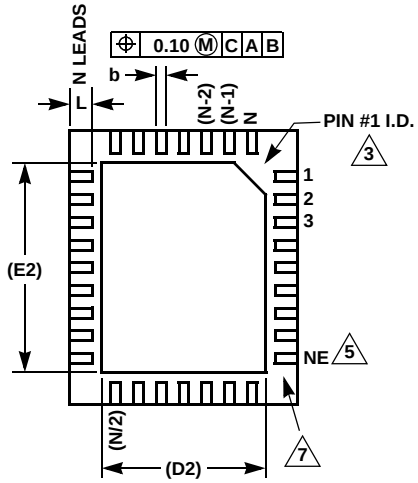
NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

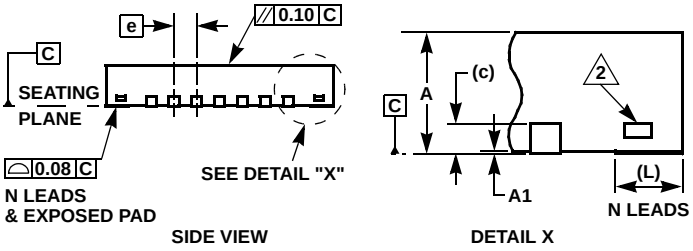
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



TOP VIEW



BOTTOM VIEW



SIDE VIEW DETAIL X

L32.5x6A (One of 10 Packages in MDP0046)
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	0.00	0.02	0.05	-
D		5.00 BSC		-
D2		2.48 REF		-
E		6.00 BSC		-
E2		3.40 REF		-
L	0.45	0.50	0.55	-
b	0.17	0.22	0.27	-
c		0.20 REF		-
e		0.50 BSC		-
N		32 REF		4
ND		7 REF		6
NE		9 REF		5

Rev 1 2/09

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation’s quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com