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ITE Tech. Inc.

IT8502E/F/G

Embedded Controller

Preliminary Specification 0.7.7

ITE TECH. INC.

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Revision History

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5	Table 5-3. Pin Descriptions of Serial Peripheral Interface (SSPI) • Added SBUSY pin.	20
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7	7.7.3.1 SMBus Master Interface • Modification for I2C compatible.	209
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7	7.7.4.18 Slave Interface Select Register (SLVISELR) • Newly added register.	237
7	7.14.4.8 External Timer 2 Counter High Byte 2 (ET2CNTLH2R) • External Timer 2 changed from 16-bit to 24-bit.	295
7	7.14.4.9External Timer/WDT Control Register (ETWCTRL) • Added bits to make EWDT be stopped.	296
7	Errata: 7.15.4.10Reset Control DMM (RSTDMMC)	 302
7	7.18.5.3SPI Control Register 2 (SPICTRL2) • Added bit 7-3. 7.18.5.4SPI Start and End Status Register (SPISTS) • Added bit 7-6. 7.18.5.5 SPI Control Register 3 (SPICTRL3) • Newly added register.	316 316 317
7	7.11.4.7 PWM Polarity Register (PWMPOL) 7.12.4.2 Group Clock Source and Mode Select Register (GCSMS) • 6.14 MHz can be available if PLLFREQ == 0011b	266 280
7	7.5.3.1 General Control Register (GCR)	193
6, 7	6.2.2.4 Chip Version (CHIPVER) 7.15.4.3 Chip Version (ECHIPVER) • Version registers were revised.	45 299

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1. Features

- **8032 Embedded Controller**
  - Twin Turbo version/3-stage pipeline
  - 9.2 MHz for EC domain and 8032 internal timer
  - Variable frequency range to gain the maximum 8032 code-fetch performance
  - Instruction set compatible with standard 8051/2

- **LPC Bus Interface**
  - Compatible with the LPC specification v1.1
  - Supports I/O read/write
  - Supports Memory read/write
  - Supports FWH read/write
  - Serial IRQ

- **Flash Interface**
  - Behaves as a LPC/FWH memory device (HLPC)
  - Supports external serial flash with 32.3~64.5 MHz
  - Up to 16M bytes Flash space shared by the host and EC side (serial flash)
  - HLPC: Hardware read protection plus hardware / software write protection

- **SMBus Controller**
  - SMBus spec. 2.0
  - 4 SMBus masters + 1 slave
  - 4 SMBus channels
  - Compatible with I2C cycles

- **System Wake Up Control**
  - Modem RI# wake up
  - Telephone RING# wake up
  - IRQ/SMI routing

- **EC Wake Up Control**
  - 48 external/internal wake up events

- **Interrupt Controller**
  - 72 interrupt events to EC
  - Fixed priority

- **Timer / Watch Dog Timer**
  - 3 internal 16-bit multi-function timers inside 8032, which is based on EC clock
  - 1 internal WDT inside 8032, which is based on EC clock
  - 1 external 16-bit timer and 1 external 24-bit timer in ETWD module, which are based on 32.768 k clock source
  - 1 external 16-bit WDT in ETWD module, which is based on 32.768 k clock source

- **UART**
  - 1 full duplex UART inside 8032
  - 1 standard serial ports (legacy 16C550 COM1)
  - Baud rate up to 460800

- **ACPI Power Management Channel**
  - 2 Power management channels
  - Compatible and enhanced mode

- **Battery-backed SRAM**
  - 192-byte battery-backed memory space
  - Supports power-switch circuit

- **GPIO**
  - Supports 73-port GPIO
  - Programmable pull up/pull down
  - Schmitt trigger for input

- **External GPIO Controller (EGPC)**
  - Communicate with 4 IT8301 chips
  - Each IT8301 supports 38 GPIO ports

- **KBC Interface**
  - 8042 style KBC interface
  - Legacy IRQ1 and IRQ12
  - Fast A20G and KB reset

- **ADC**
  - 12 ADC channels (8 external)
  - 10-bit resolution (+/- 4LSB)
  - Digital filter for noise reduction

- **DAC**
  - 6 DAC channels
  - 8-bit DAC

- **PWM**
  - 8 PWM channels
  - Base clock frequency is 32.768 kHz
  - 8 duty cycle resolution
  - 8/16-bit common input clock prescaler
  - 4 prescalers for 8 PWM output used for devices with different frequencies
  - 2 Tachometers for measuring fan speed

- **TMR**
  - Supports four channels
  - Supports 8-bit/16-bit pulse mode, and toggle mode

- **PS/2 Interface**
  - 3 PS/2 interface
  - Hardware/Software mode selection

- **KB Matrix Scan**
  - Hardware keyboard scan
  - 18x8 keyboard matrix scan

- **SPI Slave Interface (SSPI)**
  - 1-channel SPI Master, Freq between 575 kHz and 4.6MHz
  - 4-wire or 3-wire (bi-directional data) I/F
  - 8-bit or 1-bit transaction
  - SPI Mode 0, 1, 2, 3

- **In-System Programming**
  - ISP via parallel port interface on existing KBS connector
  - Fast flash programming with software provided by ITE

- **Power Consumption**
  - Standby with Sleep mode current: 250 μA

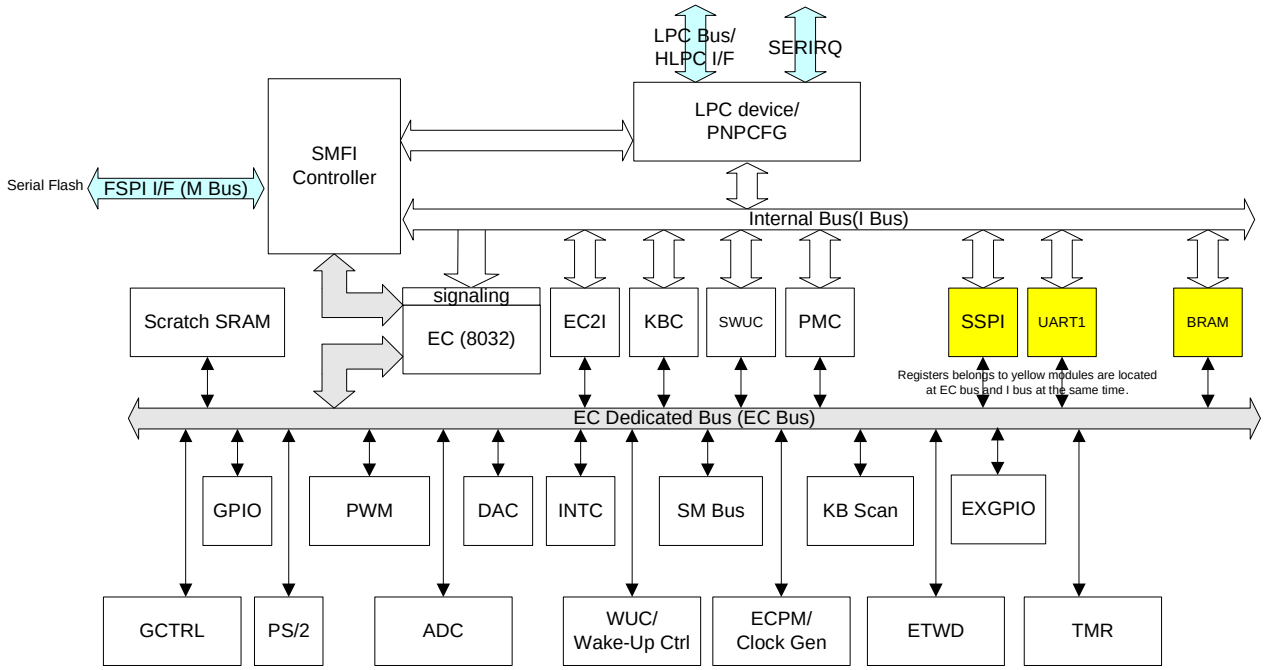
- **Package**
  - LQFP 128L / QFP 128L / TFBGA 128

2. General Description

The IT8502 is a highly integrated embedded controller with system functions suitable for mobile system applications. The IT8502 directly interfaces to the LPC bus and provides ACPI embedded controller function, keyboard controller (KBC) and matrix scan, external flash interface for system BIOS and EC code, PWM and ADC for hardware monitor, PS/2 interface for external keyboard/mouse devices, BRAM and system wake up functions for system power management. It also supports the external flash (or EPROM) to be shared by the host and EC side.

3. System Block Diagram

3.1 Block Diagram



- **Host Domain:**
  LPC, PNPCFG logic device, host parts of SMFI/SWUC/KBC/PMC logical devices and host parts of EC2I.

- **EC Domain:**
  EC 8032, INTC, WUC KB Scan, GPIO, ECPM, SMB, PS/2, DAC, ADC, PWM, HWS, ETWD, EC2I, GCTRL, BRAM, EGPC, DBGR, EC parts of SMFI/SWUC/KBC/PMC and EC parts of EC2I.

- **Double-mapping Module:**
  BRAM, SSPI and UART1

Note:
There are three SPI functions in EC. Two of them are masters and one is slave.
1. SPI memory master (abbreviated as FSPI) is connected to the SPI flash.
2. SPI master (abbreviated as SSPI) is connected to the slow (contrast to SPI flash) SPI slave(s).

3.2 Host/EC Mapped Memory Space

Figure 3-1. Host/Flash and EC/Flash Mapping (General)

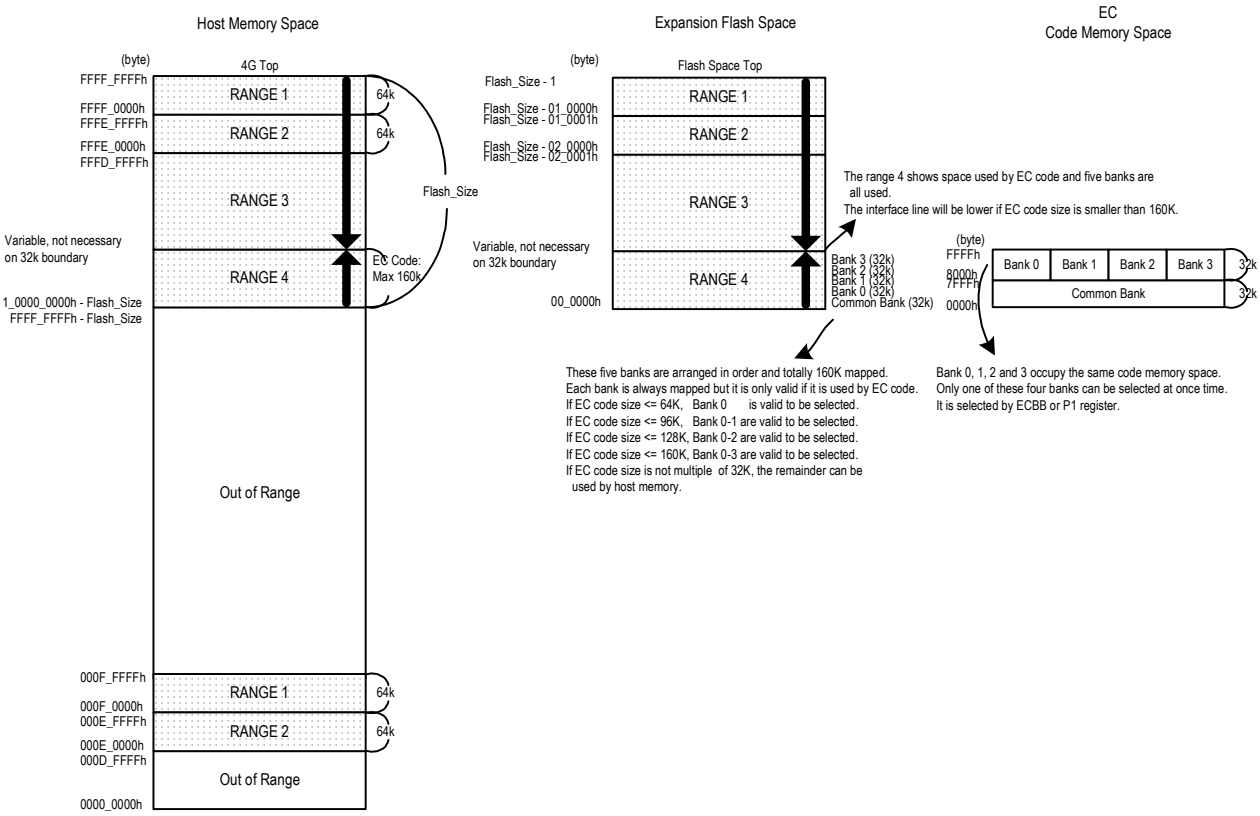
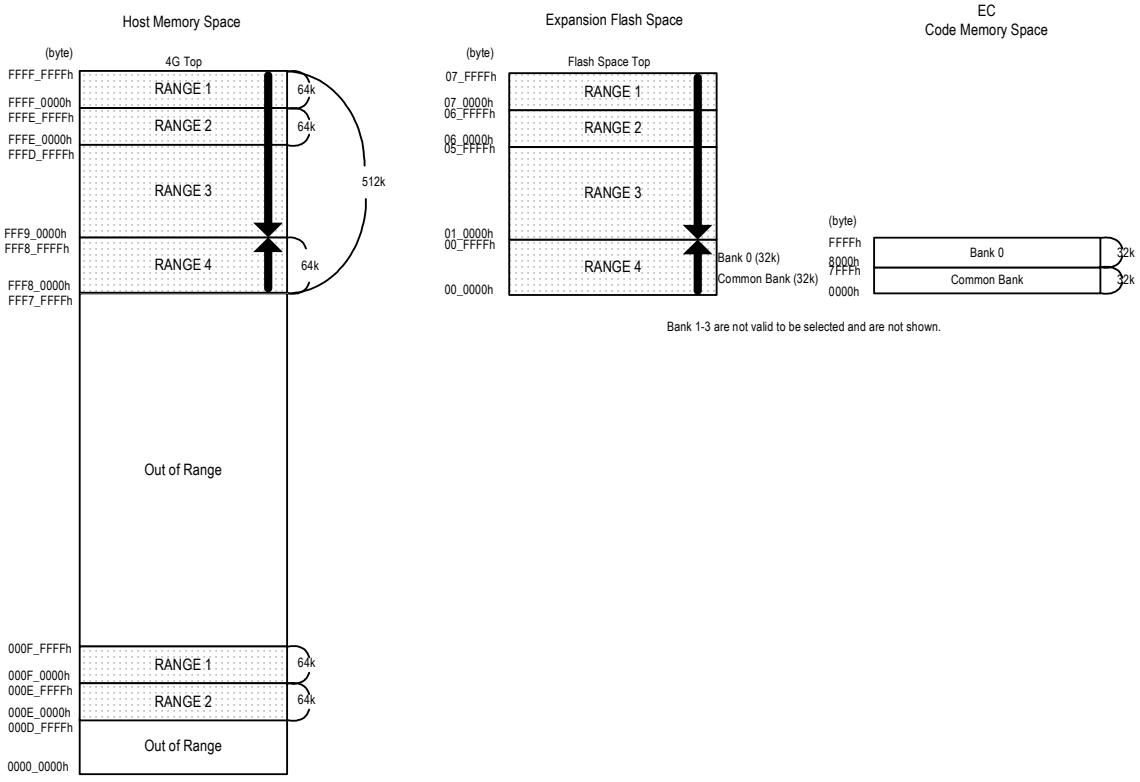


Figure 3-2. Host/Flash and EC/Flash Mapping (Flash Size = 512k, EC Code = 64k, a specific example)



The flash memory space is shared between the host side and EC side, and it is shown in Figure 3-1. An example of 512k flash size, 64k EC code size is shown in Figure 3-2.

The host memory 4G byte top is always mapped into the top of flash space and the host processor fetches the first instruction after reset at FFFF_FFF0h in the host memory, which is 16 bytes below the uppermost flash space.

The bottom of EC code is always mapped into the bottom of flash space and EC R8032TT micro-controller fetches the first instruction after reset at 00_0000h in the EC code memory, which is 1 byte in the lowermost flash space.

The interface line of host memory and EC code is variable and not necessary on 32k boundary.

Table 3-1. Host/Flash Mapping

Host Memory Space on LPC Bus (byte)	Mapped Expansion Flash Space (byte)	Size (byte)	Mapping Condition
(1_0000_0000h–Flash_Size)~ FFFF_FFFFh	00_0000h~ (Flash_Size-1)	Flash_Size	Always
000F_0000h ~ 000F_FFFFh	(Flash_Size-01_0000h)~ (Flash_Size-1)	64k	Always
000E_0000h ~ 000E_FFFFh	(Flash_Size-02_0000h)~ (Flash_Size-01_0001h)	64k	BIOSEXTS= 1
Note: The host side can map all flash range regardless of EC code space. **Note:** All host mappings are controlled by HBREN bit in HCTRL2R register. **Note:** Flash Size is defined in FMSSR register.			

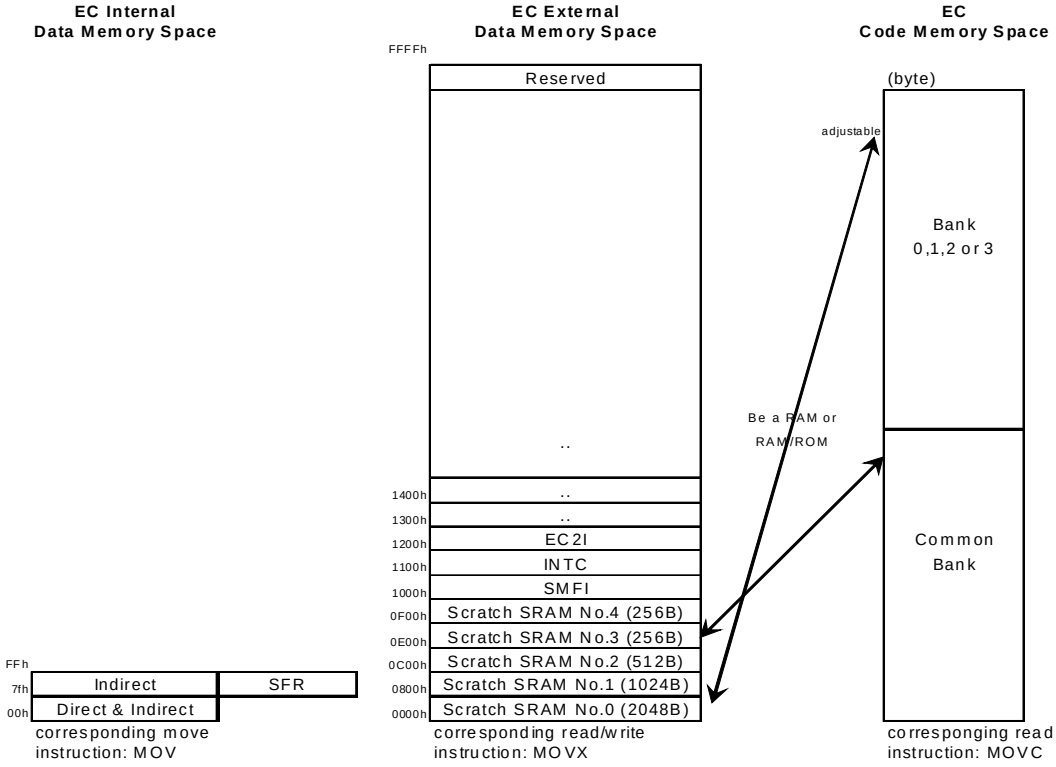
Table 3-2. EC/Flash Mapping

EC Code Memory Space (byte)	Mapped Flash Address Range (byte)	Size (byte)	Mapping Condition	Bank Selected Condition
Bank 3: 8000h ~ FFFFh	02_0000h ~ 02_7FFFh	32k	Always	ECBB=11
Bank 2: 8000h ~ FFFFh	01_8000h ~ 01_FFFFh	32k	Always	ECBB=10
Bank 1: 8000h ~ FFFFh	01_0000h ~ 01_7FFFh	32k	Always	ECBB=01
Bank 0: 8000h ~ FFFFh	00_8000h ~ 00_FFFFh	32k	Always	ECBB=00
Common Bank: 0000h ~ 7FFFh	00_0000h ~ 00_7FFFh	32k	Always	Always

Note: EC code can use the maximum 160k by banking.
Note: All EC code memory space is mapped to both EC and host side at the same time. The EC size is not necessary on 32k boundary.
Note: If BSO=1, ECBB is replaced with P1 register of 8032.
ECBB means ECBB field in FECBSR register.
BSO means BSO bit in FPCFG register.

3.3 EC Mapped Memory Space

Figure 3-3. EC 8032 Data/Code Memory Map



See also Figure 6-3. Scratch SRAM in Data Space on page 74.
See also section 8 Register List on page 337.

There are five internal Scratch SRAM No 0-4, which are always mapped into data space and may be mapped into code space if their corresponding code space mapping registers are enabled. It means that Scratch SRAM may be mapped into data and code space at the same time and the firmware on Scratch ROM can access the same Scratch RAM. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.

The EC code space is 64k bytes and physically occupies the maximum 160 k bytes at the bottom of the flash space. Refer to Figure 3-1 on page 5 for the details.

3.4 Register Abbreviation

The register abbreviations and access rules are listed below:

R	**READ ONLY**. If a register is read only, writing to this register has no effect.
W	**WRITE ONLY**. If a register is write only, reading to this register returns all zero.
R/W	**READ/WRITE**. A register with this attribute can be read and written.
RC	**READ CLEAR**. If a register is read clear, reading to this register clears the register to '0'.
R/WC	**READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, writing 1 clears the corresponding bit and writing 0 has no effect.

BFNAME@REGNAME	This abbreviation may be shown in figures to represent one bit in a register or one field in a register.

The used radix indicator suffixes in this specification are listed below:
Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

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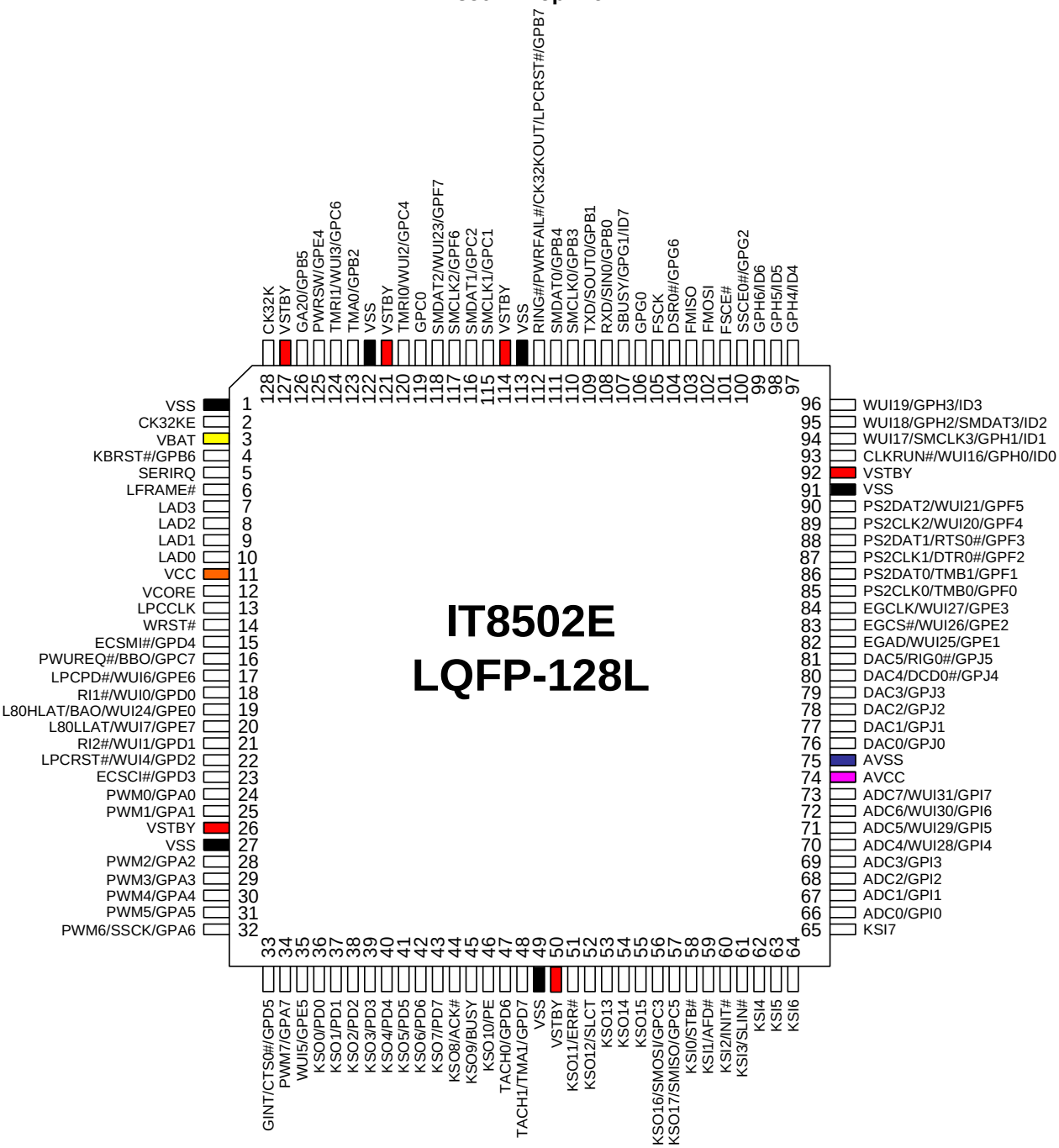
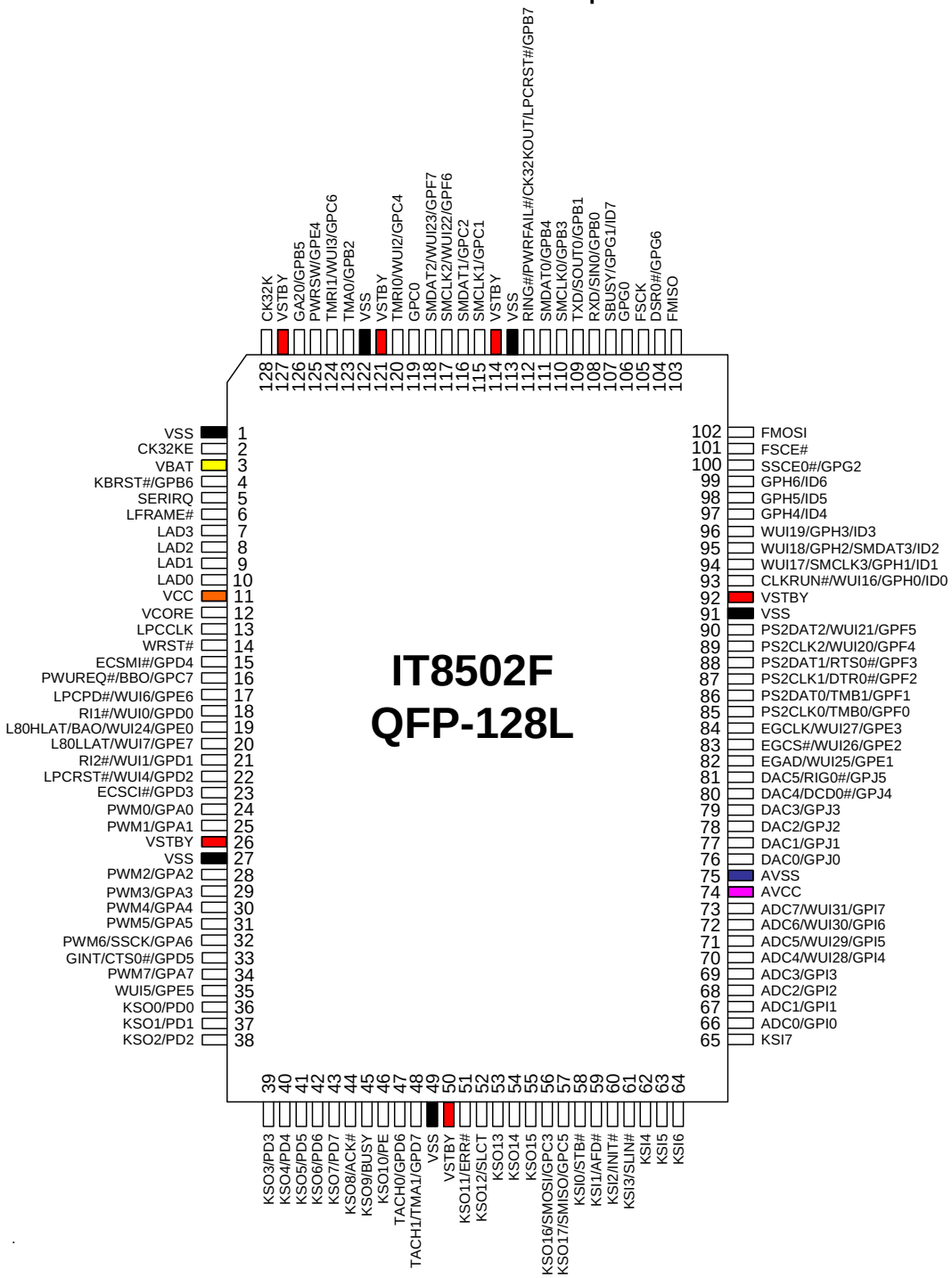
4. Pin Configuration

4.1 Top View

IT8502E Top View



IT8502F Top View



IT8502G Top View

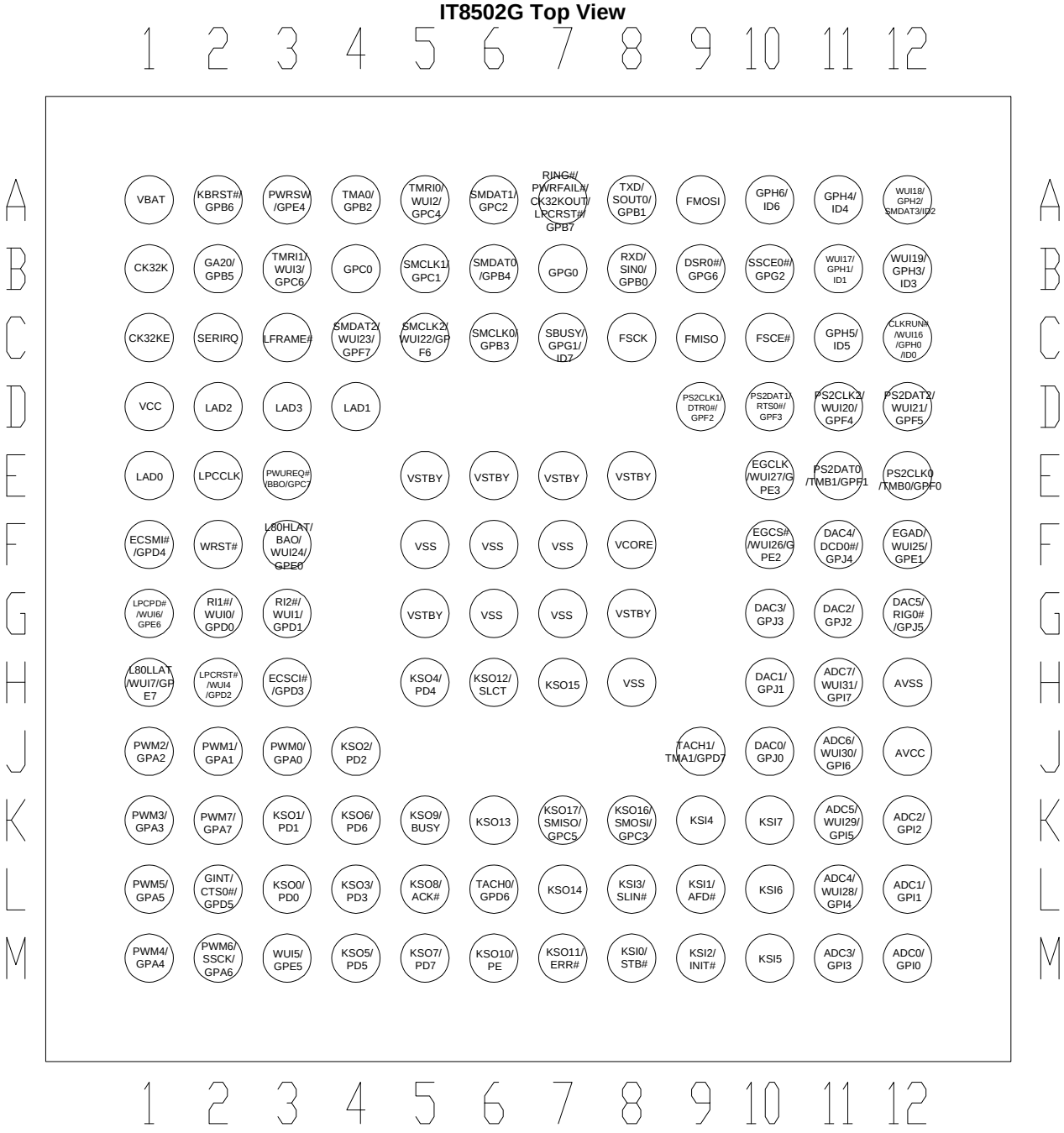


Table 4-1. Pins Listed in Numeric Order (128-pin LQFP)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VSS	33	GINT/CTS0#/GPD5	65	KSI7	97	GPH4/ID4
2	CK32KE	34	PWM7/GPA7	66	ADC0/GPI0	98	GPH5/ID5
3	VBAT	35	WUI5/GPE5	67	ADC1/GPI1	99	PH6/ID6
4	KBRST#/GPB6	36	KSO0/PD0	68	ADC2/GPI2	100	SSCE0#/GPG2
5	SERIRQ	37	KSO1/PD1	69	ADC3/GPI3	101	FSCE#
6	LFRAME#	38	KSO2/PD2	70	ADC4/WUI28/GPI4	102	FMOSI
7	LAD3	39	KSO3/PD3	71	ADC5/WUI29/GPI5	103	FMISO
8	LAD2	40	KSO4/PD4	72	ADC6/WUI30/GPI6	104	DSR0#/GPG6
9	LAD1	41	KSO5/PD5	73	ADC7/WUI31/GPI7	105	FSCK
10	LAD0	42	KSO6/PD6	74	AVCC	106	GPG0
11	VCC	43	KSO7/PD7	75	AVSS	107	SBUSY/GPG1/ID7
12	VCORE	44	KSO8/ACK#	76	DAC0/GPJ0	108	RXD/SIN0/GPB0
13	LPCCLK	45	KSO9/BUSY	77	DAC1/GPJ1	109	TXD/SOUT0/GPB1
14	WRST#	46	KSO10/PE	78	DAC2/GPJ2	110	SMCLK0/GPB3
15	ECSMI#/GPD4	47	TACH0/GPD6	79	DAC3/GPJ3	111	SMDAT0/GPB4
16	PWUREQ#/BBO/GPC7	48	TACH1/TMA1/GPD7	80	DAC4/DCD0#/GPJ4	112	RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7
17	LPCPD#/WUI6/GPE6	49	VSS	81	DAC5/RIG0#/GPJ5	113	VSS
18	RI1#/WUI0/GPD0	50	VSTBY	82	EGAD/WUI25/GPE1	114	VSTBY
19	L80HLAT/BAO/WUI24/GPE0	51	KSO11/ERR#	83	EGCS#/WUI26/GPE2	115	SMCLK1/GPC1
20	L80LLAT/WUI7/GPE7	52	KSO12/SLCT	84	EGCLK/WUI27/GPE3	116	SMDAT1/GPC2
21	RI2#/WUI1/GPD1	53	KSO13	85	PS2CLK0/TMB0/GPF0	117	SMCLK2/WUI22/GPF6
22	LPCRST#/WUI4/GPD2	54	KSO14	86	PS2DAT0/TMB1/GPF1	118	SMDAT2/WUI23/GPF7
23	ECSCI#/GPD3	55	KSO15	87	PS2CLK1/DTR0#/GPF2	119	GPC0
24	PWM0/GPA0	56	KSO16/SMOSI/GPC3	88	PS2DAT1/RTS0#/GPF3	120	TMRI0/WUI2/GPC4
25	PWM1/GPA1	57	KSO17/SMISO/GPC5	89	PS2CLK2/WUI20/GPF4	121	VSTBY
26	VSTBY	58	KSI0/STB#	90	PS2DAT2/WUI21/GPF5	122	VSS
27	VSS	59	KSI1/AFD#	91	VSS	123	TMA0/GPB2
28	PWM2/GPA2	60	KSI2/INIT#	92	VSTBY	124	TMRI1/WUI3/GPC6
29	PWM3/GPA3	61	KSI3/SLIN#	93	CLKRUN#/WUI16/GPH0/ID0	125	PWRSW/GPE4
30	PWM4/GPA4	62	KSI4	94	WUI17/SMCLK3/GPH1/ID1	126	GA20/GPB5
31	PWM5/GPA5	63	KSI5	95	WUI18/GPH2/SMDAT3/ID2	127	VSTBY(PLL)
32	PWM6/SSCK/GPA6	64	KSI6	96	WUI19/GPH3/ID3	128	CK32K

Table 4-2. Pins Listed in Numeric Order (128-pin TFBGA)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VBAT	C9	FMISO	G1	LPCPD#/WUI6/GPE6	K5	KSO9/BUSY
A2	KBRST#/GPB6	C10	FSCE#	G2	RI1#/WUI0/GPD0	K6	KSO13
A3	PWRSW/GPE4	C11	GPH5/ID5	G3	RI2#/WUI1/GPD1	K7	KSO17/SMISO/GPC5
A4	TMA0/GPB2	C12	CLKRUN#/WUI16/GPH0/ID0	G5	VSTBY	K8	KSO16/SMOSI/GPC3
A5	TMRI0/WUI2/GPC4	D1	VCC	G6	VSS	K9	KSI4
A6	SMDAT1/GPC2	D2	LAD2	G7	VSS	K10	KSI7
A7	RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	D3	LAD3	G8	VSTBY	K11	ADC5/WUI29/GPI5
A8	TXD/SOUT0/GPB1	D4	LAD1	G10	DAC3/GPJ3	K12	ADC2/GPI2
A9	FMOSI	D9	PS2CLK1/DTR0#/GPF2	G11	DAC2/GPJ2	L1	PWM5/GPA5
A10	GPH6/ID6	D10	PS2DAT1/RTS0#/GPF3	G12	DAC5/RIG0#/GPJ5	L2	GINT/CTS0#/GPD5
A11	GPH4/ID4	D11	PS2CLK2/WUI20/GPF4	H1	L80LLAT/WUI7/GPE7	L3	KSO0/PD0
A12	WUI18/GPH2/SMDAT3/ID2	D12	PS2DAT2/WUI21/GPF5	H2	LPCRST#/WUI4/GPD2	L4	KSO3/PD3
B1	CK32K	E1	LAD0	H3	ECSCI#/GPD3	L5	KSO8/ACK#
B2	GA20/GPB5	E2	LPCCLK	H5	KSO4/PD4	L6	TACH0/GPD6
B3	TMRI1/WUI3/GPC6	E3	PWUREQ#/BBO/GPC7	H6	KSO12/SLCT	L7	KSO14
B4	GPC0	E5	VSTBY	H7	KSO15	L8	KSI3/SLIN#
B5	SMCLK1/GPC1	E6	VSTBY	H8	VSS	L9	KSI1/AFD#
B6	SMDAT0/GPB4	E7	VSTBY	H10	DAC1/GPJ1	L10	KSI6
B7	GPG0	E8	VSTBY	H11	ADC7/WUI31/GPI7	L11	ADC4/WUI28/GPI4
B8	RXD/SIN0/GPB0	E10	EGCLK/WUI27/GPE3	H12	AVSS	L12	ADC1/GPI1
B9	DSR0#/GPG6	E11	PS2DAT0/TMB1/GPF1	J1	PWM2/GPA2	M1	PWM4/GPA4
B10	SSCE0#/GPG2	E12	PS2CLK0/TMB0/GPF0	J2	PWM1/GPA1	M2	PWM6/SSCK/GPA6
B11	WUI17/SMCLK3/GPH1/ID1	F1	ECSMI#/GPD4	J3	PWM0/GPA0	M3	WUI5/GPE5
B12	WUI19/GPH3/ID3	F2	WRST#	J4	KSO2/PD2	M4	KSO5/PD5
C1	CK32KE	F3	L80HLAT/BAO/WUI24/GPE0	J9	TACH1/TMA1/GPD7	M5	KSO7/PD7
C2	SERIRQ	F5	VSS	J10	DAC0/GPJ0	M6	KSO10/PE
C3	LFRAME#	F6	VSS	J11	ADC6/WUI30/GPI6	M7	KSO11/ERR#
C4	SMDAT2/WUI23/GPF7	F7	VSS	J12	AVCC	M8	KSI0/STB#
C5	SMCLK2/WUI22/GPF6	F8	VCORE	K1	PWM3/GPA3	M9	KSI2/INIT#
C6	SMCLK0/GPB3	F10	EGCS#/WUI26/GPE2	K2	PWM7/GPA7	M10	KSI5
C7	SBUSY/GPG1/ID7	F11	DAC4/DCD0#/GPJ4	K3	KSO1/PD1	M11	ADC3/GPI3
C8	FSCK	F12	EGAD/WUI25/GPE1	K4	KSO6/PD6	M12	ADC0/GPI0

Table 4-3. Pins Listed in Alphabetical Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ACK#	44,L5	GPB7	112,A7	GPJ4	80,F11	PD7	43,M5	VSS	1,VSS
ADC0	66,M12	GPC0	119,B4	GPJ5	81,G12	PE	46,M6	VSS	113,VSS
ADC1	67,L12	GPC1	115,B5	ID0	93,C12	PS2CLK0	85,E12	VSS	122,VSS
ADC2	68,K12	GPC2	116,A6	ID1	94,B11	PS2CLK1	87,D9	VSS	27,VSS
ADC3	69,M11	GPC3	56,K8	ID2	95,A12	PS2CLK2	89,D11	VSS	49,VSS
ADC4	70,L11	GPC4	120,A5	ID3	96,B12	PS2DAT0	86,E11	VSS	91,VSS
ADC5	71,K11	GPC5	57,K7	ID4	97,A11	PS2DAT1	88,D10	VSTBY	114,VSTBY
ADC6	72,J11	GPC6	124,B3	ID5	98,C11	PS2DAT2	90,D12	VSTBY	121,VSTBY
ADC7	73,H11	GPC7	16,E3	ID6	99,A10	PWM0	24,J3	VSTBY	127,E5
AFD#	59,L9	GPD0	18,G2	ID7	107,C7	PWM1	25,J2	VSTBY	26,VSTBY
AVCC	74,J12	GPD1	21,G3	INIT#	60,M9	PWM2	28,J1	VSTBY	50,G5
AVSS	75,H12	GPD2	22,H2	KBRST#	4,A2	PWM3	29,K1	VSTBY	92,VSTBY
BAO	19,F3	GPD3	23,H3	KSI0	58,M8	PWM4	30,M1	WRST#	14,F2
BBO	16,E3	GPD4	15,F1	KSI1	59,L9	PWM5	31,L1	WUI0	18,G2
BUSY	45,K5	GPD5	33,L2	KSI2	60,M9	PWM6	32,M2	WUI1	21,G3
CK32K	128,B1	GPD6	47,L6	KSI3	61,L8	PWM7	34,K2	WUI16	93,C12
CK32KE	2,C1	GPD7	48,J9	KSI4	62,K9	PWRFAIL#	112,A7	WUI17	94,B11
CK32KOUT	112,A7	GPE0	19,F3	KSI5	63,M10	PWRSW	125,A3	WUI18	95,A12
CLKRUN#	93,C12	GPE1	82,F12	KSI6	64,L10	PWUREQ#	16,E3	WUI19	96,B12
CTS0#	33,L2	GPE2	83,F10	KSI7	65,K10	RI1#	18,G2	WUI2	120,A5
DAC0	76,J10	GPE3	84,E10	KSO0	36,L3	RI2#	21,G3	WUI20	89,D11
DAC1	77,H10	GPE4	125,A3	KSO1	37,K3	RIG0#	81,G12	WUI21	90,D12
DAC2	78,G11	GPE5	35,M3	KSO10	46,M6	RING#	112,A7	WUI22	117,C5
DAC3	79,G10	GPE6	17,G1	KSO11	51,M7	RTS0#	88,D10	WUI23	118,C4
DAC4	80,F11	GPE7	20,H1	KSO12	52,H6	RXD	108,B8	WUI24	19,F3
DAC5	81,G12	GPF0	85,E12	KSO13	53,K6	SBUSY	107,C7	WUI25	82,F12
DCD0#	80,F11	GPF1	86,E11	KSO14	54,L7	SERIRQ	5,C2	WUI26	83,F10
DSR0#	104,B9	GPF2	87,D9	KSO15	55,H7	SIN0	108,B8	WUI27	84,E10
DTR0#	87,D9	GPF3	88,D10	KSO16	56,K8	SLCT	52,H6	WUI28	70,L11
ECSCI#	23,H3	GPF4	89,D11	KSO17	57,K7	SLIN#	61,L8	WUI29	71,K11
ECSMI#	15,F1	GPF5	90,D12	KSO2	38,J4	SMCLK0	110,C6	WUI3	124,B3
EGAD	82,F12	GPF6	117,C5	KSO3	39,L4	SMCLK1	115,B5	WUI30	72,J11
EGCLK	84,E10	GPF7	118,C4	KSO4	40,H5	SMCLK2	117,C5	WUI31	73,H11
EGCS#	83,F10	GPG0	106,B7	KSO5	41,M4	SMCLK3	94,B11	WUI4	22,H2
ERR#	51,M7	GPG1	107,C7	KSO6	42,K4	SMDAT0	111,B6	WUI5	35,M3
FMISO	103,C9	GPG2	100,B10	KSO7	43,M5	SMDAT1	116,A6	WUI6	17,G1
FMOSI	102,A9	GPG6	104,B9	KSO8	44,L5	SMDAT2	118,C4	WUI7	20,H1
FSCE#	101,C10	GPH0	93,C12	KSO9	45,K5	SMDAT3	95,A12		
FSCK	105,C8	GPH1	94,B11	L80HLAT	19,F3	SMISO	57,K7		
GA20	126,B2	GPH2	95,A12	L80LLAT	20,H1	SMOSI	56,K8		
GINT	33,L2	GPH3	96,B12	LAD0	10,E1	SOUT0	109,A8		
GPA0	24,J3	GPH4	97,A11	LAD1	9,D4	SSCE0#	100,B10		
GPA1	25,J2	GPH5	98,C11	LAD2	8,D2	SSCK	32,M2		
GPA2	28,J1	GPH6	99,A10	LAD3	7,D3	STB#	58,M8		
GPA3	29,K1	GPI0	66,M12	LFRAME#	6,C3	TACH0	47,L6		
GPA4	30,M1	GPI1	67,L12	LPCCLK	13,E2	TACH1	48,J9		
GPA5	31,L1	GPI2	68,K12	LPCPD#	17,G1	TMA0	123,A4		
GPA6	32,M2	GPI3	69,M11	LPCRST#	112,A7	TMA1	48,J9		
GPA7	34,K2	GPI4	70,L11	LPCRST#	22,H2	TMB0	85,E12		
GPB0	108,B8	GPI5	71,K11	PD0	36,L3	TMB1	86,E11		
GPB1	109,A8	GPI6	72,J11	PD1	37,K3	TMRI0	120,A5		
GPB2	123,A4	GPI7	73,H11	PD2	38,J4	TMRI1	124,B3		
GPB3	110,C6	GPJ0	76,J10	PD3	39,L4	TXD	109,A8		
GPB4	111,B6	GPJ1	77,H10	PD4	40,H5	VBAT	3,A1		
GPB5	126,B2	GPJ2	78,G11	PD5	41,M4	VCC	11,D1		

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GPB6	4,A2	GPJ3	79,G10	PD6	42,K4	VCORE	12,F8		

5. Pin Descriptions

5.1 Pin Descriptions

Table 5-1. Pin Descriptions of LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V CMOS I/F, 5V tolerant)			
22	**LPCRST#**	IK	***LPC Hardware Reset*** LPC hardware reset will reset LPC interface and host side modules. The source is determined by EC side register bit LPCRSTEN. This pin can be omitted if external LPC reset is not required.
13	**LPCCLK**	PI	***LPC Clock*** 33 MHz clock for LPC domain functions.
7-10	**LAD[3:0]**	PIO	***LPC Address Data***
6	**LFRAME#**	PI	***LPC LFRAME# Signal***
17	**LPCPD#**	IO2	***LPC LPCPD# Signal***
93	**CLKRUN#**	IO8	***LPC CLKRUN# Signal***
5	**SERIRQ**	PIO	***SERIRQ Signal***
15	**ECSMI#**	O8	***EC SMI# Signal*** This is SMI# signal driven by SWUC module.
23	**ECSCI#**	O8	***EC SCI# Signal*** This is SCI# signal driven by PMC module.
126	**GA20**	IO2	***Gate A20 Signal*** This is GA20 signal driven by SWUC module.
4	**KBRST#**	IO2	***KB Reset Signal*** This is KBRST# signal driven by SWUC module.
14	**WRST#**	IK	***Warm Reset*** For EC domain function, reset after power up. WRST# is not 5V tolerant.
16	**PWUREQ#**	O2	***System Power On Request*** This is PWUREQ# signal driven by SWUC module.
19	**L80HLAT**	O4	***LPC I/O Port 80, High-nibble LAD Latch*** An active high signal to latch Port 80 high-nibble for the debug purpose.
20	**L80LLAT**	O4	***LPC I/O Port 80, Low-nibble LAD Latch*** An active high signal to latch Port 80 low-nibble for the debug purpose.

Table 5-2. Pin Descriptions of External Serial Flash Interface (FSPI)

Pin(s) No.	Signal	Attribute	Description
External Serial Flash Interface (3.3V CMOS I/F, 5V tolerant)			
105	**FSCK**	O4	***Serial Flash Clock*** Clock (frequency = FreqPLL) to external serial flash. (FreqPLL is listed in Table 10-2 on page 352)
101	**FSCE#**	O4	***Serial Flash Chip Enable*** Connected to FSCE# of serial flash.
102	**FMOSI**	O4	***Serial Flash In*** Connected to FMOSI of serial flash.
103	**FMISO**	IK	***Serial Flash Out*** Connected to FMISO of serial flash. Please do not place any pull-up resistor on these four pins to reduce power consumption.

Table 5-3. Pin Descriptions of Serial Peripheral Interface (SSPI)

Pin(s) No.	Signal	Attribute	Description
External Serial Flash Interface (3.3V CMOS I/F, 5V tolerant)			
32	**SSCK**	O8	***SSPI Clock*** Clock to external device.
100	**SSCE0#**	O4	***SSPI Chip Enable*** Connected to SSCE# of serial flash.
57	**SMISO**	IOK8	***SSPI Master In/Slave Out*** Connected to SO of 4-wire SPI device, or connected to SIO of 3-wire SPI device.
56	**SMOSI**	O8	***SSPI Master Out/Slave In*** Connected to SI of 4-wire SPI device.
107	**SBUSY**	IOK8	***SSPI Busy In*** Connected to BUSY of SPI device

Table 5-4. Pin Descriptions of Keyboard Matrix Scan Interface

Pin(s) No.	Signal	Attribute	Description
KB Matrix Interface (3.3V CMOS I/F)			
57-51, 46-36	**KSO[17:0]**	O8	***Keyboard Scan Output*** Keyboard matrix scan output. KSO17 and KSO16 are function 1 of GPIO pins and are 5V tolerant.
65-58	**KSI[7:0]**	IK	***Keyboard*** Scan Input Keyboard matrix scan input for switch based keyboard.

Table 5-5. Pin Descriptions of SMBus Interface

Pin(s) No.	Signal	Attribute	Description
SMBus Interface (3.3V CMOS I/F, 5V tolerant)			
94, 117, 115, 110	**SMCLK[3:0]**	IOK4	***SMBus CLK*** 3 SMBus interface provided.
95, 118, 116, 111	**SMDAT[3:0]**	IOK4	***SMBus Data*** 3 SMBus interface provided.

Table 5-6. Pin Descriptions of PS/2 Interface

Pin(s) No.	Signal	Attribute	Description
PS/2 Interface (3.3V CMOS I/F, 5V tolerant)			
89, 87, 85	**PS2CLK[2:0]**	IOK8	***PS/2 CLK*** 3 sets of PS/2 interface, alternate function of GPIO. PS2CLK0-2 correspond to channel 1-3 respectively.
90, 88, 86	**PS2DAT[2:0]**	IOK8	***PS/2 Data*** 3 sets of PS/2 interface, alternate function of GPIO. PS2DAT0-2 correspond to channel 1-3 respectively.

Table 5-7. Pin Descriptions of PWM Interface

Signal	Pin(s) No.	Attribute	Description
PWM Interface (3.3V CMOS I/F, 5V tolerant)			
34, 32-28, 25-24	**PWM[7:0]**	O8	***Pulse Width Modulation Output*** These are general-purpose PWM signals. PWM0-7 correspond to channel 0-7 respectively.
48-47	**TACH[1:0]**	IK	***Tachometer Input*** TACH[1:0] are tachometer inputs from external fans. They are used for measuring the external fan speed.
124, 120	**TMRI[1:0]**	IK	***Counter Input*** TMRI[1:0] are timer/counter input signals connected to timer2 and timer1 of 8032. Notice that the frequency has to be less than 8032 clock to be sampled.

Table 5-8. Pin Descriptions of Wake Up Control Interface

Pin(s) No.	Signal	Attribute	Description
Wake Up Control Interface (3.3V CMOS I/F, 5V tolerant)			
Refer to Pins List Table	**WUI[31:0]**	IK	***EC Wake Up Input*** Supplied by VSTBY, used for EC wake up.
125	**PWRSW**	IK	***Power Switch Input*** Supplied by VSTBY, used to indicate the status of power switch.
21,18	**RI[2:1]#**	IK	***Ring Indicator Input*** Supplied by VSTBY, used for system wake up.
112	**RING#**	IK	***Telephone Line Ring Input*** Supplied by VSTBY, used for system wake up.

Table 5-9. Pin Descriptions of Serial Port Interface

Pin(s) No.	Signal	Attribute	Description
Serial Port Interface (3.3V CMOS I/F, 5V tolerant)			
108	**SIN0**	IOK2	***Serial Data Input*** This input receives serial data from the communications link.
109	**SOUT0**	IOK2	***Serial Data Output*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
104	**DSR0#**	IK	***Data Set Ready*** When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
88	**RTS0#**	O8	***Request to Send*** When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state.
87	**DTR0#**	O8	***Data Terminal Ready*** DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state.
33	**CTS0#**	IK	***Clear to Send*** When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
81	**RIG0#**	IK	***Ring Indicator*** When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
80	**DCD0#**	IK	***Data Carrier Detect*** When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.

Table 5-10. Pin Descriptions of UART Interface

Pin(s) No.	Signal	Attribute	Description
UART Interface (3.3V CMOS I/F, 5V tolerant)			
109	**TXD**	O	***UART TX Output*** UART TX Output from 8032
108	**RXD**	IK	***UART RX Input*** UART RX Input from 8032

Table 5-11. Pin Descriptions of External GPIO Bus (EGPC) Interface

Pin(s) No.	Signal	Attribute	Description
External GPIO Bus (EGPC) Interface (3.3V CMOS I/F, 5V tolerant)			
82	**EGAD**	IO8	***Address/Data*** The signal is used for the address or data of ITE specify Bus. Connected to IT8301 GPIO_DATA pin.
83	**EGCS#**	O8	***Address Chip Select*** The signal is used to identify the chip-select signal. Connected to IT8301 CYCLE_START pin.
84	**EGCLK**	O8	***Clock*** The clock frequency is EC clock frequency (listed in Table 10-2 on page 352). The signal only is running when the cycle is active. Connected to IT8301 GPIO_CLK pin.

Table 5-12. Pin Descriptions of Hardware Bypass (HWBP)

Pin(s) No.	Signal	Attribute	Description
External GPIO Bus (EGPC) Interface (3.3V CMOS I/F, 5V tolerant)			
19	**BAO**	O4	***Buffer A Output*** Hardware bypass path from GPI6 to BAO.
16	**BBO**	O4	***Buffer B Output*** Hardware bypass path from GPI7 to BBO.

Table 5-13. Pin Descriptions of Parallel Port Interface

Pin(s) No.	Signal	Attribute	Description
Parallel Port Interface (3.3V CMOS I/F)			
52	**SLCT**	O8	***Printer Select***
46	**PE**	O8	***Printer Paper End***
45	**BUSY**	O8	***Printer Busy***
44	**ACK#**	O8	***Printer Acknowledge***
61	**SLIN#**	IK	***Printer Select Input***
60	**INIT#**	IK	***Printer Initialize***
51	**ERR#**	O8	***Printer Error***
59	**AFD#**	IK	***Printer Auto Line Feed***
58	**STB#**	IK	***Printer Strobe***
43-36	**PD[7:0]**	O8	***Parallel Port Data[7:0]***

*: The interface can be connected to parallel port of computer through ITE-specified cable. The programmer can directly read/write flash through this interface.

Table 5-14. Pin Descriptions of GPIO Interface

Pin(s) No.	Signal	Attribute	Description
GPIO Interface (3.3V CMOS I/F, 5V tolerant)			
Refer to Pins List Table	**GPA[7:0], GPB[7:0], GPC[7:0], GPD[7:0], GPE[7:0], GPF[7:0], GPG[6,2:0], GPH[6:0], GPI[7:0], GPJ[5:0]**	IOK	***GPIO Signals*** The GPIO pins are divided into groups. Some GPIO pins have alternative function. Note that group I and J are not 5V tolerant. **PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, G2 AND GPG6 (Reserved hardware strapping)**.
33	**GINT**	IK	***General Purpose Interrupt*** General Purpose Interrupt directly input to INT28 of INTC.

Table 5-15. Pin Descriptions of Hardware Strap

Pin(s) No.	Signal	Attribute	Description
Hardware Strap (3.3V CMOS I/F, 5V tolerant)			
107, 99-93	**ID[7:0]**	IK	***Identify Input*** These hardware straps are used to identify the version for firmware usage. These input signals will be latched when the VSTBY power up. Note that these hardware straps are only available if these pins are not driven by other components on PCB.

Table 5-16. Pin Descriptions of ADC Input Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface (3.3V CMOS I/F)			
73-66	**ADC[7:0]**	AI	***ADC Input/Alternate GPIO*** These 8 ADC inputs can be used as GPIO ports (input mode only) depending on the ADC channels required.

Table 5-17. Pin Descriptions of DAC Output Interface

Pin(s) No.	Signal	Attribute	Description
DAC Interface (3.3V CMOS I/F)			
81-76	**DAC[5:0]**	AO	***DAC Output***

Table 5-18. Pin Descriptions of Clock

Pin(s) No.	Signal	Attribute	Description
Clock Interface (3.3V CMOS I/F)			
128	**CK32K**	OSCI	***32.768 kHz Crystal X1*** It is connected to internal crystal oscillator.
2	**CK32KE**	OSCIO	***32.768 kHz Crystal X2*** It is connected to internal crystal oscillator.
112	**CK32KOUT**	O4	***32.768 kHz Oscillator Output*** 32.768 kHz clock output.

Table 5-19. Pin Descriptions of Power/Ground Signals

Pin(s) No.	Signal	Attribute	Description
Power Ground Signals			
1, 27, 49, 91,113, 122	**VSS**	I	***Ground*** Digital ground.
11	**VCC**	I	***System Power Supply of 3.3V*** The power supply of LPC and related functions, which is main power of system.
26, 50, 92, 114, 121, 127	**VSTBY**	I	***Standby Power Supply of 3.3V*** The power supply of EC domain functions, which is standby power of system. Note that the power of PLL is sourced by pin 127 only.
12	**VCORE**	I/O	***Core Power Bypass*** Internal core power output. External capacitor is required to be connected between this pin and VSS and physically close to this pin. The capacitor type must be low-ESR and MLCC is required.
3	**VBAT**	I	***Battery Power Supply of 3.3V*** The power supply for BRAM and 32.768 kHz oscillator. Internal VBS power is supplied by VSTBY when it is valid and is supplied by VBAT when VSTBY is not supplied. If VBAT is not used, tie this pin to ground.
75	**AVSS**	I	***Analog Ground for Analog Component***
74	**AVCC**	I	***Analog VCC for Analog Component***

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
IKD: Schmitt Trigger Input PAD (integrated one pull-down resistor).
PIU: PCI Bus Specified Input PAD (integrated one pull-up resistor).
OSCI: Oscillator Input PAD.
AO: Analog Output PAD.
O2: 2 mA Output PAD.
O4: 4 mA Output PAD.
O6: 6 mA Output PAD.
O8: 8 mA Output PAD.
PIO: PCI Bus Specified Bidirectional PAD.
OSCIO: Oscillator Bidirectional PAD.
AIO2: 2 mA Bidirectional PAD with Analog Input PAD.
IOK2: 2 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK4: 4 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK6: 6 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK8: 8 mA Bidirectional PAD with Schmitt Trigger Input PAD.

5.2 Chip Power Planes and Power States

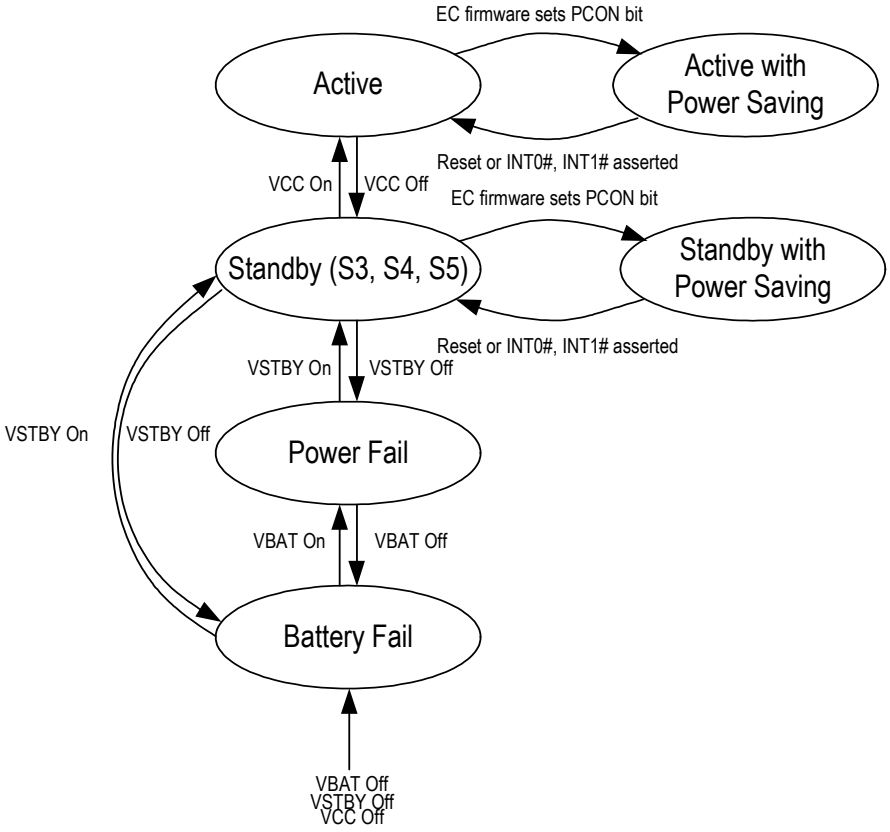
Table 5-20. Power States

Power State	VCC pin	VSTBY/AVCC pin	VBAT pin	Internal VBS
Active	Supplied	Supplied	Supplied or Not	Switched from VSTBY
Active with Power Saving	Supplied	Supplied EC is in Idle, Doze or Sleep Mode	Supplied or Not	Switched from VSTBY
Standby	Not Supplied	Supplied	Supplied or Not	Switched from VSTBY
Standby with Power Saving	Not Supplied	Supplied EC is in Idle, Doze or Sleep Mode	Supplied or Not	Switched from VSTBY
Power Fail	Not Supplied	Not Supplied	Supplied	Switched from VBS
Battery Fail	Not Supplied	Not Supplied	Not Supplied	Not Supplied

Note:

(1) The AVCC should be derived from VSTBY.
(2) All other combinations of VCC / VSTBY / VBAT are invalid.
(3) In Power Saving mode, 8032 program counter is stopped and no instruction will be executed no matter whether EC Clock is running or not.
(4) VBS is the battery-backed power. When VSTBY is valid, VBS is supplied by VSTBY. When VSTBY is not valid, VBS is supplied by VBAT.

Figure 5-1. Power State Transitions



5.3 Pin Power Planes and States

In the following tables of this section, Standby means that the VCC is not valid but VSTBY is supplied (S3, S4 or S5) and EC is in normal operation. Standby with Sleep means that 8032 and most of its functions are out of work due to PLL power-down while VSTBY is still supplied. Power Fail means only battery-backed power is supplied.

The abbreviations used in the following tables are described below:
H means EC drives high or driven high.
L means EC drives low or driven to low or output pin power off.
Z means EC tri-stated the I/O pin or output pin with enable.
RUN means that Output or I/O pins are in normal operation.
Driven means that the input pin is driven by connected chip or logic.
STOP means that the output pin keeps its logical level before the clock is stopped.
OFF means I/O pin power off.

Note that reset sources of 'Reset Finish' columns depend on Reset Types and Applied Module Table and it means the reset is finished when its corresponding power plane is supplied.
Note that GPIO pins listed in different functional tables except GPIO table indicate their pin status of the corresponding alternative function.

Table 5-21. Pin States of LPC Bus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
LPCRST# (Y)	VSTBY	Driven	L	L	L
LPCCLK	VCC	Driven	L	L	L
LAD[3:0]	VCC	RUN	OFF	OFF	OFF
LFRAME#	VCC	Driven	L	L	L
SERIRQ	VCC	Z	OFF	OFF	OFF
LPCPD# (Y)	VSTBY	Table 7-14	L	L	L
CLKRUN# (Y)	VSTBY	Table 7-14	OFF	L	OFF
ECSMI#	VSTBY	Table 7-14	RUN	Z	OFF
ECSCI# (Y)	VSTBY	Table 7-14	RUN	Z	OFF
GA20 (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
KBRST# (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
WRST#	VSTBY	Driven	Driven	Driven	L
PWUREQ#	VSTBY	Table 7-14	RUN	STOP	OFF
L80HLAT (Y)	VSTBY	Table 7-14	L	L	OFF
L80LLAT (Y)	VSTBY	Table 7-14	L	L	OFF

Table 5-22. Pin States of Keyboard Matrix Scan Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
KSO[17:0]	VSTBY	L	RUN	STOP	OFF
KSI[7:0]	VSTBY	Driven	Driven	Driven	L

Table 5-23. Pin States of SMBus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SMCLK0 (Y) SMCLK1 (Y) SMCLK2 (Y)	VSTBY	Table 7-14	RUN	Z	OFF
SMDAT0 (Y) SMDAT1 (Y) SMDAT2 (Y)	VSTBY	Table 7-14	RUN	Z	OFF

Table 5-24. Pin States of PS/2 Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PS2CLK0 (Y) PS2CLK1 (Y) PS2CLK2 (Y)	VSTBY	Table 7-14	RUN	Z	OFF
PS2DAT0 (Y) PS2DAT1 (Y) PS2DAT2 (Y)	VSTBY	Table 7-14	RUN	Z	OFF

Table 5-25. Pin States of PWM Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PWM0 (Y) PWM1 (Y) PWM2 (Y) PWM3 (Y) PWM4 (Y) PWM5 (Y) PWM6 (Y) PWM7 (Y)	VSTBY	Table 7-14	RUN	STOP	OFF

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
TACH0 (Y) TACH1 (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
TMRI0 (Y) TMRI1 (Y)	VSTBY	Table 7-14	Driven	Driven	OFF

Table 5-26. Pin States of Wake Up Control Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
WUI23-16 (Y) WUI7-0 (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
PWRSW (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
RI1# (Y) RI2# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
RING# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
PWRFAIL# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF

Table 5-27. Pin States of UART Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
RXD (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
TXD (Y)	VSTBY	Table 7-14	RUN	STOP	OFF

Table 5-28. Pin States of EGPC Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
EGAD (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
EGCS# (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
EGCLK (Y)	VSTBY	Table 7-14	RUN	STOP	OFF

Table 5-29. Pin States of SSPI Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SSCE0# (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
SSCK (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
SMOSI (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
SMISO (Y)	VSTBY	Table 7-14	Driven	Driven	OFF

Table 5-30. Pin States of Serial Port Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SIN0 (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
SOUT0 (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
CTS0# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
DSR0# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
DCD0# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
RIG0# (Y)	VSTBY	Table 7-14	Driven	Driven	OFF
DTR0# (Y)	VSTBY	Table 7-14	RUN	STOP	OFF
RTS0# (Y)	VSTBY	Table 7-14	RUN	STOP	OFF

Table 5-31. Pin States of GPIO Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
GPA0-GPL7	VSTBY	Table 7-14	Depends on its mode	STOP	OFF

Table 5-32. Pin States of ADC Input Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
ADC[7:0] (Y)	AVCC	Driven	Driven	Driven	L

Table 5-33. Pin States of DAC Output Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
DAC[5:0]	AVCC	Table 7-14	RUN	RUN	OFF

Table 5-34. Pin States of Clock

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
CK32K	VBS	Driven	RUN	RUN	RUN
CK32KE	VBS	Driven	RUN	RUN	RUN

5.4 PWRFAIL# Interrupt to INTC

The firmware may use the PWRFAIL# to do some necessary response if VSTBY is being lost. Corresponded INT0# has higher priority than INT1#.

5.5 Reset Sources and Types

Table 5-35. Reset Sources

Reset Sources	Description
VBS Power-Up Reset	Activated after VBS is power up
VSTBY Power-Up Reset	Activated after VSTBY is power up and PLL is stable It takes t_{PLLS} for PLL stabling, and the external flash has to be ready before VSTBY Power-Up Reset finish
VCC Power-Up Reset	Activated after VCC is power up
Warm Reset	Activated if WRST# is asserted
LPC Hardware Reset	Activated if LPCRST# is asserted
Super I/O Software Reset	Activated if SIOSWRST of PNPCFG is writing 1
Watch Dog Reset	Activated if 8032 WDT or External WDT time-out

Table 5-36. Reset Types and Applied Module

Reset Types	Sources	Applied Module
VBS Region Reset	VBS Power-Up Reset	BRAM, SWUC
Host Domain Hardware Reset	Warm Reset, VCC Power-Up Reset or LPC Hardware Reset LPC Hardware Reset may be unused See also HRSTS in RSTS register.	LPC, PNPCFG, Logical Devices and EC2I
Host Domain Software Reset	Super I/O Software Reset	PNPCFG, Logical Devices and EC2I
EC Domain Reset	Warm Reset, VSTBY Power-Up Reset or Watch Dog Reset	EC Domain

The WRST# should be driven low for at least t_{WRSTW} before going high (Refer to Table 10-3. Warm Reset AC Table on page 352)

.

If the firmware wants to assert an EC Domain Reset, start an internal of external watchdog without clearing its counter or write invalid data to EWDKEYR register (refer to EWDKEYEN and EWDKEYR registers).
If the firmware wants to determine the source of the last EC Domain Reset, use LRS field in RSTS register.

5.5.1 Related Interrupts to INTC

- Interrupt to INTC

LPCRST# may come from pin LPCRST#/WUI4/GPD2 or RING#/PWRFAIL#/LPCRST#/GPB7. Both pins have another interrupt related alternative function. LPCRST# can be treated as an orthogonal input and LPCRST# event can be handled in the same interrupt routine of another alternative function.

5.6 Chip Power Mode and Clock Domain

Table 5-37. Clock Types

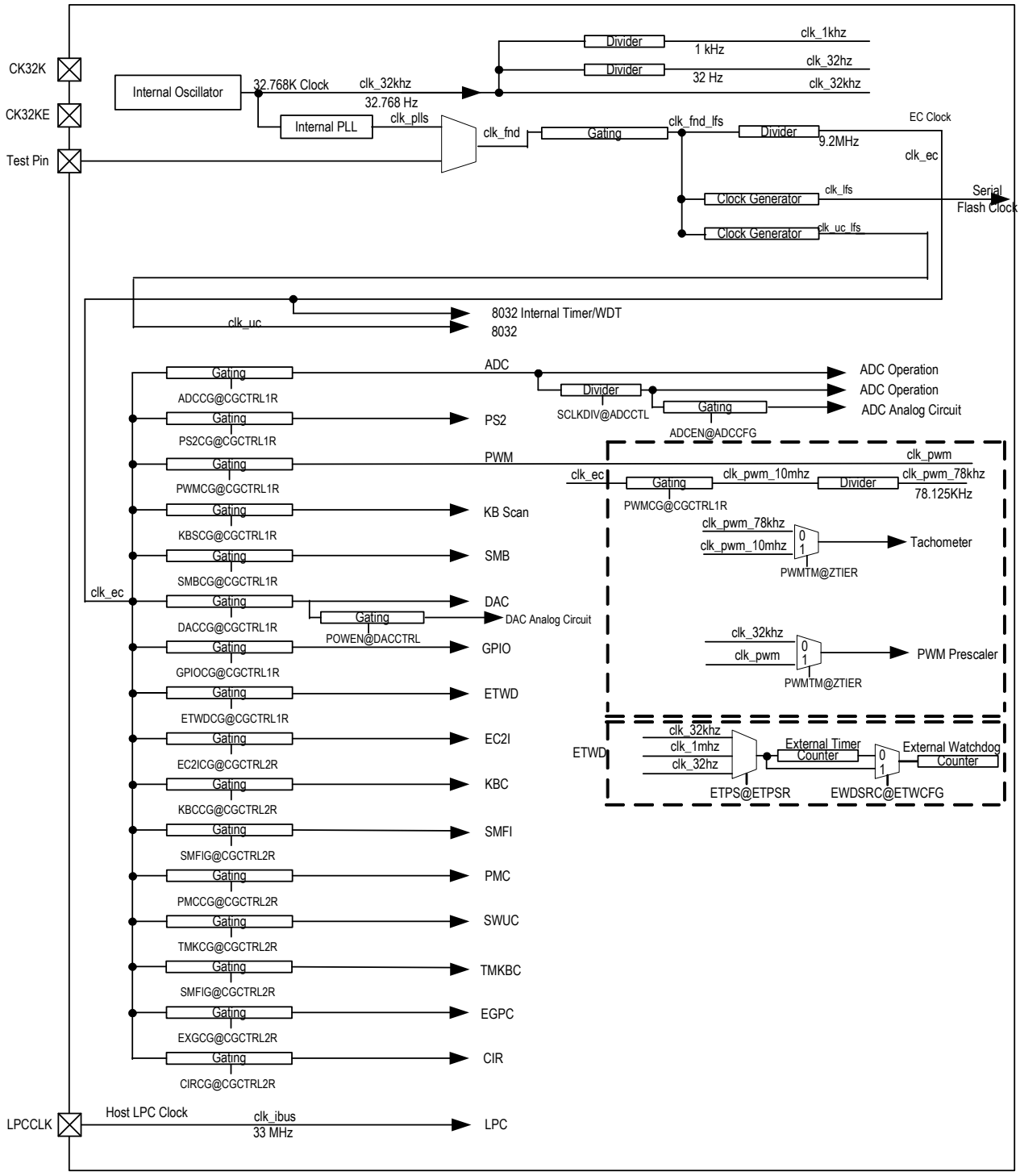
Types	Description
32.768 k Clock	32.768 kHz generated by internal oscillator
PLL Clock	Clock (frequency = FreqPLL) generated by internal PLL which feds 32.768 k PLL Clock is also the base clock of flash interface. (FreqPLL is listed in Table 10-2 on page 352
EC Clock	It's from internal PLL and its frequency is listed in Table 10-2 on page 352
8032 Clock	The clock of internal timer/WDT is from EC Clock. Core clock: The frequency is variable. Upper-bound: (FreqPLL / 2) while fetching from internal SRAM Lower-bound: Refer to section 6.3.3.9 Serial Flash Performance Consideration on page 73. (FreqPLL is listed in Table 10-2 on page 352)
Host LPC Clock	33 MHz or slower from LPCCLK pin and applied on Host Domain. See also SLWPCI bit in MBCTRL register in the host side and SHBR bit in HCTRL2R register in EC side.

The 8032 can enter Idle/Doze/Sleep mode to reduce some power consumption. After entering the Idle mode, timers and the Watch Dog timer of 8032 still work. After entering Doze/Sleep mode, clock of 8032 is stopped and internal timers are stopped but the external timer still works. After entering Doze mode, EC domain clock is stopped and all internal timers are stopped. Also see Table 5-39 on page 35 for the details.
The way to wake up 8032 from the Idle mode is to enable internal or external interrupts, or hardware reset. The way to wake up 8032 from Doze/Sleep mode is to enable external interrupts or hardware reset. Firmware may set PLLCTRL bit before setting PD bit to enter the Sleep mode, since stopping PLL can reduce more power consumption, but it takes more time to wake up from Sleep mode due to waiting for PLL being stable. The steps to enter and exit Idle/Doze/Sleep are listed below:

(a) Set related bits of IE register if they are cleared.
(b) Set channels of WUC which wants to wake up 8032 and disable unwanted channels.
(c) Set channels of INTC which wants to wake up 8032 and disable unwanted channels.
(d) Set PLLCTRL bit for Sleep mode, or clear it for Doze mode.
(e) Set IDL bit in PCON to enter the Idle mode, or set PD bit in PCON to enter the Doze/Sleep mode.
(f) 8032 waits for an interrupt to wake up.
(g) After an interrupt is asserted, 8032 executes the corresponding interrupt routine and return the next instruction after setting PCON.

The following figure describes the drivers and branches of the three clocks.
In this figure, clk_32kHz represents 32.768 k Clock; clk_src and its branches represent EC Clock; clk_ibus represents LPC Clock.

Figure 5-2. Clock Tree



FreqPLL/FreqEC are listed in Table 10-2 on page 352.

Table 5-38. Power Saving by EC Clock Operation Mode

Mode	Item	Description
Normal	Enter	VSTBY is supplied and hardware reset done
	Exit	Enter other modes
	32.768 k Clock	On
	PLL	On
	EC Domain Clock	Driven by PLL
	8032 Clock	The same as EC Domain Clock
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Idle	Enter	Set IDL bit in PCON of 8032
	Exit	Interrupt from INTC, interrupt from 8032 timer, watchdog reset or hardware reset
	32.768 k Clock	On
	PLL	On
	EC Domain Clock	Driven by PLL
	8032 Clock	Core: Off Internal timer/WDT: On
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Doze	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	On, clearing PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Sleep	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	32.768 k Clock	On
	PLL	D2EC disabled: Off, setting PLLCTRL of ECPM module is required D2EC enabled: On
	EC Domain Clock	Driven by PLL
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Note:
The PD bit in PCON register may trigger the Doze or Sleep mode of EC Domain.

Table 5-39. Module Status in Each Power State/Clock Operation

Power State and/or Clock Operation	Running Module	Stopped Module	Off Module	Note
Active *Active with Power Saving*	LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC/ BRAM			List host related modules only
Standby *Standby with Power Saving*			LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC/ BRAM	List host related modules only
Active with Idle Mode *Standby with Idle Mode*	All other EC modules 8032 internal timer/WDT	8032 core logic except its internal timer/WDT		List EC modules only
Active with Doze Mode *Standby with Doze Mode*	All other EC modules	8032		List EC modules only
Active with Sleep Mode *Standby with Sleep Mode*	GPIO, WUC and its sources, INTC and its sources from running modules, SWUC wakeup logic, PWM channel outputs, KBS, ETWD, BRAM	All other EC modules		List all
Power Fail	BRAM		All others	List all
Battery Fail			All	List all

Note: Running module means this module works well.
Stopped module means this module is frozen because its clock is stopped.
Off module means this module is turned off due to power lost.

5.7 Pins with Pull, Schmitt-Trigger or Open-Drain Function

Table 5-40. Pins with Pull Function

Pin	Pull Function	Note
KSI[7:0]	Programmable 75k pull-up resistor	Default off
KSO[17:0]	Programmable 75k pull-up resistor	Default off
GPIO with pull capability and their alternative functions	Programmable 75k pull-up/down resistor	Detail pull capability refer and default on/off refer to Table 7-14 on page 198
FLAD[3:0]	Operational 75k pull-up resistor	Pull-up the bi-directional LAD bus
ID7-0	Operational 75k pull-down resister	Pull down during VSTBY power on to process the hardware strap function

Note: 75k ohm is typical value. Refer to section 9 DC Characteristics on page 349 for details

Table 5-41. Pins with Schmitt-Trigger Function

Pin	Pull Function	Note
All GPIO pins except GPI0-J5 and their alternative functions	Fixed Schmitt-Trigger Input	
KSI[7:0]	Fixed Schmitt-Trigger Input	
WARMRST#	Fixed Schmitt-Trigger Input	

Table 5-42. Signals with Open-Drain Function

Signal	Open-Drain Function	Note
SERIRQ	Open-drain bi-directional signal	
CLKRUN#	Open-drain output signal	
KSO[17:0]	Programmable open-drain output signal	Default is push-pull
PS2CLK0, PS2DAT0 PS2CLK1, PS2DAT1 PS2CLK2, PS2DAT2	Open-drain bi-directional signal	
SMCLK0, SMDAT0 SMCLK1, SMDAT1 SMCLK2, SMDAT2	Open-drain bi-directional signal	
ECSCI#, ECSMI#, PWUREQ#	Open-drain output signal	
GPIO with open-drain capability and their alternative functions	Programmable open-drain output signal	Default is push-pull

5.8 Power Consumption Consideration

- Each input pin should be driven or pulled

Input floating causes leakage current and should be prevented.
Pins can be pulled by an external pull resistor or internal pull for a pin with programmable pull.

- Each output-drain output pin should be pulled

If an output-drain output pin is not used and is not pulled by an external pull resistor or internal pull for a pin with programmable pull, make it drive low by the firmware.

- Each input pin which belongs to VSTBY power plane is connected or pulled up to VCC power plane

Such cases may cause leakage current when VCC is not supplied and a diode may be used to isolate leakage current from VSTBY to VCC. For example, use diodes for KBRST# and GA20 if they are connected to VCC logic of South-Bridge.

- Any pin which belongs to VSTBY power plane should not be pulled to VCC in most cases.

It may cause a leakage current path when VCC is shut down. Refer to the above consideration.

- Program GPIO ports as output mode as soon as possible

Any GPIO port used in output mode should be programmed as soon as possible since this pin may not be driven (be floating) if its default value of pull is off.

- Disable unnecessary pull in power saving mode

Prevent from driving a pin low or letting a pin be driven low but its pull high function is enabled in power saving mode.
Prevent from driving a pin high or letting a pin be driven high but its pull low function is enabled in power saving mode.

- Handle the connector if no cable is plugged into it

The firmware or the hardware should prevent the wire connected to the connector from no driving if no cable is plugged into the connector such as PS/2 mouse and so on.

- Disable unnecessary pull for a programmable pull pin

Pull control may be enabled for an input pin or an open-drain output pin and should be disabled for a push-pull output pin.
Pull control should be disabled if an external pull resistor exists.
External pull resistor can control the pull current precisely since the register value of the internal pull has large tolerance. Refer to section 9 DC Characteristics on page 349 for details.

- Flash standby mode

Make flash enter standby mode to reduce power consumption if it is not used.
It's controlled by AFSTBY bit in FPCFG register.

- Prevent accessing Scratch RAM before entering power-saving mode

There is unnecessary power consumption after Scratch RAM is accessed in data space. Read any other registers of external data memory once to prevent this condition.

- Use Doze mode rather than Idle mode

Doze mode has less power consumption than Idle mode because 8032 internal timer/WDT clock is gated (stopped) in Doze mode.
Firmware design using Idle mode should be replaced with Doze mode by replacing internal timer and watchdog by external timer and watchdog.

- Use Sleep mode rather than Doze mode

Sleep mode has less power consumption than Doze mode because PLL is power-down and EC clock is

stopped in Sleep mode, although most EC modules are not available.
Refer to Table 5-39 on page 35 for the details.

- Gate clock by module in EC domain

All modules in EC domain are not clock gated in default but can be gated by module to get less power consumption.
It's controlled by CGCTRL1R and CGCTRL2R registers.

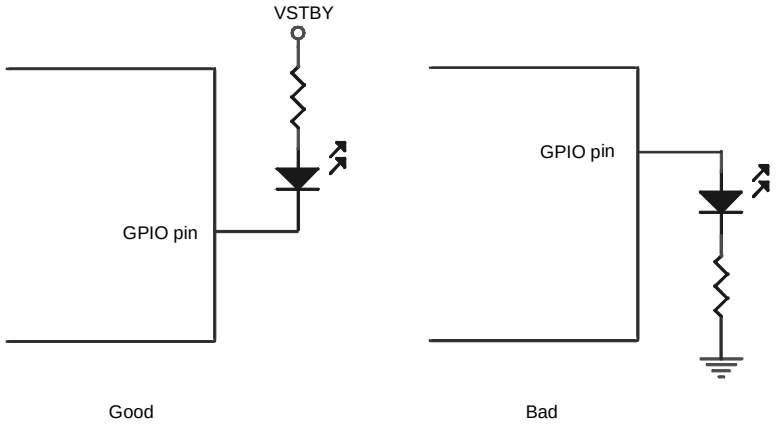
- Power-down ADC/DAC analog circuit if it is unnecessary.

ADC/DAC analog circuits are power-down in default and should be activated only if necessary.
ADC analog circuit power-down is controlled by ADCEN bit in ADCCFG register.
DAC analog circuit power-down is controlled by POWDN bit in DACCTRL register.

- Connect LED cathode to output pin

It doesn't reduce total power consumption although it reduces power consumption of IT8502.
The advantage is to reduce the temperature of IT8502 and prevent the output pad from driving large current.

Figure 5-3. LED connection



6. Host Domain Functions

6.1 Low Pin Count Interface

6.1.1 Overview

The Low Pin Count (LPC) is an interface for modern ISA-free system. It is defined in Intel's LPC Interface Specification, Revision 1.1. There are seven host-controlled modules that can be accessed by the host via the LPC interface. These host-controlled modules are "Logical Devices" defined in Plug and Play ISA Specification, Version 1.0a.

6.1.2 Features

- Complies with Intel's LPC Interface Specification, Revision 1.1
- Supports SERIRQ and complies with Serialized IRQ Support for PCI Systems, Revision 6.0
- Supports LPCPD#/CLKRUN#
- Supports Plug and Play ISA registers

6.1.3 Accepted LPC Cycle Type

The supported LPC cycle types are listed below:
* LPC I/O Read(16-bit address, 8-bit data)
* LPC I/O Write (16-bit address, 8-bit data)
* LPC Memory Read(32-bit address, 8-bit data)
* LPC Memory Write(32-bit address, 8-bit data)
* FWH Read (32-bit address, 8-bit data)
* FWH Write (32-bit address, 8-bit data)

I/O cycles are used to access PNPCFG and Logical Devices. Memory or FWH is used to access Flash content through SMFI module Host-Indirect memory cycles based on I/O cycles can also access Flash. Refer to SMFI Module for details about Host-Indirect memory access.

The following table describes how LPC module responds the I/O, Memory and FWH cycles from Host side in different conditions.

Table 6-1. LPC/FWH Response

Cycle Type/Condition		Read Response	Write Response
All Cycles before PLL Stable NOTE 4		Long-Wait	Long-Wait
I/O Cycle to PNPCFG or Logical Devices		Ready	Ready
I/O Cycle but Address Out Of Range		Cycle Ignored	Cycle Ignored
I/O Cycle to Locked PNPCFG by EC2I		Returns 00h	Cycle Ignored
Host-Indirect Memory Address NOTE 3		Ready	Ready
Memory Cycle, FWH Cycle or Host-Indirect Memory Data		Long-Waits until Ready	Long-Waits until Ready NOTE 1
Memory Cycle, FWH Cycle or	*HERES=00**	Long-Wait	Cycle Ignored
Host-Indirect Memory Data	*HERES=01*	Returns 00h	Cycle Ignored
but Address Protected by SMFI	*HERES=10*	Error-SYNC	Error-SYNC
	HERES=11	Long-Wait	Error-SYNC
Memory Cycle or Host-Indirect Memory Data but Address Out of Range		Cycle Ignored	Cycle Ignored
FWH Cycle but Address Out of Range		Ready	Ready
FWH Cycle but FWH ID is unmatched NOTE 2		Cycle Ignored	Cycle Ignored
FWH Cycle but HBREN bit in HCTRL2R register cleared		Cycle Ignored	Cycle Ignored

Note 1:
After reset, IT8502 responds Long-Waits before Ready for FWH Write Cycle.

If LPC host (South-Bridge) fails to recognize Long-Wait SYNC during FWH Write Cycle, it is recommended to use Host-Indirect Memory.

Note 2:
FWH ID is defined in FWHID field in SHMC register.

Note 3:
Host-Indirect Memory Cycles access the flash via LPC I/O Cycle. Host-Indirect Memory Address is combined with SMIMAR0, SMIMAR1, SMIMAR2 and SMIMAR3 registers. Host-Indirect Memory Data is SMIMDR register.

Note 4:
The host LPC interface is disabled in sleep mode.

6.1.4 Debug Port Function

LPC module implements two latch signals for Main-Board debug purpose. LPC I/O write cycles with address equal to 80h will cause the LPC module to assert L80HLAT and L80LLAT signals which provide a simple external logic to latch it in order to display on LED, even though I/O port 80h is not recognized by PNPCFG or any Logical Device. L80HLAT goes high when it is time to latch the high-nibble of the data written to port 80h, and L80LLAT means the low-nibble.

Port 80h data can be read via parallel port with the software provided by ITE.

6.1.5 Serialized IRQ (SERIRQ)

IT8502 has programmable IRQ number for each logical device. Available IRQ numbers are 1, 2, 3, 4 5, 6, 7, 8, 9, 10, 11, 12, 14, and 15.

Different logical devices inside IT8502 can share the same IRQ number if they have the same IRQPS bit in IRQTP register and are configured as the same triggered mode (all level-triggered or all edge triggered) in their EC side registers.

But it is not allowed to share an IRQ number with a logical device outside IT8502. Note that edge-triggered interrupts are not suitable for sharing in most cases.

6.1.6 Related Interrupts to WUC

- Interrupt to WUC
  If the LPC address of an I/O, LPC Memory or FWH Cycle on LPC bus is accepted, WU42 interrupt will be asserted.

6.1.7 LPCPD# and CLKRUN#

- LPCPD#
  LPCPD# is used as internal “power good” signal to indicate the status of VCC. It is recommended to be implemented. See also VCCDO bit in RSTS register in 7.15.4.5 on page 300.

- CLKRUN#
  When SERIRQ is in the continuous/quiet mode and LPCCLK is active, CLKRUN# is used for maintaining LPCCLK to make sure that the SERIRQ status is entirely transferred to the host side.

  When SERIRQ is in the quiet mode and LPCCLK is stopped, CLKRUN# is used for restoring LPCCLK if there is any interrupt status transition required to be transferred to the host side.

6.1.8 Check Items

If EC fails in LPC memory or I/O cycles at boot, check the following recommended items first.

- LPC/FWH memory cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether HBREN bit is enabled in HCTRL2R register.
  Check whether the firmware doesn't change the read protection control.

- LPC I/O cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether BADDR1-0 field in BADRSEL register are in correct setting.
  Check whether EC2I is not locking PNPCFG access from the host side.

6.2 Plug and Play Configuration (PNPCFG)

The host interface registers of PNPCFG (Plug and Play Configuration) are listed below. The base address can be configured via BADDR1-0 field in BADRSEL register. Note that bit 0 of SWCBALR has to be zero. To access a register of PNPCFG, write target index to address port and access this PNPCFG register via data port. If accessing the data port without writing index to address port, the latest value written to address port is used as the index. Reading the address port register returns the last value written to it.

Table 6-2. Host View Register Map, PNPCFG

	BADDR1-0 =00b	BADDR1-0 =01b	BADDR1-0 =10b	BADDR1-0 =11b
7 0	I/O Port Address			
Address Port	2Eh	4Eh	(SWCBAHR, SWCBALR)	Reserved
Data Port	2Fh	4Fh	(SWCBAHR, SWCBALR+1)	Reserved

Note 1: SWCBALR should be on boundary = 2, which means bit 0 has to be 0.
Note 2: Only use BADDR1-0=10b if the port pair is not 2Eh/2Fh or 4Eh/4Fh.

The host interface registers for Logic Device Control are listed below. The base address can be configured via the following Plug and Play Configuration Registers. Note that if a logical device is activated but with base address equal to 0000h, the host side cannot access this logical device since 0000h means I/O address range is disabled.

Table 6-3. Host View Register Map, Logical Devices

7 0	I/O Port Address
Serial Port 1 (UART1)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+07h) Base address boundary = 16 Legacy Address = 03F8h
System Wake-Up Control (SWUC)	Depend on PnP SW Used Addr: (IOBAD0+00h,+02h,+06h,+07h,13h,15h) Base address boundary = 32
KBC / Mouse Interface	Unused
KBC / Keyboard Interface	Depend on PnP SW Used Addr: (IOBAD0+00h), (IOBAD1+00h) Base address boundary = none, none Legacy Address = 60h,64h
Shared Memory/Flash Interface (SMFI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+8h,+0Ch) Base address boundary = 16
BRAM	Depend on PnP SW Used Addr: (IOBAD0+0h,+1h), (IOBAD1+0h,+1h) Base address boundary = 2, 2 Legacy Address = 70h-73h
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 62h,66h
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 68h,6Ch
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 6Ah,6Eh
Serial Peripheral Interface (SSPI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+03h) Base address boundary = 4

Note: The boundary number means the address has to be the multiple of this number.

The host interface registers for Standard Plug and Play Configuration of PNPCFG are listed below. These registers are accessed via the Index-Data I/O ports defined in Table 6-3 on page 42. Note PNPCFG registers are not allowed to be accessed if LKCFG bit in LSIOHA register of EC2I module is set. They are divided into two parts, Super I/O Configuration Registers and Logical Device Registers.

Table 6-4. Host View Register Map via Index-Data I/O Pair, Standard Plug and Play Configuration Registers

	7 0 Register Name	Index
Super I/O Configuration Registers	Logical Device Number (LDN)	07h
	Chip ID Byte 1(CHIPID1)	20h
	Chip ID Byte 2(CHIPID2)	21h
	Chip Version (CHIPVER)	22h
	Super I/O Control (SIOCTRL)	23h
	Reserved	24h
	Super I/O IRQ Configuration (SIOIRQ)	25h
	Super I/O General Purpose (SIOGP)	26h
	Reserved	27h
	Reserved	28h
	Reserved	29h
	Reserved	2Ah
	Reserved	2Bh
	Super I/O Power Mode (SIOPWR)	2Dh
	Reserved	2Eh
Logical Device Configuration Registers Selected by LDN Register	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	DMA Channel Select 0 (DMAS0)	74h
	DMA Channel Select 1 (DMAS1)	75h
	Device Specific Logical Device Configuration 1 to 10	F0h-F9h

The IRQ numbers for Logic Device IRQ via LPC/SERIRQ are listed below. The IRQ numbers can be configured via the above Plug and Play Configuration Registers.

Table 6-5. Interrupt Request (IRQ) Number Assignment, Logical Device IRQ via SERIRQ

Logical Device	IRQ number
Serial Port 1 (UART1)	Depend on PnP SW, Legacy IRQ Num=04
System Wake-Up Control (SWUC)	Depend on PnP SW
KBC / Mouse Interface	Depend on PnP SW, Legacy IRQ Num=12
KBC / Keyboard Interface	Depend on PnP SW, Legacy IRQ Num=01
Shared Memory/Flash Interface (SMFI)	Unused
BRAM	Depend on PnP SW, Legacy IRQ Num=08
Power Management I/F Channel 1 (PMC1)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 2 (PMC2)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 3 (PMC3)	Depend on PnP SW, Legacy IRQ Num=01
Serial Peripheral Interface (SSPI)	Depend on PnP SW

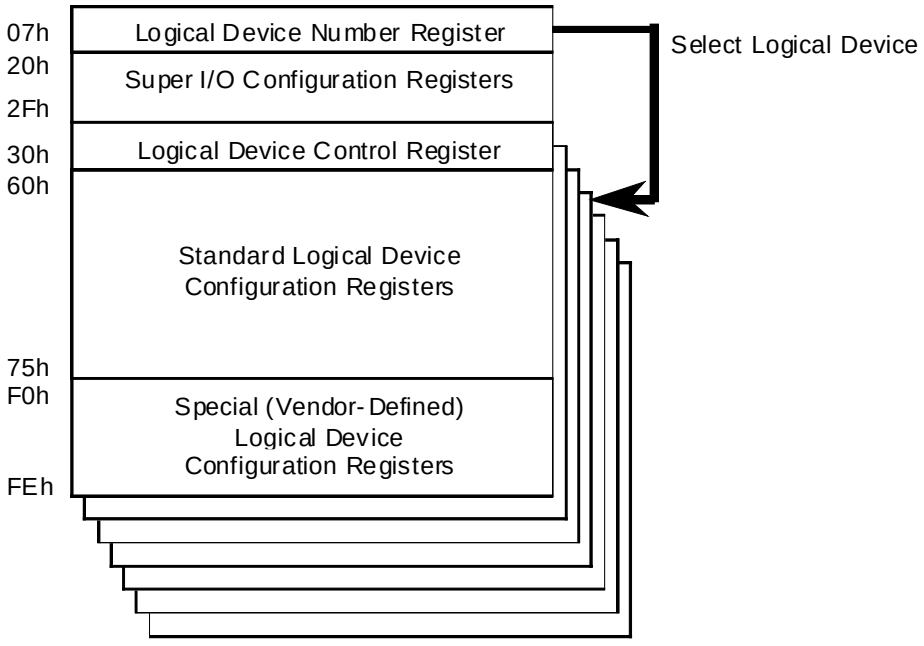
6.2.1 Logical Device Assignment

Table 6-6. Logical Device Number (LDN) Assignments

LDN	Functional Block
01h	Serial Port 1 (UART1)
04h	System Wake-Up Control (SWUC)
05h	KBC/Mouse Interface
06h	KBC/Keyboard Interface
0Fh	Shared Memory/Flash Interface (SMFI)
10h	BRAM
11h	Power Management I/F Channel 1 (PMC1)
12h	Power Management I/F Channel 2 (PMC2)
13h	Serial Peripheral Interface (SSPI)
17h	Power Management I/F Channel 3 (PMC3)

The following figure indicates the PNPCFG registers is combined with Super I/O Configuration Registers and Logical Device Configuration Registers. Logical Device Configuration Registers of a specified Logical Device is accessible only when Logical Device Number Register is filled with corresponding Logical Device Number listed in Table 6-6 on page 44 .

Figure 6-1. Host View Register Map via Index-Data Pair



6.2.2 Super I/O Configuration Registers

Registers with index from 07h to 2Eh contain Super I/O configuration settings.

6.2.2.1 Logical Device Number (LDN)

This register contains general Super I/O configurations.

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	04h	**Logical Device Number (LDN)** This register selects the current logical device. All other values are reserved.

6.2.2.2 Chip ID Byte 1 (CHIPID1)

Index: 20h

Bit	R/W	Default	Description
7-0	R	85h	**Chip ID Byte 1 (CHIPID1)** This register contains the Chip ID byte 1.

6.2.2.3 Chip ID Byte 2 (CHIPID2)

Index: 21h

Bit	R/W	Default	Description
7-0	R	02h	**Chip ID Byte 2 (CHIPID2)** This register contains the Chip ID byte 2.

6.2.2.4 Chip Version (CHIPVER)

This register contains revision ID of this chip

Index: 22h

Bit	R/W	Default	Description
7-0	R	71h	**Chip Version (CHIPVER)**

6.2.2.5 Super I/O Control Register (SIOCTRL)

This register contains general Super I/O configurations.

Index: 23h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-4	-	0h	**Reserved**
3-2	-	0h	**Reserved**
1	W	0b	**Software Reset (SIOSWRST)** Read always returns 0. 0: No action. 1: Software Reset the logical devices.
0	R/W	1b	**Super I/O Enable (SIOEN)** 0: All Super I/O logical devices are disabled except SWUC and SMFI. 1: Each Super I/O logical device is enabled according to its Activate register. (Index 30h)

6.2.2.6 Super I/O IRQ Configuration Register (SIOIRQ)

This register contains general Super I/O configurations.

Index: 25h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0b	**SMI# to IRQ2 Enable (SMI2IRQ2)** This bit enables using IRQ number 2 in the SERIRQ protocol as a SMI# interrupt. This bit is similar to LDACT bit in LDA register. 0: Disabled 1: Enabled
3-0	-	0h	**Reserved**

6.2.2.7 Super I/O General Purpose Register (SIOGP)

This register contains general Super I/O configurations.

Index: 26h

Bit	R/W	Default	Description
7	R/W	0b	**SIOGP Software Lock (SC6SLK)** 0: GPSCR can be cleared by both Hardware and Software reset. (SIOSWRST). 1: GPSCR can only be cleared by Hardware reset.
6-5	R/W	00b	**General-Purpose Scratch (GPSCR)** Reading returns the value that was previously written. Note that the EC side can access whole PNPCFG registers via EC2I.
4	-	0h	**Reserved**
3-0	-	0h	**Reserved**

6.2.2.8 Super I/O Power Mode Register (SIOPWR)

This register is a battery-backed register used by the EC side. See also 6.4.5.2.

Index: 2Dh

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0b	**Power Supply Off (PWRSLY)** It indicates the EC side that the host requests to shut down the power in legacy mode. Refer to SCRDPSO bit in SWCTL2 register on page 103 0: No action 1: It indicates power shut down if PWRSLY is Legacy mode. **Note:** It always returns 0 when read.
0	R/W	0h	**Power Button Mode (PWRBTN)** This bit controls the power button mode in the SWUC. Refer to SCRDPBM bit in SWCTL2 register on page 103 0: Legacy 1: ACPI

6.2.3 Standard Logical Device Configuration Registers

Registers with index from 30h to F9h contain Logical Device configuration settings. LDN of the wanted logical device should be written to LDN register before accessing these registers.
This section lists a standard description of these registers. Some default values for each register and more detailed information for each logical device should be referred in each section.

6.2.3.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-1	-	0h	**Reserved**
0	R/W	0b	**Logical Device Activation Control (LDACT)** 0: Disabled The registers (Index 60h-FEh) are not accessible. Refer to SIOEN bit in SIOCTRL 1: Enabled

6.2.3.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 0.

6.2.3.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 0.

6.2.3.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 1.

6.2.3.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 1.

6.2.3.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register will be read-only if it is unused by a logical device.

Index: 70h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0	**Wake-Up IRQ Enable (WKIRQEN)** Allow this logical device to trigger a wake-up event to SWUC. This bit should not be set in SWUC Logical Device since it is used to collect IRQ sources for SWUC. 0: Disabled 1: Enabled
3-0	R/W	Depend on Logical Device	**IRQ Number (IRQNUM)** Select the IRQ number (level) asserted by this logical device via SERIRQ. 00d: This logical device doesn't use IRQ. 01d-012d: IRQ1-12 are selected correspondingly. 14d-15d: IRQ14-15 are selected correspondingly. Otherwise: Invalid IRQ routing configuration.

6.2.3.7 Interrupt Request Type Select (IRQTP)

This register will be read-only if it is unused by a logical device.

Index: 71h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	Depend on Logical Device	**Interrupt Request Polarity Select (IRQPS)** This bit indicates the polarity of the interrupt request. 0: IRQ request is buffered and applied on SERIRQ. 1: IRQ request is inverted before being applied on SERIRQ. This bit should be configured before the logical device is activated.
0	R/W	Depend on Logical Device	**Interrupt Request Triggered Mode Select (IRQTMS)** This bit indicates that edge or level triggered mode is used by this logical device and should be updated by EC firmware via EC2I since the triggered mode is configured in EC side registers. This bit is just read as previously written (scratch register bit) and doesn't affect SERIRQ operation. 0: edge triggered mode 1: level triggered mode

6.2.3.8 DMA Channel Select 0 (DMAS0)

Index: 74h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 0** A value of 4 indicates that no DMA channel is active.

6.2.3.9 DMA Channel Select 1 (DMAS1)

Index: 75h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 1** A value of 4 indicates that no DMA channel is active.

6.2.4 Serial Port 1 (UART1) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-7. Host View Register Map via Index-Data I/O Pair, UART1 Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 01h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
Selected if LDN Register=04h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	High Speed Baud Rate Select (HHS)	F0h

6.2.4.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.4.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.2 on page 47.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't be written.

6.2.4.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	F8h	**Refer to section 6.2.3.3 on page 47.** Bit 3-0 (IOBAD0[3:0]) are forced to 8h and can't be written. It means the base address is on the 16-byte boundary.

6.2.4.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.4.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 47.**

6.2.4.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	04h	**Refer to section 6.2.3.6 on page 47.**

6.2.4.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.2.3.7 on page 48.**

6.2.4.8 High Speed Baud Rate Select (HHS)

Index: F0h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**High Speed Baud Rate Select (HHS)** This bit indicates that the baud rate of UART1 can be up to 230.4K/460.8K baud, which are determined by the divisor of the baud rate generator. (From Host Side) 0: Not selected 1: Selected
0	-	0b	**Reserved**

6.2.5 System Wake-Up Control (SWUC) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-8. Host View Register Map via Index-Data I/O Pair, SWUC Logical Device

	7 0	Index
	Register Name	
Super I/O Control Reg	Logical Device Number (LDN = 04h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
Selected if LDN Register=04h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.5.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.5.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.**

6.2.5.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.3 on page 47.** Bits 4-0 (IOBAD0[4:0]) are forced to 00000b and can't be written. It means the base address is on the 32-byte boundary.

6.2.5.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.5.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 47.**

6.2.5.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.6 on page 47.**

6.2.5.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.6 KBC / Mouse Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-9. Host View Register Map via Index-Data I/O Pair, KBC / Mouse Interface Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 05h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8]) –Unused	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0]) –Unused	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8]) –Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) –Unused	63h
Selected if LDN Register=05h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.6.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.6.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register is unused and read-only.

Index: 60h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.2 on page 47.**

6.2.6.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register is unused and read-only.

Index: 61h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.3 on page 47.**

6.2.6.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.6.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 47.**

6.2.6.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	0Ch	**Refer to section 6.2.3.6 on page 47.**

6.2.6.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.7 KBC / Keyboard Interface Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-10. Host View Register Map via Index-Data I/O Pair, KBC / Keyboard Interface Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 06h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=06h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.7.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.7.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.7.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	60h	**Refer to section 6.2.3.3 on page 47.**

6.2.7.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.7.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	64h	**Refer to section 6.2.3.5 on page 47.**

6.2.7.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.6 on page 47.**

6.2.7.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.8 Shared Memory/Flash Interface (SMFI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-11. Host View Register Map via Index-Data I/O Pair, SMFI Interface Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 0Fh)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=0Fh	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) –Unused	70h
	Interrupt Request Type Select (IRQTP) -Unused	71h
	Shared Memory Configuration Register (SHMC)	F4h
	HLPC RAM Base Address [15:12] (HLPCRAMBA[15:12])	F5h
	HLPC RAM Base Address [23:16] (HLPCRAMBA[23:16])	F6h

6.2.8.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.8.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.**

6.2.8.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.3 on page 47.** Bits 3-0 (IOBAD0[3:0]) are forced to 0000b and can't be written. It means the base address is on the 16-byte boundary.

6.2.8.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.8.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 47.**

6.2.8.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register is unused and read-only.

Index: 70h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.6 on page 47.**

6.2.8.7 Interrupt Request Type Select (IRQTP)

This register is unused and read-only.

Index: 71h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.7 on page 48.**

6.2.8.8 Shared Memory Configuration Register (SHMC)

Index: F4h

Bit	R/W	Default	Description
7-4	R/W	0h	**BIOS FWH ID (FWHID)** These bits correspond to the 4-bit ID which is part of a FWH transaction.
3	-	-	**Reserved**
2	-	-	**Reserved**
1	R/W	0b	**BIOS Extended Space Enable (BIOSEXTS)** This bit expands the BIOS address space to make this chip respond the Extended BIOS address range.
0	-	-	**Reserved**

6.2.8.9 HLPC RAM Base Address [15:12] (HLPCRAMBA[15:12])

The HLPC RAM base address is only within the range: FFXX_X000h. (X denotes it's programmable by registers).
The HPLC RAM function will be disabled if SPI follow mode is enabled.
The HPLC RAM function/D2EC must not be activated at the same time.

Index: F5h

Bit	R/W	Default	Description
7-4	R/W	0h	**HLPC RAM Base Address Bits [15:12] (HLPCRAMBA[15:12])** Define EC internal RAM base address on LPC memory space.
3-0	-	-	**Reserved**

6.2.8.10 HLPC RAM Base Address [23:16] (HLPCRAMBA[23:16])

Index: F6h

Bit	R/W	Default	Description
0	-	-	**HLPC RAM Base Address Bits [23:16] (HLPCRAMBA[23:16])** Define EC internal RAM base address on LPC memory space.

6.2.9 BRAM Configuration Registers

This section lists the default value for each register and more detailed information for this logical device. Some registers' bits will be read-only if unused.

Table 6-12. Host View Register Map via Index-Data I/O Pair, BRAM Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 10h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=10h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) –Unused	70h
	Interrupt Request Type Select (IRQTP) –Unused	71h
	P80L Begin Index (P80LB)	F3h
	P80L End Index (P80LE)	F4h
	P80L Current Index (P80LC)	F5h

6.2.9.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.** Refer to SIOEN bit in SIOCTRL and SIOEN bit in SIOCTRL Register.

6.2.9.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.**

6.2.9.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	70h	**Refer to section 6.2.3.3 on page 47.** Bit 0 (IOBAD0[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.2.9.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.9.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	72h	**Refer to section 6.2.3.5 on page 47.** Bit 0 (IOBAD0[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.2.9.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	08h	**Refer to section 6.2.3.6 on page 47.**

6.2.9.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.9.8 P80L Begin Index (P80LB)

Index: F3h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5-0	R/W	-	**P80L Begin Index (P80LBI)** It indicates the P80L queue begins in RTC/BRAM Bank 1. Refer to section 7.17.3.1 P80L on page 308.

6.2.9.9 P80L End Index (P80LE)

Index: F4h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R/W	-	**P80L End Index (P80LEI)** It indicates the P80L queue ends in RTC/BRAM Bank 1. Refer to section 7.17.3.1 P80L on page 308.

6.2.9.10 P80L Current Index (P80LC)

Index: F5h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	R/W	-	**P80L Current Index (P80LC)** It indicates the P80L queue current in RTC/BRAM Bank 1. Refer to section 7.17.3.1 P80L on page 308.

6.2.10 Power Management I/F Channel 1 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-13. Host View Register Map via Index-Data I/O, PMC1 Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 11h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
Selected if LDN Register=11h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.10.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.10.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.10.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	62h	**Refer to section 6.2.3.3 on page 47.**

6.2.10.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.10.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	66h	**Refer to section 6.2.3.5 on page 47.**

6.2.10.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
3-0	R/W	01h	**Refer to section 6.2.3.6 on page 47.**

6.2.10.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-2	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.11 Power Management I/F Channel 2 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-14. Host View Register Map via Index-Data I/O, PMC2 Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 12h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])	64h
	I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])	65h
Selected if LDN Register=12h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	General Purpose Interrupt (GPINTR)	F0h

6.2.11.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.11.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.11.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	68h	**Refer to section 6.2.3.3 on page 47.**

6.2.11.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.11.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Ch	**Refer to section 6.2.3.5 on page 47.**

6.2.11.6 I/O Port Base Address Bits [15:8] for Descriptor 2 (IOBAD2[15:8])

It contains Command/Status Register Base Address Register.

Index: 64h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.11.7 I/O Port Base Address Bits [7:0] for Descriptor 2 (IOBAD2[7:0])

It contains Command/Status Register Base Address Register.

Index: 65h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.5 on page 47.** Bits 3-0 (IOBAD2[3:0]) are forced to 0000b and can't be written.

6.2.11.8 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.6 on page 47.**

6.2.11.9 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.11.10 General Purpose Interrupt (GPINTR)

Index: F0h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	W	-	**General Purpose Interrupt 3 (GPINT3)** Writing 1 to this bit will issue an interrupt to INT35.
2	W	-	**General Purpose Interrupt 2 (GPINT2)** Writing 1 to this bit will issue an interrupt to INT34.
1	W	-	**General Purpose Interrupt 1 (GPINT1)** Writing 1 to this bit will issue an interrupt to INT33.
0	W	-	**General Purpose Interrupt 0 (GPINT0)** Writing 1 to this bit will issue an interrupt to INT32.

6.2.12 Power Management I/F Channel 3 Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-15. Host View Register Map via Index-Data I/O, PMC3 Logical Device

7 0 Index

	7 Register Name 0	Index
Super I/O Control Reg	Logical Device Number (LDN = 17h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=17h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.12.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.12.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 47.** Bit 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.12.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	6Ah	**Refer to section 6.2.3.3 on page 47.**

6.2.12.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 47.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.12.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Eh	**Refer to section 6.2.3.5 on page 47.**

6.2.12.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
3-0	R/W	01h	**Refer to section 6.2.3.6 on page 47.**

6.2.12.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-2	R/W	01h	**Refer to section 6.2.3.7 on page 48.**

6.2.13 Serial Peripheral Interface (SSPI) Configuration Registers

This section lists the default value for each register respectively and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-16. Host View Register Map via Index-Data I/O Pair, SSPI Logical Device

	7 0	Index
	Register Name	
Super I/O Control Reg	Logical Device Number (LDN = 12h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
Selected if LDN Register=04h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.13.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 47.**

6.2.13.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.2 on page 47.** Bit 7-4 (IOBAD0[15:12]) are forced to 0000b and can't written.

6.2.13.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.3 on page 47.** Bit 1-0 (IOBAD0[1:0]) are forced to 00b and can't be written. It means the base address is on the 4-byte boundary.

6.2.13.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 47.**

6.2.13.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 47.**

6.2.13.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.6 on page 47.**

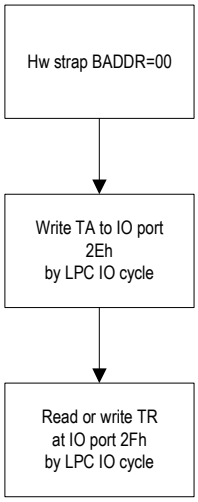
6.2.13.7 Interrupt Request Type Select (IRQTP)

Index: 71h

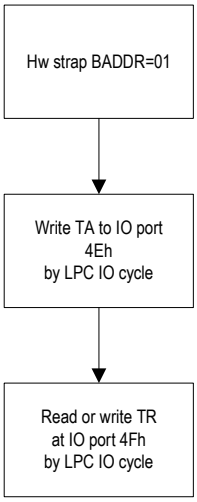
Bit	R/W	Default	Description
7-0	R/W	02h	**Refer to section 6.2.3.7 on page 48.**

6.2.14 Programming Guide

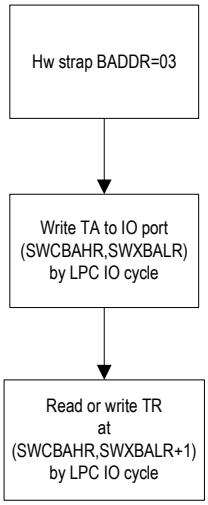
Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 1



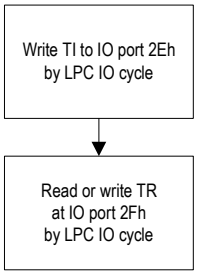
Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 2



Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 3



Host Side
To read or write the target register (TR)
at target Index (TI) of PNPCFG
TI = 00h~2Eh
(Assume BADDR=00)



Host Side
To read or write the target register (TR)
at target Index(TI) of PNPCFG
TI=30h~FEh, belongs to target logical device (TLD)
(Assume BADDR=00)

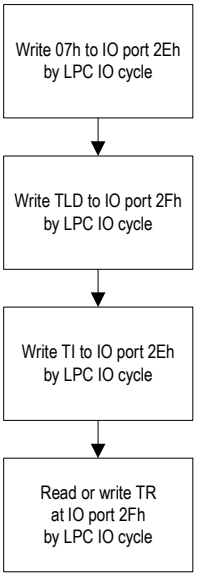
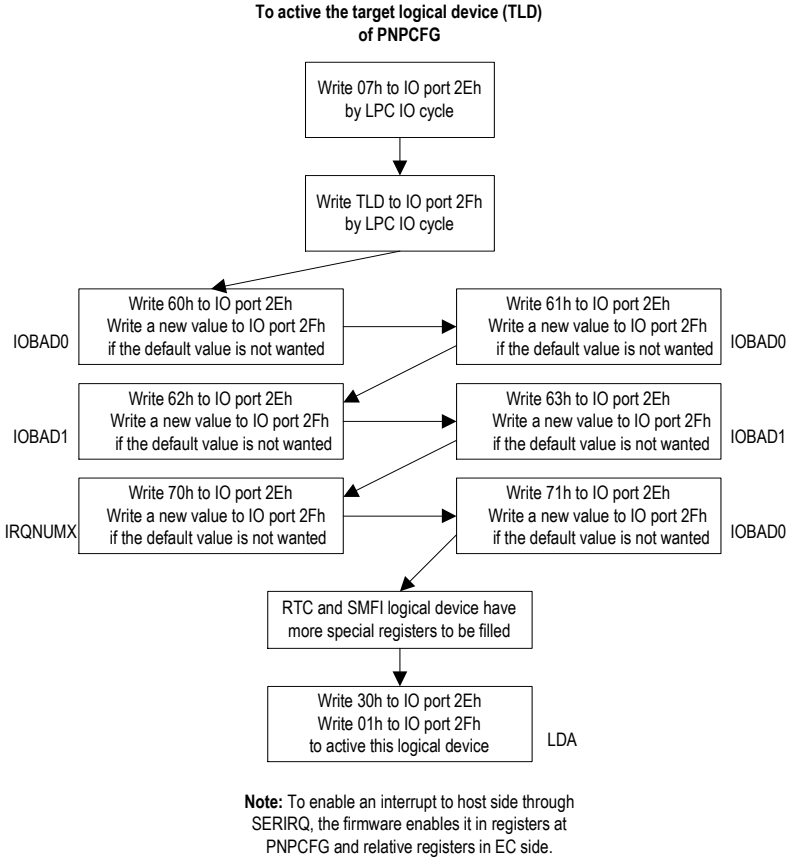


Figure 6-2. Program Flow Chart for PNPCFG



See also section 7.13.5 on page 289 for accessing PNPCFG through EC2I.

6.3 Shared Memory Flash Interface Bridge (SMFI)

6.3.1 Overview

The bridge provides the host to access the shared memory. It also provides EC code address space mapped into host domain address space, and locking mechanism for read/write protection.

6.3.2 Features

- Behaves as a LPC/FWH memory device (HLPC)
- Supports memory mapping between host domain and EC domain
- Supports read/write(program/erase) flash operations and protection mechanism
- Supports two shared memory access paths: host and EC
- Supports serial flash and up to 16M bytes

6.3.3 Function Description

6.3.3.1 Supported Interface

IT8502/SMFI can behave as a LPC/FWH memory device on LPC bus connected to the host SouthBridge and this function is abbreviated as HLPC.

6.3.3.2 Supported Flash

IT8502 – Serial Flash:

Requirement:

Only one serial flash can be attached.

6.3.3.3 HLPC: Host Translation

The SMFI provides an HLPC interface between the host bus and the M bus. The flash is mapped into the host memory address space for host accesses. The flash is also mapped into the EC memory address space for EC accesses.

An M bus transaction is generated by the host bus translations and has the following three types:

- 8-bit LPC Memory Read/Write
- 8-bit FWH Read/Write
- 8-bit Host-Indirect Memory Read/Write

After the LPC address translation is done, the host memory transaction is forwarded to M-bus (flash interface) if it is accessing an unprotected region. The host side can't issue a write transaction until the firmware write 1 to HOSTWA bit SMECCS register.

6.3.3.4 HLPC: Memory Mapping

The host memory addresses are mapped into the following regions shown in the following table. Some regions are always mapped and some are mapped only when the corresponding register is active. And these regions may be mapped into the same range in the flash space. See also Table 3-1 on page 6.

Table 6-17. Mapped Host Memory Address

Memory Address Range (byte)	Region Description
FFC0_0000h-FFFF_FFFFh	**386 Mode BIOS Range** This is the memory space whose maximum value is up to 4M bytes. If the flash size defined in FMSSR register is smaller than 4M bytes, the remaining space is treated as "Out of Range",
000F_0000h-000F_FFFFh	**Legacy BIOS Range** The total is 64K inside lower 1M legacy BIOS range.
000E_0000h-000E_FFFFh	**Extended Legacy BIOS Range** The total is 64K inside lower 1M legacy BIOS range.

The following memory transactions are based on LPC, FWH or I/O Cycles which are valid only when corresponding HBREN bit in HCTRL2R register is enabled.

Legacy BIOS Range
Always handle.

Extended Legacy BIOS Range
Handle only when BIOSEXTS bit in SHMC register is active. Otherwise, transactions are ignored.

386 Mode BIOS Range
Always handle.

Host-Indirect Memory Address
Host-Indirect Memory Cycles are memory transactions based on LPC I/O Cycles.
This address specified in SMIMAR3-0 is used as follows:
Translated 32-bit host address = { SMIMAR3[7:0], SMIMAR2[7:0], SMIMAR1[7;0], SMIMAR0[7:0]}

6.3.3.5 HLPC: Host-Indirect Memory Read/Write Transaction

The following I/O mapped registers can be used to perform an M bus transaction using an LPC I/O transaction:

- **Host-Indirect Memory Address registers (SMIMAR 3-0)**

Stand for host address bit 31 to 0.

- **Host-Indirect Memory Data register (SMIMDR)**

Stand for read or write data bit 7 to 0.

When LPC I/O writes to IMD register, SMFI begins a flash read with SMIMAR3-0 as the addresses. IT8502 responds Long-Waits until the transaction on M-bus (flash interface) is completed.
When LPC I/O read cycle from SMIMDR register begins a flash write with using the SMIMAR3-0 as the address. The data back from SMIMDR register is used to complete the LPC I/O read cycle.
Host-Indirect memory read/write transactions use the same memory mapping and protection mechanism as the LPC memory read/write transactions.

6.3.3.6 EC-Indirect Memory Read/Write Transaction

R8032TT in IT8502 can access full flash address range via "MOVX" instruction.
This kind of access is useful to

1. read flash ID for EC BIOS.
2. customize user-defined flash programming interface.
3. put extra BIOS data outside EC 64K.

- **EC-Indirect Memory Address registers (ECINDAR3-0)**

Stand for flash address bit 31 to 0.

- **EC-Indirect Memory Data register (ECINDDR)**

Stand for read or write data bit 7 to 0.

6.3.3.7 Flash Shared between Host and EC Domains

A hardware arbiter handles flash read/write translation between the host and EC side.

- **HLPC**

IT8502 bridges the memory cycles on LPC bus and bridges them to the attached SPI flash.
The SMFI internal flash controller performs interleave mechanism control to let the flash fetch for the host and EC side.

It may responde to Long-Waits on LPC bus or freeze 8032 code-fetch due to interleave mechanism.
There is no internal hard-wired mechanism to monitor whether the attached SPI flash is in the WIP (busy) state caused by the WIP instruction from the host.

When the host wants to erase or program the flash, the signaling interface (Semaphore Write or KBC/PMC extended command such as 62h/66h command) notifies the firmware to write 1 to HOSTWA bit in SMECCS register. EC 8032 will fail to code fetch due to the WIP (busy) state caused by erasing/programming so Scratch ROM must be applied (see also section 6.3.3.11). Once the host accessing to the flash is completed, the host should indicate this to the EC, allowing EC to clear HOSTWA bit and resume normal operation. The EC can clear HOSTWA bit at any time, and prevent the host from issuing any erase or program operations.

Defer SPI WIP Instruction in the Follow Mode:
This WIP instruction received by the EC will not be bridged to the flash immediately.

It returns Long-Waits to the SouthBridge.
It issues INT59 to notify the firmware in default; however, if the start addresses of this WIP and the preceding WIP instruction are within the same 4K block boundary (address bit 23-12 of this and preceding cycle are identical), INT59 will be omitted.

The firmware may check the 8-bit SPI instruction (DSINST register) and SPI address bit 23-12 (DSADR1 and DSADR2 register) then decide to allow/inhibit this WIP instruction by writing 1/0 to DISS bit in HINSTC1 register. The firmware can not modify the programmed data in the deferred mode.

6.3.3.8 Host Access Protection

HLPC:
It provides host hardware read protection, hardware write protection and software write protection.

The hardware read/write protection is controlled by two sets of registers.
Set 0: P0ZR, P0BA0R and P0BA1R registers for hardware read/write protection
Set 1: P1ZR, P1BA0R and P1BA1R registers for hardware read/write protection
Common: HINSTC2 for hardware write protection

The software write protection is controlled by the deferred mode of the WIP instruction.
Refer to HINSTC1, DSINST, DSADR1 and DSADR2 registers

6.3.3.9 Serial Flash Performance Consideration

Clock-tick number spent for each cycle = 8

Clock-tick number spent for branching instruction = M + (4 + N) x 8
M = FSCE# Min High Width = 1 + SCEMINHW
(SCEMINHW field in FLHCTRL2R register
N = 1 if “Fast Read” (SPIFR bit in FLHCTRL1R register)

The selection of these registers depends on the flash specification.
Note that the flash clock frequency is FreqPLL.
(FreqPLL is listed in Table 10-2 on page 352)

Host LPC has very poor read performance on M-bus if HOSTWA bit in SMECCS register is set.

6.3.3.10 Response to a Forbidden Access

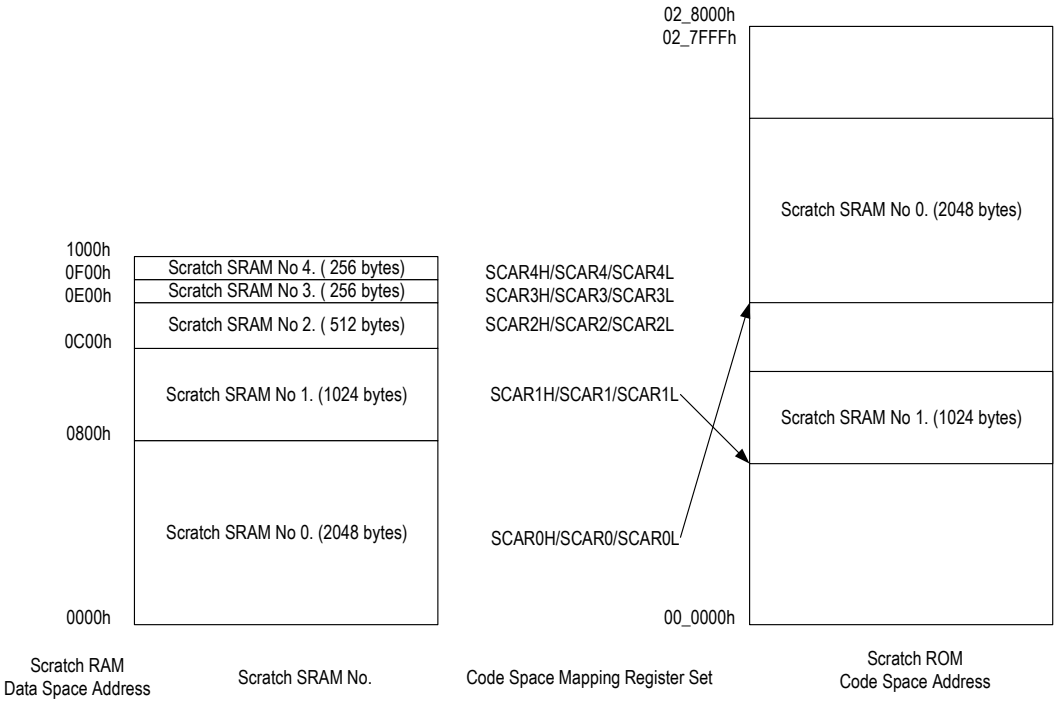
A forbidden access is generated by a translated host address which is protected.
HLPC:
The response to the host bus is according to HERES field in SMECSS register.

6.3.3.11 Scratch SRAM

There are five internal Scratch SRAM No 0-4 which are always mapped into data space and may be mapped into code space if their corresponding code space mapping registers are enabled. It also means that Scratch SRAM may be mapped into data and code space at the same time and the firmware on Scratch ROM can access the same Scratch RAM. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.

Each of these five Scratch SRAM can be mapped into code space with any base addresses without the boundary limit. More than one Scratch SRAM No. can be mapped into code space with an overlay range.

Figure 6-3. Scratch SRAM in Data Space



Each Scratch SRAM No. has three corresponding code space mapping registers in Figure 6-3. Scratch SRAM in Data Space. To enable a Scratch SRAM to be mapped into code space, refer to the following steps with code space mapping registers.

For Scratch SRAM No. 0:

SC0A17-0 field (18-bit) is the address of Scratch SRAM No. 0 and has been translated according to "Mapped Flash Address Range" field in Table 3-2. EC/Flash Mapping on page 7. Also refer to ECBB field in FECBSR register on page 81.

The base address in SC0A17-0 field is only valid if it is between 00_0000h and 02_7FFFh.

To enable the code space mapping of Scratch No. 0:
Make SC0A17-0 field is between 00_0000h and 02_7FFFh.
To disable the code space mapping of Scratch No. 0:
Write 11b to SC0A17-16 field.

Scratch SRAM No.0 is always located in data space regardless of mapping into code space.

So is Scratch SRAM No. 1-4.

This SSMC bit in FBCFG register is OBSOLETE. This register bit is only used to be compatible with old IT8510 firmware and should not be used in new firmware.

6.3.3.12 DMA for Scratch SRAM

DMA (Direct Memory Access) is used to shadow flash content of a specified address range inside code

space to Scratch SRAM. The performance of DMA is much better than "MOVC-MOVX" steps.

To enable DMA operation to Scratch SRAM No. 0, please follow the steps below:
1. Write data to SCARH register with wanted SC0A17-16 field and 1 to NSDMA bit.
2. Write data to SCAR0L register with wanted SC0A7-0 field.
3. Write data to SCAR0M register with wanted SC0A15-8 field.
4. Write data to SCARH register with wanted SC0A17-16 field and 0 to NSDMA bit.
   DMA operation is started and code space mapping is enabled after DMA operation is finished.

If the firmware wants to modify the mapped base address in code space, more steps below should be taken:

5. Write data to SCAR0H register with 11b to SC0A17-16 field.
   Disable code space mapping first since SC0A17-0 are modified in three writings and may be invalid before writing is completed.
6. Write data to SCAR0M/SCAR0L register with wanted SC0A15-0 field.
7. Write data to SCAR0H register with wanted SC0A17-16 field.
   Enable code space mapping after this step.

So is Scratch SRAM No. 1-4.
See also 7.1.10.4 Code snippet of Copying Flash Content to Scratch ROM (DMA) on page 158.

6.3.3.13 HLPC: Flash Programming via Host LPC Interface with Scratch SRAM

When programming flash is processing, the flash will be busy and code fetch from flash by 8032 and will be invalid and cause 8032 fail to execute instructions. It means the firmware must copy necessary instructions from code space to Scratch SRAM, enable mapping Scratch SRAM to Scratch ROM, and jump to Scratch ROM before programming flash.

Flash Programming Steps:
(a) The host side communicates to the EC side via KBC/PMC extended or semaphore registers
(b) EC side: Write 1 to HOSTWA bit in SMECCS register
(c) EC side: Copy necessary code to Scratch RAM (by MOVC-MOVX steps or DMA)
(d) EC side: Enable code space mapping of Scratch SRAM
(e) EC side: Make the host processor enter SMM mode if necessary
(f) EC side: Jump instruction to Scratch ROM
(g) Host side: Set related memory-write registers in South-Bridge
(h) Host side: Start flash programming
(i) End flash programming and reset EC domain if necessary.
   (Refer to section 5.5 on page 31)

Note: Do not let EC enter Idle/Doze/Sleep mode while processing flash programming flow.

6.3.3.14 Force 8032 to Code Fetch from Internal SRAM

For serial flash, it may not be accessed immediately after issuing “Release Power Down (ABh)” instruction until a time delay is listed on flash specification.

To make sure there is no access cycle on the flash after waking up from the Sleep mode, the firmware must execute a delay routine in Scratch ROM.

It means that “ORL PCON” instruction, delay routine and interrupt entry (e.g.0013h for INT1#) are all required to be code-fetch from internal SRAM (Scratch).

6.3.3.15 Force 8032 to Clear Dynamic Caches

For serial flash, after the flash is modified by the host program, the dynamic caches has to be cleared since they contain old and invalid cache content. Refer to section 7.1.10.6 Code snippet of Clearing Dynamic Caches on page 159.

6.3.3.16 HLPC: Serial Flash Programming

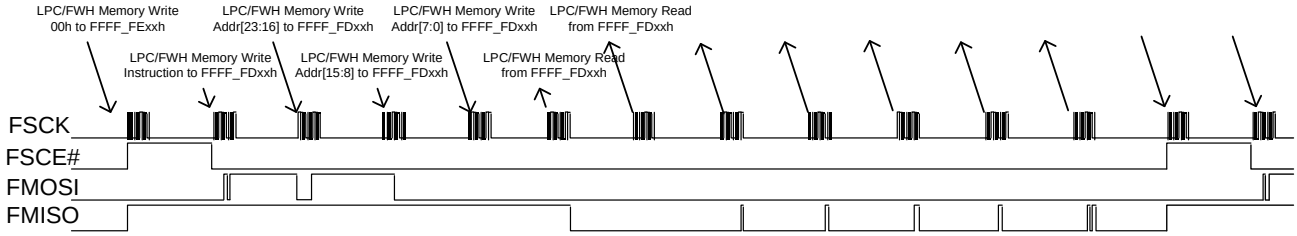
There is Follow Mode dedicated for serial flash programming through host LPC interface.
Follow Mode is enabled after

1. writing 1 to HOSTWA bit in SMECCS register in the EC side.
2. writing 00h to LPC/FWH Address FFFF_FExxh in the host side

In Follow Mode,

1. writing 00h to LPC/FWH Memory Address FFFF_FExxh generates FSCE# with high level.
2. writing data to LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and FMOSI with written data.
3. reading data from LPC/FWH Memory Address FFFF_FDxxh generates FSCE# with low level and read data from FMISO.
4. all the above actions are clocked by 8 FSCK clock-tick and FSCK is stopped in other cases.

Figure 6-4. Follow Mode for Serial Flash (e.g. Fast Read Instruction)

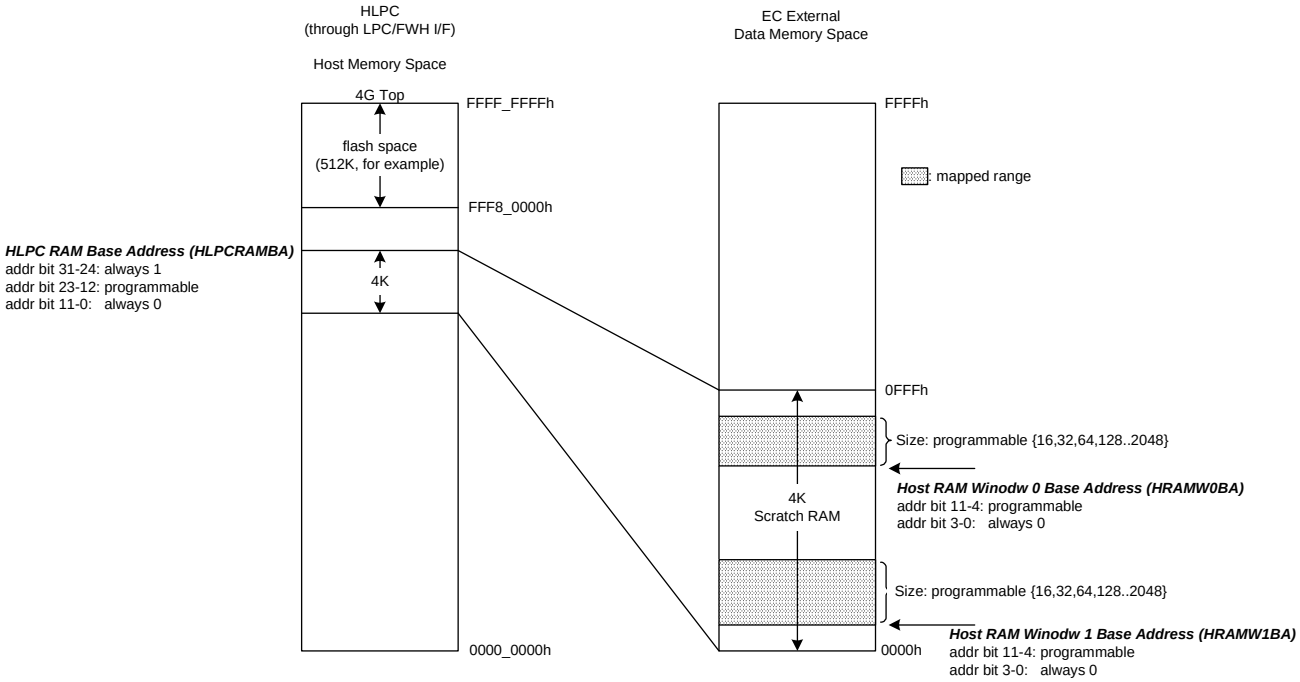


6.3.3.17 Host Side to EC Scratch RAM (H2RAM)

6.3.3.17.1 HLPC to EC Scratch RAM (H2RAM-HLPC)

- H2RAM can be used by the host side software to access 4K EC Scratch RAM through LPC Memory/FWH cycles.
- The read/write protection mechanism is also supported by this function.

Figure 6-5. H2RAM-HLPC Mapping



6.3.3.18 SPI Flash Power-on Detection

For some applications (e.g. IT8502 behaves as an SPI memory slave), the base address of EC code will be located at non-zero address in SPI flash memory.

The process of hard-wired power-on detection is described below, where the [addr xxh] represents the 8-bit content at flash address xxh:

(a) After reset, check the [addr 00h] first. If the content is the jump instruction (LJMP/SJMP/AJMP, or 02h/80h/xxx00001b), then the detection is finished and the base address of EC code will be fixed at flash address 00h. If not matched, go to the next step (b).

(b) Check the five specific contents of "[addr 00h] = 5Ah, [addr 01h] = A5h, [addr 02h] = F0h, [addr 03h] = 0Fh, [addr 06h] = 04h". If these five specific contents are all matched, scan upward every 4K (1000h) block, e.g. 0000h-00FFh, 1040h-10FFh, 2040h-20FFh, 3040h-30FFh, etc., to check whether 16 specific bytes (EC Base Signature) are within the leading 256 bytes of the 4K block.

Note that the 16 specific bytes are A5h, A5h, A5h, A5h, A5h, A5h, A5h, A5h, 85h, 12h, 5Ah, 5Ah, AAh, AAh, 55h, and 55h. Refer to section 7.1.10.7 Code snippet of EC Base Signature on page 159.

These 16 specific bytes must be located at 16-byte boundary, and the first byte A5h is equal to or greater than 40, e.g. xx40h, xx50h, … xxF0h, etc. If the contents mentioned above are all matched, the detection is finished and the base address of EC code will be fixed at flash address ([addr 45h] * 100000h + [addr 44h]} * 1000h).
For example, if [addr 45h] and [addr 44h] are 12h and 34h respectively, the base address of EC code will be fixed at flash address 234000h. If not all matched, then go to the next step (c).

(c) Scan upward every 4K block again to check whether the 16 specific bytes mentioned above are within the leading 256 bytes of the 4K block.
If all the 16 specific bytes are within one 4K block, the detection is finished and the base address of EC code will be fixed at the origin of the 4K block.
For example, if the 16 specific bytes are at flash address 2050h, the EC base address will be fixed at flash address 2000h.

(d) If the 16 bytes are not discovered after scanning all 4K blocks, the detection is also finished and the base address of EC code will be fixed at flash address 0000h.

Table 6-18. Corresponding Table of SPI Flash Power-on Detection

	Scanned Address or Scanned Range	Contents	If contents are matched, the base address of EC code will be fixed at:	Note
(a)	[addr 00h]	Jump Instruction (LJMP/SJMP/AJMP, or 02h/80h/xxx00001b)	Flash Address 00h	Detection is finished.
(b)	[addr 00h]	5Ah	Flash Address ([addr 45h] * 100000h + [addr 44h] * 1000h)	Detection is finished. The 16 specific bytes must be at 16-byte boundary, and the first byte A5h is at offset 0, e.g. xx40h, xx50h, … xxF0h, etc.
	[addr 01h]	A5h		
	[addr 02h]	F0h		
	[addr 03h]	0Fh		
	[addr 06h]	04h		
	Leading 256 bytes of every 4K (1000h) block (e.g. 0000h - 00FFh, 1040h - 10FFh, 2040h - 20FFh, etc.)	16 specific bytes: A5h, A5h, A5h, A5h, A5h, A5h, A5h, A5h, 85h, 12h, 5Ah, 5Ah, AAh, AAh, 55h, and 55h		
(c)	Leading 256 bytes of every 4K (1000h) block (e.g. 0000h - 00FFh, 1040h - 10FFh, 2040h - 20FFh, etc.)	16 specific bytes: A5h, A5h, A5h, A5h, A5h, A5h, A5h, A5h, 85h, 12h, 5Ah, 5Ah, AAh, AAh, 55h, and 55h	The origin of the matched 4K block. (All 16 specific bytes must be matched.)	Detection is finished. The 16 specific bytes must be at 16-byte boundary, and the first byte A5h is at offset 0.
(d)	All 4K blocks	The above contents are not matched.	Flash Address 0000h	Detection is finished.

6.3.4 EC Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for SMFI is 1000h.

These registers are listed below.

Table 6-19. EC View Register Map, SMFI

7 0	Offset
FBIU Configuration (FBCFG)	00h
Flash Programming Configuration Register (FPCFG)	01h
Flash EC Code Banking Select Register (FECBSR)	05h
Flash Memory Size Select Register (FMSSR)	07h
Shared Memory EC Control and Status (SMECCS)	20h
Shared Memory Host Semaphore (SMHSR)	22h
Flash Control Register 1 (FLHCTRL1R)	31h
Flash Control Register 2 (FLHCTRL2R)	32h
Reserved	33h
uC Control Register (UCCTRLR)	34h
Host Control 2 Register (HCTRL2R)	36h
EC-Indirect Memory Address Register 0 (ECINDAR0)	3Bh
EC-Indirect Memory Address Register 1 (ECINDAR1)	3Ch
EC-Indirect Memory Address Register 2 (ECINDAR2)	3Dh
EC-Indirect Memory Address Register 3 (ECINDAR3)	3Eh
EC-Indirect Memory Data Register (ECINDDR)	3Fh
Scratch SRAM 0 Address Low Byte Register (SCAR0L)	40h
Scratch SRAM 0 Address Middle Byte Register (SCAR0M)	41h
Scratch SRAM 0 Address High Byte Register (SCAR0H)	42h
Scratch SRAM 1 Address Low Byte Register (SCAR1L)	43h
Scratch SRAM 1 Address Middle Byte Register (SCAR1M)	44h
Scratch SRAM 1 Address High Byte Register (SCAR1H)	45h
Scratch SRAM 2 Address Low Byte Register (SCAR2L)	46h
Scratch SRAM 2 Address Middle Byte Register (SCAR2M)	47h
Scratch SRAM 2 Address High Byte Register (SCAR2H)	48h
Scratch SRAM 3 Address Low Byte Register (SCAR3L)	49h
Scratch SRAM 3 Address Middle Byte Register (SCAR3M)	4Ah
Scratch SRAM 3 Address High Byte Register (SCAR3H)	4Bh
Scratch SRAM 4 Address Low Byte Register (SCAR4L)	4Ch
Scratch SRAM 4 Address Middle Byte Register (SCAR4M)	4Dh
Scratch SRAM 4 Address High Byte Register (SCAR4H)	4Eh
Protect 0 Base Addr Register 0 (P0BA0R)	4Fh
Protect 0 Base Addr Register 1 (P0BA1R)	50h
Protect 0 Size Register (P0ZR)	51h
Protect 1 Base Addr Register 0 (P1BA0R)	52h
Protect 1 Base Addr Register 1 (P1BA1R)	53h
Protect 1 Size Register (P1ZR)	54h
Deferred SPI Instruction (DSINST)	55h
Deferred SPI Address 15-12 (DSADR1)	56h
Deferred SPI Address 23-16 (DSADR2)	57h
Host Instruction Control 1 (HINSTC1)	58h
Host Instruction Control 2 (HINSTC2)	59h
Host RAM Window Control (HRAMWC)	5Ah
Host RAM Window 0 Base Address [11:4] (HRAMW0BA[11:4])	5Bh
Host RAM Window 1 Base Address [11:4] (HRAMW1BA[11:4])	5Ch
Host RAM Window 0 Access Allow Size (HRAMW0AAS)	5Dh
Host RAM Window 1 Access Allow Size (HRAMW1AAS)	5Eh

6.3.4.1 FBIU Configuration Register (FBCFG)

The FBIU (Flash Bus Interface Unit) directly interfaces with the flash device. The FBIU also defines the access time to the flash base address from 00_0000h to 3F_FFFFh (4M bytes). EWR bit controls memory cycles on M-bus (flash interface).

Address Offset: 00h

Bit	R/W	Default	Description
7	-	0b	**Scratch SRAM Map Control (SSMC)** 0: Normal 1: Scratch SRAM No. 0, whose size is 2K bytes, is mapped into F800h-FFFFh in code space and overrides the settings in SCAR0H/SCAR0M/SCAR0L register. This bit is OBSOLETE and is only used to be compatible with old IT8510 firmware and should not be used in new firmware. Note that the following is the definition of this register field in IT8510. 0: Scratch RAM (data space). 1: Scratch ROM (code space).
6-2	-	0h	**Reserved**
1	-	-	**Reserved**
0	-	-	**Reserved**

6.3.4.2 Flash Programming Configuration Register (FPCFG)

This register provides general control on banking and flash standby.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	1b	**Banking Source Option (BSO)** 0: Use 8032 P1[0] and P1[1] as code banking source. 1: Use ECBB[1:0] in FECBSR register as code banking source. Using P1 as banking source has less instruction count since only "MOV" is invoked rather than "MOVX" although T2 and T2EX are used in other bits in P2.
6	R/W	Serial flash: 0b	**Auto Flash Standby (AFSTBY)** Serial flash: 1: Stop flash access in Idle/Doze/Sleep mode and issue "Deep Power Down (B9h)" instruction before entering Sleep mode and issue "Release Deep Power Down (ABh)" instruction after waking up from Sleep mode. See also section 6.3.3.14 Force 8032 to Code Fetch from Internal SRAM on page 75. 0: Prevent the flash from entering the standby mode
5	R/W	1b	**Reserved**
4	-	-	**Reserved**
3-0	R/W	11111b	**Reserved**

6.3.4.3 Flash EC Code Banking Select Register (FECBSR)

The register is used to select EC banking area Bank 0~3 when BSO =1 in FPCFG register.

Address Offset: 05h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**EC Banking Block (ECBB)** When ECBB is set to 00, EC code uses conventional code area (maximum 64k) as code memory. Common Bank 32k-byte flash mapping range is from 00_0000h to 00_7FFFh. Bank 0 32k-byte flash mapping range is from 00_8000h to 00_FFFFh. Bank 1 32k-byte flash mapping range is from 01_0000h to 01_7FFFh. Bank 2 32k-byte flash mapping range is from 01_8000h to 01_FFFFh. Bank 3 32k-byte flash mapping range is from 02_0000h to 02_7FFFh. See also Figure 3-1 on page 5. Bits 1-0: 00: Select Common Bank + Bank 0 01: Select Common Bank + Bank 1 10: Select Common Bank + Bank 2 11: Select Common Bank + Bank 3 If A15 of 8032 code memory equals to 0, select Common Bank, otherwise select Bank 0, 1, 2 or 3.

6.3.4.4 Flash Memory Size Select Register (FMSSR)

The register provides the selection for the external flash memory size.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	111111b	**Flash Memory Size Select (FMSS)** These bits select the external flash memory size. These bits only affect the host memory size "seen" by SouthBridge and don't affect address decoder in the EC side. See also Table 3-1. Host/Flash Mapping on page 6. If SouthBridge issues LPC Memory Cycles as memory transaction, this field has to be selected so as not to conflict with other memory devices on LPC bus. If SouthBridge issues FWH Cycles as memory transaction, there is no conflict issue since each FWH ID has its dedicated 4G memory space. **Bits** **543210 Memory Size (bytes)** 111111b: 4M 011111b: 2M 001111b: 1M 000111b: 512K 000011b: 256K 000001b: 128K Or 00h: 128K (2^17) 02h: 256K (2^18) 04h: 512K (2^19) 06h: 1M (2^20) 08h: 2M (2^21) 0Ah: 4M (2^22) 0Ch: 8M (2^23) 0Eh: 16M (2^24) 10h: 32M (2^25) 12h: 64M (2^26) 14h: 128M (2^27) 16h: 256M (2^28) Otherwise: Reserved

6.3.4.5 Shared Memory EC Control and Status Register (SMECCS)

The following set of registers is accessible only by the EC. The registers are applied to VSTBY.
This register provides the flash control and status of a restricted access.

Address Offset: 20h

Bit	R/W	Default	Description
7	R/W	0b	**Host Semaphore Interrupt Enable (HSEMIE)** It enables interrupt to 8032 via INT22 of INTC. 0: Disable the host semaphore (write) interrupt to the EC. 1: The interrupt is set (level high) if HSEMW bit is set.
6	R/WC	0b	**Host Semaphore Write (HSEMW)** 0: Host has not written to HSEM3-0 field in SMHSR register. 1: Host has written to HSEM3-0 field in SMHSR register. Writing 1 to this bit to clear itself and clear internal detect logic. Writing 0 has no effect.
5	R/W	0b	**Host Write Allow (HOSTWA)** This bit is for HLPC only. 0: The SMFI does not generate write transactions on M-bus. 1: The SMFI can generate write transactions on M-bus. The read performance on M-bus will be very poor for Host LPC if this bit is set.
4-3	R	01b	**Host Error Response (HERES)** These bits control response types on read/write translation from/to a protected address. 01b: Read back FFh; ignoring write Otherwise: Reserved
2	-	-	**Reserved**
1	-	-	**Reserved**
0	-	-	**Reserved**

6.3.4.6 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register is reset on host domain hardware reset.
This is the register the same as the one in section 6.3.5.6 but they are in different views.

Address Offset: 22h

Bit	R/W	Default	Description
7-4	R/W	0h	**EC Semaphore (CSEM3-0)** These four bits may be written by the EC and read by both the host and the EC
3-0	R	0h	**Host Semaphore (HSEM3-0)** These four bits may be written by the host and read by both the host and the EC.

6.3.4.7 Flash Control 1 Register (FLHCTRL1R)

Address Offset: 31h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	01b	**SPI Flash Read Mode (SPIFR)** For serial flash: 11b: Uses "Fast Read Dual Input/Output" cycle (instruction = BBh) 10b: Uses "Fast Read Dual Output" cycle (instruction = 3Bh) 01b: Uses "Fast Read" cycle (instruction = 0Bh) 00b: Uses "Read" cycle (instruction = 03h) The performance of "Read" cycle is better than "Fast Read" cycle in the same frequency since "Fast Read" cycle request 8 dummy clock ticks in each cycle. The attached must support "Fast Read" cycle since it's the default read instruction to serial flash.
3	R/W	1b	**Serial Wait 1T (LFSW1T)** For serial flash: Always write 1 to it.
2-0	-	-	**Reserved**

6.3.4.8 Flash Control 2 Register (FLHCTRL2R)

For serial flash only.

Address Offset: 32h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-0	R/W	011b	**FSCE# Min High Width (SCEMINHW)** 000b: 1T 001b: 2T 010b: 3T 011b: 4T 100b: 5T 101b: 6T 110b: 7T It depends on the "FSCE# High Time" on flash specification. Small value gets better performance. This register may needs to be modified before the PLL frequency is changed.

6.3.4.9 uC Control Register (UCCTRLR)

Address Offset: 34h

Bit	R/W	Default	Description
7	R/W	0b	**UC Burst Mode (UCBST)** 0: default 1: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. This bit can be modified only before VCC power is supplied.
6-3	-	-	**Reserved**
2-0	R/W	5h	**uC Burst Threshold (UCTH)** 5h: default 3h: for chipset that issues LPC Abort if LPC Long-wait count during a LPC Memory cycle is greater than 255. Otherwise: reserved. This field can be modified only before VCC power is supplied.

6.3.4.10 Host Control 2 Register (HCTRL2R)

Address Offset: 36h

Bit	R/W	Default	Description
7	R/W	1b	**Host Bridge Enable (HBREN)** 1: The host memory cycle is decoded 0: otherwise This bit can be modified only before VCC power is supplied.
6	R/W	0b	**Safe HLPC Bridge (SHBR)** 1: Host PCI clock is less than 33MHz. 0: otherwise It has the same affection as SLWPCI bit in MBCTRL register in the host side.
5	-	-	**Reserved**
4	-	-	**Reserved**
3	-	-	**Reserved**
2-0	-	-	**Reserved**

6.3.4.11 EC-Indirect Memory Address Register 0 (ECINDAR0)

Address Offset: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA7-0)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.3.4.12 EC-Indirect Memory Address Register 1 (ECINDAR1)

Address Offset: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA15-8)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.3.4.13 EC-Indirect Memory Address Register 2 (ECINDAR2)

Address Offset: 3Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**EC-Indirect Memory Address (ECINDA23-16)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.3.4.14 EC-Indirect Memory Address Register 3 (ECINDAR3)

Address Offset: 3Eh

Bit	R/W	Default	Description
7-4	R	Serial flash: 0000b	**EC-Indirect Memory Address (ECINDA31-28)** Read only.
3-0	R/W	0h	**EC-Indirect Memory Address (ECINDA27-24)** Define the EC-Indirect memory address when asserting a read/write cycle to EC-Indirect Memory Data Register (ECINDDR).

6.3.4.15 EC-Indirect Memory Data Register (ECINDDR)

Address Offset: 3Fh

Bit	R/W	Default	Description
7-0	R/W	-	**EC-Indirect Memory Data (ECINDD7-0)** Read/Write to this register will access one byte on the flash with the 32-bit flash address defined in ECINDAR3-0.

6.3.4.16 Scratch SRAM 0 Address Low Byte Register (SCAR0L)

Address Offset: 40h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A7-0)**

6.3.4.17 Scratch SRAM 0 Address Middle Byte Register (SCAR0M)

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 0 Address (SC0A15-8)**

6.3.4.18 Scratch SRAM 0 Address High Byte Register (SCAR0H)

Address Offset: 42h

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	**Reserved**
5-2	-	-	**Reserved**
1-0	R/W	11b	**Scratch SRAM 0 Address (SC0A17-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.3.4.19 Scratch SRAM 1 Address Low Byte Register (SCAR1L)

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 1 Address (SC1A7-0)**

6.3.4.20 Scratch SRAM 1 Address Middle Byte Register (SCAR1M)

Address Offset: 44h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 1 Address (SC1A15-8)**

6.3.4.21 Scratch SRAM 1 Address High Byte Register (SCAR1H)

Address Offset: 45h

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	**Reserved**
5-2	R/W	0h	**Reserved**
1-0	R/W	11b	**Scratch SRAM 1 Address (SC1A17-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.3.4.22 Scratch SRAM 2 Address Low Byte Register (SCAR2L)

Address Offset: 46h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 2 Address (SC2A7-0)**

6.3.4.23 Scratch SRAM 2 Address Middle Byte Register (SCAR2M)

Address Offset: 47h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 2 Address (SC2A15-8)**

6.3.4.24 Scratch SRAM 2 Address High Byte Register (SCAR2H)

Address Offset: 48h

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	**Reserved**
5-2	R/W	0h	**Reserved**
1-0	R/W	11b	**Scratch SRAM 2 Address (SC2A17-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.3.4.25 Scratch SRAM 3 Address Low Byte Register (SCAR3L)

Address Offset: 49h

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 3 Address (SC3A7-0)**

6.3.4.26 Scratch SRAM 3 Address Middle Byte Register (SCAR3M)

Address Offset: 4Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 3 Address (SC3A15-8)**

6.3.4.27 Scratch SRAM 3 Address High Byte Register (SCAR3H)

Address Offset: 4Bh

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	**Reserved**
5-2	R/W	0h	**Reserved**
1-0	R/W	11b	**Scratch SRAM 3 Address (SC3A17-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.3.4.28 Scratch SRAM 4 Address Low Byte Register (SCAR4L)

Address Offset: 4Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 4 Address (SC4A7-0)**

6.3.4.29 Scratch SRAM 4 Address Middle Byte Register (SCAR4M)

Address Offset: 4Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Scratch SRAM 4 Address (SC4A15-8)**

6.3.4.30 Scratch SRAM 4 Address High Byte Register (SCAR4H)

Address Offset: 4Eh

Bit	R/W	Default	Description
7	R/W	0b	**Next Start DMA (NSDMA)** If 1 is written to this bit, DMA will be started at the next writing.
6	-	-	**Reserved**
5-2	R/W	0h	**Reserved**
1-0	R/W	11b	**Scratch SRAM 4 Address (SC4A17-16)** The default value makes this scratch SRAM not be a scratch ROM.

6.3.4.31 Protect 0 Base Addr Register 0 (P0BA0R)

Address Offset: 4Fh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 0 Address (P0BA23-20)** The default value is uncertain.

6.3.4.32 Protect 0 Base Addr Register 1 (P0BA1R)

Address Offset: 50h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 0 Address (P0BA19-12)** The default value is uncertain.

6.3.4.33 Protect 0 Size Register (P0ZR)

Address Offset: 51h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 0 Mode (P0M)** It controls the protection mode of set 0. 00b: Read protection 01b: Write protection 10b: Read protection plus write protection 11b: Reserved
5-3	-	-	**Reserved**
2-0	R/W	0	**Protect 0 Size (P0Z)** If this field is zero, there is no memory block on SPI flash locked by "Protect 0" configuration. If this field is not zero, it means that read or write cycles from the host side to the specified SPI memory block is locked. The address defined by P0BA0R and P0BA1R is SPI physical address, not host LPC address. If write protection is enabled in P0M field, this size field must be equal to or greater than the allowed sector/block size of ERASE instruction. See also HINSTC2 register. In-System Programming Operation on page 335 is not affected by "Protect 0" configuration. 0: Disabled 1: The range is from (P0BA[23..12] << 12) to (P0BA[23..12] << 12) + ((1 << 12) - 1) and totally 2^12 (4K) bytes are locked. 2: The range is from (P0BA[23..13] << 13) to (P0BA[23..13] << 13) + ((1 << 13) - 1) and totally 2^13 (8K) bytes are locked. 3: The range is from (P0BA[23..14] << 14) to (P0BA[23..14] << 14) + ((1 << 14) - 1) and totally 2^14 (16K) bytes are locked. 4: The range is from (P0BA[23..15] << 15) to (P0BA[23..15] << 15) + ((1 << 15) - 1) and totally 2^15 (32K) bytes are locked. 5: The range is from (P0BA[23..16] << 16) to (P0BA[23..16] << 16) + ((1 << 16) - 1) and totally 2^16 (64K) bytes are locked. Otherwise: reserved

6.3.4.34 Protect 1 Base Addr Register 0 (P1BA0R)

Address Offset: 52h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	-	**Protect 1 Address (P1BA23-20)** The default value is uncertain.

6.3.4.35 Protect 1 Base Addr Register 1 (P1BA1R)

Address Offset: 53h

Bit	R/W	Default	Description
7-0	R/W	-	**Protect 1 Address (P1BA19-12)** The default value is uncertain.

6.3.4.36 Protect 1 Size Register (P1ZR)

Address Offset: 54h

Bit	R/W	Default	Description
7-6	R/W	00b	**Protect 1Mode (P1)** “Protect 1” configuration is the same as “Read Protect 0”.
5-3	-	-	**Reserved**
2-0	R/W	0	**Protect 1 Size (P1Z)** “Protect 1” configuration is the same as “Read Protect 0”.

6.3.4.37 Deferred SPI Instruction (DSINST)

Address Offset: 55h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Instruction (DSINST)** The 8-bit instruction code of deferred SPI WIP instruction.

6.3.4.38 Deferred SPI Address 15-12 (DSADR1)

Address Offset: 56h

Bit	R/W	Default	Description
7-4	R	-	**Deferred SPI Address 15-12 (DSA15-12)** The SPI address of deferred SPI WIP instruction.
3-0	-	-	**Reserved**

6.3.4.39 Deferred SPI Address 23-16 (DSADR2)

Address Offset: 57h

Bit	R/W	Default	Description
7-0	R	-	**Deferred SPI Address 23-16 (DSA23-16)** The SPI address of deferred SPI WIP instruction.

6.3.4.40 Host Instruction Control 1 (HINSTC1)

Address Offset: 58h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5-4	-	-	**Reserved**
3	W	-	**DISS Valid (DISSV)** Write 1: Write DISS bit in this register is valid. Write 0: Write DISS bit in this register is ignored. Only write 1 to this bit while INT59 is active.
2	R/W	-	**Deferred Instruction's Succeeding Step (DISS)** 1: Allow the deferred WIP instruction to be bridged to the flash. 0: Inhibit and discard the deferred WIP instruction. Writing to this bit and writing 1 to DISSV bit must be in the same write cycle, or this writing action to DISS bit is ignored.
1	R/W	0b	**Enable Deferring PROG Instruction (ENDPI)** HLPC: Enable deferring a PROG/AAI instruction in the Follow mode by returning Long-Waits and issuing INT59.
0	R/W	0b	**Enable Deferring ERASE Instruction (ENDEI)** HLPC: Enable deferring an ERASE instruction in the Follow mode by returning Long-Waits and issuing INT59.

6.3.4.41 Host Instruction Control 2 (HINSTC2)

This register is only valid when LPC hardware protection is enabled by setting P0ZR and P1ZR register.

Some SPI flashes provide two or more sector/block ERASE instructions, e.g. 4K and 64K ERASE instruction.
If one specified 4K block is set as hardware protection, it may be erased by 64K ERASE instruction.

To accomplish the hardware protectin on the SPI flash, the size defined in P0Z/P1Z field in P0ZR/P1ZR register must be equal to or greater than the allowed sector/block size of ERASE instruction.

For the above example, if an SPI flash provides the 4K ERASE instruction (code 20h) and 64K ERASE instruction (code D8h), the write protection can work well if the size defined in P0Z/P1Z field is equal to or greater than 64K; otherwise, the 64K ERASE instruction should be inhibited by setting DISEID8 bit.

Address Offset: 59h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3	R/W	0b	**Disable Erase Instruction D8h (DISEID8)** Erase sector/block instruction D8h will be inhibited.
2	R/W	0b	**Disable Erase Instruction D7h (DISEID7)** Erase sector/block instruction D7h will be inhibited.
1	R/W	0b	**Disable Erase Instruction 52h (DISEI52)** Erase sector/block instruction 52h will be inhibited.
0	R/W	0b	**Disable Erase Instruction 20h (DISEI20)** Erase sector/block instruction 20h will be inhibited.

6.3.4.42 Host RAM Window Control (HRAMWC)

Address Offset: 5Ah

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	-	-	**Reserved**
3-2	-	-	**Reserved**
1-0	R/W	0b	**H2RAM Window 0/1 Enable (H2RAMWE)** 00b: Disabled 01b: Window 0 enabled 10b: Window 1 enabled 11b: Both enabled

6.3.4.43 Host RAM Winodw 0 Base Address [11:4] (HRAMW0BA[11:4])

Address Offset: 5Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Host RAM Window 0 Base Address Bits [11:4] (HRAMW0BA[11:4])** Define RAM window 0 base address.

6.3.4.44 Host RAM Window 1 Base Address [11:4] (HRAMW1BA[11:4])

Address Offset: 5Ch

Bit	R/W	Default	Description
0	R/W	00h	**Host RAM Window 1 Base Address Bits [11:4] (HRAMW1BA[11:4])** Define RAM window 1 base address.

6.3.4.45 Host RAM Window 0 Access Allow Size (HRAMW0AAS)

Address Offset: 5Dh

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 0 Read Protect Enable (HRAMW0RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 0 Write Protect Enable (HRAMW0WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 0 Size (HRAMW0S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.3.4.46 Host RAM Window 1 Access Allow Size (HRAMW1AAS)

Address Offset: 5Eh

Bit	R/W	Default	Description
7-6	R/W	0h	**Host RAM Window 1 Read Protect Enable (HRAMW1RPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
5-4	R/W	0h	**Host RAM Window 1 Write Protect Enable (HRAMW1WPE)** 00b: Disabled 01b: Lower half of RAM window protected 10b: Upper half of RAM window protected 11b: All protected
3	-	-	**Reserved**
2-0	R/W	0h	**Host RAM Window 1 Size (HRAMW1S)** 0h: 16 bytes 1h: 32 bytes 2h: 64 bytes 3h: 128 bytes 4h: 256 bytes 5h: 512 bytes 6h: 1024 bytes 7h: 2048 bytes

6.3.5 Host Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor.
The SMFI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SMFI logical device number is 0Fh (LDN=0Fh).
These registers are listed below

Table 6-20. Host View Register Map, SMFI

7	0	Offset
Shared Memory Indirect Memory Address (SMIMAR0-3)		00h-03H
Shared Memory Indirect Memory Data (SMIMDR)		04h
Shared Memory Host Semaphore (SMHSR)		0Ch
M-Bus Control Register (MBCTRL)		0Fh

6.3.5.1 Shared Memory Indirect Memory Address Register 0 (SMIMAR0)

The following set of registers is accessible only by the host. The registers are applied to VCC.
This register defines the addresses 7-0 for a read or write transaction to the memory.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR7-0)**

6.3.5.2 Shared Memory Indirect Memory Address Register 1 (SMIMAR1)

This register defines the addresses 15-8 for a read or write transaction to the memory.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR15-8)**

6.3.5.3 Shared Memory Indirect Memory Address Register 2 (SMIMAR2)

This register defines the addresses 23-16 for a read or write transaction to the memory.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR23-16)**

6.3.5.4 Shared Memory Indirect Memory Address Register 3 (SMIMAR3)

This register defines the addresses 31-24 for a read or write transaction to the memory.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR31-24)**

6.3.5.5 Shared Memory Indirect Memory Data Register (SMIMDR)

This register defines the Data bits 7-0 for a read or write transaction to the memory.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Data (IMDA7-0)**

6.3.5.6 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register reset on host domain hardware reset.
This is the register the same as the one in section 6.3.4.9 on page 84 but they are in different views.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-4	R	0h	**EC Semaphore (CSEM3-0)** Four bits that may be updated by the EC and read by both the host and the EC.
3-0	R/W	0b	**Host Semaphore (HSEM3-0)** Four bits that may be updated by the host and read by both the host and the EC.

6.3.5.7 M-Bus Control Register (MBCTRL)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	0b	**Slow PCI Clock Register (SLWPCI)** 1: Host PCI clock is less than 33MHz. 0: otherwise It has the same affection as SHBR bit in HCTRL2R register in EC side.

6.4 System Wake-Up Control (SWUC)

6.4.1 Overview

SWUC detects wakeup events and generate SCI#, SMI# and PWUREQ# signals to the host side, or alert EC by interrupts to WUC.

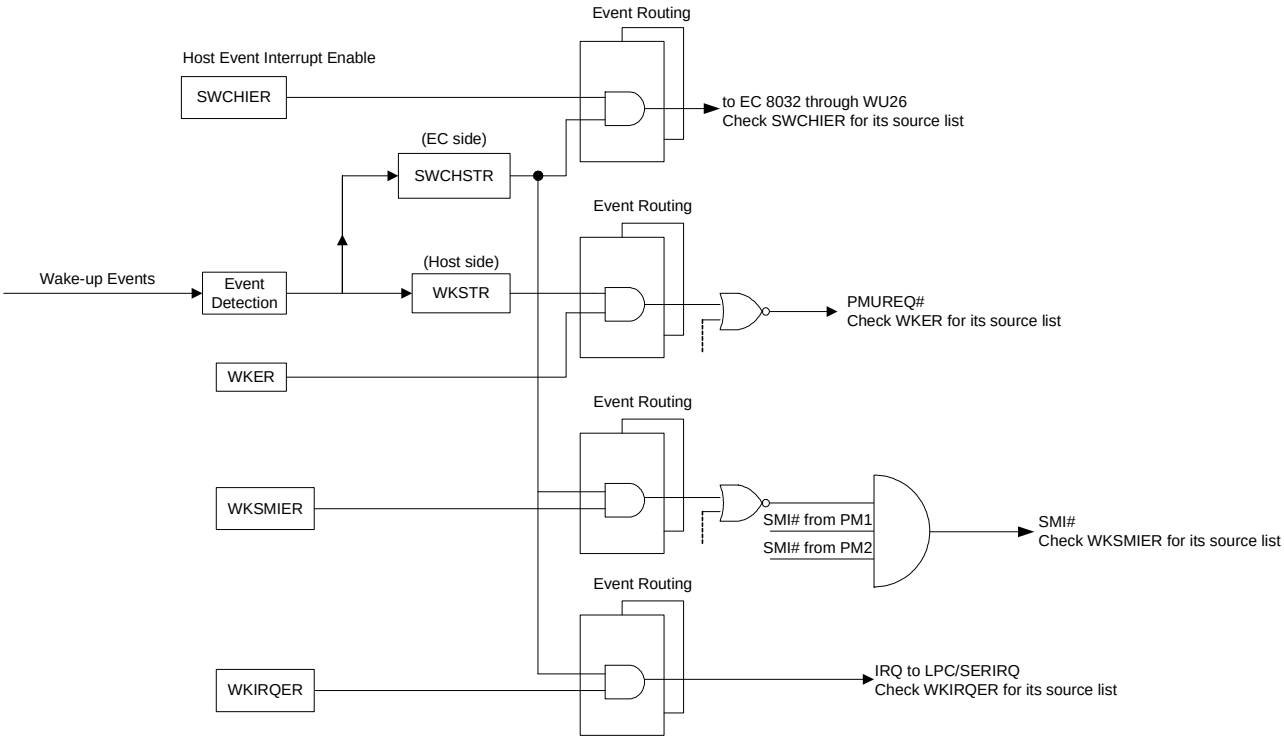
6.4.2 Features

- Supports programmable wake-up events source from the host controlled modules.
- Generates SMI# or PWUREQ# interrupt to host to wake-up system.

6.4.3 Functional Description

The wakeup event and gathering scheme is shown in Figure 6-6. Wakeup Event and Gathering Scheme on page 95.

Figure 6-6. Wakeup Event and Gathering Scheme



6.4.3.1 Wake-Up Status

When the wake up event is detected, the related status bit is set to 1 in both host and EC status registers, no matter whether any event enable bits are set or not. A status bit is cleared by writing 1 to it. Writing 0 to a status bit does not change its value. Clearing the event enable bit does not affect the status bit, but prevents it from issuing an event to output. The host uses a mask register (WKSMIER) to decide what the status bits will respond to.

6.4.3.2 Wake-Up Events

When a wake up event is detected, it is recorded on a status bit in WKSTR (host view) register and SWCHSTR register (EC view), regardless of the enabled bit. Each event behavior is determined by a wake up control logic controlled by a set of dedicated registers.

Input events are detected by the SWUC shown as follows:
- Module IRQ Wake up Event
- Modem Ring (RI1 and RI2)
- Telephone Ring (RING input)
- Software event
- Legacy off event
- ACPI state change Event

Module IRQ Wake-Up Event
A module IRQ wake-up event from each logical device is asserted when the leading edge of the module IRQ is detected.
The related enable bit (WKIRQEN) has to be set to 1 to enable and trigger a wake-up event. Refer to the IRQNUM and WKIRQEN fields in IRQNUMX register. When the event is detected, MIRQ bit in WKSTR register is set to 1. If MIRQE in WKER register is also set to 1, the PWUREQ# output is still asserted and until the status bit is cleared.

Modem Ring
If transitions form high to low on RI1# (or RI2#) is detected on the Serial Port 1 connected to a modem, and then when the signal goes high on RI1#(or RI2#), it will cause a ring wake-up event asserted if the RI1#(or RI2#) event enable bit is set 1 in the WKER register (bit0 for RI1#, and bit1 for RI2#).

Telephone Ring
If transitions form high to low on the Ring input pin, and then when the signal goes high on Ring input pin. It will cause a ring wake-up event asserted when the ring event enable bit is set 1 in the WKER register (BIT3).

Software Event
This bit may trigger a wake event by software control. When the SIRQS (Software IRQ Event Status bit) in WKSTR register is set, a software event to the host is active. When the SIRQS bit in SWCHSTR register is set, a software event to the EC is active. The software event may be activated by the EC via access to the Host Controlled Module bridge regardless of the VCC status.
The SIRQS bit in SWCHSTR may be set when the respective bit toggles in WKSTR from 0 to 1 and when HSECM=0 is in SWCTL1 register. When HSECM =1 t, the SIRQS bit in SWCHSTR is set on a write of a 1 to the respective bit in WKSTR. The SIRQS bit in SWCHSTR is cleared by writing 1 to it.

Legacy Off Events
The host supports either legacy or ACPI mode. The operation mode is assigned on PWRBTN bit in the Super I/O Power Mode Register (SIOPWR). When EISCRDPBM bit in SWCIER register is set, any change in this bit will generate an interrupt to the EC. The EC may read this bit, using SCRDPBM bit in SWCTL2 register, to determine the other power state. In the legacy mode, the PWRSLY bit in SIOPWR register represents a turn power off request. When this bit is set and SCRDPSO bit in SWCTL2 register is set, an interrupt is generated to EC if EISCRDPSO bit in SWCIER register is also set.

ACPI State Change Events
The bits (S1-S5) in WKACPIR register are used to provide a set of 'system power state change request'. The host uses these bits to issue an ACPI state change request. A write of 1 to any of these bits represents a state change request to the EC, the request may be also read out in SWCTL2 register even S0 is represented when all bits in WKACPI is cleared to 0. When any of S0-S5 bits in SWCTL2 is set and the respective mask bit in SWCIER register is set, an interrupt is generated to EC. All interrupt outputs may be cleared either writing 1 to the status bit or clearing the masking interrupt enable register.

6.4.3.3 Wake-Up Output Events

The SWUC output four types of wake up events:
IRQ Interrupt through SERIRQ to host side, which is activated by SWUC logical device of

PNPCFG.
PWUREQ# Routing as an SCI event.
SMI# Routing as an SMI event.
WU26 An interrupt to the WUC module in the EC domain which is handled by EC firmware.

Output events are generated to host when their status bit is set (1 in WKSTR). Output event to the EC through the WUC is generated when their EC status bit is set (1 in SWCHSTR). The host can program three Event Routing Control registers (WKSTR, WKSMIER and WKIRQER) to handle each of the host events to be asserted. This allows selective routing of these events output to PWUREQ#, SMI# and/or SWUC interrupt request (IRQ). After an output event is asserted, it can be cleared either by clearing its status bit or being masked. The current status of the event may be read out at the Wake-Up Event Status Register(WKSTR), and Wake-Up Signals Monitor Register (WKSMR). The SWUC also handles the wake up event coming from the PMC 1 and 2 for SMI# event. In the EC domain, Wake-Up Event Interrupt Enable register (SWCHIER) holds an enable bit to allow selective routing of the event to output the EC wake-up interrupt (WU26) to the WUC.

6.4.3.4 Other SWUC Controlled Options

Additionally, the SWUC handles the following system control signals:
Host Keyboard Reset (KBRST#)
GA20 Signal
Host Configuration Address Option

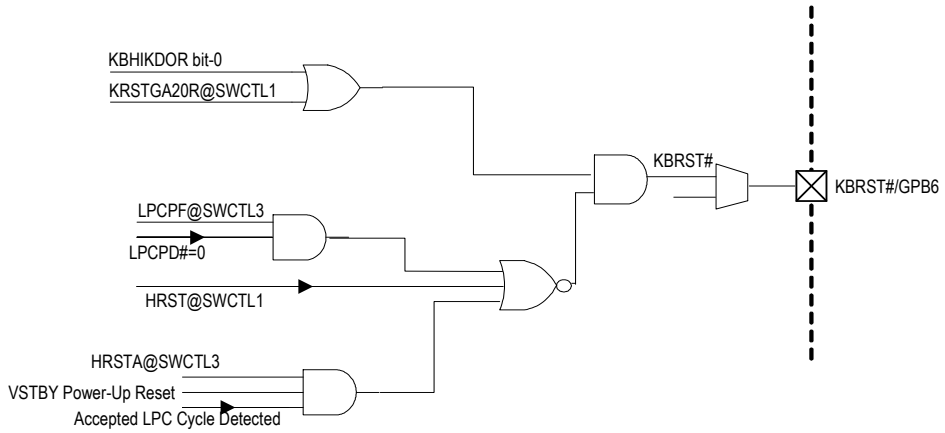
- **Host Keyboard Reset (KBRST#)**

The Host Keyboard Reset output (KBRST#) can be asserted either by software or hardware:
Software: KBRST# will be asserted when the EC firmware issues a reset command by writing 1 to HRST in SWCTL1 register. Clear this bit to de-assert the KBRST#.
Hardware: KBRST# will be asserted during VSTBY Power-Up reset if HRAPU bit in SWCTL3 register is set and an LPC transaction is started.

The KBRST# signal will be active in the following conditions:
(1) HRSTA bit in the SWUC is enabled and LPC cycle is active when the VSTBY is power-on.
(2) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(3) HRST bit in the SWUC is enabled.
(4) Bit 0 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The KBRST# output scheme is shown in Figure 6-7 on page 97.
Note it is another way to use GPIO output function to send KBRST# signal.

Figure 6-7. KBRST# Output Scheme



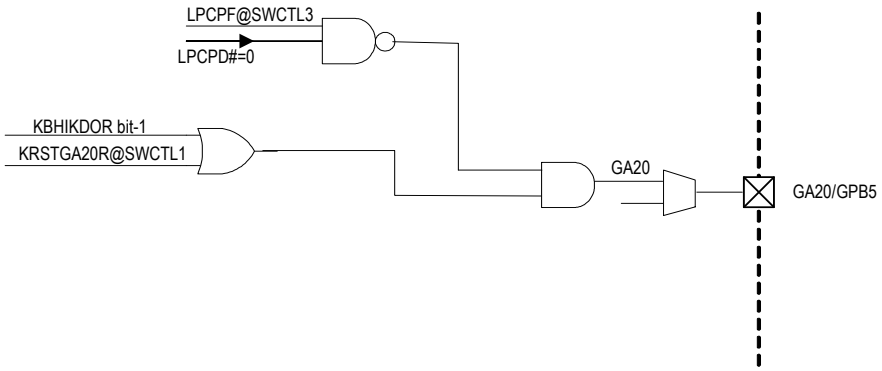
- **GA20 Signal**

In the chip, the GA20 is connected to a GPIO signal that is configured as output. Port GPB5 is recommended to be used as GA20 since its initial state is output driving high.
EC can assert the GA20 signal state by
1. modifying GPB5 in GPIO register
2. writing 1 to LPCPF in SWCTL3 register and GA20 signal will be asserted while LPCPD# signal is active.

The GA20 signal will be active in the following conditions:
(1) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(2) Bit-1 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The GA20 output scheme is shown in Figure 6-8 on page 98.
Note it is another way to use GPIO output function to send GA20 signal.

Figure 6-8. GA20 Output Scheme



- **Host Configuration Address Option**

The contents of SWCBAHR and SWCBALR change only during VSTBY Power -Up reset. To update the base address of the PNPCFG registers, refer to the followings:
1. Clear HCAV bit in SWCTL1 register by writing 1 to it.
2. Write the lower byte of the address to SWCBALR (LSB has to be cleared).
3. Write the higher byte of the address to SWCBAHR.
4. Set HCAL bit to prevent the unintended change in the SWCBALR and SWCBAHR register.

6.4.4 Host Interface Registers

The registers of SWUC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor.
SWUC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SWUC logical device number is 04h (LDN=04h).
SWUC host interface registers are battery-backed. These registers are listed below.

Table 6-21. Host View Register Map, SWUC

7	0	Offset
Wake-Up Event Status Register (WKSTR)		00h
Wake-Up Enable Register (WKER)		02h
Wake-Up Signals Monitor Register (WKSMR)		06h
Wake-Up ACPI Status Register (WKACPIR)		07h
Wake-Up SMI Enable Register (WKSMIER)		13h
Wake-Up Interrupt Enable Register (WKIRQER)		15h

6.4.4.1 Wake-Up Event Status Register (WKSTR)

The register is used to monitor the status of wake-up events. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming the HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0 and writing 1 to this bit, the value of this bit will be inverted. When HSECM=1 and writing 1 to this bit, the bit is set to 1. The bit will be cleared when the SIRQS bit in SWUC Host Event Status Register (SWCHSTR) is written to 1. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved.**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.4.4.2 Wake-Up Event Enable Register (WKER)

The register is used to enable the individual wake-up events to generate PWUREQ# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQE)** 0: Disable. 1: Enable.
6	R/W	0b	**Software IRQ Event Enable (SIRQE)** 0: Disable. 1: Enable.
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2E)** 0: Disable. 1: Enable.
0	R/W	0b	**RI1# Event Enable (RI1E)** 0: Disable. 1: Enable.

6.4.4.3 Wake-Up Signals Monitor Register (WKSMR)

The register is used to monitor the value of the SMI# and PWUREQ# signals and identify the generated source. This register is a read-only register.

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R	0b	**PWUREQ# Output from SWUC (PWUREQOS)** 0: PWUREQ# output from SWUC is low. 1: PWUREQ# output from SWUC is high.
4	R	0b	**PWUREQ# Signal Status (PWUREQS)** 0: PWUREQ# signal is low. 1: PWUREQ# signal is high.
3	R	0b	**SMI# Output from PMC2 (PM2SMI)** 0: SMI# output from PM channel 2 is low. 1: SMI# output from PM channel 2 is high.
2	R	0b	**SMI# Output from PMC1 (PM1SMI)** 0: SMI# output from PM channel 1 is low. 1: SMI# output from PM channel 1 is high.
1	R	0b	**SMI# Output from SWUC (SWCSMI)** 0: SMI# output from SWUC is low. 1: SMI# output from SWUC is high.
0	R	0	**SMI# Signal Status (SMIS)** 0: SMI# signal is low. 1: SMI# signal is high.

6.4.4.4 Wake-Up ACPI Status Register (WKACPIR)

The register is used to monitor the status of ACPI. When this register is read, its value always returns 00h.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5	R/W	0b	**Change to S5 State (S5)** The host uses this bit to request the EC to change the ACPI S5 state. 0: Not request to change S5 state. 1: Request to change S5 state.
4	R/W	0b	**Change to S4 State (S4)** The host uses this bit to request the EC to change the ACPI S4 state. 0: Not request to change S4 state. 1: Request to change S4 state.
3	R/W	0b	**Change to S3 State (S3)** The host uses this bit to request the EC to change the ACPI S3 state. 0: Not request to change S3 state. 1: Request to change S3 state.
2	R/W	0b	**Change to S2 State (S2)** The host uses this bit to request the EC to change the ACPI S2 state. 0: Not request to change S2 state. 1: Request to change S2 state.
1	R/W	0b	**Change to S1 State (S1)** The host uses this bit to request the EC to change the ACPI S1 state. 0: Not request to change S1 state. 1: Request to change S1 state.
0	R	0b	**Reserved**

6.4.4.5 Wake-Up SMI Enable Register (WKSMIER)

The register is used to enable the individual wake-up events to generate SMI# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 13h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to SMI Enable (SSMIE)** 0: Disable. 1: Enable.
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to SMI Enable (RINGSMIE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to SMI Enable (RI2SMIE)** 0: Disable. 1: Enable.
0	R/W	0b	**RI1# Event to SMI Enable (RI1SMIE)** 0: Disable. 1: Enable.

6.4.4.6 Wake-Up IRQ Enable Register (WKIRQER)

The register is used to enable the individual wake-up events to generate the interrupt signal that is assigned by SWUC. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 15h

Bit	R/W	Default	Description
7	R/W	0b	**Reserved**
6	R/W	0b	**Software IRQ Event to IRQ Enable (SIRQE)** 0: Disable. 1: Enable.
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event to IRQ Enable (RINGIRQE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event to IRQ Enable (RI2IRQE)** 0: Disable. 1: Enable.
0	R/W	0b	**RI1# Event to IRQ Enable (RI1IRQE)** 0: Disable. 1: Enable.

6.4.5 EC Interface Registers

The registers of SWUC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for SWUC is 1400h.
These registers are listed below.

Table 6-22. EC View Register Map, SWUC

7	0	Offset
SWUC Control Status 1 Register (SWCTL1)		00h
SWUC Control Status 2 Register (SWCTL2)		02h
SWUC Control Status 3 Register (SWCTL3)		04h
SWUC Host Configuration Base Address Low Byte Register (SWCBALR)		08h
SWUC Host Configuration Base Address High Byte Register (SWCBAHR)		0Ah
SWUC Interrupt Enable Register (SWCIER)		0Ch

7	0	Offset
SWUC Host Event Status Register (SWCHSTR)		0Eh
SWUC Host Event Interrupt Enable Register (SWCHIER)		10h

6.4.5.1 SWUC Control Status 1 Register (SWCTL1)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up. Bit 0 is only cleared when the warm reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1b	**KB Reset/GA20 Routing (KRSTGA20R)** 0: Enable routing bit-0 of KBHIKDOR as KBRST# source Enable routing bit-1 of KBHIKDOR as GA20 source 1: Disable above
6	R/W	0b	**Reserved**
5	R/W	0b	**Host Software Event Clear Mode (HSECM)** This bit is used to control the clear mode of SIRQS bit at the Wake-Up Event Status Register (WKSTR).
4	R/W	0b	**Host Configuration Address Lock (HCAL)** When the bit is written to 1, the Host Configuration Address and the bit will be locked. The bit is only cleared at the following condition: VSTBY power-up or watchdog reset.
3	R/WC	0b	**Host Configuration Address Valid (HCAV)** This bit is set after writing SWCBAHR register. 1: Indicate Host Configuration Base Address stored in SWCBALR and SWCBAHR registers are valid. 0: SWCBALR and SWCBAHR registers are not valid. The bit can be cleared by writing to 1.
2	R	0b	**LPC Reset Active (LPCRST)** 0: LPCRST# is inactive. 1: LPCRST# is active.
1	R	-	**VCC Power On (VCCPO)** 0: VCC is power-off. 1: VCC is power-on. See also VCCDO bit in RSTS register in 7.15.4.5 on page 300.
0	R/W	-	**Host Reset Active (HRST)** When this bit is 1, the KBRST# is active to generate one host software reset.

6.4.5.2 SWUC Control Status 2 Register (SWCTL2)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up and LPCRST# is active.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/WC	0b	**Super I/O Configuration SIOPWR Power Supply Off (SCRDPSO)** The bit is used to monitor the Power Supply Off (PWRSLY) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the bit and the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.
6	R/WC	0b	**Super I/O Configuration SIOPWR Power Button Mode (SCRDPBM)** The bit is used to monitor the Power Button Mode (PWRBTN) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the interrupt signal caused by the value change in this bit. A write of 0 to this bit is ignored.
5-1	R/WC	00000b	**ACPI request S5-1 (ACPIRS5-1)** These bits are used to monitor the S5-1 bit at the Wake-Up ACPI Status Register (WKACPIR). When the bit is written to 1, clear the bit and the interrupt signal caused by ACPI. A write of 0 to this bit is ignored.
0	R/WC	0b	**ACPI request S0 (ACPIRS0)** If all S5-1 bits at the WKACPIR are written to 0, the bit will be set to 1. The bit will be cleared if the bit is written to 1.

6.4.5.3 SWUC Control Status 3 Register (SWCTL3)

The register is used to control the individual wake-up action on SWUC. The register will only be cleared when the VSTBY power is power-up.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	R	00h	**Reserved**
2	-	-	**Reserved**
1	R/W	0b	**LPC Power Fail Turn Off KBRST# and GA20 (LPCPF)** If the bit is set to 1, the KBRST# and GA20 will be forced to low when the LPCPD# signal is active.
0	R/W	1b	**Host Reset Active During VSTBY Power-Up (HRSTA)** If the bit is set to 1, the KBRST# signal will be active when the LPC cycle is active until VSTBY Power-Up Reset is finished. Writing to this bit is ignored if HCAL bit is set.

6.4.5.4 SWUC Host Configuration Base Address Low Byte Register (SWCBALR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-2 on page 42 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address Low Byte (BALB)**

6.4.5.5 SWUC Host Configuration Base Address High Byte Register (SWCBAHR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-2 on page 42 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address High Byte (BAHB)**

6.4.5.6 SWUC Interrupt Enable Register (SWCIER)

The register is used to enable the individual interrupt source on SWUC. The interrupt can be cleared by clearing the status bit or masking the source. On the other hand, the register will be cleared when the warm reset is active.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Supply Off (EISCRDPSO)** 1: Generate high-level interrupt when the SCRDPSO bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
6	R/W	0b	**Enable Interrupt from Super I/O Configuration SIOPWR Power Button Mode (EISCRDPBM)** 1: Generate high-level interrupt when the SCRDPBM bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
5-1	R/W	00000b	**Enable Interrupt from ACPI Request S5-1 (EIACPIRS5-1)** 1: Generate high-level interrupt when the ACPIRS5-1 bit in SWUC Control Status 2 Register (SWCTL2) is changed. 0: Disable the interrupt source.
0	-	-	**Reserved**

6.4.5.7 SWUC Host Event Status Register (SWCHSTR)

The information of this register is mirror as the Wake-Up Event Status Register (WKSTR). The status bits can be cleared by writing to the corresponding bit in the two registers. The register will be cleared when the VSTBY power is power-up, or the host software reset occurs.

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/WC	0b	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0b	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0, this bit is set to 1 when SIRQS toggles to 1 in WKSTR register. When HSECM=1 and this bit is set to 1 while writing 1 to SIRQS in WKSTR register. This bit will be cleared by writing 1 to it. 0: Event is not active. 1: Event is active.
5-4	R	00b	**Reserved**
3	R/WC	0b	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	0b	**Reserved**
1	R/WC	0b	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0b	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.4.5.8 SWUC Host Event Interrupt Enable Register (SWCHIER)

The register is used to enable the individual wake-up events to generate one interrupt to the EC 8032 via WU26 of WUC. The register will be cleared when the warm reset occurs.

Address Offset: 10h

Bit	R/W	Default	Description
7	R/W	0b	**Module IRQ Event Enable (MIRQEE)** 0: Disable. 1: Enable.
6	R/W	0b	**Software IRQ Event Enable (SIRQEE)** 0: Disable. 1: Enable.
5-4	R	00b	**Reserved**
3	R/W	0b	**RING# Event Enable (RINGEE)** 0: Disable. 1: Enable.
2	R	0b	**Reserved**
1	R/W	0b	**RI2# Event Enable (RI2EE)** 0: Disable. 1: Enable.
0	R/W	0b	**RI1# Event Enable (RI1EE)** 0: Disable. 1: Enable.

6.5 Keyboard Controller (KBC)

6.5.1 Overview

This Keyboard Controller supports a standard keyboard and mouse controller interface.

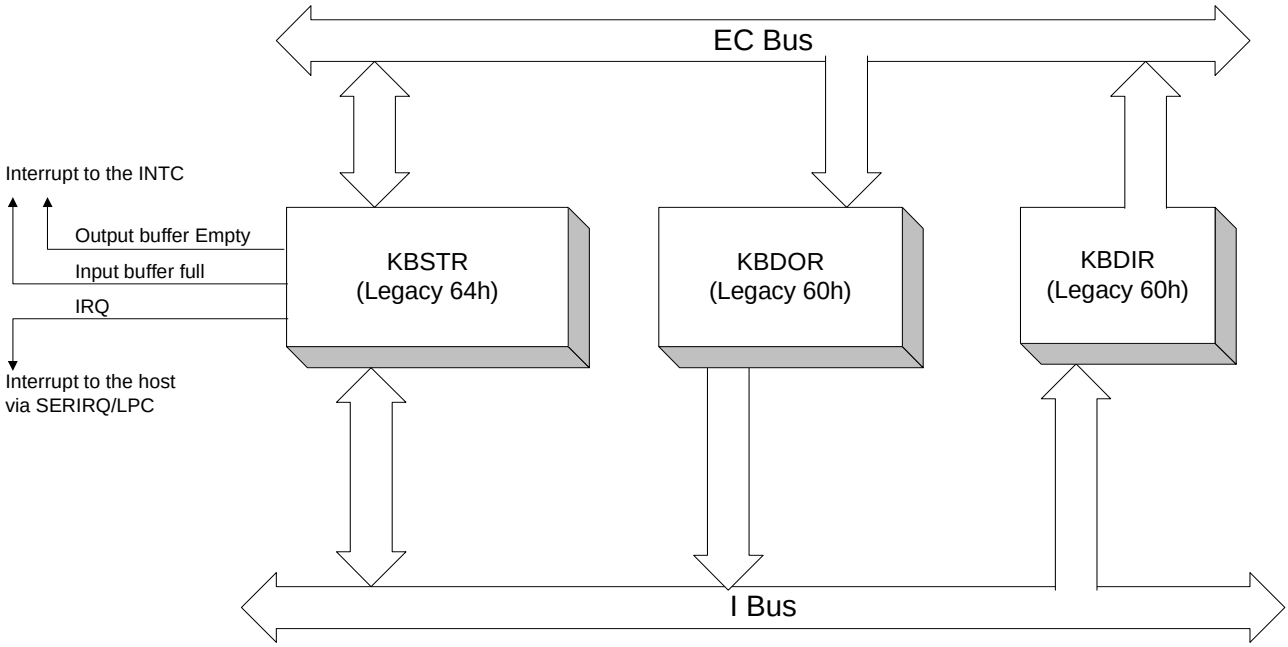
6.5.2 Features

- Compatible with the legacy 8042 interface keyboard controller.
- Supports two standard registers for programming: Command/Data Register and Status Register.
- Automatically generates interrupts to the host side and EC side when the KBC status is changed.

6.5.3 Functional Description

This Keyboard Controller is compatible with the legacy 8042 interface keyboard controller.

Figure 6-9. KBC Host Interface Block Diagram



Status

The host processor can read the status of KBC from the KBC Status Register. The internal 8032 can read the status of KBC from the KBC Host Interface Keyboard/Mouse Status Register.

Host Write Data to KBC Interface

When writing to address 60h or 64h (programmable), the IBF bit in the KBC Status Register is set and A2 bit in the KBC Status Register indicates 8032 whose address was written. When writing to address 60h, A2 bit is 0. When writing to address 64h, A2 bit is 1.

EC 8032 can identify that the input buffer is full by either polling IBF bit in the Status register or detecting an interrupt (INT24) if the interrupt is enabled. EC 8032 can read the data from the KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR), and the IBF bit in the Status Register is cleared.

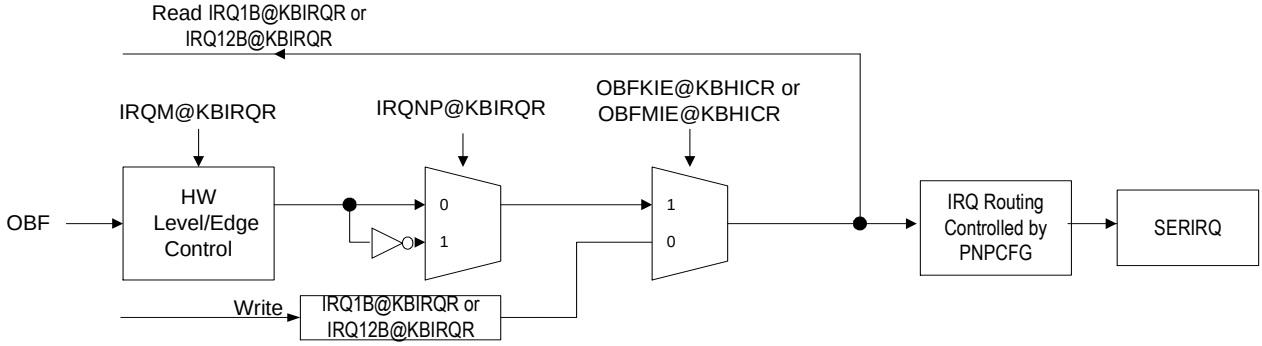
EC 8032 Write Data to KBC Interface

EC 8032 can write data to the KBC when it needs to send data to the host. When EC 8032 writes data to the KBC Host Interface Keyboard Data Output Register (KBHIKDOR), the OBF bit in the Status Register is set. If the IRQ1 interrupt is enabled, the IRQ1 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When EC 8032 writes data to the KBC Host Interface Mouse Data Output Register (KBHIMDOR), the OBF bit in the Status Register is set. If the IRQ12 interrupt is enabled, the IRQ12 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When the Output Buffer Empty interrupt to INTC (INT2) is enabled,

the interrupt signal is set high if the output buffer is empty.

Interrupts
There are two interrupts (Input Buffer Full Interrupt and Output Buffer Empty) connected to the INTC.
There are two interrupts (IRQ1 and IRQ12) connected to the host side (SERIRQ).
The IRQ numbers of KBC are programmable and use IRQ1 and IRQ12 as abbreviations in this section.

Figure 6-10. IRQ Control in KBC Module



GA20 and KBRST#
Refer to section 6.4.3.4 on page 97.

6.5.4 Host Interface Registers

The registers of KBC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The KBC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The KBC/Keyboard logical device number is 06h (LDN=06h) and the KBC/Mouse logical device number is 05h (LDN=05h). For compatibility issue, the two I/O Port Base Addresses of KBC/Keyboard are suggested to configure at 60h and 64h.

These registers are listed below.

Table 6-23. Host View Register Map, KBC

7 ... 0	Offset
KBC Data Input Register (KBDIR)	Legacy 60h
KBC Data Output Register (KBDOR)	Legacy 60h
KBC Command Register (KBCMDR)	Legacy 64h
KBC Status Register (KBSTR)	Legacy 64h

Legacy 60h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 64h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-3 on page 42.

6.5.4.1 KBC Data Input Register (KBDIR)

When the host processor is writing this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be cleared. If the IBFCIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the write action will cause one interrupt to 8032 processor via INT24 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	W	-	**KBC Data Input (KBDI)** The data is used to output for Keyboard/Mouse.

6.5.4.2 KBC Data Output Register (KBDOR)

When the host processor is reading this register, The OBF bit in KBC Status Register (KBSTR) will be cleared. The reading access will also clear the interrupt for host processor when the IRQM bits of KBC Interrupt Control Register (KBIRQR) are programmed to be at level mode. If the OBECIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the read action will cause one interrupt to 8032 processor via INT2 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	R	-	**KBC Data Output (KBDO)** The data comes from the Keyboard/Mouse source.

6.5.4.3 KBC Command Register (KBCMDR)

When the register is written, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be set.

Address Offset: 00h for I/O Port Base Address 1, Legacy 64h

Bit	R/W	Default	Description
7-0	W	-	**KBC Command (KBCMD)** The command data is used to output for Keyboard/Mouse.

6.5.4.4 KBC Status Register (KBSTR)

The host processor uses the register to monitor the status of KBC. The same information is similar to the KBC Host Interface Keyboard/Mouse Status Register (KBHISR). It is used by the internal 8032.

Address Offset: 01h for I/O Port Base Address 0, Legacy 64h

Bit	R/W	Default	Description
7-4	R	0h	**Programming Data 3-0 (PD3-0)** The data is used by the 8032 firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the last write operation that the host processor accessed the KBC.
2	R	0b	**Programming Data II (PDII)** The function is the same as the PD3-0.
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when the KBDIR or KBCMDR is read by the 8032 firmware.
0	R	0b	**Output Buffer Full (OBF)** When the EC 8032 is writing data to KBDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host processor.

6.5.5 EC Interface Registers

The registers of KBC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for KBC is 1300h.

These registers are listed below

Table 6-24. EC View Register Map, KBC

7	0	Offset
KBC Host Interface Control Register (KBHICR)		00h
KBC Interrupt Control Register (KBIRQR)		02h
KBC Host Interface Keyboard/Mouse Status Register (KBHISR)		04h
KBC Host Interface Keyboard Data Output Register (KBHIKDOR)		06h
KBC Host Interface Mouse Data Output Register (KBHIMDOR)		08h
KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)		0Ah

.

6.5.5.1 KBC Host Interface Control Register (KBHICR)

Address Offset: 00h

Bit	R/W	Default	Description
7	R	0b	**Reserved**
6	R/W	0b	**PM Channel 1 Input Buffer Full 8032 Interrupt Enable (PM1ICIE)** The bit is used to enable the interrupt to 8032 for PM channel 1 when the input buffer is full via INT25 of INTC.
5	R/W	0b	**PM Channel 1 Output Buffer Empty 8032 Interrupt Enable (PM1OCIE)** The bit is used to enable the interrupt to 8032 for PM channel 1 when the output buffer is empty via INT3 of INTC.
4	R/W	0b	**PM Channel 1 Host Interface Interrupt Enable (PM1HIE)** 0: The IRQ11 is controlled by the IRQ11B bit in KBC Interrupt Control Register (KBIRQR). 1: Enables the interrupt to the host side via SERIRQ for PM channel 1 when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
3	R/W	0b	**Input Buffer Full 8032 Interrupt Enable (IBFCIE)** The bit is used to enable the interrupt to 8032 for Keyboard/Mouse when the input buffer is full via INT24 of INTC.
2	R/W	0b	**Output Buffer Empty 8032 Interrupt Enable (OBECIE)** The bit is used to enable the interrupt to 8032 for Keyboard/Mouse when the output buffer is empty via INT2 of INTC.
1	R/W	0b	**Output Buffer Full Mouse Interrupt Enable (OBFMIE)** 0: The IRQ12 is controlled by the IRQ12B bit in KBIRQR. 1: Enables the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
0	R/W	0b	**Output Buffer Full Mouse Interrupt Enable (OBFKIE)** 0: The IRQ1 is controlled by the IRQ1B bit in KBIRQR. 1: Enables the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.

6.5.5.2 KBC Interrupt Control Register (KBIRQR)

Address Offset: 02h

Bit	R/W	Default	Description
7	R	0b	**Reserved**
6	R/W	0b	**Interrupt Negative Polarity (IRQNP)** The bit is enabled, and then the interrupt level is inverted.
5-3	R/W	0b	**Interrupt Mode (IRQM)** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is high and a negative pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from SCIPM field in PMCTL register and SMIPM field in PMIC register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	1b	**IRQ11 Control Bit (IRQ11B)** When the PMHIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ11 signal. The bit can be used to monitor the status of IRQ11 signal. Reading this bit returns the status of IRQ11 signal, so the read value is not equal to the written value directly.
1	R/W	1b	**IRQ12 Control Bit (IRQ12B)** When the OBFMIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ12 signal. The bit can be used to monitor the status of IRQ12 signal. Reading this bit returns the status of IRQ12 signal, so the read value is not equal to the written value directly.
0	R/W	1b	**IRQ1 Control Bit (IRQ1B)** When the OBFKIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ1 signal. The bit can be used to monitor the status of IRQ1 signal. Reading this bit returns the status of IRQ1 signal, so the read value is not equal to the written value directly.

6.5.5.3 KBC Host Interface Keyboard/Mouse Status Register (KBHISR)

The 8032 firmware uses the register to monitor the status of KBC. It can use bit 7-4 and bit 2 to send the information to the host processor. The data of this register is the same as the data of KBC Status Register (KBSTR).

Address Offset: 04h

Bit	R/W	Default	Description
7-4	R/W	0h	**Programming Data 3-0 (PD3-0)** The data is used by the 8032 firmware to be the general-purpose setting.
3	R	0b	**A2 Address (A2)** The bit is used to keep the A2 address information of the write operation while the host processor accesses the KBC.
2	R/W	0b	**Programming Data II (PDII)** The function is the same as PD3-0.
1	R	0b	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when KBHIDIR is read by the 8032 firmware.
0	R	0b	**Output Buffer Full (OBF)** When 8032 is writing data to KBHIKDOR and KBHIMDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host.

6.5.5.4 KBC Host Interface Keyboard Data Output Register (KBHIKDOR)

The 8032 firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	W	-	**KBC Keyboard Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.5.5.5 KBC Host Interface Mouse Data Output Register (KBHIMDOR)

The 8032 firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	W	-	**KBC Mouse Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.5.5.6 KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)

The 8032 firmware can read the register to get the data of the KBC Data Input Register (KBDIR). Besides, the action will clear the IBF bit in the KBC Status Register (KBSTR). If the IBFCIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**KBC Keyboard/Mouse Data Input (KBKMDI)** The data is the same as the data of KBC Data Input Register (KBDIR).

6.6 Power Management Channel (PMC)

6.6.1 Overview

The power management channel is defined in ACPI specification and used as a communication channel between the host processor and embedded controller.

6.6.2 Features

- Supports two PM channels
- Supports compatible mode and enhanced mode (all channels)
- Supports shared and private interface
- Supports Command/Status and Data ports
- Supports IRQ/SMI/SCI generation

6.6.3 Functional Description

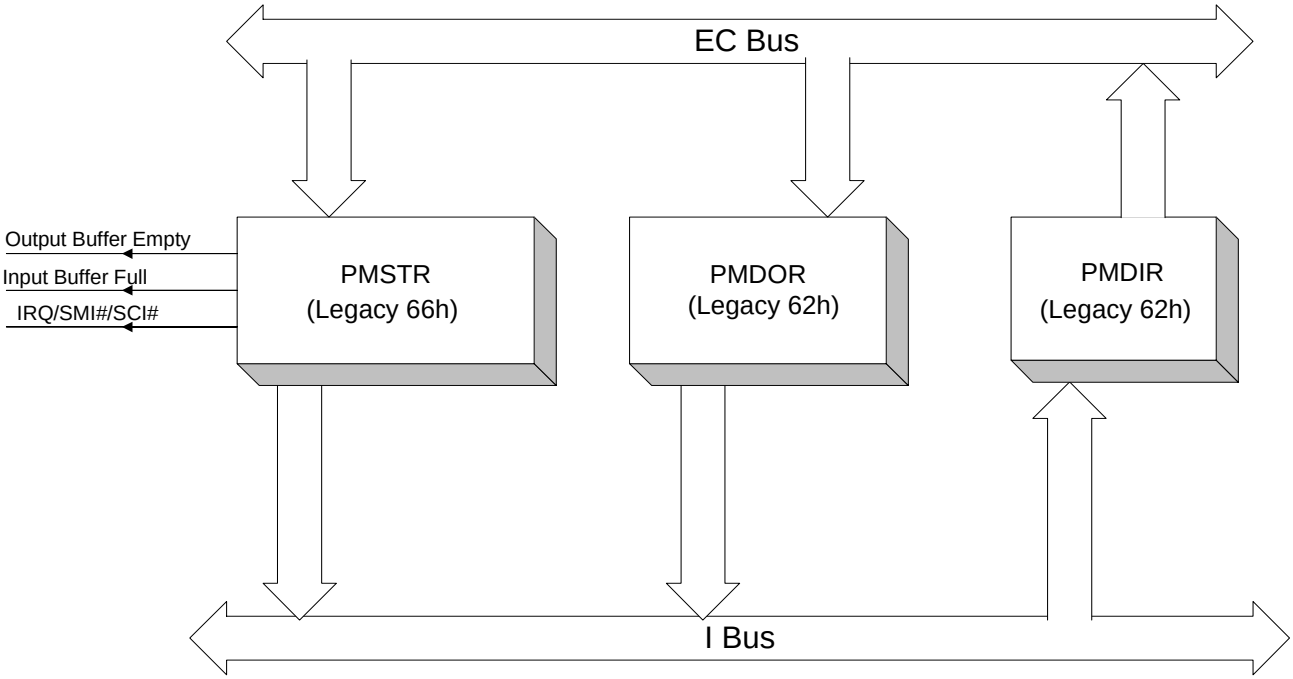
To generate the SCI and SMI interrupts to the host

6.6.3.1 General Description

The PM channel supports two operation modes: one is called Compatible mode that is available for channel 1 only. The other is called Enhanced mode. PMC is available for all channels. The PM channel provides four registers: PMDIR, PMDOR, PMCMDR and PMSTR for communication between the EC and host side. The PMDIR register can be written to by the host and read by the EC. The PMDOR register can be written to by the EC and read by the host. The PMCMDR/PMSTR register can be read by both the EC and Host side.

The PMC host interface block diagram is shown below.

Figure 6-11. PMC Host Interface Block Diagram

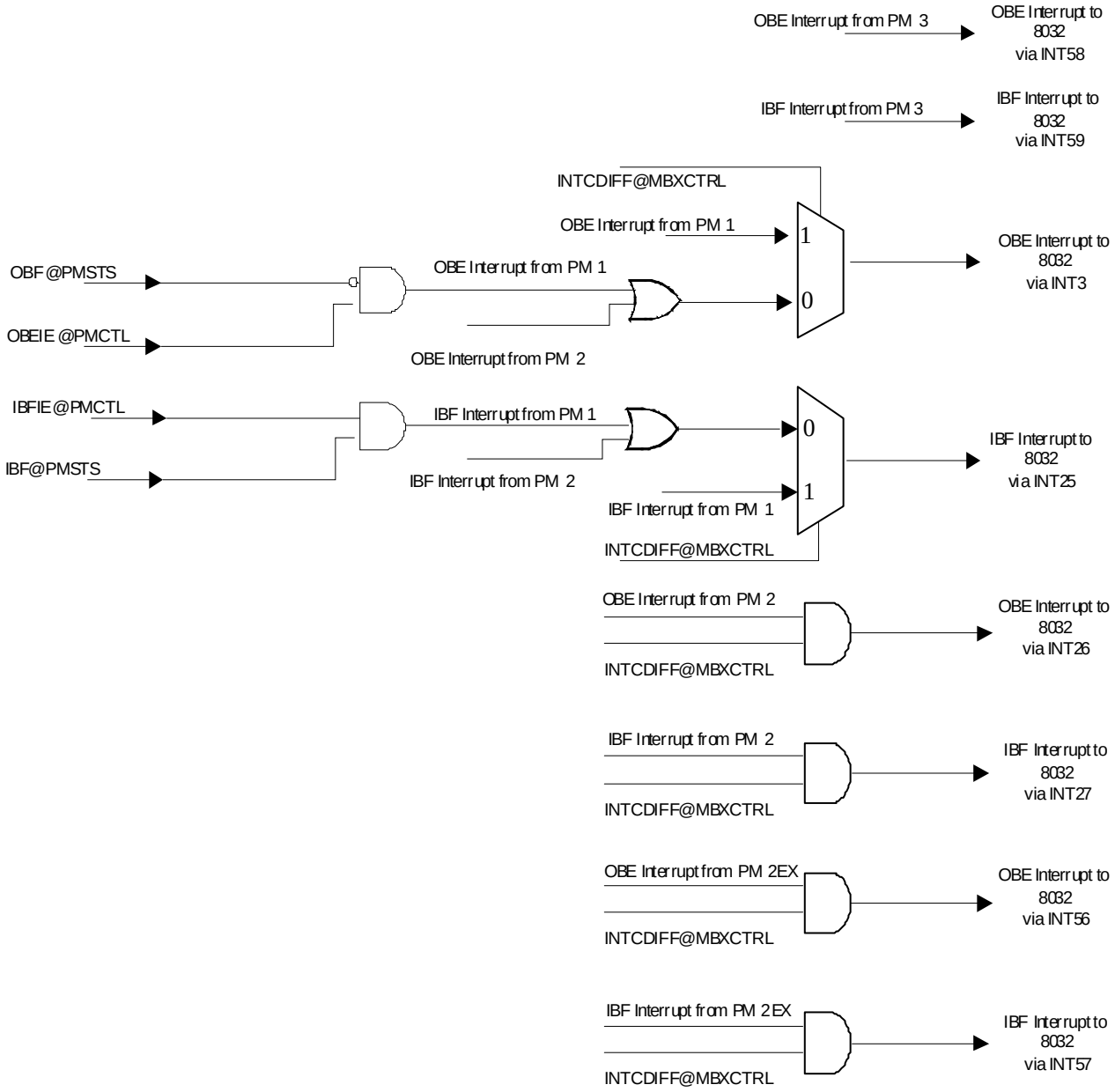


EC Interrupts
Two interrupts (IBF and OBF) are connected to INTC. These interrupts are enabled by OBEIE and IBFIE in PMCTLn register respectively.

The diagram of PMC interrupt to EC 8032 via INT3/INT25/INT26/INT27/INT64/INT65/INT66/INT67 of INTC

is shown below.

Figure 6-12. EC Interrupt Request for PMC



Host Interrupt

The EC can select to access to different address space to generate IRQ, SMI or SCI interrupt when either IBF or OBF is set.

The IRQ numbers of PMC are programmable and use IRQ11 as the abbreviation in the following section. The abbreviation, n, represents channel 1 and/or channel 2 of this register.

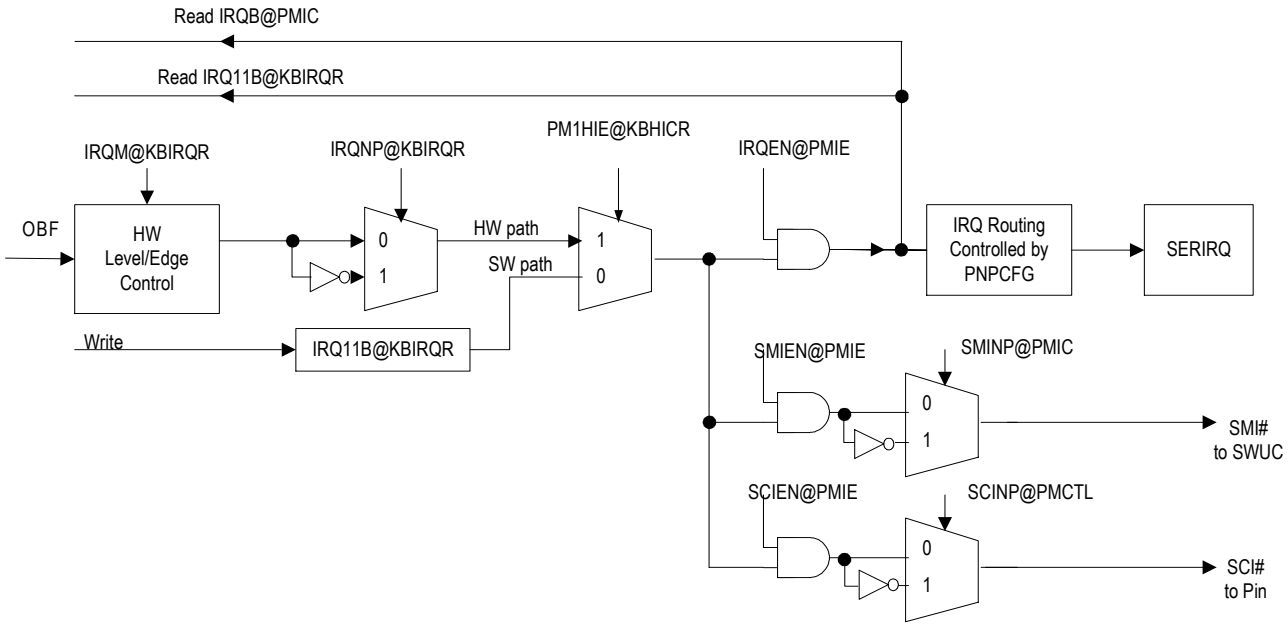
6.6.3.2 Compatible Mode

When IRQ numbers in host configuration register are assigned by host software, and the interrupt can be generated either by hardware via PM1HIE in KBHICR register or by programming KBIRQR register. In Normal Polarity mode (IRQNP in KBIRQR register is cleared), IT8502 supports legacy level for PM compatible mode interrupt. When a level interrupt is selected (IRQM in KBIRQR register is cleared), the interrupt signal is asserted when the OBF flag has been set, which is still asserted until the output buffer is read (i.e.,OBF flag is cleared). The EC can control the interrupts generated by the PM channel to the one as follows:

IRQ signal to LPC/SERIRQ, when IRQEN bit in PMIEn register is set.
SMI# output to SWUC, when SMIEN bit in PMIEn register is set.
SCI# signal, using the SCIEC output, when SCIEN bit in PMIEn register is set.

The IRQ/SCI#/SMI# control diagram in PMC compatible mode is shown below.

Figure 6-13. IRQ/SCI#/SMI# Control in PMC Compatible Mode

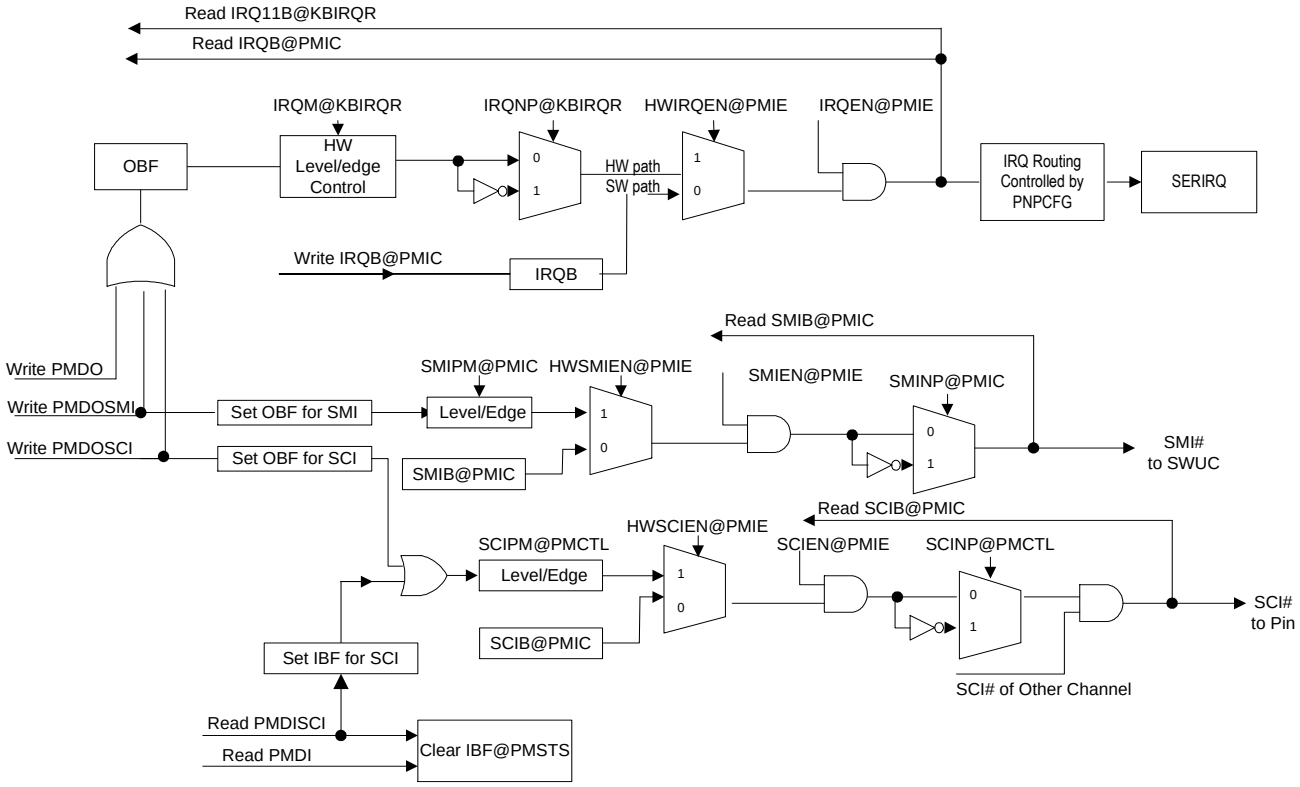


6.6.3.3 Enhanced PM mode

Enhanced PM mode is activated when APM is set to 1 in PMCTLn register. The generated IRQ, SMI or SCI interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PMIEn register. SCI and SMI are generated when EC writes to the Data output buffer. SCI is generated when EC reads the Data Input buffer. Different data register generates different interrupt. The OBF flag in PMSTSn register is set and both SMI and SCI interrupts are deasserted when data is written to PMDOn register. The OBF_SMI interrupt is generated when PMDOSMIn register is written into data. The OBF_SMI flag is cleared when OBF flag is cleared. The OBF_SCI interrupt is generated When PMDOSCIn register is written into data.OBF_SCI which is cleared when OBF is cleared.
The IBF flag is cleared and SCI interrupt is generated when PMDISCIn register is read out data. The IBF flag is cleared and SCI interrupt is not asserted when PMDIn register is read out data.

The IRQ/SCI/SMI control diagram in PMC enhanced mode is shown below.

Figure 6-14. IRQ/SCI#/SMI# Control in PMC Enhanced Mode



6.6.3.4 PMC2EX

There is a channel 2 extended (PMC2EX) mailbox (MBX) function based on PMC channel 2, which is constructed by a 16-byte mailbox shared with BRAM. See also Figure 7-37. BRAM Mapping Diagram on page 308.

This 16-byte mailbox can be accessed from both the EC side (named MBXEC0-15) and host side (MBXH0-15).
In the EC side, MBXEC0-15 is always located in PMC module offset F0h-FFh and shared with the topmost 16-byte in BRAM.
In the host side, MBXH0-15 address is based on the descriptor 2 of Power Management I/F Channel 2 logic device inside LPC I/O space. (Refer to section 6.2.11.6 and 6.2.11.7 on page 64)

The PMC2EX (channel 2 extended) shares the same interrupt generation resource and registers (offset 10h-18h).

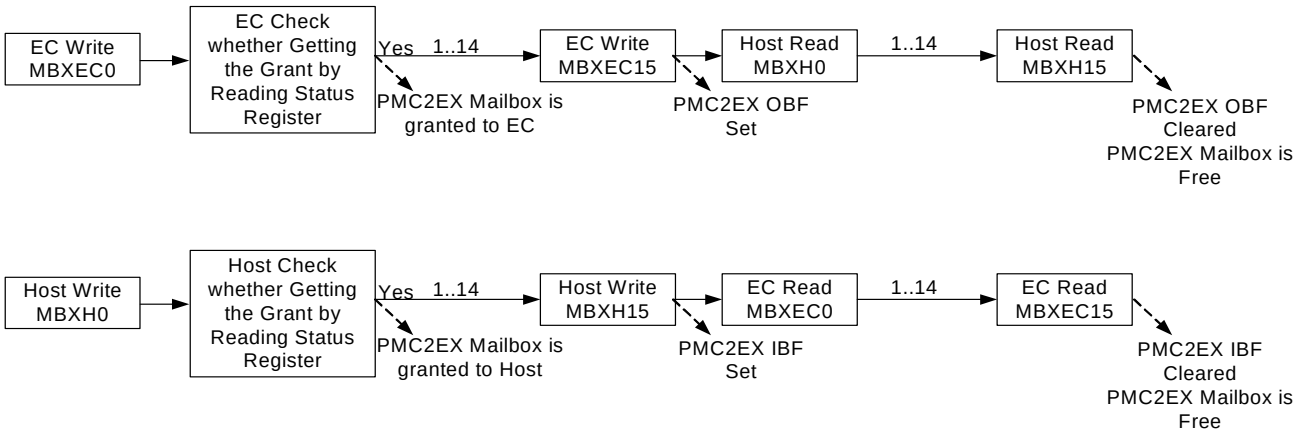
For registers, PMC2EX shares the same registers (offset 10h-18h) and has its dedicated MBXCTRL register (offset 19h).

For interrupt generation, PMC2EX shares the same interrupt logic with channel 2. If MBXEN is set, IBF/OBF interrupt source of PMC2EX is ORed with channel 2.

The EC/host side should check whether to get the grant from the internal arbiter after writing to MBXEC0/MBXH0 (respectively).

The typical PMC2EX mailbox operation is described below.

Figure 6-15. Typical PMC2EX Mailbox Operation

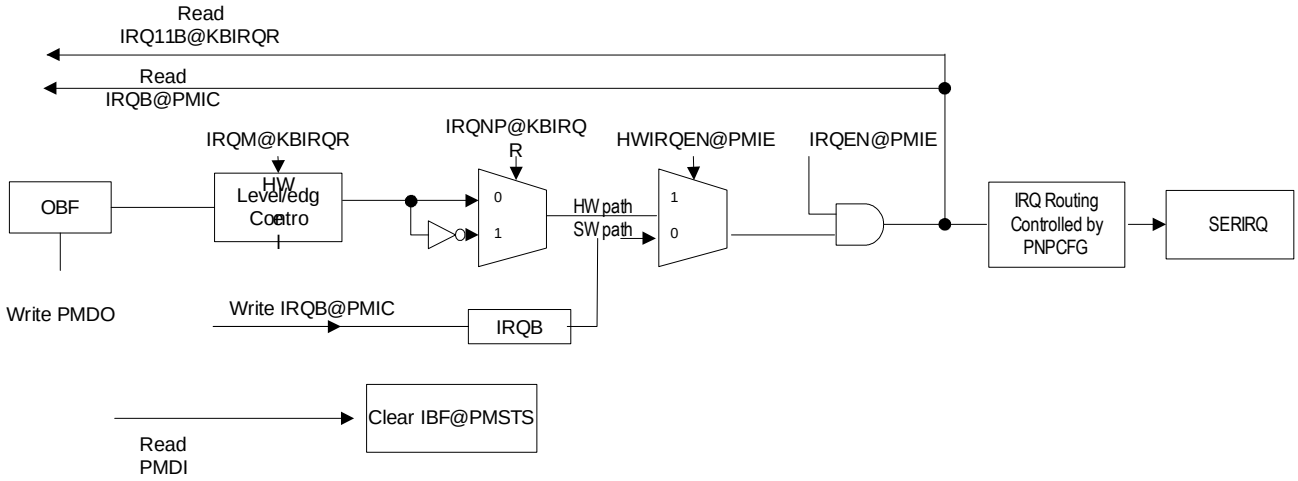


6.6.3.5 PMC3

Only Enhanced PM mode is activated in PM channel 3 and only IRQ interrupt is generated. The generated IRQ interrupt can be selected to output via software control or hardware, which is determined by programming IRQEN bit in PMIE3 register.The OBF flag in PMSTS3 register is set when data is written to PMDO3 register. The IBF flag is cleared when PMDIn register is read out data.

The IRQ control diagram in PMC3 is shown below.

Figure 6-15. IRQ Control in PM Channel 3



6.6.4 Host Interface Registers

The registers of PMC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The PMC Channel 1 and 2 reside at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The channel 1 logical device number is 11h (LDN=11h) and the channel 2 logical device number is 12h (LDN=12h). For compatibility issue, the two I/O Port Base Addresses of channel 1 are suggested to configure at 62h and 66h.

These registers are listed below.

Table 6-25. Host View Register Map, PMC

7	0	Offset
PMC Data Input Register (PMDIR)		Legacy 62h
PMC Data Output Register (PMDOR)		Legacy 62h
PMC Command Register (PMCMDR)		Legacy 66h

7							0	Offset
PMC Status Register (PMSTR)								Legacy 66h

Legacy 62h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 66h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-3 on page 42.

6.6.4.1 PMC Data Input Register (PMDIR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Data Input Register Bit [7:0] (DIRB)** This is the data input register for power management channel data communication between the host and EC side. When the host writes this port, data is written to PMDIR register and EC 8032 can read it. Notice that when the Command/Status register is written, the data is also stored into PMDIR register. Users must read A2 to decide whether the PMDIR data is data or command.

6.6.4.2 PMC Data Output Register (PMDOR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	R	00h	**Data Output Register Bit [7:0] (DORB)** This is the data output register for power management channel data communication between the host and EC. When the host reads this port, data is read from PMDOR register and EC 8032 can write it.

6.6.4.3 PMC Command Register (PMCMDR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-0	W	00h	**Command Register Bit [7:0] (CRB)** The port is written by the host when A2 = 1 in PMSTR register.

6.6.4.4 Status Register (PMSTR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general purpose flag used for signaling between the host and EC side. When used as ACPI PM channel, the predefined meaning is burst, SCI event and SMI event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	**A2 (A2)** This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written by the host is data. If this bit is 1, it represents that the data written by the host is command.
2	R/W	0b	**General Purpose flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data input register or command register and is cleared when the EC 8032 reads the data input register. Notice that the write to data input register or command register by the host all trigger this flag and EC must use A2 to distinguish whether the write is a command or data.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data output port and is cleared when the host reads the data out buffer.

6.6.5 EC Interface Registers

The registers of PMC can be divided into two parts, Host Interface Registers and EC Interface Registers. This section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address is 1500h.

These registers are listed below.

Table 6-26. EC View Register Map, PMC

7	0	Offset
Host Interface PM Channel 1 Status (PM1STS)		00h
Host Interface PM Channel 1 Data Out Port (PM1DO)		01h
Host Interface PM Channel 1 Data Out Port with SCI (PM1DOSCI)		02h
Host Interface PM Channel 1 Data Out Port with SMI (PM1DOSMI)		03h
Host Interface PM Channel 1 Data In Port (PM1DI)		04h
Host Interface PM Channel 1 Data In Port with SCI (PM1DISCI)		05h
Host Interface PM Channel 1 Control (PM1CTL)		06h
Host Interface PM Channel 1 Interrupt Control (PM1IC)		07h
Host Interface PM Channel 1 Interrupt Enable (PM1IE)		08h
Host Interface PM Channel 2 Status (PM2STS)		10h
Host Interface PM Channel 2 Data Out Port (PM2DO)		11h
Host Interface PM Channel 2 Data Out Port with SCI (PM2DOSCI)		12h
Host Interface PM Channel 2 Data Out Port with SMI (PM2DOSMI)		13h
Host Interface PM Channel 2 Data In Port (PM2DI)		14h
Host Interface PM Channel 2 Data In Port with SCI (PM2DISCI)		15h
Host Interface PM Channel 2 Control (PM2CTL)		16h
Host Interface PM Channel 2 Interrupt Control (PM2IC)		17h
Host Interface PM Channel 2 Interrupt Enable (PM2IE)		18h
Mailbox Control (MBXCTRL)		19h
Host Interface PM Channel 3 Status (PM3STS)		20h
Host Interface PM Channel 3 Data Out Port (PM3DO)		21h
Host Interface PM Channel 3 Data In Port (PM3DI)		22h
Host Interface PM Channel 3 Control (PM3CTL)		23h
Host Interface PM Channel 3 Interrupt Control (PM3IC)		24h
Host Interface PM Channel 3 Interrupt Enable (PM3IE)		25h
16-byte PMC2EX Mailbox 0 (MBXEC0)		F0h
…		…
16-byte PMC2EX Mailbox 15 (MBXEC15)		FFh

6.6.5.1 PM Status Register (PMSTS)

This register is the same as the Status register in host side but reside in the EC side.

Address Offset: 00h/10h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 1 and channel 2 with MBXEN cleared: This is a general-purpose flag used for signaling between the host and EC. When used as ACPI PM channel, the predefined meaning is burst, SCI event and SMI event. For channel 2 with MBXEN set: Bit 7: IBF of PMC channel 2 extended (PMC2EX) Bit 6: OBF of PMC channel 2 extended (PMC2EX) Bits 5-4: 00b: PMC2EX mailbox is not granted to both sides. 01b: PMC2EX mailbox is granted to the EC side. 10b: PMC2EX mailbox is granted to the host side. 11b: Reserved
3	R	0b	**A2 (A2)** This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written to the data port is data. If this bit is 1, it represents that the data written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general-purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereascleared when the host reads the data output buffer.

6.6.5.2 PM Data Out Port (PMDO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 01h/11h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out (PMDO[7:0])** This is the data output buffer.

6.6.5.3 PM Data Out Port with SCI (PMDOSCI)

This register is the PMDOR buffer with SCI. The data written to this register is stored in PMDOR. SCI is generated upon write.

Address Offset: 02h/12h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SCI (PMDOSCI[7:0])** This is the data output buffer with SCI. Writing to this port will generate hardware SCI if enabled.

6.6.5.4 PM Data Out Port with SMI (PMDOSMI)

This register is the PMDOR buffer with SMI. The data written to this register is stored in PMDOR. SMI is

generated upon write.

Address Offset: 03h/13h

Bit	R/W	Default	Description
7-0	W	00h	**PM Data Out with SMI (PMDOSMI[7:0])** This is the data output buffer with SMI. Writing to this port will generate hardware SMI if enabled.

6.6.5.5 PM Data In Port (PMDI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 04h/14h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In (PMDI[7:0])** This is the data input buffer.

6.6.5.6 PM Data In Port with SCI (PMDISCI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer. Reading this register (EC) generates SCI.

Address Offset: 05h/15h

Bit	R/W	Default	Description
7-0	R	00h	**PM Data In with SCI (PMDISCI[7:0])** This is the data input buffer with SCI. Reading this port will generate SCI when enabled.

6.6.5.7 PM Control (PMCTL)

Address Offset: 06h/16h

Bit	R/W	Default	Description
7	R/W	0b	**Enhance PM Mode (APM)** Setting this bit to '1' enables the enhance PM mode. The interrupts (IRQ, SCI or SMI) are automatically generated by hardware operations if enabled.
6	R/W	1b	**SCI Negative Polarity (SCINP)** Setting this bit to '1' causes the SCI polarity inversed (low active).
5-3	R/W	0h	**SCI Pulse Mode (SCIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.6.5.8 PM Interrupt Control (PMIC)

Address Offset: 07h/17h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	1b	**SMI Negative Polarity (SMINP)** Setting this bit to '1' causes the SMI polarity inversed.
5-3	R/W	000b	**SMI Pulse Mode (SMIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000b: Level-triggered mode. 001b: Edge-triggered mode with 1-cycle pulse width. 010b: Edge-triggered mode with 2-cycle pulse width. 011b: Edge-triggered mode with 4-cycle pulse width. 100b: Edge-triggered mode with 8-cycle pulse width. 101b: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	0b	**Host SCI Control Bit (SCIB)** This bit is the SCI generation bit when hardware SCI is disabled. Read always returns the current value of SCI.
1	R/W	0b	**Host SMI Control Bit (SMIB)** This bit is the SMI generation bit when hardware SMI is disabled. Read always returns the current value of SMI.
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.6.5.9 PM Interrupt Enable (PMIE)

Address Offset: 08h/18h

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R/W	0b	**Hardware SMI Enable (HWSMIEN)** Setting this bit to '1' enables the SMI generated by hardware control. Writing to the SMIB bit generates the SMI if this bit is set to '0'.
4	R/W	0b	**Hardware SCI Enable (HWSCIEN)** Setting this bit to '1' enables the SCI generated by hardware control. Writing to the SCIB bit generates the SCI if this bit is set to '0'.
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing to the IRQB bit generates the IRQ if this bit is set to '0'.
2	R/W	0b	**SMI Enable (SMIEN)** Setting this bit to '1' enables the SMI generated by this module.
1	R/W	0b	**SCI Enable (SCIEN)** Setting this bit to '1' enables the SCI generated by this module.
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.6.5.10 Mailbox Control (MBXCTRL)

Address Offset: 19h

Bit	R/W	Default	Description
7	R/W	0b	**Mailbox Enable (MBXEN)** 1b: Enable 16-byte PMC2EX mailbox 0b: Otherwise
6	-	-	**Reserved**
5	R/W	0b	**Dedicated Interrupt (DINT)** 0b: INT3: PMC Output Buffer Empty Int INT25: PMC Input Buffer Full Int 1b: INT3: PMC1 Output Buffer Empty Int INT25: PMC1 Input Buffer Full Int INT26: PMC2 Output Buffer Empty Ir INT27: PMC2 Input Buffer Full Int INT64: PMC2EX Output Buffer Int. INT65: PMC2EX Input Buffer Full Int. INT66 : PMC3 Output Buffer Empty Int INT67 : PMC3 Input Buffer Full Int (All are High Level Trig)
6-0	-	-	**Reserved**

6.6.5.11 PMC3 Status Register (PM3STS)

This register is the same as the Status register in host side but resides in the EC side.

Address Offset: 20h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** For channel 3: This is a general-purpose flag used for signaling between the host and EC.
3	R	0b	**A2 (A2)** This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents what written to the data port is data. If this bit is 1, it represents what written to the data port is command.
2	R/W	0b	**General Purpose Flag (GPF)** This bit is used as a general purpose flag.
1	R	0b	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data port or command port whereas cleared when the EC read the data in the buffer.
0	R	0b	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port whereas cleared when the host reads the data output buffer.

6.6.5.12 PMC3 Data Out Port (PM3DO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	W	00h	**PM 3 Data Out (PM3DO[7:0])** This is the data output buffer.

6.6.5.13 PMC3 Data In Port (PM3DI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R	00h	**PMC3 Data In (PM3DI[7:0])** This is the data input buffer.

6.6.5.14 PMC3 Control (PM3CTL)

Address Offset: 23h

Bit	R/W	Default	Description
7-2	-	0b	**Reserved**
1	R/W	0b	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0b	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.6.5.15 PMC3 Interrupt Control (PM3IC)

Address Offset: 24h

Bit	R/W	Default	Description
7-1	-	0b	**Reserved**
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.6.5.16 PMC3 Interrupt Enable (PM3IE)

Address Offset: 25h

Bit	R/W	Default	Description
7-4	-	00b	**Reserved**
3	R/W	0b	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing data to the IRQB bit generates the IRQ if this bit is set to '0'.
2-1	-	0b	**Reserved**
0	R/W	0b	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.6.5.17 16-byte PMC2EX Mailbox 0-15 (MBXEC0-15)

Address Offset: F0h-FFh

Bit	R/W	Default	Description
7-0	R/W	-	**Mailbox Byte Content** This byte is the 16-byte PMC2EX mailbox in the EC side.

6.7 BRAM in Host Domain

6.7.1 Overview

BRAM module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.17 Battery-backed SRAM (BRAM) for the EC domain function description on page 308.

6.8 Serial Peripheral Interface (SSPI) in Host Domain

6.8.1 Overview

SSPI module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.18 Serial Peripheral Interface (SSPI) for the EC domain function description on page 311.

SSPI can be accessed by the software in the host or EC side, however, the SSPI function should be controlled by a side only. See also section 7.15.4.10 Reset Control DMM (RSTDMMC) on page 302 and section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 206.

6.9 Serial Port 1 (UART1) in Host Domain

6.9.1 Overview

UART1 module is located at I-bus and EC-bus at the same time. It means it can be accessed by the host and EC side without software arbitration. Refer to section 7.19 Serial Port (UART) for the EC domain function description on page 320.

UART1 can be accessed by the software in the host or EC side, however, the UART1 function should be controlled by a side only. See also section 7.15.4.10 Reset Control DMM (RSTDMMC) on page 302 and section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 206.

7. EC Domain Functions

7.1 8032 Embedded Controller (EC)

7.1.1 Overview

The embedded controller is an 8032 micro-controller which is an 8051-compatible micro-controller.

7.1.2 Features

- Supports Sleep (a.k.a. power-down) and Idle mode
- Supports two external interrupts and one power fail interrupt
- Supports 64K code/data space
- Supports 256 bytes internal(w.r.t. 8032) RAM, with 128 bytes special function register
- Supports 3x16-bit timer/counter from GPE5, TMRI0 and TMRI1
- Supports 1xwatch dog timer
- Supports full duplex UART
- Memory mapped I/O configuration

7.1.3 General Description

The 8032TT is a high-performance 8051 family compatible micro-controller based on RISC architecture & Pipeline design. This IP Specification of interface timing, external Data Memory read / write timing and external Program Memory read timing are different from that of the standard 80C52. But instruction-set is fully compatible with standard 8051 family.

Table 7-1. 8032 Port Usage

Signal	Port	Note
8032 External Data Bus	P0[7:0], P2[7:0], P3[7:6]	EC Bus MOVX instruction
INT0#	P3[2]	Driven by INTC
INT1#	P3[3]	Driven by INTC
TXD	P3[1]	TXD signal on pin
RXD	P3[0]	RXD signal on pin
T0 Timer	P3[4]	Driven by GPE5
T1 Timer	P3[5]	Driven by TMRI0 pin
T2 Timer	P1[0] Note: T2 and T2EX should be taken care of if 8032 banks are switched by P1. See also section 6.3.4.2 on page 80	Driven by TMRI1 pin (input only and clock-out not available)
T2EX Timer	P1[1]	Unused

7.1.4 Functional Description

Memory
The 8032 manipulates operands in four memory spaces. There are 64K-byte Program Memory space, 64K-byte External Data Memory space, 256-byte Internal Data Memory, and with a 16-bit Program Counter space. The Internal Data Memory address space is further divided into the 256-byte Internal Data RAM and 128-byte Special Function Register address space. The up 128-bytes RAM can be reached by indirect addressing. Four Register Banks, 128 addressable bits, and the stack reside in the Internal Data RAM.

I/O ports
The 8032 has 8-bit I/O ports. The four ports provide 32 I/O lines to interface to the external world. All four ports are both byte and bit addressable. Port 0 is used as an Address/Data bus and Port 2 is used as the upper 8-bits address when external memory/device is accessed. Port 3 contains special control signals such as the read and write strobes. Port 1 is used for both I/O and external interrupts.

Interrupts
In the 8032 there are six hardware resources that generate an interrupt request. The starting addresses of the interrupt service program for each interrupt source are like standard 8052. The external interrupt request inputs (INT0# , INT1#) can be programmed for either negative edge or low level-activated operation.

Timers / Counters
The 8032 has three 16-bit timers/counters that are the same as the timers of the standard 8051 family. The 8032 has two additional watchdog timers for system failure monitor.

Serial I/O ports
The 8032 has one programmable, full-duplex serial I/O port whose function is the same as that of 8051 family and dependent on the requirement.

Power Management
The 8032 supports Idle and Doze/Sleep modes of operation. In the Idle mode, the EC 8032 is stopped operation while the peripherals continue operating. In the Doze/Sleep mode, all the clocks are stopped. The Doze/Sleep mode can be waked up by INT0# or INT1# external interrupt with level trigger.

Dual Data Pointer
The 8032 has two data pointers (DTPR, DTPR1). These two data pointers can help users enhance lots of block data memory moving. Using dual data pointers to move block data almost saves half of the time spent by original 8051 codes.

Watch Dog Timers Interrupt / Reset
The 8032 creates one programmable watchdog timers to monitor system failure. That is maximum 2^26.

Hardware Multiply
8032 includes a hardware multiplier to enhance calculating speed. 8032 can finish one multiply instruction at 1 machine cycle.

7.1.5 Memory Organization

In 8032, the memory is organized as three address spaces and the program counter.
The memory spaces are shown in EC Memory Map.
- 16-bit Program Counter
- 64k-byte Program Memory address space
- 64k-byte External Data Memory address space
- 256-byte Internal Data Memory address

The 16-bit Program Counter register provides 8032 with its 64k addressing capabilities. The program Counter allows users to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

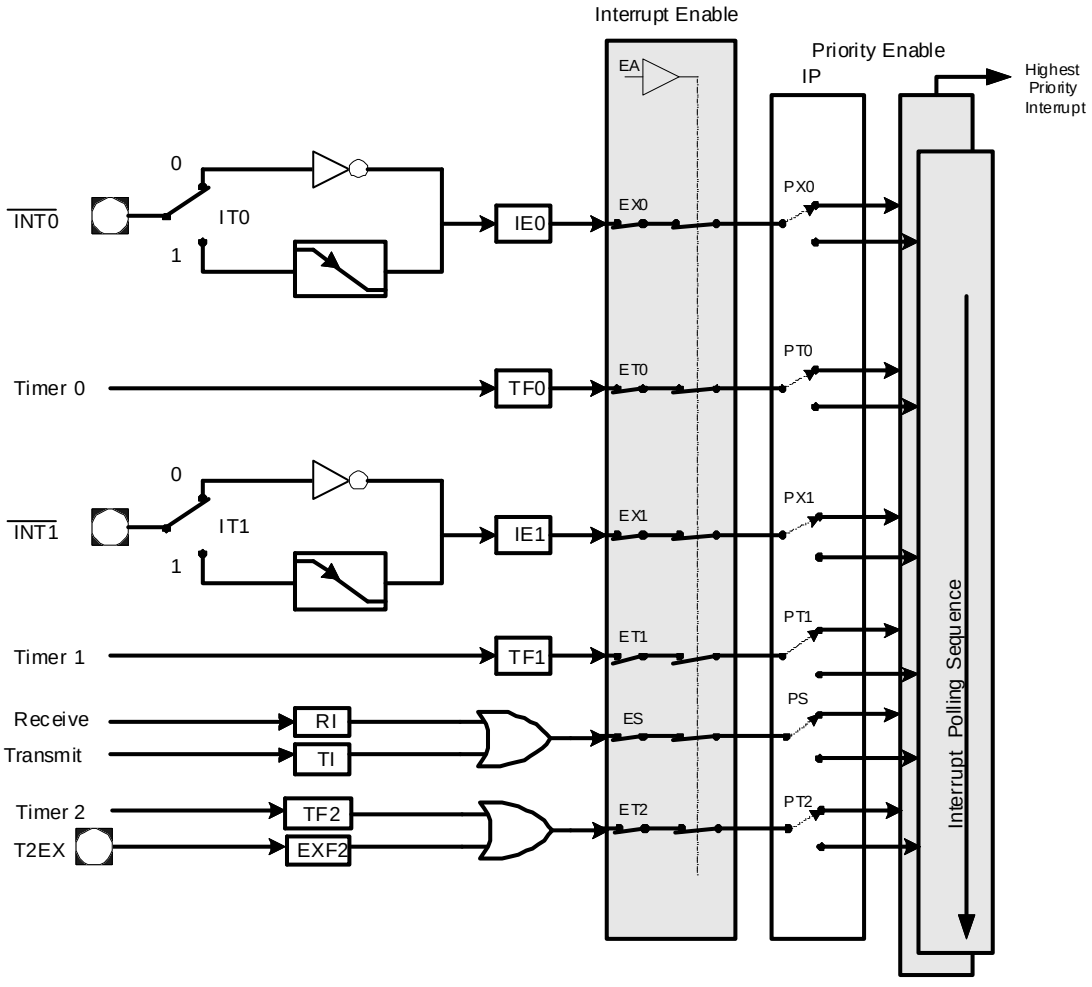
The 64k-byte Program Memory address space is located by dedicated address bus. The 64k-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address Space and a 128-byte Special Function Register address space as shown in the SFRs Map. The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit location ns of the on-chip RAM are accessible through Direct Addressing.

7.1.6 On-Chip Peripherals

Table 7-2. System Interrupt Table

Interrupt Source	Request Flag	Priority Flag	Enable Flag	Vector Address	Priority-Within-Level	Flag Cleared by Hardware?
External Request	IE0/TCON.1	PX0/IP.0	EX0/IE.0	0003h	1	Edge-Yes Level-No
Internal Timer0/Counter0	TF0/TCON.5	PT0/IP.1	ET0/IE.1	000Bh	2	Yes
External Request	IE1/TCON.3	PX1/IP.2	EX1/IE.2	0013h	3	Edge-Yes Level-No
Internal Timer1/Counter1	TF1/TCON.7	PT1/IP.3	ET1/IE.3	001Bh	4	Yes
Internal Serial Port	Xmit TI/SCON.1	PS/IP.4	ES/IE.4	0023h	5	No
	Rcvr RI/SCON.0					
Internal Timer2/Counter2	TF2/T2CON.7	PT2/IP.5	ET2/IE.5	002Bh	6	No
	EXF2/TSCON.6					

Figure 7-1. Interrupt Control System Configuration



Note: T2EX is tied to logic high and is not available in IT8502.

External Interrupt
External Interrupt INT0# and INT1# input signal may each be programmed to be level-triggered or edge triggered depending upon bits IT0 and IT1 in the TCON register. If IT0 or IT1 = 0, INT0# or INT1# is triggered by detected low at the input signal. If IT0 or IT1 = 1, INT0# or INT1# is negative-edge triggered. External interrupts are enabled with bits EX0 and EX1in the IE register. Evens on the external interrupt input signals set the interrupt flags IE0 or IE1 in TCON. These request bits are cleared by hardware vectors to service routines only if the interrupt is negative-edge triggered. If the interrupt is level triggered, the interrupt service routine must clear the request bit. External hardware must release INT0# or INT1# before the service routine completes, or an additional interrupt is requested.

External interrupt input signals are sampled once every oscillator clock's rising edge. A level-triggered interrupt input signal held low or high for at least three clocks guarantees detection. Edge-triggered external interrupts only the request input signal for one clock time. This ensures edge recognition and sets interrupt request bit EX0 or EX1. The 8032 clears EX0 or EX1 automatically during service routine fetch cycles for edge-triggered interrupts.

Timer Interrupts
Sources of timer 0, timer 1 and timer 2 are GPE5, TMRI0 and TMRI1 from pins. Three timer-interrupt request bits TF0, TF1 and TF2 are set by timer 0, timer 1 and timer 2 overflow. When timer 0 and timer 1 interrupts are generated, the bits TF0 and TF1 are cleared by an on-chip hardware vector to an interrupt service routine. Timer 2 is different from timer 0 or timer 1. Timer 2 has to clear TF2 bit by software writing when timer 2 interrupt is generated. Timer interrupts are enabled by bits ET0, ET1, and ET2 in the IE register.

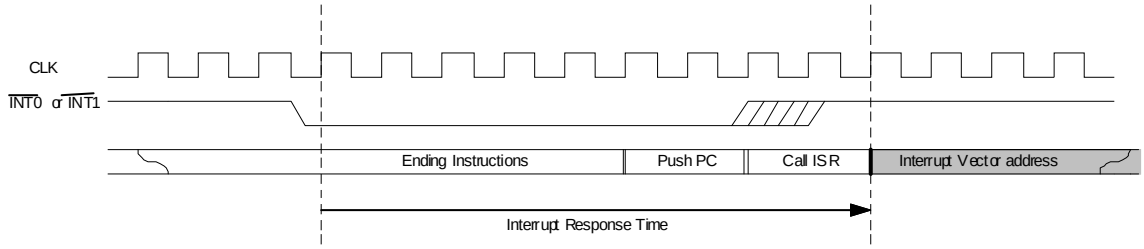
Timer 2 interrupts are generated by a logical OR of bits TF2 and EXF2 in register T2CON. Neither flag is cleared by a hardware vector to a service routine. In fact, the interrupt service routine must determine if TF2 or EXEF2 generates the interrupt, and then clear the bit. Timer 2 interrupt is enabled by ET2 in register IE.

Serial Port Interrupt
Serial port interrupts are generated by the logical OR of bits RI and TI in the SCON register. Neither flag is cleared by a hardware vector to the service routine. The service routine resolves RI and TI interrupt generation and clears the serial port request flag. The serial port interrupt is enabled by bit ES in the IE register in the same way by using serial port 1.

Interrupt Priority
8032 has 2 level priorities. Setting / clearing a bit in the Interrupt Priority register (IP) establish its associated interrupt request as a high / low priority. If a low-priority level interrupt is being serviced, a high-priority level interrupt will interrupt it. However, an interrupt source cannot interrupt a service program of the same or higher level. The interrupt priority is shown on Interrupt Control System Configuration.

Interrupt Response Time
The Figure of Interrupt Response Time shows the response time is between the interrupt request being active and the interrupt service routing being executed. The minimum interrupt response time is eight clocks that when an interrupt request asserts after the ending instruction execution completes. The maximum interrupt response time is 24 clocks when an interrupt request asserts during the ending instruction, DJNZ direct, rel or other instruction sets whose operation period is 16 clocks and is decoded ok. However, a high priority interrupt asserts while a low priority interrupt service program is executing. The minimum and the maximum interrupt response time is 8 clocks and 24 clocks respectively.

Figure 7-2. Interrupt Response Time



7.1.7 Timer / Counter

Timer 0

Timer 0 functions as either a timer or event counter in four modes of operation. Timer 0 is controlled by the four low-order bits of the TMOD register and bits 5, 4, 1 and 0 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/T), and mode of operation (M1, M0). The TCON register provides timer 0 control functions: overflag (TF0), run control (TR0), interrupt flag (IE0), and interrupt type control (IT0). For normal timer operation (GATE = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE and TR0 allows INT0# to control timer operation.

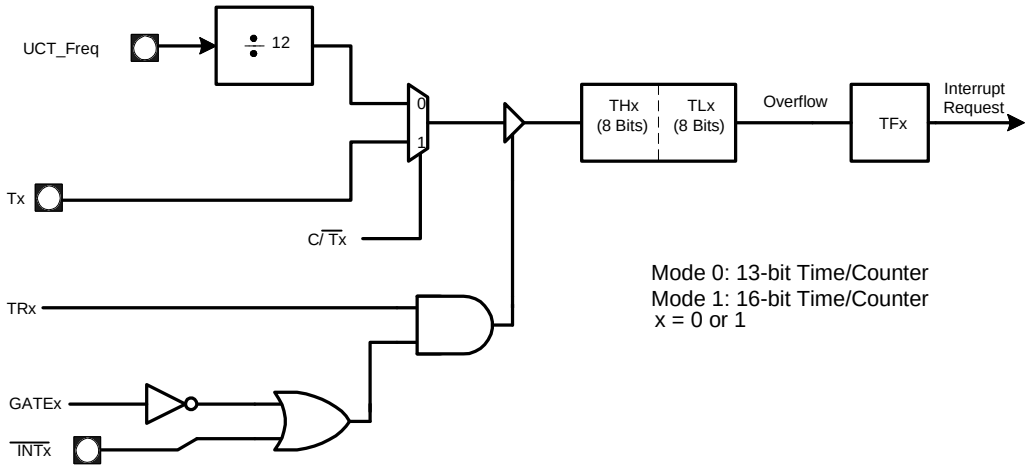
Timer0/Mode 0 (13-bit Timer)

Mode 0 configures timer 0 as a 13-bit timer which is set up as an 8-bit timer (TH0 register) with a module 32 prescaler implemented with the lower five bits of the TL0 register. The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

Timer 0/ Mode 1 (16-bit Timer)

Mode 1 configures timer 0 as a 16-bit timer with TH0 and TL0 connected in cascade. The selected input increments TL0.

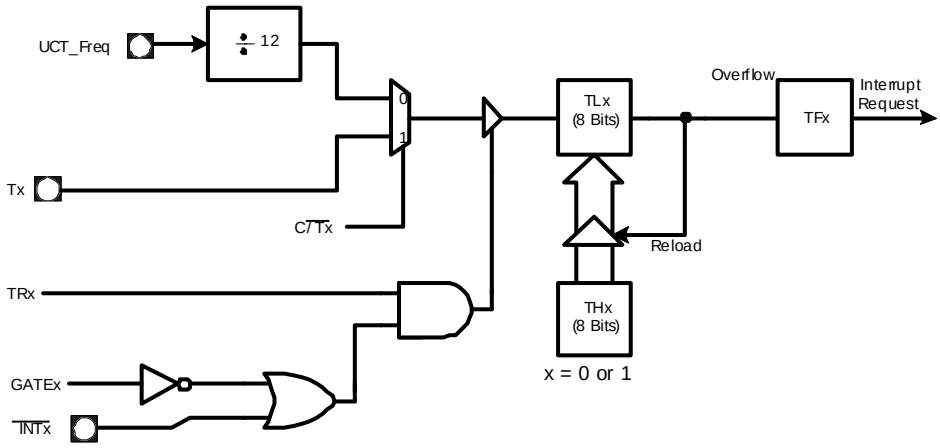
Figure 7-3. Timer 0/1 in Mode 0 and Mode 1



Timer 0/ Mode 2 (8-bit Timer With Auto-reload)

Mode 2 configures timer 0 as an 8-bit timer (TL0 register) that automatically reloads from the TH0 register. TL0 overflow sets the timer overflow flag (TF0) in the TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged.

Figure 7-4. Timer 0/1 in Mode 2, Auto-Reload

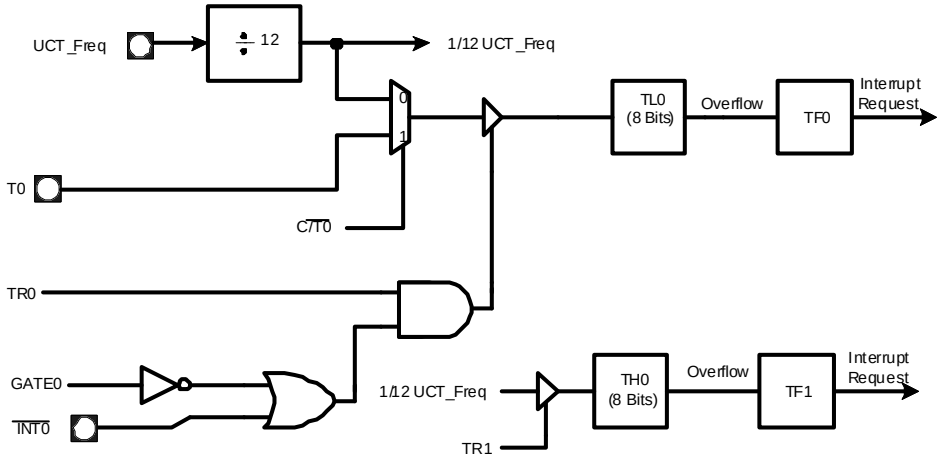


Timer 0/ Mode 3(Two 8-bit Timers)

Mode 3 configures timer 0 such that registers TL0 and TH0 operate as separate 8-bit timers. This mode is provided for application requiring an additional 8-bit timer or counter. TL0 uses the timer 0 control bits C/T and GATE in TMOD, and TR0 in TCON in the normal manner. TH0 is locked into a timer function (counting UCT_Freq/12) and takes over use of the timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of timer 1 is restricted when timer 0 is in mode 3.

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 10-2 on page 352).

Figure 7-5. Timer 0 in Mode 3 Two 8-bit Timers



Timer 1

Timer 1 functions as either a timer or event counter in three modes of operation. The logical configuration for modes 0, 1 and 2 is the same as that of Timer 0. Mode 3 of timer 1 is a hold-count mode.

Timer 1 is controlled by the four high-order bits of the TMOD register and bits 7, 6, 3 and 2 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/ T), and mode of operation (M1 and M0). The TCON register provides timer 1 control functions: overflow flag (TF1), run control (TR1), interrupt flag(IE1), and interrupt type control (IT1).

For normal timer operation (GATE = 0), setting TR1 allows timer register TL1 to be incremented by the selected input. Setting GATE and TR1 allows external input signal INT1# to control timer operation. This setup can be used to make pulse width measurements.

Timer 1/ Mode 0 (13-bit Timer)
Mode 0 configures timer 0 as a 13-bit timer, which is set up as an 8-bit timer (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register. The upper 3 bits of the TL1 register are ignored. Prescaler overflow increment the TH1 register.

Timer1/ Mode 1 (16-bit Timer)
Mode 1 configures timer 1 as a 16-bit timer with TH1 and TL1 connected in cascade. The selected input increments TL1.

Timer 1/ Mode 2 (8-bit Timer)
Mode 2 configures timer 1 as an 8-bit timer (TL1 register) with automatic reload from the TH1 register on overflow. Overflow from TL1 sets overflow flag TF1 in the TCON register and reloads TL1 with the contents of TH1, which is preprogrammed by software. The reload leaves TH1 unchanged.

Timer 1/ Mode 3 (Halt)
Placing timer in mode 3 causes it to halt and its count. This can be used to halt timer 1 when the TR1 run control bit is not available, i.e., when timer 0 is in mode 3.

Timer 2
Timer 2 is a 16-bt timer/count maintained by two eight-bit timer registers, TH2 and TL2, which are connected in cascade. The timer/counter 2 mode control register T2MOD and the timer /counter control register T2CON control the operation of timer 2.

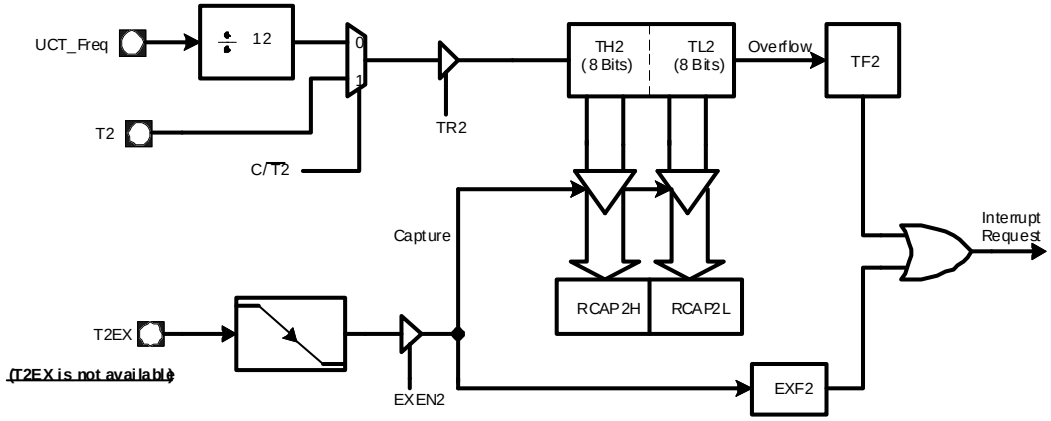
Timer 2 provides the following operating modes: capture mode, auto-reload mode, baud rate generator mode, and programmable clock-out mode. Select the operating mode with T2MOD and TCON register bits as shown in table of Timer 2 Modes of Operation. Auto-reload is the default mode. Setting RCLK and/or TCLK selects the baud rate generator mode.

Timer 2 operation is similar to timer 0 and timer 1. C/2 T selects UCT_Freq/12 (timer operation) or external input signal T2 (counter operation) as the timer register input. Setting TF2 to be incremented by the selected input.

Timer 2/ Capture Mode
In the capture mode, timer 2 functions as a 16-bit timer or counter. An overflow condition sets bit TF2, which you can use to request an interrupt. Setting the external enable bit EXEN2 allows the RCAP2Hand RCAP2L registers to capture the current value in timer registers TH2 and TL2 in response to a l-to-0 transition at external input T2EX. The transition at T2EX also sets bit EXF2 on T2CON. The EXF2 bit, like TF2, can generate an interrupt. TR2 has to be enabled when this mode is run.

Note: T2EX is tied to logic high and is not available in IT8502.

Figure 7-6. Timer 2: Capture Mode



Note: T2EX is tied to logic high and is not available in IT8502.

Timer 2/ Auto-reload Mode
The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. The timer operates as an up counter or up/down counter, as determined by the down counter enable bit (DCEN). At device reset, DCEN is cleared, so in the auto-reload mode, timer 2 defaults to operation as an up counter. TR2 has to be enabled when this mode is run.

Up Counter Operation
When DCEN = 0, timer 2 operates as an up counter. If EXEN = 0, timer 2 counts up to FFFFh and sets the TF2 overflow flag. The overflow condition loads the 16-bit value in the reload/capture registers (RCAP2H, RCAP2L) into the timer registers (TH2, TL2). The values in RCAP2H and RCAP2L are preset by software.

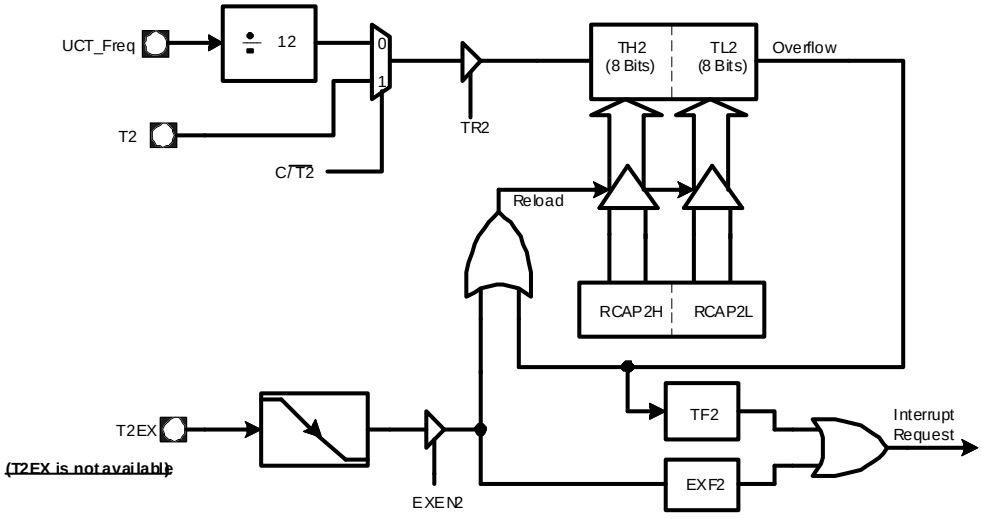
If EXEN2 = 1, the timer registers are reloaded by either a timer overflow or a high-to-low transition at external input T2EX. This transition also sets the EXF2 bit in the T2CON register. Either TF2 or EXF2 bit can generate a timer 2 interrupt request. TR2 has to be enabled when its mode is run.

Up/Down Counter Operation
When DCEN = 1, timer 2 operates as an up/down counter. External input signal T2EX controls the direction of the count. When T2EX is high, timer 2 counts up. The timer overflow occurs at FFFFh, which sets the timer 2 overflow flag (TF2) and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers (TH2, TL2) equals the value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and reloads FFFFh into the timer registers.

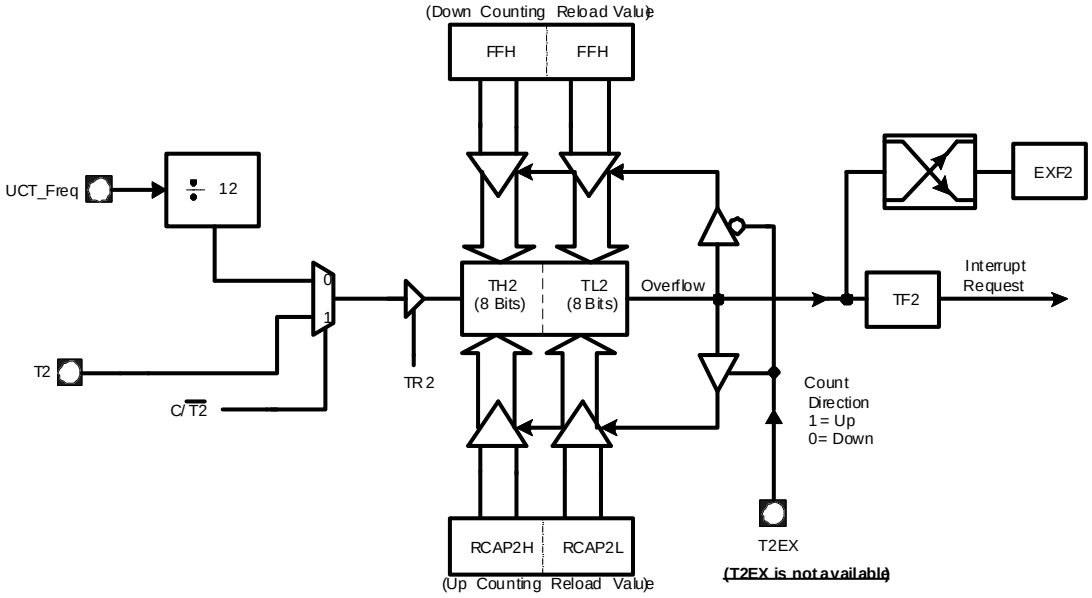
The EXF2 bit toggles when timer 2 overflows or underflows changing the direction of the count. When timer 2 operates as an up/down counter, EXF2 does not generate an interrupt. This bit can be used to provide 17-bit resolution. TR2 has to be enabled when his mode is run.

Figure 7-7. Timer 2: Auto Reload (DCEN = 0)



Note: T2EX is tied to logic high and is not available in IT8502.

Figure 7-8. Timer 2: Auto Reload Mode (DCEN = 1)



Note: T2EX is tied to logic high and is not available in IT8502.

Timer 2/ Baud Rate Generator Mode
This mode configures timer 2 as a baud rate generator for use with the serial port. Select this mode by setting the RCLK and/or TCLK bits in T2CON.

Timer 2/ Clock-out Mode
In the clock-out mode, timer 2 functions as a 50%-duty-cycle, variable-frequency clock. The input clock increments TL0 at frequency UCT_Freq/2. The timer repeatedly counts to overflow from a preloaded value. At overflow, the contents of the RCAP2H and RCAP2L registers are loaded into TH2/TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

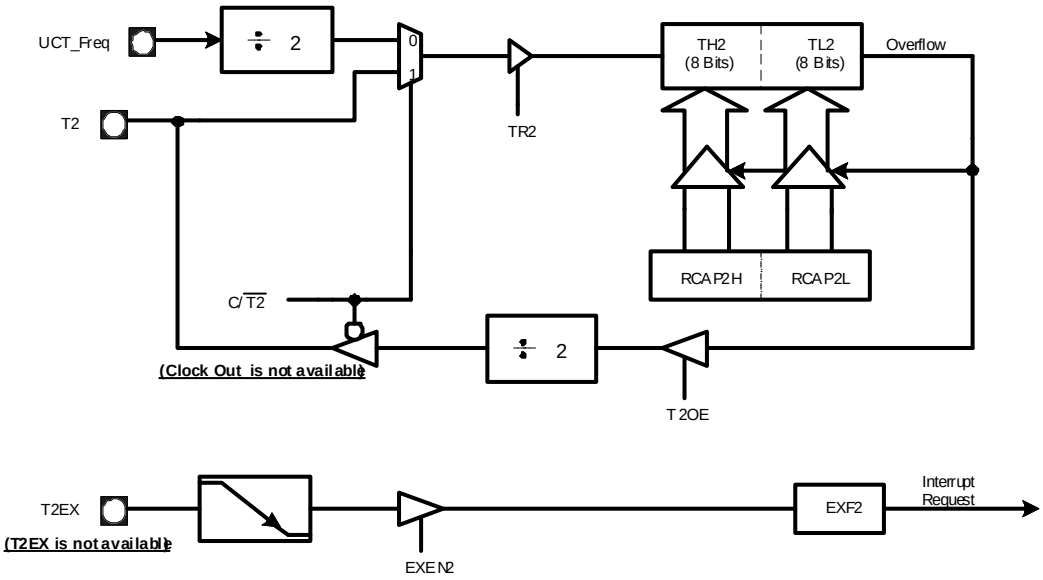
Clock-out Frequency = UCT_Freq / {4X(65536 - RCAP2H, RCAP2L)}

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 10-2 on page 352).

Table 7-3. Timer 2 Modes of Operation

Mode	RCLK OR TCLK (in T2COON)	CP/RL2# (in T2MOD)	T2OE (in T2MOD)
Auto-reload Mode	0	0	0
Capture Mode	0	1	0
Baud Rate Generator Mode	1	X	X
Programmable Clock-Out	X	0	1

Figure 7-9. Timer 2: Clock Out Mode

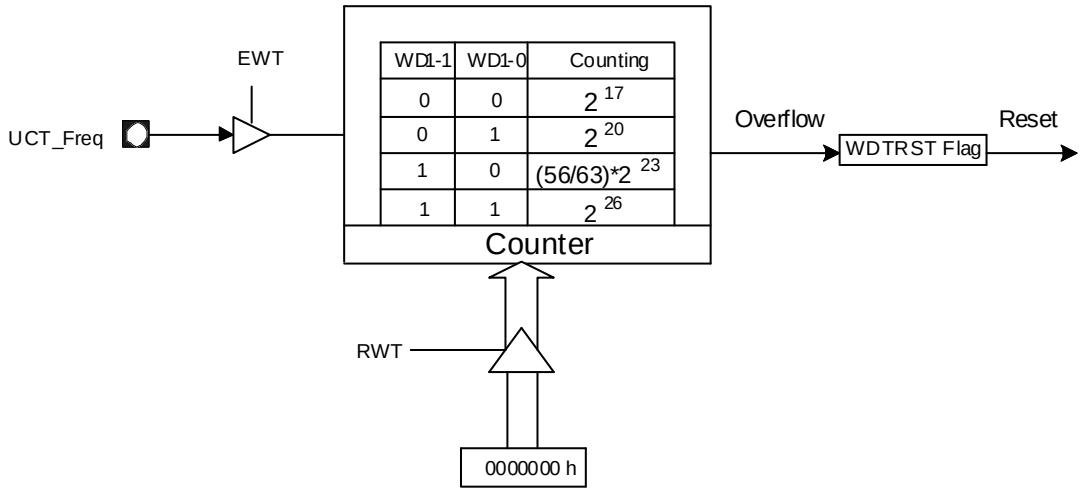


Note: T2EX is tied to logic high and is not available in IT8502.

Watchdog Timer

The watchdog timer has system reset functions. Users can set WD1-1, WD1-0 (in register CKCON, 8Eh) to choose 2^17, 2^20, (56/63)*2^23 or 2^26 counter for Watchdog Timer. After the Watchdog Timer counts the specific counter and an overflow occurs, set WDTRST Flag (in register WDTCON, D8h) and finally reset the 8032. If 8032 has been reset by Watchdog Timer, WDTEN Flag remains one.

Figure 7-10. Watchdog Timer



SERIAL I/O PORT

The serial I/O port provides both asynchronous communication modes. It operates as a universal asynchronous receiver and transmitter (UART) in three full-duplex modes (modes 1, 2, and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates.

Mode 1 and 3 operate over a wide range of baud rates, which are generated by timer 1 and timer 2.

The serial port signals are defined in Table of Serial Port Signals, and the serial port special function registers

(SBUF, SCON) are described in the section of Special Function Registers.

For the three asynchronous modes, the UART transmits on the TXD pin and receives on the RXD pin. The SBUF register, which holds received bytes and bytes to be transmitted, actually consists of two physically different registers. To send, software writes a byte to SBUF; to receive, software reads SBUF. The receive shift register allows reception of a second byte before the byte has been read from SBUF. However, if software has not read the first byte by the time the second byte is received, the second byte will overwrite the first. The UART sets interrupt bits TI and RI on transmission and reception respectively. These two bits share a single interrupt request and interrupt vector.

Figure 7-11. Serial Port Block Diagram

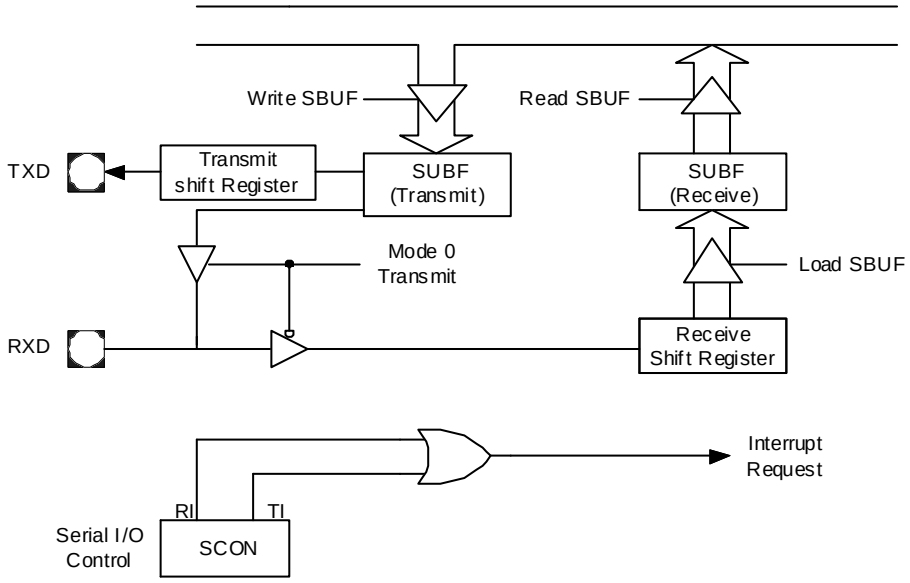


Table 7-4. Serial Port Signals

Function Name	Type	Description	Multiplexed With
TXD	O	Transmit Data. In modes 1, 2 and 3,TXD transmits serial data.	P3.1
RXD	I	Receive Data. In mode 1, 2 and 3, RXD receives serial data.	P3.0

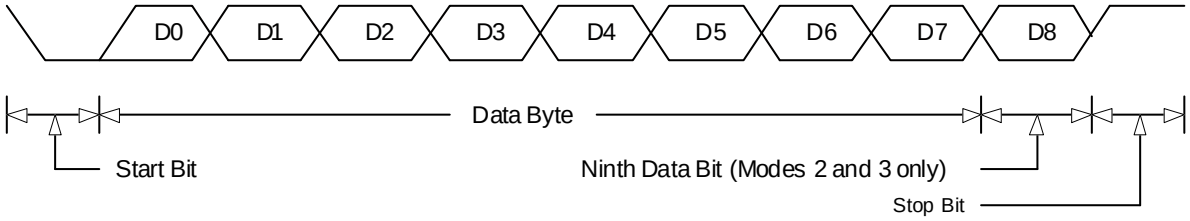
(Mode 0 is not available)

Asynchronous Modes (Modes 1, 2, and 3)
The serial port has three asynchronous modes of operation.

Mode 1
Mode 1 is a full-duplex and asynchronous mode. The data frame consists of 10 bits: one start bit, eight data bits, and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. When a message is received, the stop bit is read in the RB8 bit in the SCON register. The baud rate is generated by overflow of timer 1 or timer 2.

Mode 2 and 3
Mode 2 and 3 are full-duplex and asynchronous modes. The data frame consists of 11 bits: one start bit, eight data bits (transmitted and received LSB first), one programmable ninth data bit, and one stop bit which is read from the RB8 bit in the SCON register. On transmit, the ninth data bit is written to the TB8 bit in the SCON register. Alternatively, you can use the ninth bit as a command/data flag.
- In mode 2, the baud rate is programmable to 1/32 or 1/64 of the oscillator frequency.
- In mode 3, the baud rate is generated by overflow of timer 1 or timer 2.

Figure 7-12. Data Frame (Mode 1, 2 and 3)



Transmission (Mode 1, 2, 3)

Follow these steps below to initiate a transmission:
1. Write to the SCON register. Select the mode with the SM0 and SM1 bits, and clear the REN bit.
For mode 2 and 3, write the ninth bit to the TB8 bit.
2. Write the byte to be transmitted to the SBUF register. This write starts the transmission.

Reception (Mode 1, 2, 3)

To prepare for a reception, set the REN bit in the SCON register. The actual reception is then initiated by a detected high-to-low transition on the RXD pin.

Baud Rates

Baud Rates for Mode 2

Mode 2 has a two-baud rate, which is selected by the SMOD bit in the PCON register. The following expression defines the baud rate:
Serial I/O Mode 2 Baud Rate = (2 ^ SMOD) x (UCT_Freq / 64)
UCT_Freq equals to EC Clock Frequency (listed in Table 10-2 on page 352).

Baud Rates for Mode 1 and 3

In mode 1 and 3, the baud rate is generated by overflow of timer (default) and/or timer 2. You may select either or both timers to generate the baud rate(s) for the transmitter and/or the receiver.

Timer 1 Generated Baud Rates (Mode 1 and 3)

Timer 1 is the default baud rate generator for the transmitter and the receiver in mode 1 and 3. The baud rate is determined by the timer 1 overflow rate and the value of SMOD, as shown in the following formula:
Serial I/O Mode 1 and 3 Baud Rate = (2 ^ SMOD) x (Timer 1 Overflow Rate) / 32

Selecting Timer 1 as the Baud Rate Generator

To select timer 1 as the baud rate generator:
• Disable the timer interrupt by clearing the IE0 register.
• Configure timer 1 as a timer or an event counter (set or clear the C/T bit in the TMOD register).
Serial I/O Mode 1 and 3 Baud Rate = (2 ^ SMOD) x UCT_Freq / (32 x 12 x (256 – TH1))

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 10-2 on page 352).

• Select timer mode 0-3 by programming the M1 and M0 bits in the TMOD register.
In most applications, timer 1 is configured as a timer in auto-reload mode (high nibble of TMOD = 0010B). The resulting baud rate is defined by the following expression:
Timer 1 can generate very low baud rates by the following setups:
• Enable the timer 1 interrupt by setting the ET1 bit in the IE register.
• Configure timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B).
• Use the timer 1 interrupt to initiate a 16-bit software reload.

Timer 2 Generated Baud Rates (Mode 1 and 3)

Timer 2 may be selected as the baud rate generator for the transmitter and/or receiver. The baud rate generator mode of timer 2 is similar to the auto-reload mode. A rollover in the TH2 register reloads registers TH2 and TL2 with the 16-bit value on registers RCAP2H and RCAP2L, which are presented by software.
The baud rate of timer 2 is expressed by the following formula:
Serial I/O Mode 1 and 3 Baud Rate = (Timer 2 Overflow Rate) / 16

Selecting Timer 2 as the Baud Rate Generator

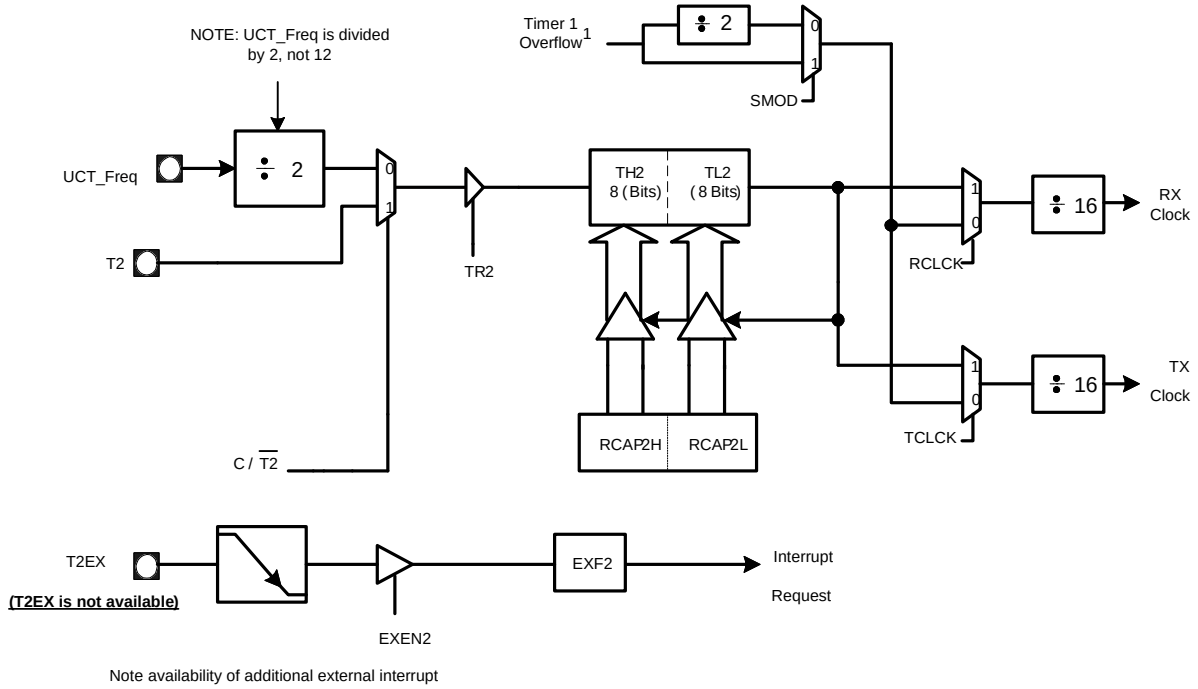
To select timer 2 as the baud rate generator for the transmitter and/or receiver, program the RCLCK and TCLCK bits in the T2CON register. Setting RCLK and/or TCLK puts timer 2 into its baud rate generator mode. In this mode, a rollover in the TH2 register does not set the TF2 bit in the T2CON register. Besides, a high-to-low transition at the T2EX input signal sets the EXF2 bit in the T2CON register but does not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). You can use the T2EX input signal as an additional external interrupt by setting the EXEN2 bit in T2CON.

Note: T2EX is tied to logic high and is not available in IT8502.
Note: Turn off the timer (clear the TR2 bit in the T2CON register) before accessing registers TH2, TL2, CAP2H and RCAP2L. You may configure timer 2 as a timer or a counter. In most applications, it is configured for timer operation (i.e., the C/T2 bit is cleared in the T2CON register).

Table 7-5. Selecting the Baud Rate Generator(s)

RCLK Bit	TCLCK Bit	Receiver Baud Rate Generator	Transmitter Baud Rate generator
0	0	Timer 1	Timer 1
0	1	Timer 1	Timer 2
1	0	Timer 2	Timer 1
1	1	Timer 2	Timer 2

Figure 7-13. Timer 2 in Baud Rate Generator Mode



Note: T2EX is tied to logic high and is not available in IT8502.

Note that timer 2 increments every state time (2Tosc) when it is in the baud rate generator mode. In the baud rate formula that follows, “RCAP2H, RCAP2L” denoting the contents of RCAP2H and RCAP2L is taken as a 16-bit unsigned integer:
Serial I/O Mode 1 and 3 Baud Rate = UCT_Freq x (32 X [65536 - (RCAP2H,RACAP2L)])

Note: UCT_Freq equals to EC Clock Frequency (listed in Table 10-2 on page 352).

When timer 2 is configured as a timer and is in baud rate generator mode, do not read or write the TH2 or TL2 registers. The timer is being incremented every state time, and the result of a read or write may not be accurate. In addition, you may read but not write to the RCAP2 registers; a write may overlap a reload and cause write and/or reload errors.

7.1.8 Idle and Doze/Sleep Mode

Idle Mode
When set IDL bit in PCON(87h), the 8032 will enter an Idle mode. In the Idle mode, the 8032 is idle while all the on-chip peripherals remain active. The internal RAM and SFRs registers remain unchanged during this mode. The Idle mode can be terminated by any enabled internal/external interrupt or by a hardware reset.

Doze/Sleep Mode
When PD bit is set in PCON(87h), the 8032 will enter a Doze/Sleep mode. In the Doze/Sleep mode, the 8032 clock is stopped, and PLL may be alive or stopped depending on PLLCTRL. The Doze/Sleep mode can be waked up by the hardware reset or by the external enabled interrupt with level trigger activation (ITx in register TCON is set to 0). The Program Counter, internal RAM and SFRs registers retain their values and will not be changed after the exiting Doze/Sleep mode by external interrupt. The reset will restart the 8032, while the SFRs with initial values and the internal RAM retain their values.

7.1.9 EC Internal Register Description

The embedded 8032 internal memory space and special function registers (F0h-80h) are listed below.

Table 7-6. Internal RAM Map

7							0	Index
Bank 0								07h-00h
Bank 1								0Fh-08h
Bank 2								17h-10h
Bank 3								1Fh-18h
Addressable Bits								2Fh-20h
General Purpose RAM								7Fh-2Fh
Indirect Addressing Register								FFh-80h

7							0	SFR Index
PCON	DPS	DPH1	DPL1	DPH	DPL	SP	P0	80h
	CKCON	TH1	TH0	TL1	TL0	TMOD	TCON	88h
							P1	90h
						SBUF	SCON	98h
							P2	A0h
							IE	A8h
							P3	B0h
							IP	B8h
		STATUS						C0h
		TH2	TL2	RCAP2H	RCAP2L	T2MOD	T2CON	C8h
							PSW	D0h
							WDTCON	D8h
							ACC	E0h
								E8h
MPREFC							B	F0h
								F8h

7.1.9.1 Port 0 Register (P0R)

Address: 80h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P0 Register Bit [7:0] (P0)** This is the 8-bit 8032 port 0.

7.1.9.2 Stack Pointer Register (SPR)

Address: 81h

Bit	R/W	Default	Description
7-0	R/W	07h	**Stack Pointer Bit [7:0] (SP)** This is the 8-bit stack pointer.

7.1.9.3 Data Pointer Low Register (DPLR)

Address: 82h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data Pointer Low Bit [7:0] (DPL)** This is the 8-bit data pointer low byte.

7.1.9.4 Data Pointer High Register (DPHR)

Address: 83h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data Pointer High Bit [7:0] (DPH)** This is the 8-bit data pointer high byte.

7.1.9.5 Data Pointer 1 Low Register (DP1LR)

Address: 84h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data Pointer 1 Low Bit [7:0] (DPL1)** This is the 8-bit data pointer 1 low byte.

7.1.9.6 Data Pointer 1 High Register (DP1HR)

Address: 85h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data Pointer 1 High Bit [7:0] (DPH1)** This is the 8-bit data pointer 1 high byte.

7.1.9.7 Data Pointer Select Register (DPSR)

Address: 86h

Bit	R/W	Default	Description
7-1	-	00h	**Reserved**
0	R/W	0b	**Data Pointer Select (DPS)** Setting '1' selects the data pointer 1 (DPL1, DPH1) while setting '0' selects the data pointer (DPL, DPH).

7.1.9.8 Power Control Register (PCON)

Address: 87h

Bit	R/W	Default	Description
7	R/W	0b	**Serial Port Double Baud Rate (SMOD1)** Setting '1' doubles the baud rate when timer 1 is used and mode 1, 2, or 3 is selected in SCON register.
6	-	0b	**Reserved**
5-2	-	0h	**Reserved**
1	R/W	0b	**Power Down Mode (PD)** Set "1" to enter a Sleep (a.k.a. power-down) or Doze mode immediately. The Sleep or Doze mode is controlled by PPDC bit. Exit Sleep or Doze mode and clear this bit by external interrupt or hardware reset.
0	R/W	0b	**Idle Mode (IDL)** Set "1" to enter idle mode immediately. Exit idle mode and clear this bit by internal interrupt and external interrupt or hardware reset.

7.1.9.9 Timer Control Register (TCON)

Address: 88h

Bit	R/W	Default	Description
7	R/W	0b	**Timer 1 Overflow (TF1)** This bit is set by hardware when timer 1 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
6	R/W	0b	**Timer 1 Run Control (TR1)** Setting '1' enables timer 1 operation and setting '0' disables timer 1.
5	R/W	0b	**Timer 0 Overflow (TF0)** This bit is set by hardware when timer 0 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
4	R/W	0b	**Timer 0 Run Control (TR0)** Setting '1' enables timer 0 operation and setting '0' disables the timer 0.
3	R/W	0b	**Interrupt 1 Edge Detect (IE1)** This bit is set by hardware when an edge or a level is detected on external INT1 (depends on the setting of **IT1**). This bit is cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.
2	R/W	0b	**Interrupt 1 Type Select (IT1)** Setting '1' selects the edge-triggered for INT1. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and needs IT0 and IT1 to be set as level-low triggered.
1	R/W	0b	**Interrupt 0 Edge Detect (IE0)** Set by hardware when an edge or a level is detected on external INT0 (depends on the setting of **IT0**). Cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.
0	R/W	0b	**Interrupt 0 Type Select (IT0)** Setting '1' selects the edge-triggered for INT0. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and needs IT0 and IT1 to be set as level-low triggered.

7.1.9.10 Timer Mode Register (TMOD)

Address: 89h

Bit	R/W	Default	Description
7	R/W	0b	**Timer 1 Gate (GATE1)** 0: Timer 1 will clock when **TR1**=1, regardless of the state of INT1. 1: Timer 1 will clock only when **TR1**=1 and INT1 is deasserted.
6	R/W	0b	**Timer 1 Source (SRC1)** 0: timer 1 counts the divided-down EC clock. 1: timer 1 counts negative transitions on T1 input of 8032 from TMRI0 pin.
5-4	R/W	0b	**Timer 1 Mode (MODE1)** 0h: 8-bit timer/counter (TH1) with 5-bit prescaler (TL1) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL1). Reload from TH1 at overflow. 3h: timer 1 halted. Retains count.
3	R/W	0b	**Timer 0 Gate (GATE0)** 0: Timer 0 will clock when TR0=1, regardless of the state of INT0. 1: Timer 0 will clock only when TR0=1 and INT0 is deasserted.
2	R/W	0b	**Timer 0 Source (SRC0)** 0: timer 0 counts the divided-down EC clock. 1: timer 0 counts negative transitions on T0 input of 8032 from GPE5.
1-0	R/W	0b	**Timer 0 Mode (MODE0)** 0h: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL0). Reload from TH0 at overflow. 3h: timer 0 halted. Retains count.

7.1.9.11 Timer 0 Low Byte Register (TL0R)

Address: 8Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 0 Low Byte Bit [7:0] (TL0)** Timer 0 low byte register.

7.1.9.12 Timer 1 Low Byte Register (TL1R)

Address: 8Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 1 Low Byte Bit [7:0] (TL1)** Timer 1 low byte register.

7.1.9.13 Timer 0 High Byte Register (TH0R)

Address: 8Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 0 High Byte Bit [7:0] (TH0)** Timer 0 high byte register.

7.1.9.14 Timer 1 Low Byte Register (TH1R)

Address: 8Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 1 High Byte Bit [7:0] (TH1)** Timer 1 high byte register.

7.1.9.15 Clock Control Register (CKCON)

Address: 8Eh

Bit	R/W	Default	Description
7-6	R/W	00b	**Watch Dog Time Out Counter Select (WD[1:0])** 0h: 17-bit counter 1h: 20-bit counter 2h: (56/63)*2^{23} counter 3h: 26-bit counter
5	R/W	0b	**Timer 2 Clock (T2M)** 0: timer 2 clock is EC clock / 12. 1: timer 2 clock is EC clock / 4.
4	R/W	0b	**Timer 1 Clock (T1M)** 0: timer 1 clock is EC clock / 12. 1: timer 1 clock is EC clock / 4.
3	R/W	0b	**Timer 0 clock (T0M)** 0: timer 0 clock is EC clock / 12. 1: timer 0 clock is EC clock / 4.
2-0	-	-	**Reserved**

7.1.9.16 Port 1 Register (P1R)

Address: 90h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P1 Register Bit [7:0] (P1)** This is the 8-bit 8032 port 1.

7.1.9.17 Serial Port Control Register (SCON)

Address: 98h

Bit	R/W	Default	Description
7	R/W	0b	**Serial Port Mode 0 (SM0_0)** Serial port mode control is set/cleared by software. Mode 1-3 are supported.
6	R/W	0b	**Serial Port Mode 1 (SM1_0)** Serial port mode control is set/cleared by software. Mode 1-3 are supported.
5	-	0b	**Reserved**
4	R/W	0b	**Receive Enable (REN)** Receiver enable bit. Setting '1' enables the serial data reception. Setting '0' disables the serial data reception.
3	R/W	0b	**Transmit Bit 8 (TB8)** Transmit bit 8, set/cleared by hardware to determine the state of the ninth data bit transmitted in 9-bit UART mode.
2	R/W	0b	**Receive Bit 8 (RB8)** Receive bit 8, set/cleared by hardware to determine the state of the ninth data bit received in 9-bit UART mode.
1	R/W	0b	**Transmit Interrupt (TI)** Transmit interrupt, set by hardware when the byte is transmitted and cleared by software after serving.
0	R/W	0b	**Receive Interrupt (RI)** Receive interrupt, set by hardware when the byte is received and cleared by software when data is processed.

7.1.9.18 Serial Port Buffer Register (SBUFR)

Address: 99h

Bit	R/W	Default	Description
7-0	R/W	00h	**Serial Port Buffer Bit [7:0] (SBUF)** This is the 8-bit 8032 serial port data buffer. Writing to **SBUF** loads the transmit buffer to the serial I/O port. Reading **SBUF** reads the receive buffer of the serial port.

7.1.9.19 Port 2 Register (P2R)

Address: A0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P2 Register Bit [7:0] (P2)** This is the 8-bit 8032 port 2.

7.1.9.20 Interrupt Enable Register (IE)

Address: A8h

Bit	R/W	Default	Description
7	R/W	0b	**Global Interrupt Enable (EA)** Setting this bit enables all interrupts that are individually enabled by bit 0-6. Clearing this bit disables all interrupts.
6	R/W	0b	**Serial Port 1 Interrupt Enable (ES1)** Setting this bit enables the serial port 1 interrupt.
5	R/W	0b	**Timer 2 Overflow Interrupt Enable (ET2)** Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0b	**Serial Port 0 Interrupt Enable (ES0)** Setting this bit enables the serial port 0 interrupt.
3	R/W	0b	**Timer 1 Overflow Interrupt Enable (ET1)** Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0b	**External Interrupt 1 Enable (EX1)** Setting this bit enables the external interrupt 1.
1	R/W	0b	**Timer01 Overflow Interrupt Enable (ET0)** Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0b	**External Interrupt 0 Enable (EX0)** Setting this bit enables the external interrupt 0.

7.1.9.21 Port 3 Register (P3R)

Address: B0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P3 Register Bit [7:0] (P3)** This is the 8-bit 8032 port 3.

7.1.9.22 Interrupt Priority Register (IP)

Address: B8h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	-	-	**Reserved**
5	R/W	0b	**Timer 2 Overflow Interrupt Priority (PT2)** Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0b	**Serial Port 0 Interrupt Priority (PS0)** Setting this bit enables the serial port 0 interrupt.
3	R/W	0b	**Timer 1 Overflow Interrupt Priority (PT1)** Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0b	**External Interrupt 1 Priority (PX1)** Setting this bit enables the external interrupt 1.
1	R/W	0b	**Timer01 Overflow Interrupt Priority (PT0)** Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0b	**External Interrupt 0 Priority (PX0)** Setting this bit enables the external interrupt 0.

7.1.9.23 Status Register (STATUS)

Address: C5h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**High priority interrupt status (HIP)**
5	R/W	0b	**Low priority interrupt status (LIP)**
4-2	-	-	**Reserved**
1	R/W	0b	**Serial Port 0 Transmit Activity Monitor (SPTA0)**
0	R/W	0b	**Serial Port 0 Receive Activity Monitor (SPRA0)**

7.1.9.24 Timer 2 Control Register (T2CON)

Address: C8h

Bit	R/W	Default	Description
7	R/W	0b	**Timer 2 Overflow (TF2)** Set by hardware when the timer 2 overflows. It has to be cleared by software. TF2 is not set if RCLK=1 or TCLK=1.
6	R/W	0b	**Timer 2 External Flag (EXF2)** If EXEN2=1, a capture or reload is caused by a negative transition on T2EX sets EFX2. EFX2 dose not cause an interrupt in up/down counter mode (DCEN=1).
5	R/W	0b	**Receive Clock (RCLK)** Selects timer 2 overflow pulses (RCLK=1) or timer 1 overflow pulses (RCLK=0) as the baud rate generator for port mode 1 and 3.
4	R/W	0b	**Receive Clock (RCLK)** Selects timer 2 overflow pulses (TCLK=1) or timer 1 overflow pulses (TCLK=0) as the baud rate generator for port mode 1 and 3.
3	R/W	0b	**Timer 2 External Enable (EXEN2)** Setting EXEN2 causes a capture or reload to occur as a result of a negative transition on T2EX unless timer 2 is being used as the baud rate generator for the serial port. Clearing EXEN2 causes timer 2 to ignore events at T2EX.
2	R/W	0b	**Timer 2 Run Control (TR2)** Setting this bit starts the timer.
1	R/W	0b	**Timer/Counter 2 Select (CT2)** 0: timer 2 counts the divided-down EC clock. 1: timer 2 counts negative transitions on T2 input of 8032 from TMRI1 pin.
0	R/W	0b	**Capture/Reload (CPRL2)** When this bit is set, captures occur on negative transitions at T2EX if EXEN2=1. When reloads occur o if EXEN2=1, the CP/ 2 RL bit is ignored and timer 2 is forced to auto-reload on timer 2 overflow if RCLK =1 or TCLK = 1.

7.1.9.25 Timer Mode Register (T2MOD)

Address: C9h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**Timer 2 Output Enable (T2OE)** In the timer 2 clock-out mode, this bit connects the programmable clock output to External signal T2.
0	R/W	0b	**Down Count Enable (DCEN)** This bit configures timer 2 as an up/down counter.

7.1.9.26 Timer 2 Capture Low Byte Register (RCAP2LR)

Address: CAh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 2 Capture Low Byte Bit [7:0] (RCAP2L)** Low byte of the timer2 reload/recapture register. This register stores 8-bit value to be loaded into or captured from the timer register TL2 in timer 2.

7.1.9.27 Timer 2 Capture High Byte Register (RCAP2HR)

Address: CBh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 2 Capture High Byte Bit [7:0] (RCAP2H)** High byte of the timer2 reload/recapture register. This register stores 8-bit value to be loaded into or captured from the timer register TH2 in timer 2.

7.1.9.28 Timer 2 Low Byte Register (TL2R)

Address: CCh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 2 Low Byte Bit [7:0] (TL2)** Timer 2 low byte register.

7.1.9.29 Timer 2 High Byte Register (TH2R)

Address: CDh

Bit	R/W	Default	Description
7-0	R/W	00h	**Timer 2 High Byte Bit [7:0] (TH2)** Timer 2 high byte register.

7.1.9.30 Program Status Word Register (PSW)

Address: D0h

Bit	R/W	Default	Description
7	R/W	0b	**Carry Flag (CF)** CY is set if the operation result in a carry out of (during addition) or a borrow into (during subtraction) the high-order bit in the result; otherwise CY is cleared.
6	R/W	0b	**Auxilary Carry Flag (AC)** AC is set if the operation result in a carry out of the low-order 4 bits of the result (during addition) or a borrow form the high-order bits into the low-order 4 bits (during subtraction); otherwise AC is cleared.
5	R/W	0b	**User Flag 0 (F0)** General-purpose flag.
4-3	R/W	0b	**Register Bank Select Bit [1:0](RS1:0)** 0h: bank 0, 00h-07h 1h: bank 1, 08h-0Fh 2h: bank 2, 10h-17h 3h: bank 3, 18h-1Fh
2	R/W	0b	**Overflow Flag (OV)** This bit is set if an addition or signed variables result in an overflow error (i.e., if the magnitude of the sum or difference is too great for the seven LSBs in 2's – complement representation). The overflow flag is also set if the multiplication product overflows one byte or if a division by zero is attempted.
1	R/W	0b	**User Defined Flag (UD)** General-purpose flag.
0	R/W	0b	**Parity Flag (P)** This bit indicates the parity of the accumulator. It is set if an odd number of bits in the accumulator is set. Otherwise, it is cleared. Not all instructions update the parity bit. The parity bit is set or cleared by instructions that change the contents to the accumulator.

7.1.9.31 Watch Dog Timer Control Register (WDTCON)

Address: D8h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6-2	-	-	**Reserved**
1	R/W	0b	**Watch Dog Timer Enable (WDTEN)** Setting '1' enables the watchdog timer.
0	R/W	0b	**Watch Dog Timer Reset (WDTRST)** Setting '1' resets the watchdog timer.

7.1.9.32 Accumulator Register (ACC)

Address: E0h

Bit	R/W	Default	Description
7-0	R/W	00h	**Accumulator Bit [7:0] (ACC[7:0])** The instruction uses the accumulator as both source and destination for calculations and moves.

7.1.9.33 B Register (BR)

Address: F0h

Bit	R/W	Default	Description
7-0	-	00h	**B Register (B[7:0])** The B Register is used as both a source and destination in multiply and divide operations.

7.1.9.34 Manual Prefetch Register (MPREFC)

Address: F7h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-0	W	-	**Manually Prefetch Count (MPREFCN)** This register is dedicated to clear internal dynamic caches. Refer to section 7.1.10.6 Code snippet of Clearing Dynamic Caches on page 159.

7.1.10 Programming Guide

7.1.10.1 IT8502 Coding Consideration

Coding consideration is to speed up the 8032 code-fetch performance while fetching from serial flash. There are some recommendations for coding consideration.

- If a code section is usually fetched, consider shadowing it to Scratch SRAM or let it be recognized by on-chip cache mechanism.
- Consider grouping usual fetched code and link them as a consecutive address in a code section, then shadow them to Scratch SRAM.
- The number of shadowed code sections are up five sections in different size and totally 4096 bytes. Also consider re-shadow different code sections while servicing different events.
- The on-chip cache mechanism automatically recognize a loop which is constructed with “CJNE” or “DJNZ” instruction.
- If a function contains only few bytes, consider replacing it with macro function.
- R8032TT code-fetch frequency is variable while fetching from serial flash. A delay routine which is formed by a loop routine can have a known delay time even code-fetch frequency is variable since the loop is fetched from loop or not. A delay routine can be implemented by WNCKR register. However, this is a simple way.

7.1.10.2 Code Snippet of Entering Idle/Doze/Sleep Mode

```
; Power-down ADC/DAC analog circuit
; Disable unnecessary channel of INTC/WUC

mov     dptr, #1e03h        ; PLLCTRL register
mov     a, #01h             ; 00h for Doze mode
                            ; 01h for Sleep mode
movx    @dptr, a

nop                         ; Reserved
orl     pcon, #01h          ; #01h for Idle mode
                            ; #02h for Doze/Sleep mode

; Repeat "nop" eight times immediately
; for internal bus turn-around
nop                         ; 1st
nop                         ; 2nd
nop                         ; 3rd
nop                         ; 4th
nop                         ; 5th
nop                         ; 6th
nop                         ; 7th
nop                         ; 8th
```

7.1.10.3 Code snippet of Copying Flash Content to Scratch ROM 4 (MOVC-MOVX by PIO)

```
        ; First copy data from code space to Scratch RAM in data space,
        ; then enable code space mapping of Scratch ROM

        ; copy 256 bytes from code space to scratch RAM
        ;   code space: ff00h ~ ffffh (byte)
        ;   data space: 0700h ~ 07ffh (byte)

        mov     r6, #00h
copy_loop:
        mov     dptr, #0ff00h           ; read from code space from ff00h (byte)
        mov     a, r6
        movc    a,  @a+dptr
        mov     dph, #07h               ; write to  data space from 0700h (byte)
        mov     dpl, r6
        movx    @dptr, a

        inc     r6
        cjne    r6, #00h, copy_loop     ; copy 256 bytes

        ; enable mapping Scratch SRAM to Scratch ROM
        mov     dptr, #104Eh            ; SCAR4H register
        mov     a, #03h                 ; disable code space mapping first
        movx    @dptr, a

        mov     dptr, #104Ch            ; SCAR4L register
        mov     a, #00h                 ;
        movx    @dptr, a

        mov     dptr, #104Dh            ; SCAR4 register
        mov     a, #0ffh                ;
        movx    @dptr, a

        mov     dptr, #104Eh            ; SCAR4H register
        mov     a, #00h                 ;
        movx    @dptr, a                ; enable code space mapping
```

7.1.10.4 Code snippet of Copying Flash Content to Scratch ROM (DMA)

```
        ; DMA copies256 bytes from code space to scratch RAM then
        ;   enable code space mapping
        ;
        ;   code space: ff00h ~ ffffh (byte)
        ;   data space: 0700h ~ 07ffh (byte)

        mov     dptr, #104Eh        ; SCAR4H register
        mov     a, #80h             ;
        movx    @dptr, a

        mov     dptr, #104Ch        ; SCAR4L register
        mov     a, #00h             ;
        movx    @dptr, a

        mov     dptr, #104Dh        ; SCAR4 register
        mov     a, #0ffh            ;
        movx    @dptr, a

        mov     dptr, #104Eh        ; SCAR4H register
        mov     a, #00h             ;
        movx    @dptr, a            ; start DMA then enable code space mapping
```

7.1.10.5 Code snippet of Changing PLL Frequency

```
        mov     b,#07h              ; let reg. b = new PLLFREQR value
        mov     dptr,#1e06h         ; PLLFREQR reg. addr
        movx    a,@dptr             ; check whether PLLFREQR value
        cjne    a,b,pll_chgfreq     ;
        sjmp    bypass_pll_chgfreq

pll_chgfreq:
        xch     a,b
        movx    @dptr,a             ;    modify PLLFREQR reg.

        mov     dptr,#1e03h         ; PLLCTRL reg. addr.
        mov     a,#01h              ; 1: Sleep mode; 0: Doze mode
        movx    @dptr,a             ;    modify PLLCTRL reg.

        clr     ea                  ; intentionally clear EA
        orl     pcon,#02h           ; enter Sleep mode then immediately
                                    ;   wakeup with new frequency
        nop
        nop
        nop
        nop
        nop
        nop
        nop
        nop

bypass_pll_chgfreq:
        .....
```

7.1.10.6 Code snippet of Clearing Dynamic Caches

```
; after flash is modified by the host program, the dynamic caches has to be
; cleared since they contain old and invalid cache content
; uC should execute these lines if the program counter leaves Scratch ROM

mov     0f7h, #01h ; MPREFC reg
nop
mov     0f7h, #01h ; MPREFC reg
nop
mov     0f7h, #01h ; MPREFC reg
nop
mov     0f7h, #01h ; MPREFC reg
nop
```

7.1.10.7 Code snippet of EC Base Signature

```
org     40h                     ;  available list: 40h, 50h
                                ;  ... E0h, F0h (interval 10h)

db      0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h, 0A5h
db      085h, 012h, 05Ah, 05Ah, 0AAh, 0AAh, 055h, 055h
```

7.2 Interrupt Controller (INTC)

7.2.1 Overview

INTC mainly collects several interrupts from modules. Using interrupt driven design has a better performance than polling-driven.

It traps PWRFAIL#, ROM match interrupt and samples interrupt channels, then outputs to the INT0# and INT1# of 8032.

Both interrupts INT0# and INT1# to 8032 are generated by INTC, and don't write 1 to IT0 and IT1 bit in TCON because interrupt triggered type is considered in INTC and needs IT0 and IT1 to be set as level-low triggered.

Note INT0# and INT1# are external interrupts of 8032 and they are controlled by EA, EX0 and EX1 in IE register.

External interrupts can wakeup 8032 from Idle/Doze/Sleep mode, but internal interrupts can wakeup 8032 from Idle mode only.

7.2.2 Features

- Configurable level-triggered and edge-triggered mode
- Configurable interrupt polarity of triggered mode
- Clear registers for edge-triggered interrupts
- Each interrupt source can be enabled/masked individually
- Special handler for power-fail (INT0# of 8032)

7.2.3 Functional Description

7.2.3.1 Power Fail Interrupt

The INTC collects interrupts sources from internal and external (through WUC) and provides two interrupt requests INT0# and INT1# to 8032. 8032 treats INT0# as a higher priority interrupt request than INT1#. INTC uses INT0# as a power-fail interrupt and INT1# as a maskable interrupt. The firmware should enable the IE0 and IE1 bit in TCON before all.

To implement a power-fail application, connect GPB7 to external circuit. Firmware puts the GPB7 in alternative function, enables the Schmitt Trigger of GPB7 to receive an asynchronous external input, and provides related INT0# interrupt routine.

There are two methods to trap a power-fail event: “Trap Enabled” and “Trap Enabled and Locked”. Users select “Trap Enabled” by setting TREN bit in PFAILR and select “Trap Enabled and Locked” by setting TRENL bit in PFAILR. If both bits are selected, TREN bit is ignored. If “Trap Enabled” is used, power-fail event is detected by falling edge transition of PWRFAIL#, and INT0# to 8032 is asserted. After INT0# is set, TREN bit is cleared. “Trap Enabled and Locked” method is similar to “Trap Enabled” method but TRENL will not be cleared after INT0# is set.

7.2.3.2 ROM Match Interrupt

Refer to section 7.20 Debugger (DBGR) on page 332.

7.2.3.3 Programmable Interrupts

INTC also collects 72 maskable interrupt sources and make a request on INT1 # of 8032 if triggered. Each channel can be individually enabled or masked by IERx. If an interrupt channel is masked and one interrupt request is triggered, the request is masked (inhibited, not canceled), and will be asserted the request on INT1# if it is enabled.

The ISRx indicates the status of interrupt regardless of IERx. In the level-triggered mode, ISRx is affected by corresponding interrupt sources, and firmware should clear the interrupt status on interrupt sources after its request is handled. In edge-triggered mode, ISRx is set by selected edge transition (determined by IELMRx) of corresponding interrupts sources, and firmware should write 1 to clear to ISRx after this request is handled.

Firmware may use the IVECT to determine which channel is to be serviced first or have its priority rule by reading ISRx and IERx. IVECT treats INT1 as the lowest priority interrupt and INT79 as the highest priority interrupt.

The 8032 always wakes up from Idle/Doze/Sleep mode when it detects an enabled external interrupt and it wakes up from Idle mode by internal interrupt, too. Firmware should disable unwanted interrupt sources to prevent from waking up unexpectedly.

Normally interrupts from WUC are high level-triggered. Note that interrupts from WUC are not always level-triggered interrupts since they may be just throughout WUC if the corresponding channels at WUC are disabled (bypassed). If an edge-triggered passes through WUC and INTC with WUC corresponding channel is disabled and INTC corresponding channel is level-trig mode, it may cause 8032 interrupt routine called but finds no interrupt source to service, or it may cause 8032 to wake up from Idle/Doze/Sleep mode and enters interrupt routine but finds no interrupt source to service.

7.2.4 EC Interface Registers

The EC interface registers are listed below. The base address for INTC is 1100h.

Table 7-7. EC View Register Map, INTC

7	0	Offset
Interrupt Status Register 0 (ISR0)		00h
Interrupt Status Register 1 (ISR1)		01h
Interrupt Status Register 2 (ISR2)		02h
Interrupt Status Register 3 (ISR3)		03h
Interrupt Status Register 4 (ISR4)		14h
Interrupt Status Register 6 (ISR6)		1Ch
Interrupt Status Register 7 (ISR7)		20h
Interrupt Status Register 8 (ISR8)		24h
Interrupt Status Register 9 (ISR9)		28h
Interrupt Enable Register 0 (IER0)		04h
Interrupt Enable Register 1 (IER1)		05h
Interrupt Enable Register 2 (IER2)		06h
Interrupt Enable Register 3 (IER3)		07h
Interrupt Enable Register 4 (IER4)		15h
Interrupt Enable Register 6 (IER6)		1Dh
Interrupt Enable Register 7 (IER7)		21h
Interrupt Enable Register 8 (IER8)		25h
Interrupt Enable Register 9 (IER9)		29h
Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)		08h
Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)		09h
Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)		0Ah
Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)		0Bh
Interrupt Edge/Level-Triggered Mode Register 4 (IELMR4)		16h
Interrupt Edge/Level-Triggered Mode Register 6 (IELMR6)		1Eh
Interrupt Edge/Level-Triggered Mode Register 7 (IELMR7)		22h
Interrupt Edge/Level-Triggered Mode Register 8 (IELMR8)		26h
Interrupt Edge/Level-Triggered Mode Register 9 (IELMR9)		2Ah
Interrupt Polarity Register 0 (IPOLR0)		0Ch
Interrupt Polarity Register 1 (IPOLR1)		0Dh
Interrupt Polarity Register 2 (IPOLR2)		0Eh
Interrupt Polarity Register 3 (IPOLR3)		0Fh
Interrupt Polarity Register 4 (IPOLR4)		17h
Interrupt Polarity Register 6 (IPOLR6)		1Fh
Interrupt Polarity Register 7 (IPOLR7)		23h
Interrupt Polarity Register 8 (IPOLR8)		27h
Interrupt Polarity Register 9 (IPOLR9)		2Bh
Interrupt Vector Register (IVECT)		10h
INT0# status (INT0ST)		11h
Power Fail Register (PFAILR)		12h

7.2.4.1 Interrupt Status Register 0 (ISR0)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 00h

Bit	R/W	Default	Description
7-1	R/WC Or R	-	**Interrupt Status (IS7-1)** It indicates the interrupt input status of INTx. INTST7 to INTST1 correspond to INT7 to INT1 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.
0	R	0b	**Reserved**

7.2.4.2 Interrupt Status Register 1 (ISR1)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS15-8)** It indicates the interrupt input status of INTx. INTST15 to INTST8 correspond to INT15 to INT8 respectively.

7.2.4.3 Interrupt Status Register 2 (ISR2)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS23-16)** It indicates the interrupt input status of INTx. INTST23 to INTST16 correspond to INT23 to INT16 respectively.

7.2.4.4 Interrupt Status Register 3 (ISR3)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS31-24)** It indicates the interrupt input status of INTx. INTST31 to INTST24 correspond to INT31 to INT24 respectively.

7.2.4.5 Interrupt Status Register 4 (ISR4)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS39-32)** It indicates the interrupt input status of INTx. INTST39 to INTST32 correspond to INT39 to INT32 respectively.

7.2.4.6 Interrupt Status Register 6 (ISR6)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS55-48)** It indicates the interrupt input status of INTx. INTST55 to INTST48 correspond to INT55 to INT48 respectively.

7.2.4.7 Interrupt Status Register 7 (ISR7)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS63-56)** It indicates the interrupt input status of INTx. INTST63 to INTST56 correspond to INT63 to INT56 respectively.

7.2.4.8 Interrupt Status Register 8 (ISR8)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS71-64)** It indicates the interrupt input status of INTx. INTST71 to INTST64 correspond to INT71 to INT64 respectively.

7.2.4.9 Interrupt Status Register 9 (ISR9)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS79-72)** It indicates the interrupt input status of INTx. INTST79 to INTST72 correspond to INT79 to INT72 respectively.

7.2.4.10 Interrupt Enable Register 0 (IER0)

Address Offset: 04h

Bit	R/W	Default	Description
7-1	R/W	0h	**Interrupt Enable (IE7-0)** Each bit determines whether its corresponding interrupt channel (INT7-0) is masked or enabled. Note that it has no effect on INT0 0: Masked 1: Enabled
0	-	0b	**Reserved**

7.2.4.11 Interrupt Enable Register 1 (IER1)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE15-8)** Each bit determines whether its corresponding interrupt channel (INT15-8) is masked or enabled.

7.2.4.12 Interrupt Enable Register 2 (IER2)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE23-16)** Each bit determines whether its corresponding interrupt channel (INT23-16) is masked or enabled.

7.2.4.13 Interrupt Enable Register 3 (IER3)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE31-24)** Each bit determines whether its corresponding interrupt channel (INT31-24) is masked or enabled.

7.2.4.14 Interrupt Enable Register 4 (IER4)

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE39-32)** Each bit determines whether its corresponding interrupt channel (INT39-32) is masked or enabled.

7.2.4.15 Interrupt Enable Register 6 (IER6)

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE55-48)** Each bit determines whether its corresponding interrupt channel (INT55-48) is masked or enabled.

7.2.4.16 Interrupt Enable Register 7 (IER7)

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE63-56)** Each bit determines whether its corresponding interrupt channel (INT63-56) is masked or enabled.

7.2.4.17 Interrupt Enable Register 8 (IER8)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE71-64)** Each bit determines whether its corresponding interrupt channel (INT71-64) is masked or enabled.

7.2.4.18 Interrupt Enable Register 9 (IER9)

Address Offset: 29h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE79-72)** Each bit determines whether its corresponding interrupt channel (INT79-72) is masked or enabled.

7.2.4.19 Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)

It determines whether its corresponding interrupt channel is level-triggered or edge-triggered.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00000000b	**Interrupt Edge/Level-Triggered Mode (IELM7-0)** Each bit determines the triggered mode of the corresponding interrupt channel (INT7-0). 0: Level-triggered 1: Edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

7.2.4.20 Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00000000b	**Interrupt Edge/Level-Triggered Mode (IELM15-8)** Each bit determines the triggered mode of the corresponding interrupt channel (INT15-8).

7.2.4.21 Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00011100b	**Interrupt Edge/Level-Triggered Mode (IELM23-16)** Each bit determines the triggered mode of the corresponding interrupt channel (INT23-16).

7.2.4.22 Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	01100000b	**Interrupt Edge/Level-Triggered Mode (IELM31-24)** Each bit determines the triggered mode of the corresponding interrupt channel (INT31-24).

7.2.4.23 Interrupt Edge/Level-Triggered Mode Register 4 (IELMR4)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R	11111111b	**Interrupt Edge/Level-Triggered Mode (IELM39-32)** Each bit determines the triggered mode of the corresponding interrupt channel (INT39-32).

7.2.4.24 Interrupt Edge/Level-Triggered Mode Register 6 (IELMR6)

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	00000000b	**Interrupt Edge/Level-Triggered Mode (IELM55-48)** Each bit determines the triggered mode of the corresponding interrupt channel (INT55-48).

7.2.4.25 Interrupt Edge/Level-Triggered Mode Register 7 (IELMR7)

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R	11110111b	**Interrupt Edge/Level-Triggered Mode (IELM63-56)** Each bit determines the triggered mode of the corresponding interrupt channel (INT63-56).

7.2.4.26 Interrupt Edge/Level-Triggered Mode Register 8 (IELMR8)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R	00000000b	**Interrupt Edge/Level-Triggered Mode (IELM71-64)** Each bit determines the triggered mode of the corresponding interrupt channel (INT71-64).

7.2.4.27 Interrupt Edge/Level-Triggered Mode Register 9 (IELMR9)

Address Offset: 2Ah

Bit	R/W	Default	Description
7-0	R	00000000b	**Interrupt Edge/Level-Triggered Mode (IELM79-72)** Each bit determines the triggered mode of the corresponding interrupt channel (INT79-72).

7.2.4.28 Interrupt Polarity Register 0 (IPOLR0)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL7-0)** Each bit determines the active high/low of the corresponding interrupt channel (INT7-0). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered Always write-1-clear to the corresponding bit in ISR register after modifying these bits if edge-triggered is selected.

7.2.4.29 Interrupt Polarity Register 1 (IPOLR1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL15-8)** Each bit determines the active high/low of the corresponding interrupt channel (INT15-8).

7.2.4.30 Interrupt Polarity Register 2 (IPOLR2)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL23-16)** Each bit determines the active high/low of the corresponding interrupt channel (INT23-16

7.2.4.31 Interrupt Polarity Register 3 (IPOLR3)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL31-24)** Each bit determines the active high/low of the corresponding interrupt channel (INT31-24).

7.2.4.32 Interrupt Polarity Register 4 (IPOLR4)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R	0h	**Interrupt Polarity (IPOL39-32)** Each bit determines the active high/low of the corresponding interrupt channel (INT39-32).

7.2.4.33 Interrupt Polarity Register 6 (IPOLR6)

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	0h	**Interrupt Polarity (IPOL55-48)** Each bit determines the active high/low of the corresponding interrupt channel (INT55-48).

7.2.4.34 Interrupt Polarity Register 7 (IPOLR7)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R	0h	**Interrupt Polarity (IPOL63-56)** Each bit determines the active high/low of the corresponding interrupt channel (INT63-56).

7.2.4.35 Interrupt Polarity Register 8 (IPOLR8)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R	0h	**Interrupt Polarity (IPOL71-64)** Each bit determines the active high/low of the corresponding interrupt channel (INT71-64).

7.2.4.36 Interrupt Polarity Register 9 (IPOLR9)

Address Offset: 2Bh

Bit	R/W	Default	Description
7-0	R	0h	**Interrupt Polarity (IPOL79-72)** Each bit determines the active high/low of the corresponding interrupt channel (INT79-72).

7.2.4.37 Interrupt Vector Register (IVCT)

Address Offset: 10h

Bit	R/W	Default	Description
7	R	0b	**Reserved**
6-0	R	0010000b	**Interrupt Vector (IVECT)** It contains the interrupt number, which is the highest priority, enabled and pending interrupt. The valid values range from 10h. Note that INT1 has the lowest priority. If no enabled interrupt is pending, it returns 10h.

7.2.4.38 8032 INT0# Status (INT0ST)

INT0PF is set when falling edge transition of PWRFAIL# with TREN or TRENL bit in PFAILR is set, and it is clear when being reset or read its content.

INT0RM is set when the trigger address matches the 8032 program counter.

Address Offset: 11h

Bit	R/W	Default	Description
7-1	-	00h	**Reserved**
1	R	-	**INT0# from ROM Match Status (INT0RM)** 0: INT0# is deasserted by an 8032 ROM match. 1: INT0# is asserted by an 8032 ROM match.
0	R	-	**INT0# from PWRFAIL# Status (INT0PF)** 0: INT0# is deasserted by a power-fail. 1: INT0# is asserted by a power-fail.

7.2.4.39 Power Fail Register (PFAILR)

It provides two methods to trap the PWRFAIL# event.
This register can't be reset by WDT Reset.

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**PWRFAIL# Trap Enabled and Locked (TRENL)** Firmware sets this bit to enable PWRFAIL# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of PWRFAIL# is detected. This bit can't be cleared by writing 0 to it until reset. 0: No PWRFAIL# Trap 1: PWRFAIL# Trap
1	R	-	**PWRFAIL# Status (PFAILST)** 0: PWRFAIL# is low (asserted) 1: PWRFAIL# is high (deasserted)
0	R/W	0b	**PWRFAIL# Trap Enabled (TREN)** Firmware sets this bit to enable PWRFAIL# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of PWRFAIL# is detected, and TREN will be cleared. This bit is ignored when TRENL bit is set. 0: No PWRFAIL# Trap 1: PWRFAIL# Trap

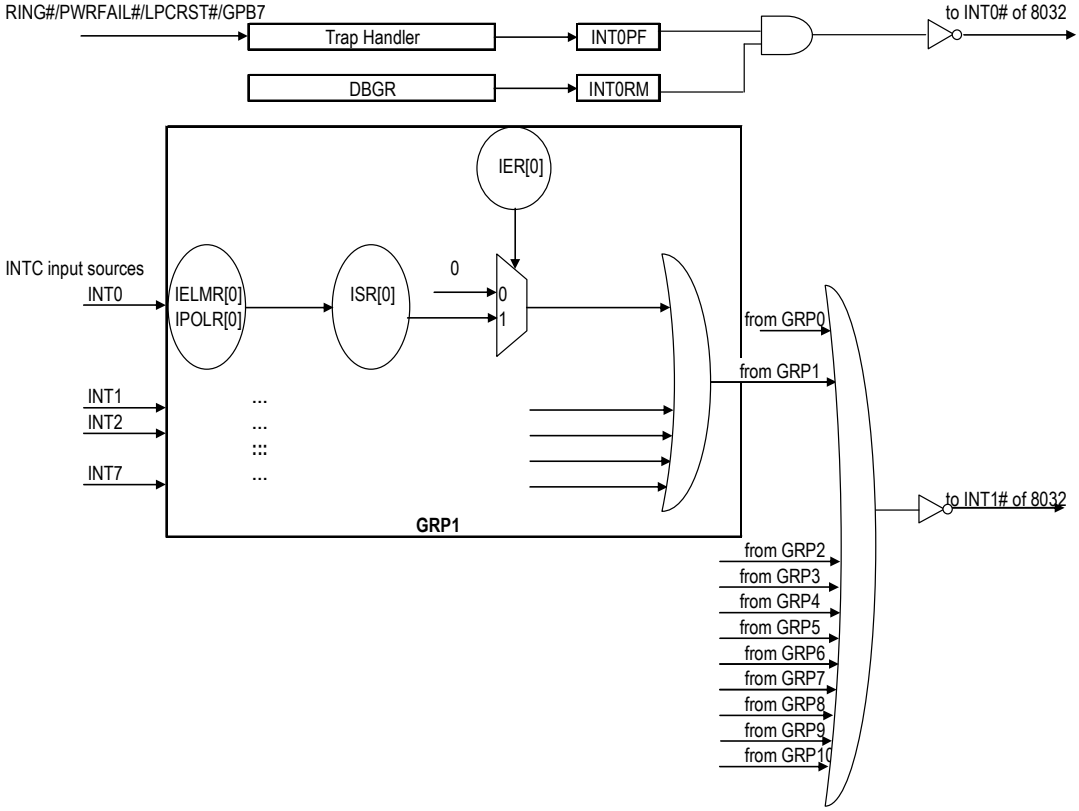
7.2.5 INTC Interrupt Assignments

Table 7-8. INTC Interrupt Assignments

Interrupt	Source	Default Type(Adjustable)	Description	Reference
INT0	Reserved	-	-	-
INT1	External/WUC	High-Level Trig	WKO[20]	Figure 7-16, p183
INT2	Internal	High-Level Trig	KBC Output Buffer Empty Interrupt	Section 6.5.3, p107
INT3	Internal	High-Level Trig	PMC Output Buffer Empty Intr. PMC1 Output Buffer Empty Intr.	Section 6.6.3.1, p113 Section 6.6.3.1, p113
INT4	Internal	High-Level Trig	SMBus D Interrupt	Section 7.7.3.1, p209
INT5	External/WUC	High-Level Trig	WKINTAD (WKINTA or WKINTD)	Figure 7-16, p183
INT6	External/WUC	High-Level Trig	WKO[23]	Figure 7-16, p183
INT7	Internal	High-Level Trig	PWM Interrupt	Section 7.11.4.17, p270
INT8	Internal	High-Level Trig	ADC Interrupt	Section 7.10.3.1, p247
INT9	Internal	High-Level Trig	SMBus A Interrupt	Section 7.7.3.1, p209
INT10	Internal	High-Level Trig	SMBus B Interrupt	Section 7.7.3.1, p209
INT11	Internal	High-Level Trig	KB Matrix Scan Interrupt	Section 7.4.2, p185
INT12	External/WUC	High-Level Trig	WKO[26]	Figure 7-16, p183
INT13	External/WUC	High-Level Trig	WKINTC	Figure 7-16, p183
INT14	External/WUC	High-Level Trig	WKO[25]	Figure 7-16, p183
INT15	-	-	-	-
INT16	Internal	High-Level Trig	SMBus C Interrupt	Section 7.7.3.1, p209
INT17	External/WUC	High-Level Trig	WKO[24]	Figure 7-16, p183
INT18	Internal	Rising-Edge Trig	PS/2 Interrupt 2	Section 7.8.2, p240
INT19	Internal	Rising-Edge Trig	PS/2 Interrupt 1	Section 7.8.2, p240
INT20	Internal	Rising-Edge Trig	PS/2 Interrupt 0	Section 7.8.2, p240
INT21	External/WUC	High-Level Trig	WKO[22]	Figure 7-16, p183
INT22	Internal	High-Level Trig	SMFI Semaphore Interrupt	Section 6.3.4.6, p83
INT23	-	-	-	-
INT24	Internal	High-Level Trig	KBC Input Buffer Full Interrupt	Section 6.5.3, p107
INT25	Internal	High-Level Trig	PMC Input Buffer Full Interrupt PMC1 Input Buffer Full Interrupt	Section 6.6.3.1, p113 Section 6.6.3.1, p113
INT26	Internal	High-Level Trig	PMC2 Output Buffer Empty Intr.	Section 6.6.3.1, p113
INT27	Internal	High-Level Trig	PMC2 Input Buffer Full Intr.	Section 6.6.3.1, p113
INT28	External	High-Level Trig	GINT from function 1 of GPD5	Table 5-14, p22
INT29	Internal	Rising-Edge Trig	EGPC Interrupt	Section 7.16.3, p305
INT30	Internal	Rising-Edge Trig	External Timer 1 Interrupt	Section 7.14.3, p292
INT31	External/WUC	High-Level Trig	WKO[21]	Figure 7-16, p183
INT32	Internal	Rising-Edge Trig (Not Adjustable)	GPINT0	Section 6.2.11.10, p64
INT33	Internal		GPINT1	Section 6.2.11.10, p64
INT34	Internal		GPINT2	Section 6.2.11.10, p64
INT35	Internal		GPINT3	Section 6.2.11.10, p64
INT36	-		-	-
INT37	Internal		SSPI Interrupt	Section 7.18.5.2, p315
INT38	Internal		UART1 Interrupt	Section 7.19.5.3, p322
INT39	-		-	-

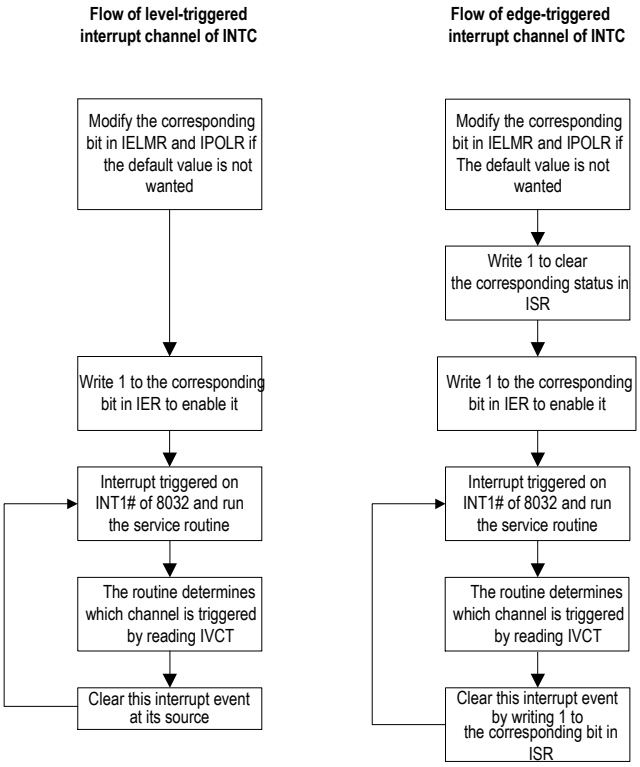
Interrupt	Source	Default Type(Adjustable)	Description	Reference
-	-	-	-	-
INT48	External/WUC	High-Level Trig (Not Adjustable)	WKO[60]	Figure 7-16, p183
INT49	External/WUC		WKO[61]	Figure 7-16, p183
INT50	External/WUC		WKO[62]	Figure 7-16, p183
INT51	External/WUC		WKO[63]	Figure 7-16, p183
INT52	External/WUC		WKO[64]	Figure 7-16, p183
INT53	External/WUC		WKO[65]	Figure 7-16, p183
INT54	External/WUC		WKO[66]	Figure 7-16, p183
INT55	External/WUC		WKO[67]	Figure 7-16, p183
INT56	-	Rising-Edge Trig (Not Adjustable)	-	-
INT57	-		-	-
INT58	Internal		External Timer 2 Interrupt	Section 7.14.3, p292
INT59	Internal	High-Level Trig (Not Adjustable)	Deferred SPI Instruction Interrupt	Section 6.3.4.40, p91
INT60	Internal	Rising-Edge Trig (Not Adjustable)	TMRINTA0	7.12.3.6, p278
INT61	Internal		TMRINTA1	7.12.3.6, p278
INT62	Internal		TMRINTB0	7.12.3.6, p278
INT63	Internal		TMRINTB1	7.12.3.6, p278
INT64	Internal	High-Level Trig (Not Adjustable)	PMC2EX Output Buffer Empty Intr.	Section 6.6.3.1, p113
INT65	Internal		PMC2EX Input Buffer Full Intr.	Section 6.6.3.1, p113
INT66	Internal		PMC3 Output Buffer Empty Intr.	Section 6.6.3.1, p113
INT67	Internal		PMC3 Input Buffer Full Intr.	Section 6.6.3.1, p113
INT68	-	-	-	-
INT69	-	-	-	-
INT70	-	-	-	-
INT71	-	-	-	-
INT72	External/WUC	High-Level Trig (Not Adjustable)	WKO[70]	Figure 7-16, p183
INT73	External/WUC		WKO[71]	Figure 7-16, p183
INT74	External/WUC		WKO[72]	Figure 7-16, p183
INT75	External/WUC		WKO[73]	Figure 7-16, p183
INT76	External/WUC		WKO[74]	Figure 7-16, p183
INT77	External/WUC		WKO[75]	Figure 7-16, p183
INT78	External/WUC		WKO[76]	Figure 7-16, p183
INT79	External/WUC		WKO[77]	Figure 7-16, p183

Figure 7-14. INTC Simplified Diagram



7.2.6 Programming Guide

Figure 7-15. Program Flow Chart for INTC



Note: The routine may has its own interrupt priority by reading ISR register.
Note: If this channel source comes from WUC, the corresponding bit in WUESR needs to be cleared, too

7.3 Wake-Up Control (WUC)

7.3.1 Overview

WUC groups internal and external inputs, and asserts wake-up signals to INTC that allows 8032 to exit an Idle/Doze/Sleep mode.

7.3.2 Features

- Supports up to 48 wake-up, internal and external interrupt inputs.
- Supports both the rising-edge and falling-edge triggered mode.
- Input can be connected to INTC directly.

7.3.3 Functional Description

Input sources of WUC are external inputs such as pins about PS/2, GPIO and KB Matrix Scan, or inputs from internal module such as SWUC, LPC and SMBus that handle external inputs.

Each channel can be selected to be rising or falling edge triggered mode. If one channel is disabled, the input bypasses WUC pending logic and is connected directly to INTC.

7.3.4 EC Interface Registers

The EC interface registers are listed below. The base address for WUC is 1B00h.

Table 7-9. EC View Register Map, WUC

7	0	Offset
Wake-Up Edge Mode Register 1 (WUEMR1)		00h
Wake-Up Edge Mode Register 2 (WUEMR2)		01h
Wake-Up Edge Mode Register 3 (WUEMR3)		02h
Wake-Up Edge Mode Register 4 (WUEMR4)		03h
Wake-Up Edge Mode Register 6 (WUEMR6)		10h
Wake-Up Edge Mode Register 7 (WUEMR7)		14h
Wake-Up Edge Sense Register 1 (WUESR1)		04h
Wake-Up Edge Sense Register 2 (WUESR2)		05h
Wake-Up Edge Sense Register 3 (WUESR3)		06h
Wake-Up Edge Sense Register 4 (WUESR4)		07h
Wake-Up Edge Sense Register 6 (WUESR6)		11h
Wake-Up Edge Sense Register 7 (WUESR7)		15h
Wake-Up Enable Register 1 (WUENR1)		08h
Wake-Up Enable Register 2 (WUENR2)		09h
Wake-Up Enable Register 3 (WUENR3)		0Ah
Wake-Up Enable Register 4 (WUENR4)		0Bh
Wake-Up Enable Register 6 (WUENR6)		12h
Wake-Up Enable Register 7 (WUENR7)		16h

7.3.4.1 Wake-Up Edge Mode Register 1 (WUEMR1)

This register configures the trigger mode of input signals WU10 to WU17.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM17-10)** 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected. Always write-1-clear to the corresponding bit in WUESR register after modifying these bits.

7.3.4.2 Wake-Up Edge Mode Register 2 (WUEMR2)

This register configures the trigger mode of input signals WU20 to WU27.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM27-20)**

7.3.4.3 Wake-Up Edge Mode Register 3 (WUEMR3)

This register configures the trigger mode of input signals WU30 to WU37.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM37-30)**

7.3.4.4 Wake-Up Edge Mode Register 4 (WUEMR4)

This register configures the trigger mode of input signals WU40 to WU47.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM47-40)**

7.3.4.5 Wake-Up Edge Mode Register 6 (WUEMR6)

This register configures the trigger mode of input signals WU60 to WU67.

Address Offset: 10h

Bit	R/W	Default	Description
7-0	R	0h	**Wake-Up Edge Mode (WUEM67-60)**

7.3.4.6 Wake-Up Edge Mode Register 7 (WUEMR7)

This register configures the trigger mode of input signals WU70 to WU77.

Address Offset: 14h

Bit	R/W	Default	Description
7-4	R/W	0h	**Wake-Up Edge Mode (WUEM77-74)** 0: Rising-edge triggered is selected. 1: Either-edge (rising-edge or falling-edge) triggered is selected. Always write-1-clear to the corresponding bit in WUESR register after modifying these bits.
3-0	R/W	0h	**Wake-Up Edge Mode (WUEM73-70)**

7.3.4.7 Wake-Up Edge Sense Register 1 (WUESR1)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU10 to WU17.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES17-10)** For each bit: Read 1: It indicates a trigger condition occurs on the corresponding input. Read 0: otherwise For each bit: Write 1: Clear this bit Write 0: No action

7.3.4.8 Wake-Up Edge Sense Register 2 (WUESR2)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU20 to WU27.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES27-20)**

7.3.4.9 Wake-Up Edge Sense Register 3 (WUESR3)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU30 to WU37.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES37-30)**

7.3.4.10 Wake-Up Edge Sense Register 4 (WUESR4)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU40 to WU47.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES47-40)**

7.3.4.11 Wake-Up Edge Sense Register 6 (WUESR6)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU60

to WU67.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES67-60)**

7.3.4.12 Wake-Up Edge Sense Register 7 (WUESR7)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU70 to WU77.

Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES77-70)**

7.3.4.13 Wake-Up Enable Register 1 (WUENR1)

This register enables a wake-up function of the corresponding input signal WU10 to WU17.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN17-10)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending.

7.3.4.14 Wake-Up Enable Register 2 (WUENR2)

This register enables a wake-up function of the corresponding input signal WU20 to WU27.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN27-20)**

7.3.4.15 Wake-Up Enable Register 3 (WUENR3)

This register enables a wake-up function of the corresponding input signal WU30 to WU37.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN37-30)**

7.3.4.16 Wake-Up Enable Register 4 (WUENR4)

This register enables a wake-up function of the corresponding input signal WU40 to WU47.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN47-40)**

7.3.4.17 Wake-Up Enable Register 6 (WUENR6)

This register enables a wake-up function of the corresponding input signal WU60 to WU67.

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN67-60)**

7.3.4.18 Wake-Up Enable Register 7 (WUENR7)

This register enables a wake-up function of the corresponding input signal WU70 to WU77.

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN77-70)**

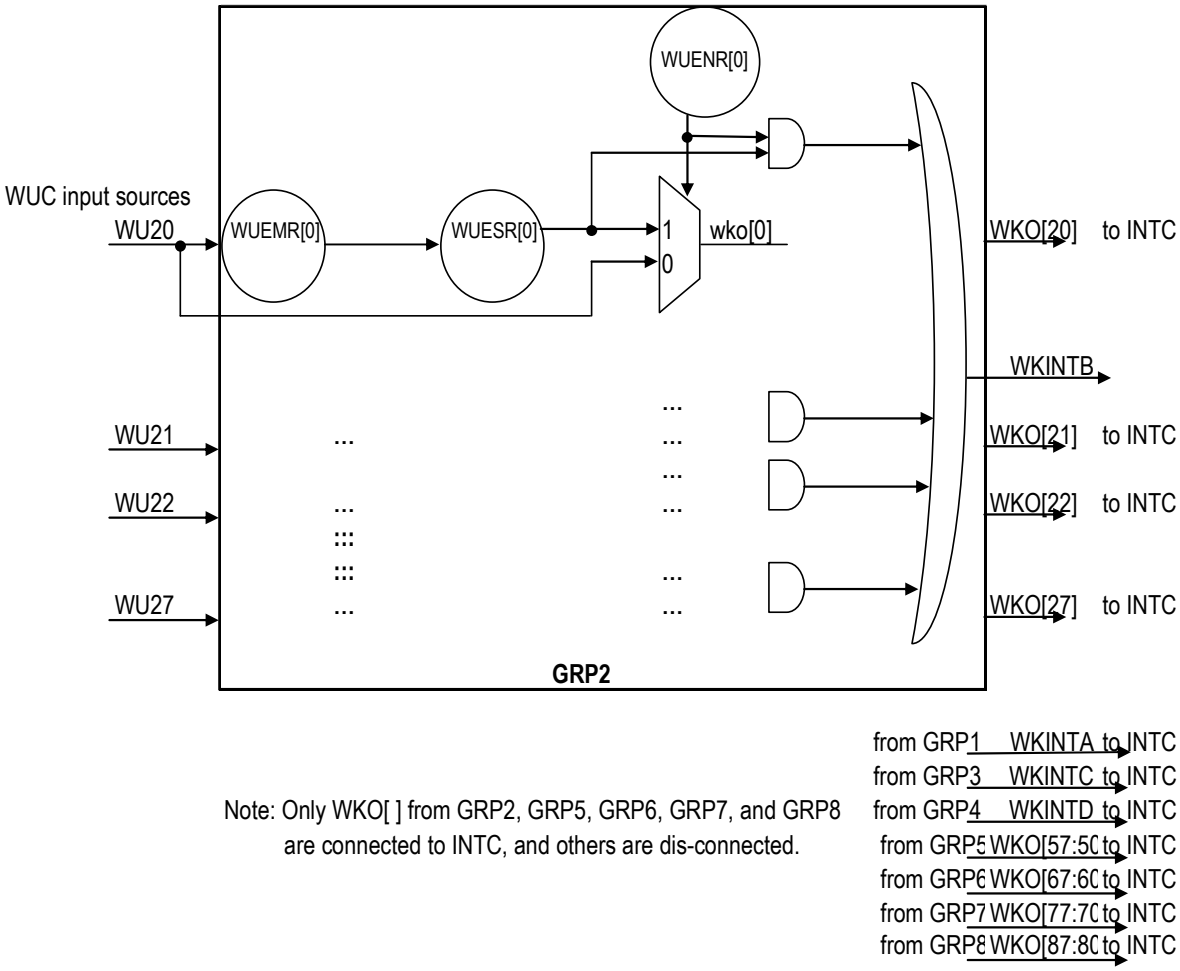
7.3.5 WUC Input Assignments

Table 7-10. WUC Input Assignments

WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
WU10	PS2CLK0	External Source from Pin	WKINTA, to INT5	Rising Edge Trig
WU11	PS2DAT0	External Source from Pin		Rising Edge Trig
WU12	PS2CLK1	External Source from Pin		Rising Edge Trig
WU13	PS2DAT1	External Source from Pin		Rising Edge Trig
WU14	PS2CLK2	External Source from Pin		Rising Edge Trig
WU15	PS2DAT2	External Source from Pin		Rising Edge Trig
WU16	Reserved			
WU17	Reserved			
WU20	WUI0	External Source from Pin	WKO[20], to INT1	Rising Edge Trig
WU21	WUI1	External Source from Pin	WKO[21], to INT31	Rising Edge Trig
WU22	WUI2	External Source from Pin	WKO[22], to INT21	Rising Edge Trig
WU23	WUI3	External Source from Pin	WKO[23], to INT6	Rising Edge Trig
WU24	WUI4	External Source from Pin	WKO[24], to INT17	Rising Edge Trig
WU25	PWRSW	External Source from Pin	WKO[25], to INT14	Rising Edge Trig
WU26	SWUC Wake Up	From SWUC Module	WKO[26], to INT12	Rising Edge Trig
WU27	Reserved			
WU30	KSI[0]	External Source from Pin	WKINTC, to INT13	Rising Edge Trig
WU31	KSI[1]	External Source from Pin		Rising Edge Trig
WU32	KSI[2]	External Source from Pin		Rising Edge Trig
WU33	KSI[3]	External Source from Pin		Rising Edge Trig
WU34	KSI[4]	External Source from Pin		Rising Edge Trig
WU35	KSI[5]	External Source from Pin		Rising Edge Trig
WU36	KSI[6]	External Source from Pin		Rising Edge Trig
WU37	KSI[7]	External Source from Pin		Rising Edge Trig
WU40	WUI5	External Source from Pin	WKINTD, to INT5	Rising Edge Trig
WU41	-	-		-
WU42	LPC Access	LPC Cycle with Address Recognized See also Section 6.1.6, p40		Rising Edge Trig
WU43	SMDAT0	External Source from Pin		Rising Edge Trig
WU44	SMDAT1	External Source from Pin		Rising Edge Trig
WU45	WUI6	External Source from Pin		Rising Edge Trig
WU46	WUI7	External Source from Pin		Rising Edge Trig
WU47	SMDAT2	External Source from Pin		Rising Edge Trig
-	-	-	-	-
WU60	WUI16	External Source from GPH0	WKO[60], to INT48	Rising EdgeTrig (Not adjustable)
WU61	WUI17	External Source from GPH1	WKO[61], to INT49	
WU62	WUI18	External Source from GPH2	WKO[62], to INT50	
WU63	WUI19	External Source from GPH3	WKO[63], to INT51	
WU64	WUI20	External Source from GPF4	WKO[64], to INT52	
WU65	WUI21	External Source from GPF5	WKO[65], to INT53	
WU66	WUI22	External Source from GPF6	WKO[66], to INT54	
WU67	WUI23	External Source from GPF7	WKO[67], to INT55	

WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
WU70	WUI24	External Source from GPE0	WKO[70], to INT72	Rising EdgeTrig (Not adjustable)
WU71	WUI25	External Source from GPE1	WKO[71], to INT73	
WU72	WUI26	External Source from GPE2	WKO[72], to INT74	
WU73	WUI27	External Source from GPE3	WKO[73], to INT75	
WU74	WUI28	External Source from GPI4	WKO[74], to INT76	Rising Edge Trig
WU75	WUI29	External Source from GPI5	WKO[75], to INT77	Rising Edge Trig
WU76	WUI30	External Source from GPI6	WKO[76], to INT78	Rising Edge Trig
WU77	WUI31	External Source from GPI7	WKO[77], to INT79	Rising Edge Trig

Figure 7-16. WUC Simplified Diagram



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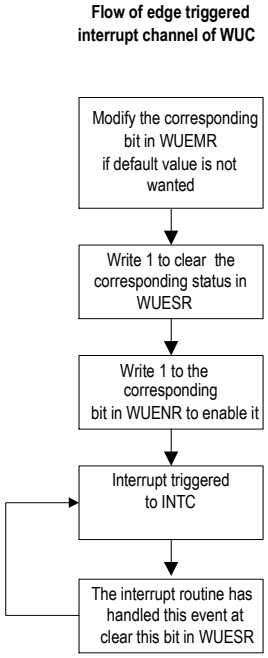
If the WUC source is from GPIO port, the firmware should not enable the corresponding channel when this GPIO is not in alternate function.

Figure 7-17. Program Flow Chart for WUC



7.4 Keyboard Matrix Scan Controller

7.4.1 Overview

The module provides control for keyboard matrix scan.

7.4.2 Features

- Supports 18 x scan output
- Supports 8 x scan input
- Supports Schmitt trigger input pin
- Supports programmable pull-up on all output/input pins
- Supports one interrupt (connected to INT11 of INTC) for any KSI inputs to go low to wake up the system
- Supports GPIO mode for some KBS pins (GPIO mode overrides EPP mode)

7.4.3 Functional Description

- **KSI/KSO Used as Keyboard Matrix**

Normal usage.

- **KSI/KSO Used as GPIO**

If the EC is applied to a platform without keyboard matrix, KSI/KSO pins excluding DBGR/PP purpose can be used as GPIO. See also Figure 7-44. Parallel Port Female 25-Pin Connector on page 335.

Table 7-11. KSI/KSO as GPIO List

KSI0/STB#	—	EPP Signal	—
KSI1/AFD#	Hardware strap	EPP Signal	—
KSI2/INIT#	Hardware strap	EPP Constant Signal	—
KSI3/SLIN#	—	EPP Signal	—
KSI4	Hardware strap	—	—
KSI5	Hardware strap	—	—
KSI6	—	—	Could be used as GPIO
KSI7	—	—	Could be used as GPIO
KSO0/PD0	—	EPP Signal	—
KSO1/PD1	—	EPP Signal	—
KSO2/PD2	—	EPP Signal	—
KSO3/PD3	—	EPP Signal	—
KSO4/PD4	—	EPP Signal	—
KSO5/PD5	—	EPP Signal	—
KSO6/PD6	—	EPP Signal	—
KSO7/PD7	—	EPP Signal	—
KSO8/ACK#	—	EPP Constant Signal	Could be used as GPIO
KSO9/BUSY	—	EPP Signal	—
KSO10/PE	—	EPP Constant Signal	Could be used as GPIO
KSO11/ERR#	—	EPP Constant Signal	Could be used as GPIO
KSO12/SLCT	—	EPP Constant Signal	Could be used as GPIO
KSO13	—	—	Could be used as GPIO
KSO14	—	—	Could be used as GPIO
KSO15	—	—	Could be used as GPIO

7.4.4 EC Interface Registers

The keyboard matrix scan registers are listed below. The base address is 1D00h.

Table 7-12. EC View Register Map, KB Scan

7	0	Offset
Keyboard Scan Out [7:0] (KSOL)		00h
Keyboard Scan Out [15:8] (KSOH1)		01h
Keyboard Scan Out Control (KSOCTRL)		02h
Keyboard Scan Out [17:16] (KSOH2)		03h
Keyboard Scan In [7:0] (KSI)		04h
Keyboard Scan In Control (KSICTRL)		05h
Keyboard Scan In GPIO Control Register (KSIGCTRL)		06h
Keyboard Scan In GPIO Ouput Enable Register (KSIGOEN)		07h
Keyboard Scan In GPIO Data Register (KSIGDAT)		08h
Keyboard Scan In GPIO Data Mirror Register (KSIGDMRR)		09h
Keyboard Scan Out GPIO Control Register (KSOGCTRL)		0Ah
Keyboard Scan Out GPIO Output Enable Register (KSOGOEN)		0Bh
Keyboard Scan Out GPIO Data Mirror Register (KSOGDMRR)		0Ch

7.4.4.1 Keyboard Scan Out Low Byte Data Register (KSOL)

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out Low Data [7:0] (KSOL)** This is the 8-bit keyboard scan output register which controls the KSO[7:0] pins.

7.4.4.2 Keyboard Scan Out High Byte Data 1 Register (KSOH1)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Keyboard Scan Out High Data 1 [7:0] (KSOH1)** This is the 8-bit keyboard scan output register which controls the KSO[15:8] pins. In GPIO mode, this register is used as KSO[15:10] and KSO[8] Data Register (Refer to the related KSO GPIO registers).

7.4.4.3 Keyboard Scan Out Control Register (KSOCTRL)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-3	-	-	**Reserved**
2	R/W	0b	**KSO Pull Up (KSOPU)** Setting 1 enables the internal pull up of the KSO[15:0] pins. To pull up KSO[17:16], set the GPCR registers of their corresponding GPIO ports. In GPIO mode, the internal pull-up of the pins KSO[15:10] and KSO[8] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	R/W	0b	**KSO Open Drain (KSOOD)** Setting 1 enables the open-drain mode of the KSO[17:0] pins. Setting 0 selects the push-pull mode. In GPIO mode, the open-drain mode of the pins KSO[15:10] and KSO[8] is always disabled even if this bit is set.

7.4.4.4 Keyboard Scan Out High Byte Data 2 Register (KSOH2)

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Keyboard Scan Out High Data 2 [1:0] (KSOH2)** This is the 2-bit keyboard scan output register which controls the KSO[17:16] pins.

7.4.4.5 Keyboard Scan In Data Register (KSIR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	00h	**Keyboard Scan In High Data [7:0] (KSI)** This is the 8-bit keyboard scan input register which shows the value of the KSI[7:0] pins.

7.4.4.6 Keyboard Scan In Control Register (KSICTRLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Override PP from KBS (OVRPPK)** This bit overrides PP function which is enabled by hardware strap in KBS interface and disables it.
3	-	-	**Reserved**
2	R/W	0b	**KSI Pull Up (KSIPU)** Setting 1 enables the internal pull up of the KSI[7:0] pins. In GPIO mode, the internal pull-up of the pins KSI[7:6] and KSI[2] is always disabled even if this bit is set.
1	-	-	**Reserved**
0	-	-	**Reserved**

7.4.4.7 Keyboard Scan In GPIO Control Register (KSIGCTRLR)

Address Offset: 06h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Control (KSI7GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSI6 GPIO Control (KSI6GCTRL)** 0: KBS mde 1: GPIO mode
5-3	-	-	**Reserved**
2	-	-	**Reserved**
1-0	-	-	**Reserved**

7.4.4.8 Keyboard Scan In GPIO Output Enable Register (KSIGOENR)

Address Offset: 07h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Output Enable (KSI7GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSI6 GPIO Output Enable (KSI6GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5-3	-	-	**Reserved**
2	-	-	**Reserved**
1-0	-	-	**Reserved**

7.4.4.9 Keyboard Scan In GPIO Data Register (KSIGDATR)

Address Offset: 08h

Bit	R/W	Default	Description
7	R/W	0b	**KSI7 GPIO Data (KSI7GDAT)** In GPIO mode, KSI7 will output this bit if the corresponding Output Enable bit is enabled.
6	R/W	0b	**KSI6 GPIO Data (KSI6GDAT)** In GPIO mode, KSI6 will output this bit if the corresponding Output Enable bit is enabled.
5-3	-	-	**Reserved**
2	-	-	**Reserved**
1-0	-	-	**Reserved**

7.4.4.10 Keyboard Scan In GPIO Data Mirror Register (KSIGDMRRR)

Address Offset: 09h

Bit	R/W	Default	Description
7	R	0b	**KSI7 GPIO Data Mirror (KSI7GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI7 status on reads.
6	R	0b	**KSI6 GPIO Data Mirror (KSI6GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSI6 status on reads.
5-3	-	-	**Reserved**
2	-	-	**Reserved**
1-0	-	-	**Reserved**

7.4.4.11 Keyboard Scan Out GPIO Control Register (KSOGCTRLR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Control (KSO15GCTRL)** 0: KBS mode 1: GPIO mode
6	R/W	0b	**KSO14 GPIO Control (KSO14GCTRL)** 0: KBS mode 1: GPIO mode
5	R/W	0b	**KSO13 GPIO Control (KSO13GCTRL)** 0: KBS mode 1: GPIO mode
4	R/W	0b	**KSO12 GPIO Control (KSO12GCTRL)** 0: KBS mode 1: GPIO mode
3	R/W	0b	**KSO11 GPIO Control (KSO11GCTRL)** 0: KBS mode 1: GPIO mode
2	R/W	0b	**KSO10 GPIO Control (KSO10GCTRL)** 0: KBS mode 1: GPIO mode
1	-	-	**Reserved**
0	R/W	0b	**KSO8 GPIO Control (KSO8GCTRL)** 0: KBS mode 1: GPIO mode

7.4.4.12 Keyboard Scan Out GPIO Output Enable Register (KSOGOENR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7	R/W	0b	**KSO15 GPIO Output Enable (KSO15GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
6	R/W	0b	**KSO14 GPIO Output Enable (KSO14GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
5	R/W	0b	**KSO13 GPIO Output Enable (KSO13GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
4	R/W	0b	**KSO12 GPIO Output Enable (KSO12GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
3	R/W	0b	**KSO11 GPIO Output Enable (KSO11GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
2	R/W	0b	**KSO10 GPIO Output Enable (KSO10GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.
1	-	0b	**Reserved**
0	R/W	0b	**KSO8 GPIO Output Enable (KSO8GOEN)** 0: Disable GPIO output 1: Enable GPIO output In KBS mode, this bit has no effect.

7.4.4.13 Keyboard Scan Out GPIO Data Mirror Register (KSOGDMRRR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R	0b	**KSO15 GPIO Data Mirror (KSO15GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO15 status on reads.
6	R	0b	**KSO14 GPIO Data Mirror (KSO14GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO14 status on reads.
5	R	0b	**KSO13 GPIO Data Mirror (KSO14GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO13 status on reads.
4	R	0b	**KSO12 GPIO Data Mirror (KSO12GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO12 status on reads.
3	R	0b	**KSO11 GPIO Data Mirror (KSO11GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO11 status on reads.
2	R	0b	**KSO10 GPIO Data Mirror (KSO10GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO10 status on reads.
1	-	0b	**Reserved**
0	R	0b	**KSO8 GPIO Data Mirror (KSO8GDMRR)** In KBS mode, this bit always returns 0 on reads. In GPIO mode, this bit returns the pin KSO8 status on reads.

7.5 General Purpose I/O Port (GPIO)

7.5.1 Overview

The General Purpose I/O Port is composed of independent I/O pins controlled by registers.

There are also other available general purpose I/O such as External GPIO Control (EGPC) and hardware strap ID7-0

7.5.2 Features

- I/O pins individually configured as input, output or alternate function
- Supports 73-port GPIO with serial flash
- Configurable internal pull-up resistors
- Configurable internal pull-down resistors
- Supports Schmitt-Trigger input on all ports except group I and groupJ

7.5.3 EC Interface Registers

The EC interface registers are listed below. The base address for GPIO is 1600h.

Table 7-13. EC View Register Map, GPIO

7 … 0	Offset
General Control Register (GCR)	00h
General Control 1 Register (GCR1)	F0h
General Control 2 Register (GCR2)	F1h
General Control 3 Register (GCR3)	F2h
General Control 4 Register (GCR4)	F3h
Port Data Register (GPDRA)	01h
Port Data Register (GPDRB)	02h
…	…
Port Data Register (GPDRJ)	0Ah
Port Control n Registers (GPCRA0)	10h
Port Control n Registers (GPCRA1)	11h
…	…
Port Control n Registers (GPCRJ5)	5Dh
Port Data Mirror Register (GPDMRA)	61h
Port Data Mirror Register (GPDMRB)	62h
…	…
Port Data Mirror Register (GPDMRJ)	6Ah
Output Type Register (GPOTB)	72h
Output Type Register (GPOTD)	74h
Output Type Register (GPOTH)	78h

7.5.3.1 General Control Register (GCR)

This register individually controls the bus state of each port. The input gating and output floating control signals can be used to reduce power consumption in various system conditions.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	0h	**GPB5 Follow LPCRST# Enable (GFLE)** 1: Refer to GFLES0 bit in this register 0: Otherwise Note that GA20 is function 1 of GPB5, LPCRST# is function 1 of GPD2 and WUI4 is function 2 of GPD2.
6	R/W	0b	**WUI7 Enable (WUI7EN)** When set, WUI7 is on input from GPE7. It is valid only when GPMD is input or output mode.
5	R/W	0b	**WUI6 Enable (WUI6EN)** When set, WUI6 is on input from GPE6. It is valid only when GPMD is input or output mode.
4-3	-	00b	**Reserved**
2-1	R/W	10b	**LPC Reset Enable (LPCRSTEN)** 00: Reserved 01: LPC Reset is enabled on GPB7. 10: LPC Reset is enabled on GPD2. 11: LPC Reset is disabled.
0	R/W	0b	**GFLE Set (GFLES0)** 1: GPDRB bit 5 will be set if WUI4 is level-low. 0: GPDRB bit 5 will be set immediately if there is a high-to-low transition on WUI4. If this “set” action occurs between a “reading from GPDRB” and “writing to GPDRB”, the GPDRB bit 5 is not writable in the “writing to GPDRB” action.

7.5.3.2 General Control 1 Register (GCR1)

Address Offset: F0h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**Support SSPI BUSY Pin (SSSPIBP)** 0b: SSPI does not support BUSY pin 1b: SSPI supports BUSY pin
5-4	R/W	00b	**SPI Control (SPICTRL)** If this field is zero, the corresponding function 3 of SPI is disabled. Otherwise, partial of them will be set as function 3 if their corresponding GPCRn is 00b. 00b: SPI channel 0 is disabled. 10b: Reserved 01b: SSCK/SMOSI/SMISO/SSCE0# are enabled. 11b: Reserved
3-2	-	-	**Reserved**
1-0	R/W	00b	**UART1 Control (U1CTRL)** If this field is zero, the corresponding function 3 of UART1 is disabled. Otherwise, partial or all of them are set as function 3 if their corresponding GPCRn is 00b. 00b: UART1 is disabled. 01b: SIN0/SOUT0 are enabled. 10b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0# are enabled. 11b: SIN0/SOUT0/DSR0#/RTS0#/DTR0#/CTS0#/DCD0#/RIG0# are enabled.

7.5.3.3 General Control 2 Register (GCR2)

Address Offset: F1h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**CK32K Out Enable (CK32OE)** 0b: Disable 1b: GPB7 will select CK32KOUT as its alternative function.
5	R/W	0b	**SMBus Channel 4 Enable (SMB4E)** 0b: Disable 1b: GPH1/GPH2 will select SMCLK3/SMDAT3 as its alternative function.
4	-	-	**Reserved**
3	R/W	0b	**TMB1 Enabled (TMB1EN)** Refer to Table 7-14. GPIO Alternate Function on page 198.
2	R/W	0b	**TMB0 Enabled (TMB0EN)** Refer to Table 7-14. GPIO Alternate Function on page 198.
1	R/W	0b	**TMA1 Enabled (TMA1EN)** Refer to Table 7-14. GPIO Alternate Function on page 198.
0	R/W	0b	**TMA0 Enabled (TMA0EN)** Refer to Table 7-14. GPIO Alternate Function on page 198.

7.5.3.4 General Control 3 Register (GCR3)

If VCC power-down and I/O port pins have been configured as their respective alternative function mode,

enabling these bits will turn off corresponding I/O port pins.

Address Offset: F2h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5	R/W	0b	**UART1 VCC Power-down Gating (UART1PDG)** 0b: Disable 1b: Turn off UART1 related pins if VCC power-down.
4	R/W	0b	**UART0 VCC Power-down Gating (UART0PDG)** 0b: Disable 1b: Turn off UART0 related pins if VCC power-down.
3	R/W	0b	**SSPI VCC Power-down Gating (SSPIPDG)** 0b: Disable 1b: Turn off SSPI related pins if VCC power-down.
2	-	-	**Reserved**
1	R/W	0b	**ECSMI#/ECSCI# VCC Power-down Gating (EEPDG)** 0b: Disable 1b: Turn off ECSMI#/ECSCI# related pins if VCC power-down. Please note that this pin is disabled if in GPO mode.
0	R/W	0b	**CLKRUN#/GA20/KBRST# VCC Power-down Gating (CGKPDG)** 0b: Disable 1b: Turn off CLKRUN#/GA20/KBRST# related pins if VCC power-down. Please note that this pin is disabled if in GPO mode.

7.5.3.5 General Control 4 Register (GCR4)

Address Offset: F3h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Hardware Bypass Enable (HWBPE)** 00b: Disable 01b: GPI6 input will be directly bypassed to BAO. 10b: GPI7 input willl be directly bypassed to BBO. 11b: BAO and BBO are both enabled.

7.5.3.6 Port Data Registers A-J (GPDRA-GPDRJ)

The Port Data register (GPDR) is an 8-bit register. The pin function is controlled by Port Control Register (GPCRn). When the pin function is set to be a general output pin, the value of the GPDRx bit is directly output to its corresponding pin. When the pin function is set to be a general input pin, the pin level status can be detected by reading the corresponding register bit. Each register contains one group which has eight ports at most.

Address Offset: 01h-0Ah

Bit	R/W	Default	Description
7-0	R/W	GPDRB[5] :1b GPDRG[0] : 1b Otherwise: 0b	**Port Data Register (GPDRn[7:0])** When the pin function is set to be a general output pin, the value of this bit is directly output to its corresponding pin. In the output mode, reading returns the last written data to GPDRn. In other modes, reading this register returns the pin level status. For group I/J, the return data may have no meaningful in the function 1 mode.

7.5.3.7 Port Data Mirror Registers A-J (GPDMRA-GPDMRJ)

Address Offset: 61h-6Ah

Bit	R/W	Default	Description
7-0	R	-	**Port Data Mirror Register (GPDMRn[7:0])** Reading this register returns the pin level status. For group I/J, the return data may have no meaningful in the function 1 mode.

7.5.3.8 Port Control n Registers (GPCRn, n = A0-I7)

These registers are used to control the functions of each I/O port pin. Each register is responsible for the settings of one pin in the port.
If Operation Mode is “Alternate Function”, Function 1 and/or Function 2 will be enabled. Refer to Table 7-14. GPIO Alternate Function on page 198 for details. Please note that GPI0-GPI7 don’t have output mode and the corresponding GPMD cannot be assigned as 01.

Address Offset: 10h-17h for GPCRA0- GPCRA7, respectively (Group A)
Address Offset: 18h-1Fh for GPCRB0- GPCRB7, respectively (Group B)
Address Offset: 20h-27h for GPCRC0- GPCRC7, respectively (Group C)
Address Offset: 28h-2Fh for GPCRD0- GPCRD7, respectively (Group D)
Address Offset: 30h-37h for GPCRE0- GPCRE7, respectively (Group E)
Address Offset: 38h-3Fh for GPCRF0- GPCRF7, respectively (Group F)
Address Offset: 40h-47h for GPCRG0- GPCRG7, respectively (Group G)
Address Offset: 48h-4Eh for GPCRH0- GPCRH6, respectively (Group H)
Address Offset: 50h-57h for GPCRI0- GPCRI7, respectively (Group I)
Address Offset: 58h-5Dh for GPCRJ0- GPCRJ5, respectively (Group J)
Address Offset: 90h-97h for GPCRK0- GPCRK7, respectively (Group K)
Address Offset: 98h-9Fh for GPCRL0- GPCRL7, respectively (Group L)

Bit	R/W	Default	Description
7-6	R/W	GPCRB5: 01b GPCRB6: 00b Otherwise: 10b	**Port Pin Mode (GPMD[1:0])** These bits are used to select the GPIO operation Mode. Note that group I doesn't have output mode and the corresponding GPMD cannot be assigned as 01. **GPMD[1:0]** / **Pin Status** / **READ GPDRn** / **WRITE GPDRn** 00b / Alternate Function / Pin Status / GPDR is writable but it has no effects on the pin status. 01b / Output / Pin Status / The value written to GPDR is output to pin. 10b / Input / Pin Status / GPDR is writable but it has no effects on the pin status. 11b / Reserved / - / -
5-3	R/W	000b	**Port Pin Output Driving Capability (GPOD)** The adjustable output driving capability is only available on port GPA0-A3, B0, B1, C7, E0, E7 and H0-H6, totally 16 ports and this register field is reversed for all other GPIO ports. The following driving currents capability are denoted by sourcing/sinking. 000b: 4/4 mA 001b: treated as 010b 010b: 8/8 mA 011b: 12/12 mA 110b: treated as 111b 111b: 16/16 mA otherwise: reserved
2	R/W	Refer to Table 7-14 on page 198	**Port Pin Pull Up (GPPU)** This bit is used to pull the port. It is always valid regardless of GPMD, input or output. Enable this bit will increase power consumption. Note that if one port is operated in output mode, it should not enable this bit unless its output type is open-drain. For example, clear this bit when DAC0/GPJ0 is switched to alternative function.
1	R/W	Refer to Table 7-14 on page 198	**Port Pin Pull Down (GPPD)** This bit is used to pull the port. This bit is always valid regardless of GPMD, input or output. Never enable pull up/down of a port at the same time or it forms a DC path and has unnecessary leakage current.
0	R/W	0	**Reserved**

7.5.3.9 Output Type Registers B/D/H (GPOTB/D/H)

The Output Type register (GPOT) is an 8-bit register. These registers control the output type of GPIO. Each register contains one group which has eight ports at most. Note that these bits are valid only when corresponding GPMD equals to 01 (Output mode).

Address Offset: 72h, 74h, 78h

Bit	R/W	Default	Description
7-0	R/W	00h	**Output Type Register (GPOTn[7:0])** The adjustable output types are only available on port GPB0-B7, GPD0-D7 and GPH0-H6. For each bit: 0: Push-pull output 1: Open-drain output

7.5.4 Alternate Function Selection

The following lists function 1 and function 2 of each GPIO port. Notice that the GA20 function can be implemented by GPO or function 1 which is implemented at KBC module. Function 1 of GPB6 is KBRST# from KBC module through SWUC mode. LPCRST# is recommended to input from GPD2 port.

Table 7-14. GPIO Alternate Function

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Sch Trig	Pull Cap	Def Pull	Def Mode
GPIOA	0	1610h	24	PWM0	GPCRA0[7:6]=00					4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	1	1611h	25	PWM1	GPCRA1[7:6]=00					4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	2	1612h	28	PWM2	GPCRA2[7:6]=00					4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	3	1613h	29	PWM3	GPCRA3[7:6]=00					4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	4	1614h	30	PWM4	GPCRA4[7:6]=00					8	Y	Up/Dn	Up	GPI
	5	1615h	31	PWM5	GPCRA5[7:6]=00					8	Y	Up/Dn	Up	GPI
	6	1616h	32	PWM6	GPCRA6[7:6]=00			SSCK	GPCRA6[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	Up	GPI
	7	1617h	34	PWM7	GPCRA7[7:6]=00					8	Y	Up/Dn	Up	GPI
GPIOB	0	1618h	108	RXD	GPCRB0[7:6]=00			SIN0	GPCRB0[7:6]=00 / U1CTRL>0	4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	1	1619h	109	TXD	GPCRB1[7:6]=00			SOUT0	GPCRB1[7:6]=00 / U1CTRL>0	4/4 ~ 16/16	Y	Up/Dn	Up	GPI
	2	161Ah	123					TMA0	GPCRB2[7:6]=00 TMA0EN=1	8	Y	Up/Dn	Dn	GPI
	3	161Bh	110	SMCLK0	GPCRB3[7:6]=00					4	Y	Up/Dn		GPI
	4	161Ch	111	SMDAT0	GPCRB4[7:6]=00					4	Y	Up/Dn		GPI
	5	161Dh	126	GA20	GPCRB5[7:6]=00					2	Y	Up/Dn		GPO
	6	161Eh	4	KBRST#	GPCRB6[7:6]=00					2	Y	Up/Dn	Up	Func1
	7	161Fh	112	RING#	GPCRB7[7:6]=00	PWRFAIL#/ LPCRST#	GPCRB7[7:6]=00 /LPCRSTEN=01			2	Y	Up/Dn	Dn	GPI

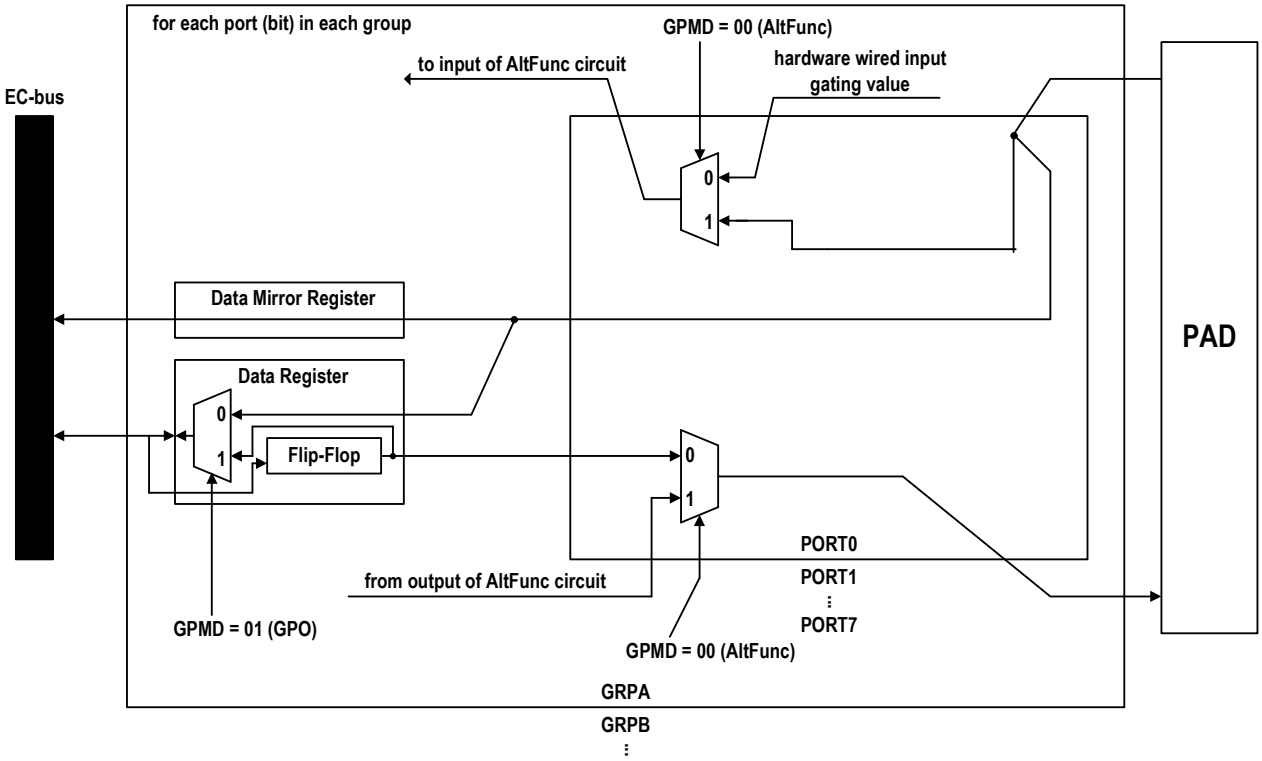
Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Sch Trig	Pull Cap	Def Pull	Def Mode
GPIOC	0	1620h	119							2	Y	Up/Dn	Dn	GPI
	1	1621h	115	SMCLK1	GPCRC1[7:6]=00					4	Y	Up/Dn		GPI
	2	1622h	116	SMDAT1	GPCRC2[7:6]=00					4	Y	Up/Dn		GPI
	3	1623h	56	KSO16	GPCRC3[7:6]=00			SMOSI	GPCRC3[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	Dn	GPI
	4	1624h	120	TMRI0	GPCRC4[7:6]=00	WUI2	GPCRC4[7:6]=00			2	Y	Up/Dn	Dn	GPI
	5	1625h	57	KSO17	GPCRC5[7:6]=00			SMISO	GPCRC5[7:6]=00 / SPICTRL>0	8	Y	Up/Dn	Dn	GPI
	6	1626h	124	TMRI1	GPCRC6[7:6]=00	WUI3	GPCRC6[7:6]=00			2	Y	Up/Dn	Dn	GPI
	7	1627h	16	PWUREQ#	GPCRC7[7:6]=00					4/4 ~ 16/16	Y	Up/Dn	Up	GPI
GPIOD	0	1628h	18	RI1#	GPCRD0[7:6]=00	WUI0	GPCRD0[7:6]=00			4	Y	Up/Dn	Up	GPI
	1	1629h	21	RI2#	GPCRD1[7:6]=00	WUI1	GPCRD1[7:6]=00			4	Y	Up/Dn	Up	GPI
	2	162Ah	22	LPCRST#	LPCRSTEN=10	WUI4	GPCRD2[7:6]=00			8	Y	Up/Dn	Up	Func1
	3	162Bh	23	ECSCI#	GPCRD3[7:6]=00					8	Y	Up/Dn	Up	GPI
	4	162Ch	15	SMI#	GPCRD4[7:6]=00					8	Y	Up/Dn	Up	GPI
	5	162Dh	33	GINT	GPCRD5[7:6]=00			CTS0#	GPCRD5[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	Up	GPI
	6	162Eh	47	TACH0	GPCRD6[7:6]=00					2	Y	Up/Dn	Dn	GPI
	7	162Fh	48	TACH1	GPCRD7[7:6]=00 TMA1EN=0			TMA1	GPCRD7[7:6]=00 TMA1EN=0	2	Y	Up/Dn	Dn	GPI
GPIOE	0	1630h	19	L80HLAT	GPCRE0[7:6]=00	WUI24	Always			4/4 ~ 16/16	Y	Up/Dn	Dn	GPI
	1	1631h	82	EGAD	GPCRE1[7:6]=00	WUI25	Always			8	Y	Up/Dn	Dn	GPI
	2	1632h	83	EGCS#	GPCRE2[7:6]=00	WUI26	Always			8	Y	Up/Dn	Dn	GPI
	3	1633h	84	EGCLK	GPCRE3[7:6]=00	WUI27	Always			8	Y	Up/Dn	Dn	GPI
	4	1634h	125	PWRSW	GPCRE4[7:6]=00					2	Y	Up/Dn	Up	GPI
	5	1635h	35			WUI5	GPCRE5[7:6]=00			2	Y	Up/Dn	Dn	GPI
	6	1636h	17	LPCPD#	GPCRE6[7:6]=00	WUI6	WUI6EN bit GCR register			2	Y	Up/Dn	Dn	GPI
	7	1637h	20	L80LLAT	GPCRE7[7:6]=00	WUI7	WUI7EN bit GCR register			4/4 ~ 16/16	Y	Up/Dn	Up	GPI

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Sch Trig	Pull Cap	Def Pull	Def Mode
GPIOF	0	1638h	85	PS2CLK0	GPCRF0[7:6]=00 TMB0EN=0			TMB0	GPCRF0[7:6]=00 TMB0EN=1	8	Y	Up/Dn	Up	GPI
	1	1639h	86	PS2DAT0	GPCRF1[7:6]=00 TMB1EN=0			TMB1	GPCRF1[7:6]=00 TMB1EN=1	8	Y	Up/Dn	Up	GPI
	2	163Ah	87	PS2CLK1	GPCRF2[7:6]=00			DTR0#	GPCRF2[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	Up	GPI
	3	163Bh	88	PS2DAT1	GPCRF3[7:6]=00			RTS0#	GPCRF3[7:6]=00 / U1CTRL>1	8	Y	Up/Dn	Up	GPI
	4	163Ch	89	PS2CLK2	GPCRF4[7:6]=00	WUI20	Always			8	Y	Up/Dn	Up	GPI
	5	163Dh	90	PS2DAT2	GPCRF5[7:6]=00	WUI21	Always			8	Y	Up/Dn	Up	GPI
	6	163Eh	117	SMCLK2	GPCRF6[7:6]=00	WUI22	Always			4	Y	Up/Dn	Up	GPI
	7	163Fh	118	SMDAT2	GPCRF7[7:6]=00	WUI23	Always			4	Y	Up/Dn	Up	GPI
GPIOG	0	1640h	106						GPCRG0[7:6]=00 / SPICTRL[1]>0	4	Y	Up/Dn		GPO
	1	1641h	107							4	Y	Up/Dn	Dn	GPO/ID7
	2	1642h	100					SSCE0#	GPCRG2[7:6]=00 / SPICTRL[0]>0	4	Y	Up/Dn		
	6	1646h	104					DSR0#	GPCRG6[7:6]=00 / U1CTRL>1	4	Y	Up/Dn		GPI
GPIOH	0	1648h	93	CLKRUN#	GPCRH0[7:6]=00	WUI16	Always			4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID0
	1	1649h	94			WUI17	Always			4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID1
	2	164Ah	95			WUI18	Always			4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID2
	3	164Bh	96			WUI19	Always			4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID3
	4	164Ch	97							4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID4
	5	164Dh	98							4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID5
	6	164Eh	99							4/4 ~ 16/16	Y	Up/Dn	Dn	GPI/ID6

Group		Addr	Pin Loc	Func 1	Condition	Func 2	Condition	Func 3	Condition	Output Driving (mA)	Sch Trig	Pull Cap	Def Pull	Def Mode
GPIOI	0	1650h	66	ADC0						(input only)				GPI
	1	1651h	67	ADC1						(input only)				GPI
	2	1652h	68	ADC2						(input only)				GPI
	3	1653h	69	ADC3						(input only)				GPI
	4	1654h	70	ADC4		WUI28	Always			(input only)				GPI
	5	1655h	71	ADC5		WUI29	Always			(input only)				GPI
	6	1656h	72	ADC6		WUI30	Always			(input only)				GPI
	7	1657h	73	ADC7		WUI31	Always			(input only)				GPI
GPIOJ	0	1658h	76	DAC0						4	Y	Up/Dn		GPI
	1	1659h	77	DAC1						4	Y	Up/Dn		GPI
	2	165Ah	78	DAC2						4	Y	Up/Dn		GPI
	3	165Bh	79	DAC3						4	Y	Up/Dn		GPI
	4	165Ch	80	DAC4				DCD0#	GPCRJ4[7:6]=00 / U1CTRL>1	4	Y	Up/Dn		GPI
	5	165Dh	81	DAC5				RIG0#	GPCRJ5[7:6]=00 / U1CTRL=3	4	Y	Up/Dn		GPI

Note: Since all GPIO belong to VSTBY power plane, and there are some special considerations below:
(1) If it is output to external VCC derived power plane circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power plane circuit, this external circuit must consider not floating the GPIO input.

Figure 7-18. GPIO Simplified Diagram



7.5.5 Programming Guide

The firmware should modify LPCRSTEN when it boots up if necessary.

7.6 EC Clock and Power Management Controller (ECPM)

7.6.1 Overview

The EC Clock and Power Management module provide the EC clock control and power management.

7.6.2 Features

- Supports programmable EC clock frequency
- Supported by module power-down mode control
- Supports PLL power-down when 8032 enters a Sleep mode

7.6.3 EC Interface Registers

The clock generation and power management registers are listed below. The base address is 1E00h.

Table 7-15. EC View Register Map, ECPM

7	0	Offset
Reserved		00h
Clock Gating Control 1 (CGCTRL1R)		01h
Clock Gating Control 2 (CGCTRL2R)		02h
Clock Gating Control 3 (CGCTRL3R)		05h
PLL Control (PLLCTRL)		03h
Auto Clock Gating (AUTOCG)		04h
PLL Frequency (PLLFREQR)		06h

7.6.3.1 Clock Gating Control 1 Register (CGCTRL1R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	0b	**GPIO Clock Gating (GPIOCG)** 0: Operation 1: Clock to this module is gated
6	R/W	0b	**ETWD Clock Gating (ETWDCG)** 0: Operation 1: Clock to this module is gated
5	R/W	0b	**SMB Clock Gating (SMBCG)** 0: Operation 1: Clock to this module is gated
4	R/W	0b	**Keyboard Scan Clock Gating (KBSCG)** 0: Operation 1: Clock to this module is gated
3	R/W	0b	**PS/2 Clock Gating (PS2CG)** 0: Operation 1: Clock to this module is gated
2	R/W	0b	**PWM/TMR Clock Gating (PWMCG)** 0: Operation 1: Clock to this module is gated
1	R/W	0b	**DAC Clock Gating (DACCG)** 0: Operation 1: Clock to this module is gated
0	R/W	0b	**ADC Clock Gating (ADCCG)** 0: Operation 1: Clock to this module is gated

7.6.3.2 Clock Gating Control 2 Register (CGCTRL2R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 02h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	0b	**EGPC Clock Gating (EXGCG)** 0: Operation 1: Clock to this module is gated
5	-	-	**Reserved**
4	R/W	0b	**SWUC Clock Gating (SWUCCG)** 0: Operation 1: Clock to this module is gated
3	R/W	0b	**PMC Clock Gating (PMCCG)** 0: Operation 1: Clock to this module is gated
2	R/W	0b	**KBC Clock Gating (KBCCG)** 0: Operation 1: Clock to this module is gated
1	R/W	0b	**EC2I Clock Gating (EC2ICG)** 0: Operation 1: Clock to this module is gated
0	R/W	0b	**SMFI Clock Gating (SMFICG)** 0: Operation 1: Clock to this module is gated

7.6.3.3 Clock Gating Control 3 Register (CGCTRL3R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 05h

Bit	R/W	Default	Description
7	W	0b	**R8032TT UART Clock Gating(UARTCG)** 0: Operation 1: Clock to this function is gated.
6	W	1b	**Reserved** Always write 1 to this bit.
5-4	-	-	**Reserved**
3	-	-	**Reserved**
2	R/W	0b	**UART Clock Gating (UART12CG)** 0: Operation 1: Clocks to UART1 module is gated.
1	R/W	0b	**SSPI Clock Gating (SSPICG)** 0: Operation 1: Clock to this module is gated.
0	R/W	1b	**DBGR Clock Gating (DBGRCG)** 0: Operation 1: Clock to this module is gated.

7.6.3.4 PLL Control (PLLCTRL)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 03h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	1b	**PLL Power Down Control (PPDC)** 0: PLL will not be powered down by software until VSTBY is not supplied. Setting PD bit in PCON will enter an EC Doze mode. 1: PLL will be powered down after setting PD bit in PCON and enter an EC power-down mode.

7.6.3.5 Auto Clock Gating (AUTOCG)

This register is reset by VSTBY Power-Up reset only.

For the PS/2 module, normally it can not be accomplished to gate the clock of PS/2 module in the Idle/Doze mode if it's clock-gated by PS2CG bit since the clock of PS/2 module should be released immediately after an activity on PS/2 interface. However, it can be accomplished by setting APS2CG bit with enabling its interrupt path.
APS2CG required interrupt path: (corresponding WU10~15) -> INT5 -> 8032 INT1#

For SMB modules, it is similar.
ASMBCG required interrupt path: (corresponding WU43,44,47) -> INT5 -> 8032 INT1#

Address Offset: 04h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	R/W	1b	**Auto UART1 Clock Gating (AUART1CG)** 1: The UART1 clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides UART12CG bit in CGCTRL3R register. If UART1SD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Idle/Doze/Sleep mode. If UART1SD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The UART1 clock is gated by UART12CG bit in CGCTRL3R register.
5	-	-	**Reserved**
4	R/W	1	**Auto SSPI Clock Gating (ASSPICG)** 1: The SSPI clock will be automatically gated if the corresponding port of GPIO is not in its alternative function. It also overrides SSPICG bit in CGCTRL3R register. If SSPISD bit in RSTDMMC register is 1, the clock will also be gated if the chip is in the Idle/Doze/Sleep mode. If SSPISD bit in RSTDMMC register is 0, the clock will also be gated if VCC is off. 0: The SSPI clock is gated by SSPICG bit in CGCTRL3R register.
3	-	-	**Reserved**
2	-	-	**Reserved**
1	R/W	0b	**Auto PS/2 Clock Gating (APS2CG)** 1: The PS/2 clock will be automatically gated by channel if the corresponding port of GPIO is not in its alternative function or the chip is in the Idle/Doze/Sleep mode. It also overrides PS2CG bit in CGCTRL1R register. 0: The PS/2 clock is gated by PS2CG bit in CGCTRL1R register.
0	R/W	0b	**Auto SMB Clock Gating (ASMBCG)** 1: The SMB clock will be automatically gated by channel if the corresponding port of GPIO is not in its alternative function or the chip is in the Idle/Doze/Sleep mode. It also overrides SMBCG bit in CGCTRL1R register. 0: The SMB clock is gated by SMBCG bit in CGCTRL1R register. This bit should be 0b if SLVISEL field in SLVISELR register equals to 00b.

7.6.3.6 PLL Frequency (PLLFREQR)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 06h

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	R/W	0011b	**PLL Frequency (PLLFREQ)** 0011b: Select 32.3MHz as PLL frequency. 0101b: Select 46.0MHz as PLL frequency. 0111b: Select 64.5MHz as PLL frequency. Otherwise: Reserved Read returns the current PLL frequency setting. Writing to this register doesn't change PLL frequency immediately until wakeup from the Sleep mode. Refer to section 7.1.10.5 Code snippet of Changing PLL Frequency on page 158. SCEMINHW field in FLHCTRL2R register may be required before the PLL frequency is changed.

7.7 SMBus Interface (SMB)

7.7.1 Overview

The SMBus interface includes four SMBus channels. The module can maintain bi-directional communication with the external devices through the interface SMCLK0/SMDAT0, SMCLK1/SMDAT1, SMCLK2/SMDAT2 and SMCLK3/SMDAT3 pins. It is compatible with ACCESS BUS and I2C BUS.

7.7.2 Features

- Supports SMBus 2.0.
- Supports four SMBus channels.
- Performs SMBus messages with packet error checking (PEC) either enabled or disabled.
- Compatible with I2C cycles.

7.7.3 Functional Description

The SMBus Channel A contains one SMBus master and one SMBus slave.
The SMBus Channel B contains one SMBus master.
The SMBus Channel C contains one SMBus master.
The SMBus Channel D contains one SMBus master.

The default interface of the SMBus slave is located at SMCLK0/SMDAT0. The interface of the SMBus slave can be switched to SMCLK1/SMDAT1, SMCLK2/SMDAT2, or SMCLK3/ SMDAT3.

The master supports seven command protocols of the SMBus (see System Management Bus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, and Block Read/Write. The master also supports the I2C-compatible cycles (see The I2C-Bus Specification). The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.

7.7.3.1 SMBus Master Interface

When an interrupt to INTC (INT9, INT10, INT16, and INT4 for channel A, B, C, and D respectively) is detected, software can read the Host Status Register to know the interrupt source. There are 5 interrupt conditions: Byte Done, Failed, Bus Error, Device Error, and Finish.

Quick Command:
In the Quick Command, the Transmit Slave Address Register is sent. Software should force the PEC_EN bit in Host Control Register and I2C_EN bit in Host Control 2 Register to 0 when this command is run.

Send Byte/ Receive Byte:
In the Send Byte command, the Transmit Slave Address and Host Command Registers are sent.
In the Receive Byte command, the Transmit Slave Address Register is sent. The received data is stored in the Host DATA 0 register. Software must force the I2C_EN bit in Host control 2 Register to 0 when this command is run.

Write Byte/ Write Word
In the Write Byte command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Registers are sent.
In the Write Word command, the Transmit Slave Address Register, Host Command Register, Host Data 0, and Host Data 1 Registers are sent.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Read Byte/ Read Word
In the Read Byte command, the Transmit Slave Address Register and Host Command Register are sent. Data is received into the Host Data 0 Register.

In the Read Word command, the Transmit Slave Address Register and Host Command Register are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Process Call
In the Process Call command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data1 registers are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register. When the I2C_EN bit in Host Control 2 Register is set to 1, the Host Command Register will not be sent.
Note: The Process Call command with I2C_EN bit set and the PEC_EN bit set produce undefined results.

Block Write/ Block Read
In the Block Write command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 (byte count) register are sent. Data is then sent from the Host Block Data Byte register.
In the Block Read commands, the Transmit Slave Address Register, and Host Command Register are sent. The first byte (byte count) received is stored in the Host Data 0 register, and the remaining bytes are stored in the Host Block Data Byte register.
The Byte Done Status bit in the Host Status Register will be set 1 when the master has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands).
Note: On the block read command, software shall write 1 to LAST BYTE bit in Host Control Register when the next byte will be the last byte to be received.

I2C Block Read
This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent. Bit 0 of the Transmit Slave Address Register has to be 0. The received data is stored in the Host Block Data Byte register.

I2C-compatible Write Command
In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent and the transmitted data is set in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has completed transmission of a byte.

Note: Software shall write 0 to I2C_EN bit in Host Control Register 2 when the cycle is decided to be finished.

I2C-compatible Read Command
In I2C-compatible Read Command, the Transmit Slave Address Register is sent and the received data is stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set to 1 when the host has received a byte.

Note: Software shall write 1 to LAST_BYTE bit in the Host Control Register when the next byte to be received is the last one.

I2C-compatible Combined Command
This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in I2C-compatible cycles.
In I2C-compatible Combined Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent. Bit 0 of the Transmit Slave Address Register is set to decide the direction of the cycle and the received data is also stored in the Host Block Data Byte Register. The Byte Done Status bit in the Host Status Register will be set 1 when the host has completed transmission of a byte or received a byte.

Note: Software shall control the I2C_SE_EN bit and I2C_SW_WAIT bit in Host Control Register 2 when the direction switch is decided to be performed.

7.7.3.2 SMBus Slave Interface

The slave supports the following three types of messages: Byte Write, Byte Read, and Host Notify.
When an interrupt to INTC (INT9 for SMBus slave) is detected, software can read the Slave Status Register to know the interrupt source. There are 3 interrupt conditions: Slave Timeout Status, Slave Data Status, and Host Notify Status.

Byte Write
In the byte write command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data. The SMCLK line will be held low until the data is read. After the data is read, the third byte (Data) is received and stored in the Slave Data Register. The SMCLK line will be held low until the data is read.

Byte Read
In the byte read command, the value of the first received byte (Slave Address) must match the value in Receive Slave Address Register. If the value of the first received byte matches, the second byte (Command Data) will be received and stored in the Slave Data Register and waiting for the software to read the data. The SMCLK line will be held low until the data is read. After the Repeated Start and Slave Address cycle, the software shall write the data to the Slave Data Register and this register will be sent during the Data Byte Cycle.

Host Notify Command
In the host notify command, the first received byte must be 0001000b. The second received byte is stored in the Notify Device Address Register. The next two bytes are stored in the Notify Data Low Byte Register and Notify Data High Byte Register.

7.7.3.3 SMBus Porting Guide

(1).SMBus Master Interface:

The SMBus controller requires that various data and command registers be setup for the message to be sent. When the START bit in the Host Control Register is set, the SMBus controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing of a new command.

The “Timing Registers” (22h~28h) should be programmed before the transaction starts. Besides the 25ms Register, all of the other count numbers are based on EC clock. For example, write the 1Bh (37 / FreqEC ~= 4.0us) into the 4.0us register.
(FreqEC is listed in Table 10-2 on page 352 and this example assumes FreqEC = 9.2 MHz.)

The IT8502 SMBus Interface can perform SMBus messages with either packet error checking (PEC) enabled or disabled (PEC_EN bit = 1 or 0 in the Host Control Register). The actual PEC calculation and checking is performed in software.
Here is the steps the software shall follow to program the registers for various command.

1. Quick Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Quick Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register).
(3). Start the transaction (Write 41h to the Host Control Register, which will select the “Quick Command”, enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt is generated. Software can read the Host Status Register to know the source of the interrupt.

Note: After reading the Status Register, the software must write 1 to clear it.

2. Send Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Send Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to the Transmit Slave Address Register and Host Command Register) (Host Command Register is used for transmitting data here). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

3. Receive Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Receive Byte Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Receive Byte Command, the received data is stored in the Host Data 0 Register. Software can read this register to get the data.

4. Write Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Byte Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

5. Write Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Write Word Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register. And this register will be sent, too.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

6. Read Byte Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).

I2C_EN bit has to be 0 in this command.
(2). In Read Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Byte Command, the data received is stored in the Host Data 0 Register. Software can read this register to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

7. Read Word Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Read Word Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
(4). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Word Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

8. Process Call Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Process Call Command will skip the command code.
(3). In Process Call Command, the Transmit Slave Address Register, Host Command Register (if I2C_EN = 0), Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(4). Start the transaction (Write 51h to the Host Control Register, which will select the "Process Call Command", enable the interrupts, and start the transaction).
(5). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.
(6). In Process Call Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

9. Block Write Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(3). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0) are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0. The data is then sent from the Host Block Data Byte

Register (Software shall write data to this register).
(4). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(5). When the data in Host Block Data Byte Register is sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, then the data is sent from this register by SMBus logic.
(7). Repeat step (5) and (6) for the other data byte until all of the data were sent.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
(8). When the data transmission is completed, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

10. Block Read Command

(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 1.
(3). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(4). When the byte count and the first byte data are received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software read the data from the Host Data 0 Register to get the byte count, and read the data from the Host Block Data Byte Register to get the first data byte.
(6). When the next data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software read the data from the Host Block Data Byte Register to get the data.
(8). Repeat step (6) and (7) until the last byte.
(9). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(10). Get an interrupt and receive the last byte.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

11. I2C Block Read Command

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
(1). Enable the SMBus Host Controller (SMBus Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit has to be 0 in this command.
(2). In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(3). Start the transaction (Write 59h to the Host Control Register, which will select the "I2C Block Read Command", enable the interrupts, and start the transaction).
(4). When the data is received, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software can read the data from the Host Block Data Byte Register to get the data.
(6). Repeat step (4) and (5) until the last byte.
(7). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(8). Get an interrupt and receive the last byte.

12. I2C-compatible Write Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Write Command, the Transmit Slave Address Register and Host Block Data Byte Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register has to be 0.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(5). When the data in the Host Block Data Byte Register has been transmitted, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is transmitted from this register by the SMBus logic.
(7). Repeat step (5) and (6) for the other data bytes until software wants to finish the cycle.
(8). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(9). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

13. I2C-compatible Read Command

(1). Enable the SMBus Host Controller (SMHEN bit in the Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit in the Host Control Register 2 to 1.
(3). In I2C-compatible Read Command, the Transmit Slave Address Register is sent (Software shall write data to this register). Bit 0 of the Transmit Slave Address Register has to be 1 and the received data byte is stored in the Host Block Data Byte Register.
(4). Start the transaction (Write 5Dh to the Host Control Register, which will select the "Extend Command", enable the interrupts, and start the transaction).
(5). When the data has been received from the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LAST_BYTE bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

14. I2C-compatible Combined Command

This command allows the SMBus logic to perform direction switch from I2C Write Command to I2C Read Command or from I2C Read Command to I2C Write Command in the I2C-compatible cycles.

From I2C Write Command to I2C Read Command:
(1). In the I2C Write Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Read Command.
(2). After the last transmitted data byte has been sent in the I2C Write Command, the Byte Done interrupt will be generated. Then, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Read Command.
(3). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Read Command.
(5). When the data has been received and stored in the Host Block Data Byte Register, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done

Status is 1).
(6). Software reads the data from the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register.
(7). Repeat step (5) and (6) for the other data bytes until the last byte is going to be received.
(8). Set the LAST_BYTE bit in the Host Control Register after the Byte Done interrupt is generated to indicate that the next byte will be the last to be received.
(9). Get the Byte Done interrupt of the last byte, and receive the last data byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(10). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

From I2C Read Command to I2C Write Command:
(1). In the I2C Read Command mentioned above, software can control the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to switch the direction to the I2C Write Command.
(2). In the I2C Read Command, after setting the LAST_BYTE bit in the Host Control Register, software can set 1 to the I2C_SW_EN bit and I2C_SW_WAIT bit in the Host Control Register 2 to make the SMBus logic wait for the setting by software for the I2C Write Command.
(3). Get the Byte Done interrupt of the last byte, and receive the last byte from the Host Block Data Byte Register. Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(4). Software writes the transmitted data byte in the Host Block Data Byte Register.
(5). Set 0 to the I2C_SW_WAIT bit in the Host Control Register 2 to start the I2C Write Command.
(6). When the data in the Host Block Data Byte Register has been sent, an interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software writes the data to the Host Block Data Byte Register, and writes one to clear the Byte Done Status bit in the Host Status Register. Then, the data is sent from this register by the SMBus logic.
(8). Repeat step (6) and (7) for the other data bytes until software wants to finish the cycle.
(9). If software wants to finish the cycle, set I2C_EN bit in the Host Control Register 2 to 0 after the last transmitted data byte has been sent (Byte Done interrupt is generated).
(10). Software shall write one to clear the Byte Done Status bit in the Host Status Register.
(11). When the cycle is completed, a Finish interrupt will be generated. Software can read the Host Status Register to know the source of the interrupt (Finish interrupt is 1).

(2).SMBus Slave Interface:

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.
Here are the steps the software shall follow to program the registers for various commands.

1. Byte Write

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the data transmission from the external SMBus device.
(4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(5). Software can read the data from the Slave Data Register. (This data byte is the command code.)
(6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(7). Software can read the data from the Slave Data Register. (This data byte is the Data Byte in SMBus Protocol.)

2. Byte Read

(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to respond the

data transmission from the external SMBus device.

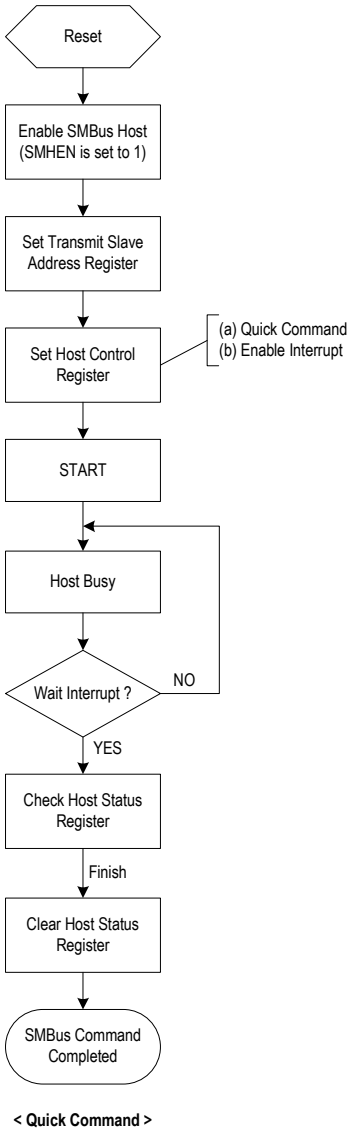
(4). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Read Command).
(5). Software can read the data from the Slave Data Register. (This data byte is the command code.)
(6). When the next interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 0Ah for Byte Read Command).
(7). Software can write the data to the Slave Data Register. (This data will be sent to the external device.)

3. Host Notify Command

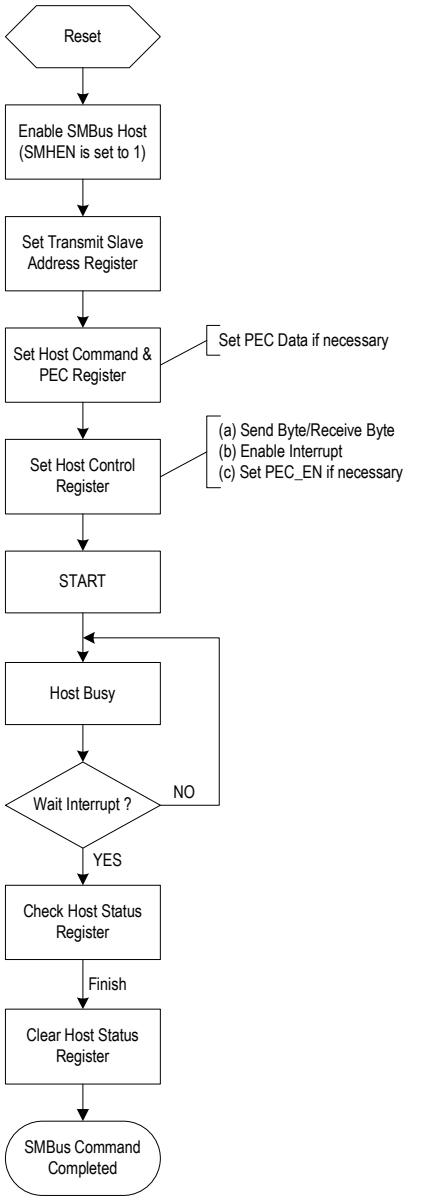
(1). Enable the SMBus Slave Device (SLVEN bit in the Host Control Register 2 is set to 1).
(2). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(3). When an interrupt is generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 01h for Host Notify Command).
(4). Software can read the data from the Notify Device Address Register, Notify Data Low Byte Register, and Notify Data High Byte Register.

7.7.3.4 SMBus Master Programming Guide

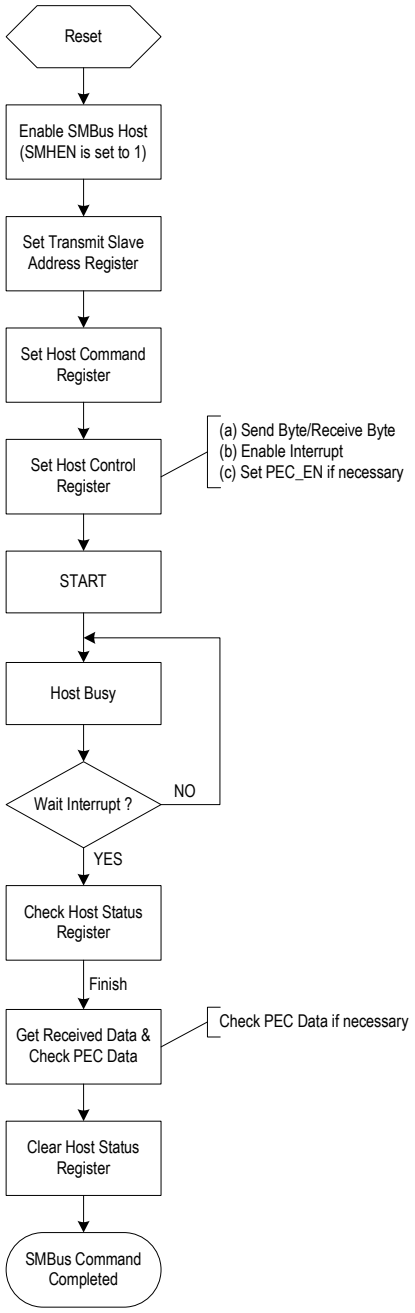
Figure 7-19. Program Flow Chart of SMBus Master Interface



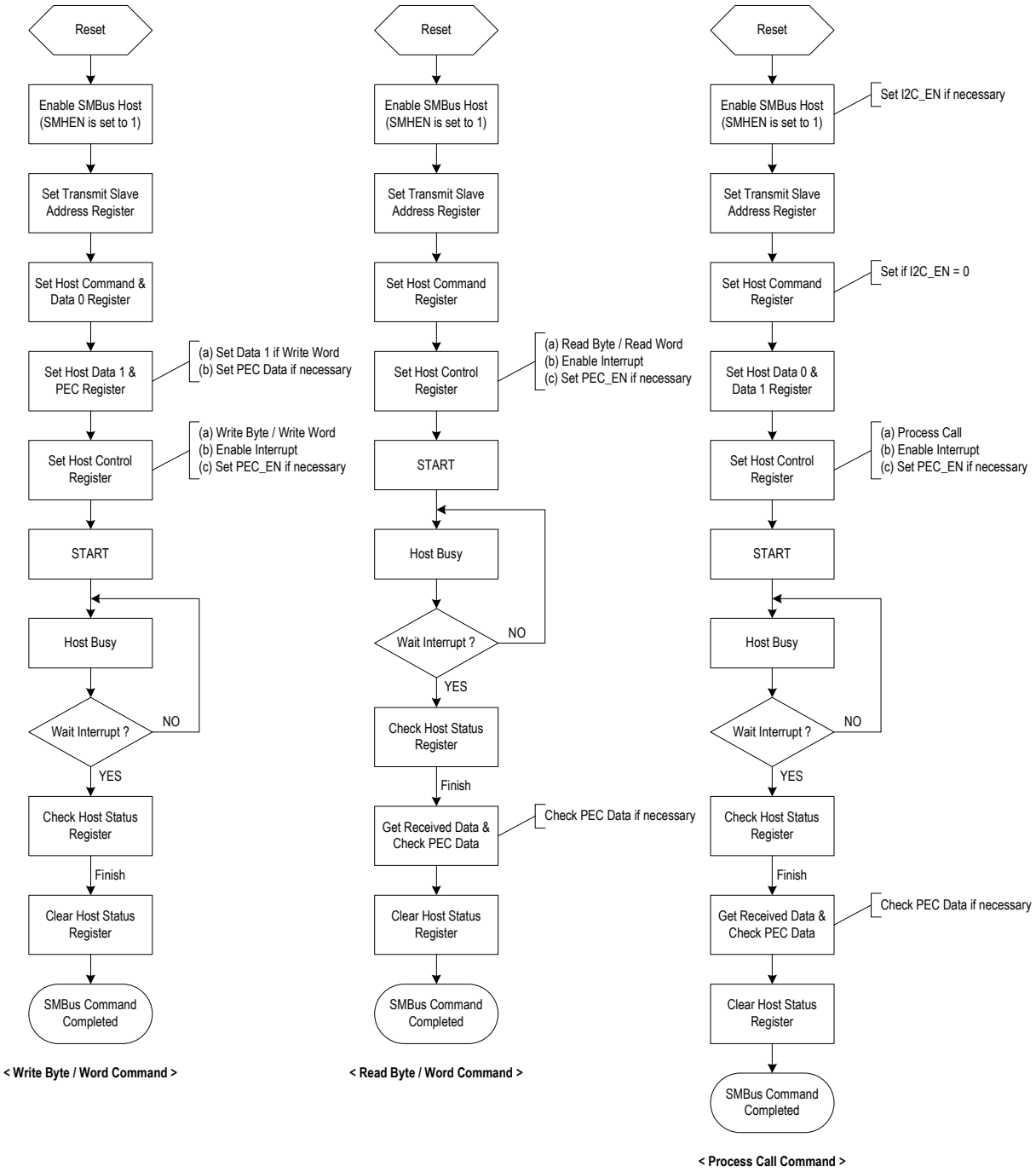
< Quick Command >

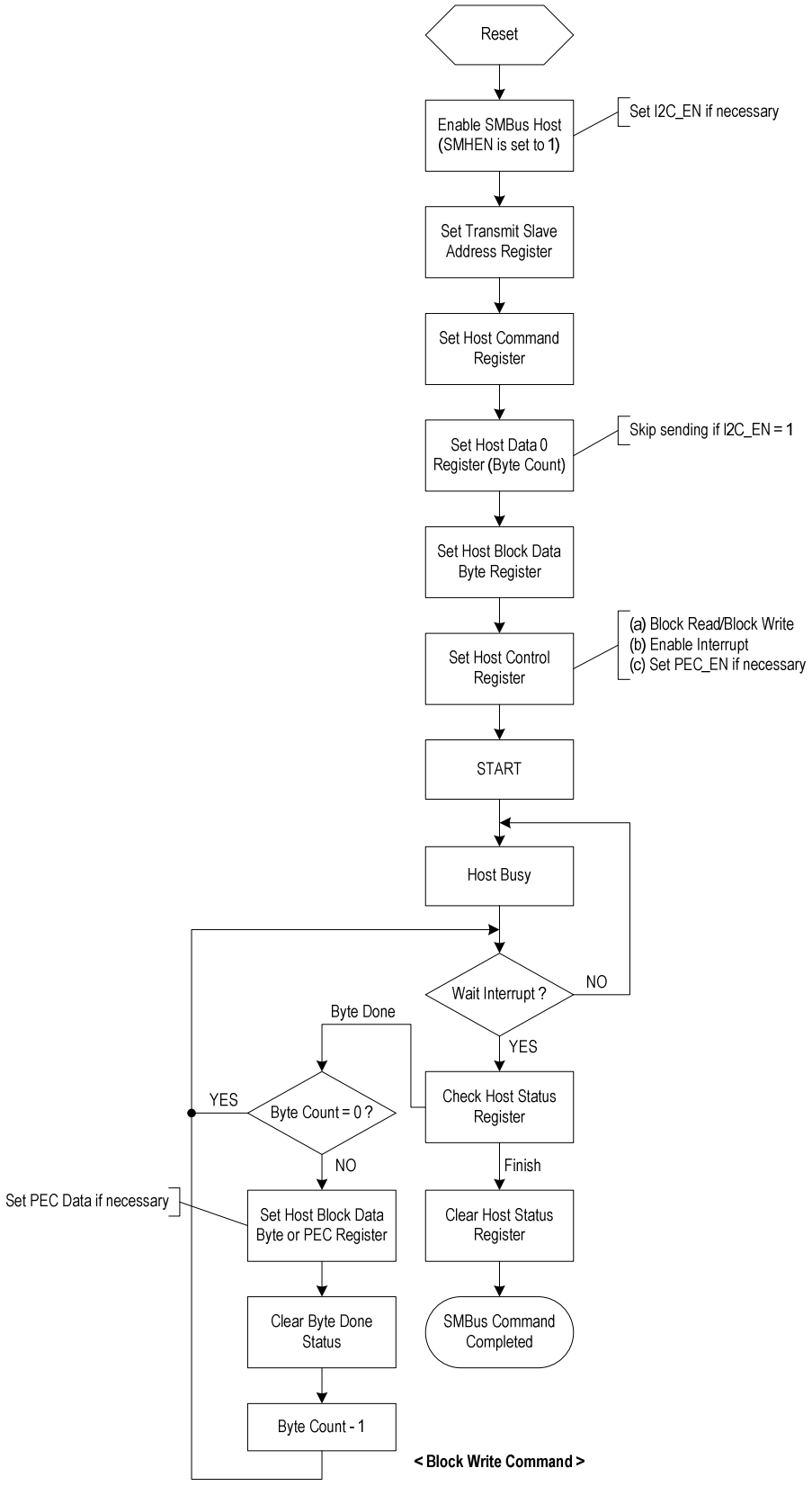


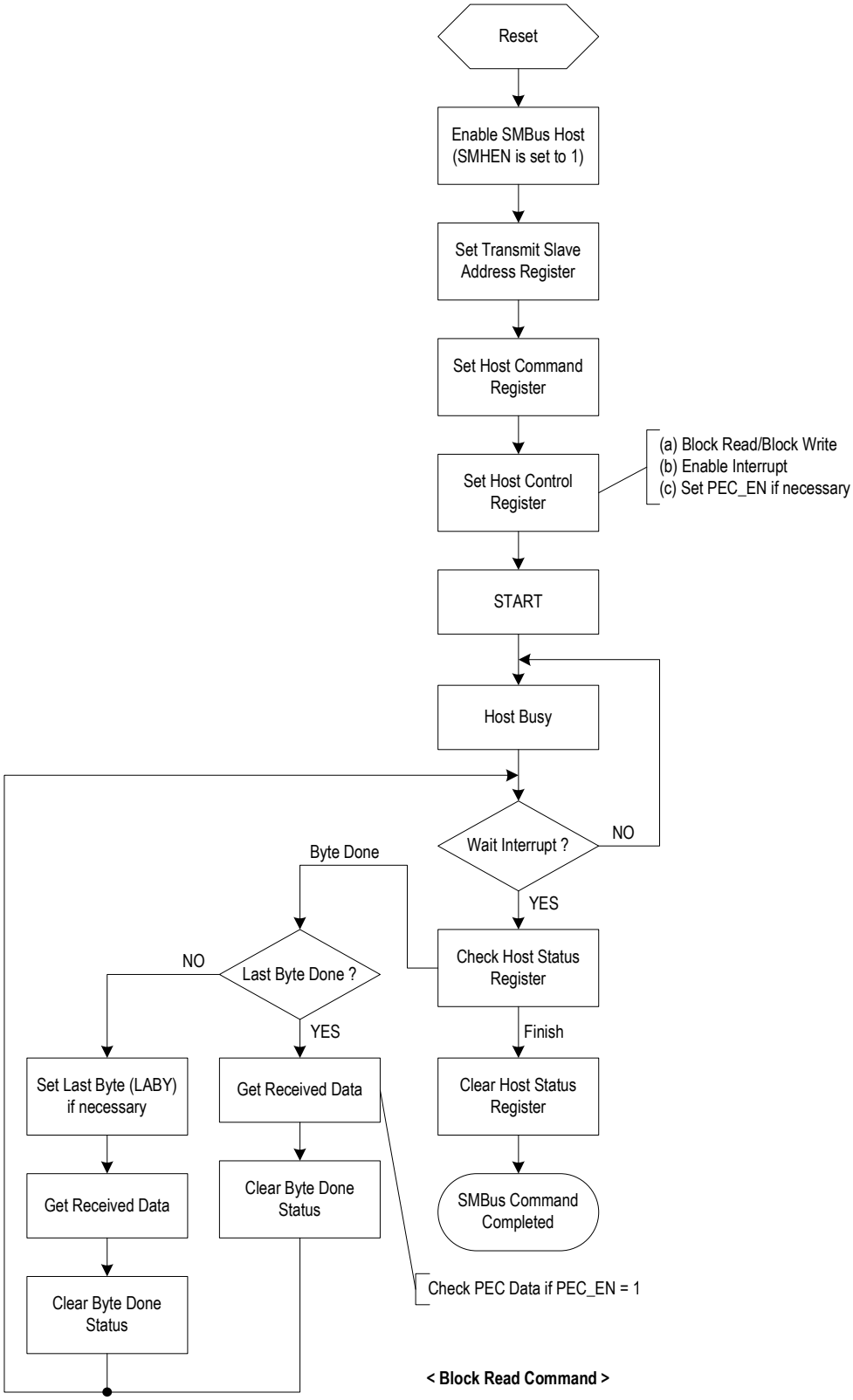
< Send Byte Command >



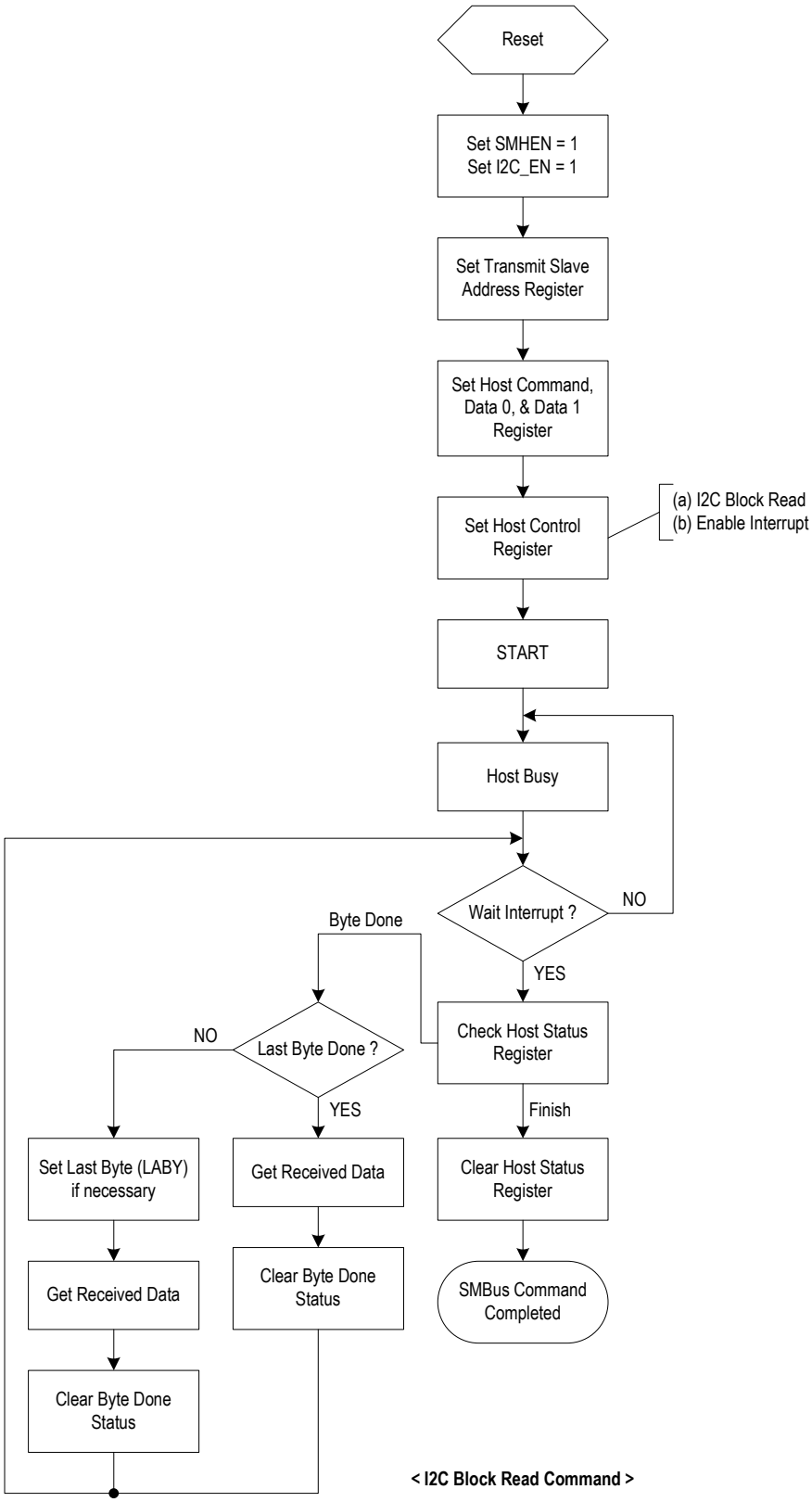
< Receive Byte Command >


Reset
Enable SMBus Host (SMHEN is set to 1)
Set Transmit Slave Address Register
Set Host Command & Data 0 Register
Set Host Data 1 & PEC Register
(a) Set Data 1 if Write Word
(b) Set PEC Data if necessary
Set Host Control Register
(a) Write Byte / Write Word
(b) Enable Interrupt
(c) Set PEC_EN if necessary
START
Host Busy
Wait Interrupt ?
NO
YES
Check Host Status Register
Finish
Clear Host Status Register
SMBus Command Completed
< Write Byte / Word Command >
Reset
Enable SMBus Host (SMHEN is set to 1)
Set Transmit Slave Address Register
Set Host Command Register
Set Host Control Register
(a) Read Byte / Read Word
(b) Enable Interrupt
(c) Set PEC_EN if necessary
START
Host Busy
Wait Interrupt ?
NO
YES
Check Host Status Register
Finish
Get Received Data & Check PEC Data
Check PEC Data if necessary
Clear Host Status Register
SMBus Command Completed
< Read Byte / Word Command >
Reset
Enable SMBus Host (SMHEN is set to 1)
Set I2C_EN if necessary
Set Transmit Slave Address Register
Set Host Command Register
Set if I2C_EN = 0
Set Host Data 0 & Data 1 Register
Set Host Control Register
(a) Process Call
(b) Enable Interrupt
(c) Set PEC_EN if necessary
START
Host Busy
Wait Interrupt ?
NO
YES
Check Host Status Register
Finish
Get Received Data & Check PEC Data
Check PEC Data if necessary
Clear Host Status Register
SMBus Command Completed
< Process Call Command >

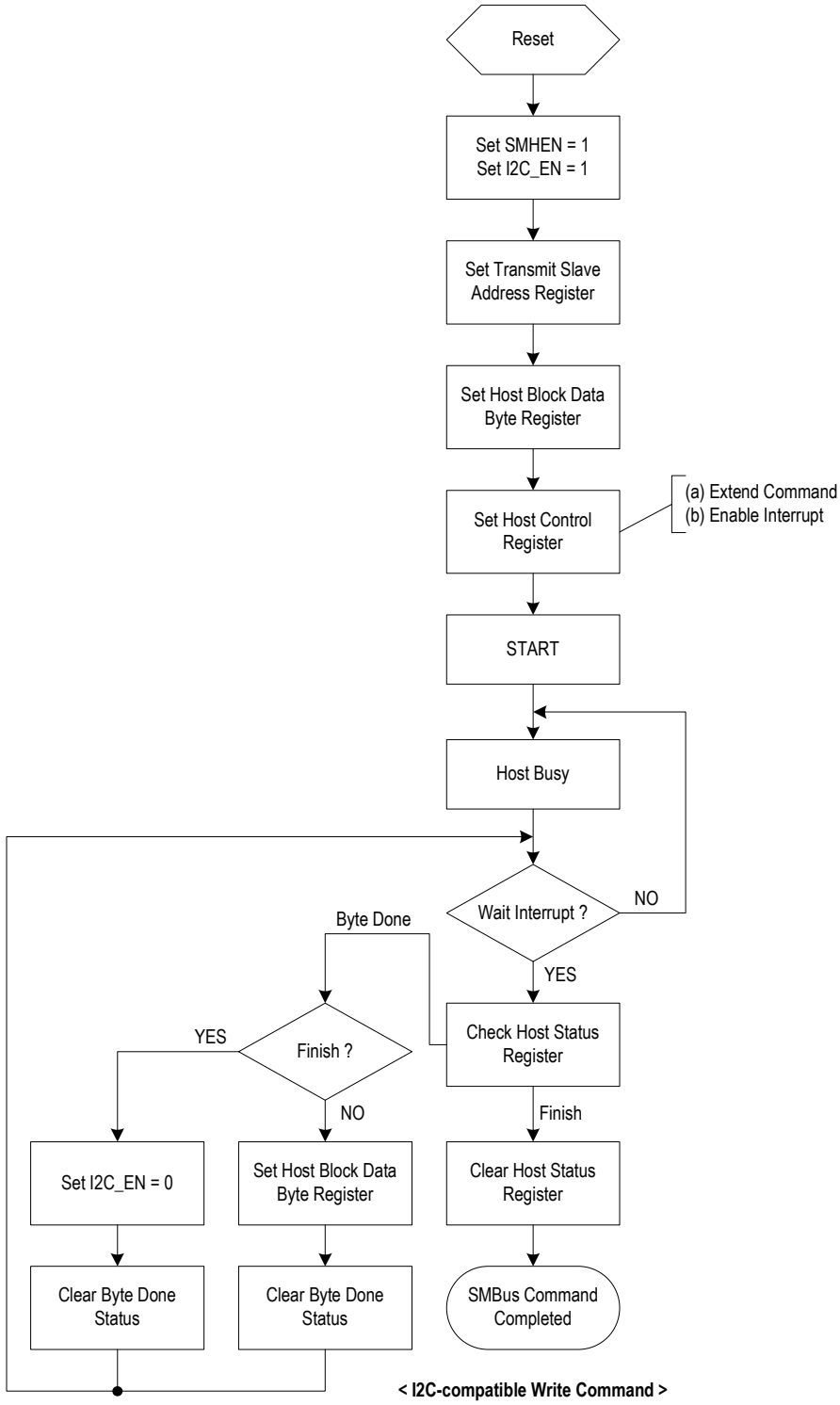

Reset
Enable SMBus Host (SMHEN is set to 1)
Set I2C_EN if necessary
Set Transmit Slave Address Register
Set Host Command Register
Set Host Data 0 Register (Byte Count)
Skip sending if I2C_EN = 1
Set Host Block Data Byte Register
Set Host Control Register
(a) Block Read/Block Write
(b) Enable Interrupt
(c) Set PEC_EN if necessary
START
Host Busy
Wait Interrupt ?
NO
YES
Byte Done
Check Host Status Register
Byte Count = 0 ?
YES
NO
Finish
Set PEC Data if necessary
Set Host Block Data Byte or PEC Register
Clear Host Status Register
Clear Byte Done Status
SMBus Command Completed
Byte Count - 1
< Block Write Command >



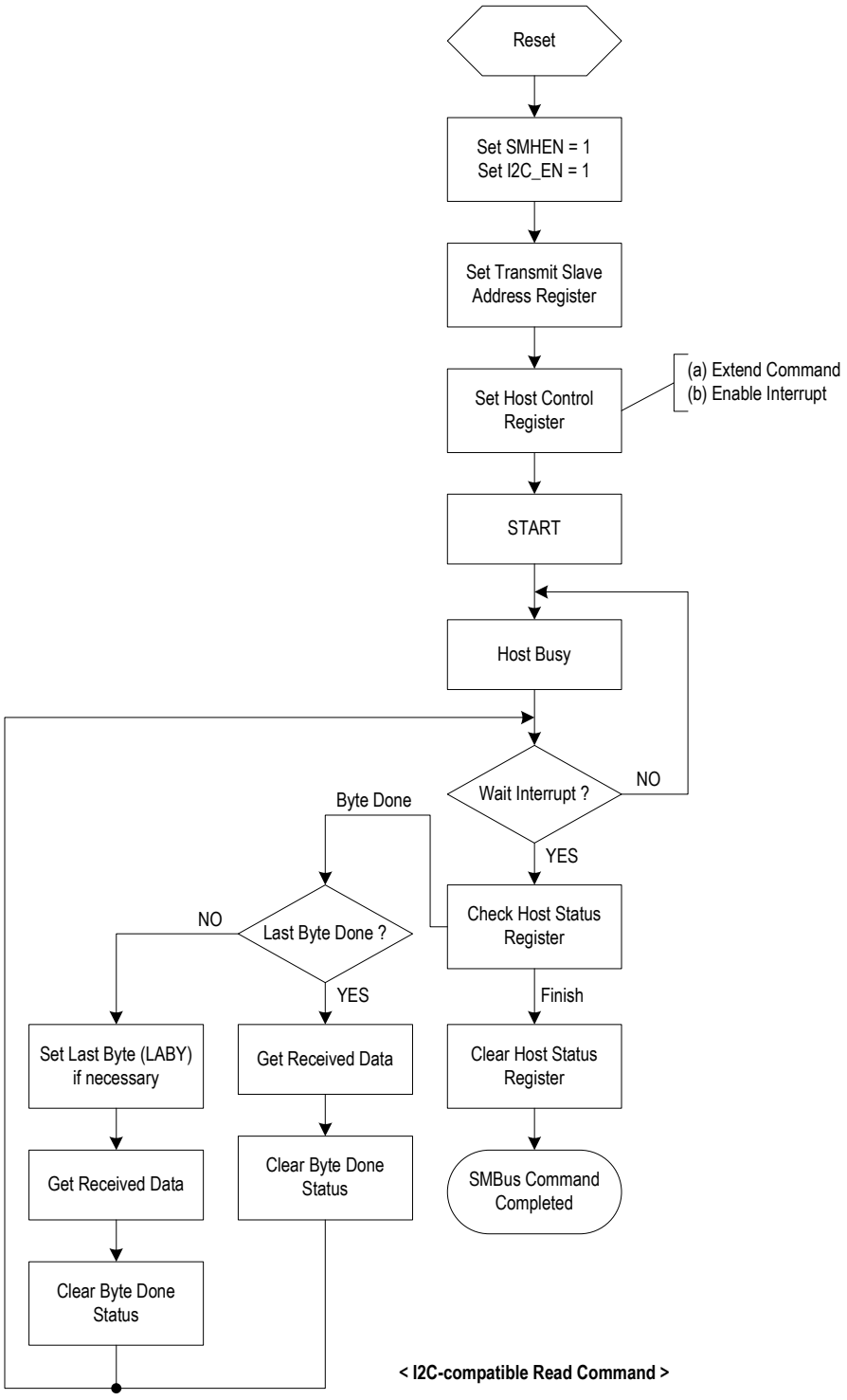
< Block Read Command >



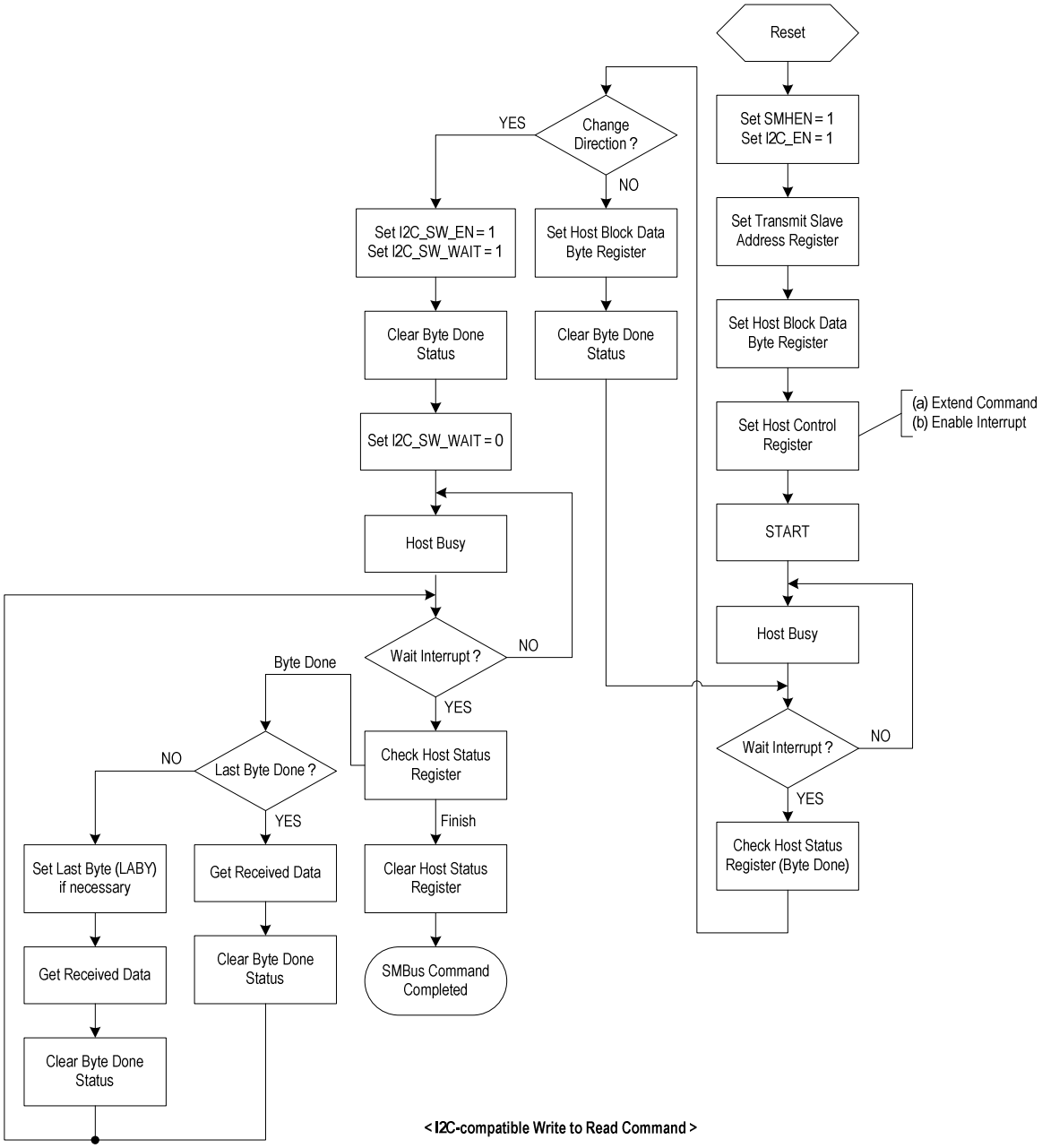
< I2C Block Read Command >



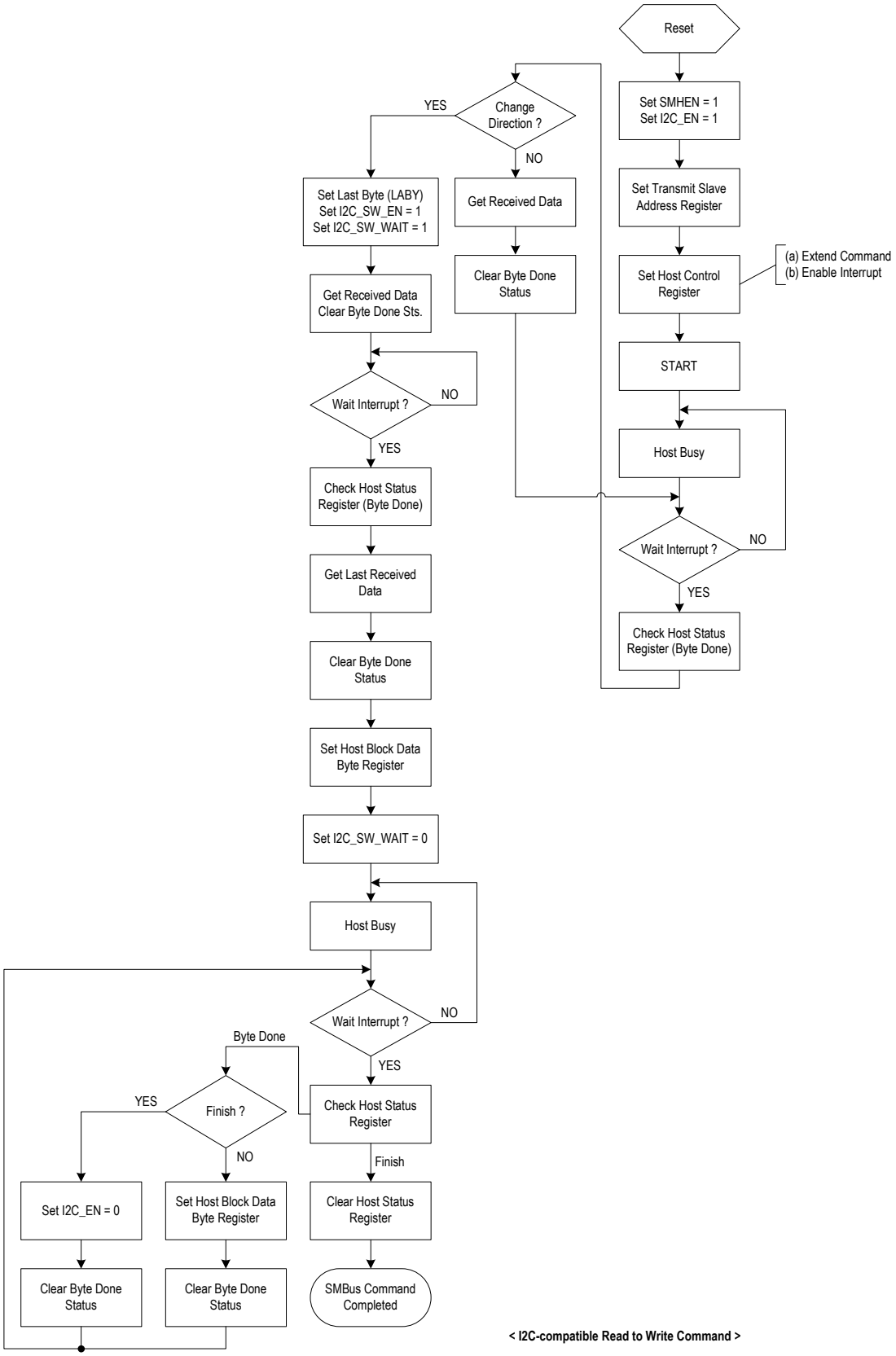
< I2C-compatible Write Command >



< I2C-compatible Read Command >



< I2C-compatible Write to Read Command >



< I2C-compatible Read to Write Command >

7.7.3.5 Description of SMCLK and SMDAT Line Control in Software Mode

(1) Control the SMCLK and SMDAT line by setting SDACTL bit and SCLCTL bit in SMBus Pin Control register (a.k.a., in software mode).
(2) When the SMCLK and SMDAT line are controlled in software mode, the hardware's SMBus logic will be reset, so the hardware will release the SMCLK and SMDAT line.
(3) The hardware's mechanism of 25 ms time-out will not work in software mode.

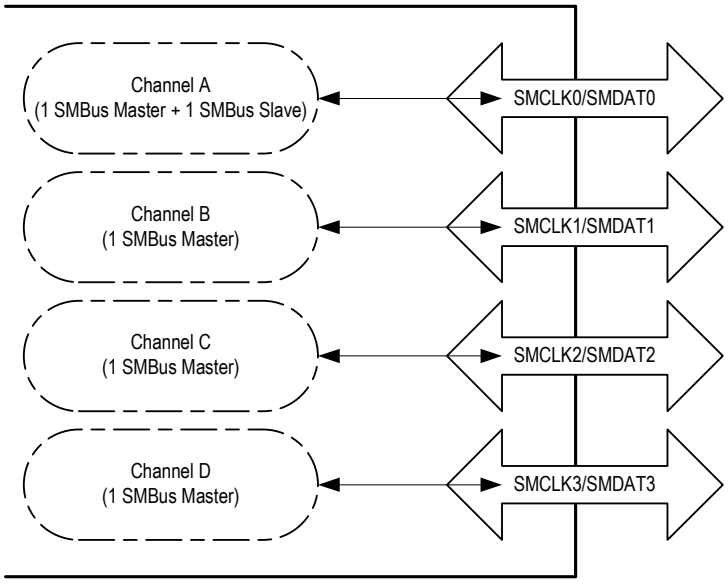
Note: It is recommended that SMCLK and SMDAT line should be controlled in software mode and hardware mode simultaneously.

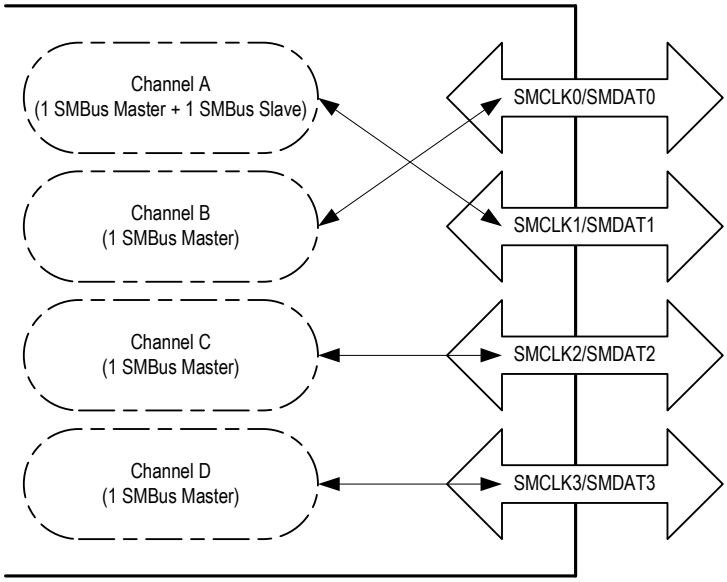
7.7.3.6 Description of SMBus Slave Interface Select

The interface of the SMBus slave can be switched from SMCLK0/SMDAT0 (default) to SMCLK1/SMDAT1, SMCLK2/SMDAT2, or SMCLK3/SMDAT3 by setting the SLVISEL bits in the Slave Interface Select Register. Followings are the detailed description:

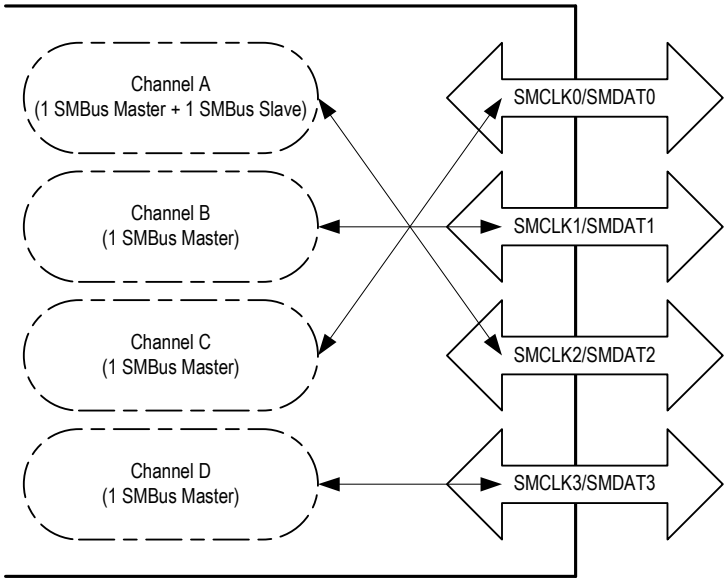
(1) When the interface of the SMBus slave is switched to SMCLK1/SMDAT1 (set the SLVISEL bits to 01b), it represents that the interface of Channel A and Channel B are exchanged, as shown in Figure 7-20.
(2) When the interface of the SMBus slave is switched to SMCLK2/SMDAT2 (set the SLVISEL bits to 10b), it represents that the interface of Channel A and Channel C are exchanged, as shown in Figure 7-21.
(3) When the interface of the SMBus slave is switched to SMCLK3/SMDAT3 (set the SLVISEL bits to 11b), it represents that the interface of Channel A and Channel D are exchanged, as shown in Figure 7-22.

Figure 7-20. Schematic Diagram of SMBus Slave Interface Select

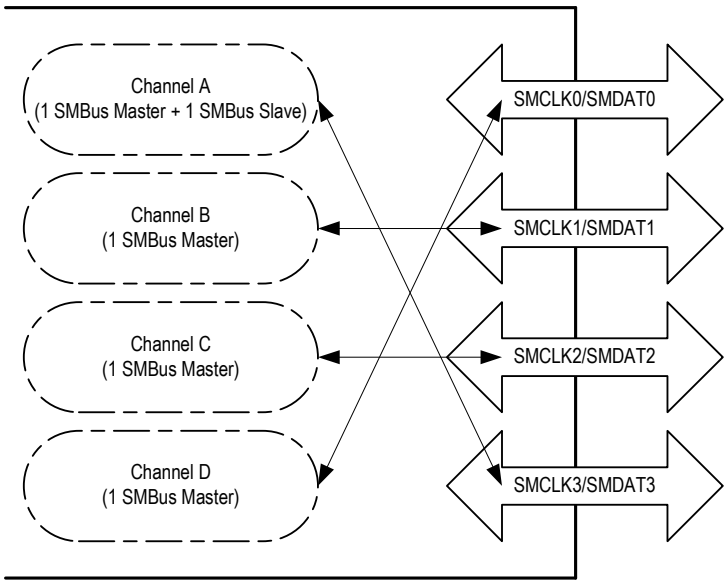




The interface of the SMBus slave is switched to SMCLK1/SMDAT1.



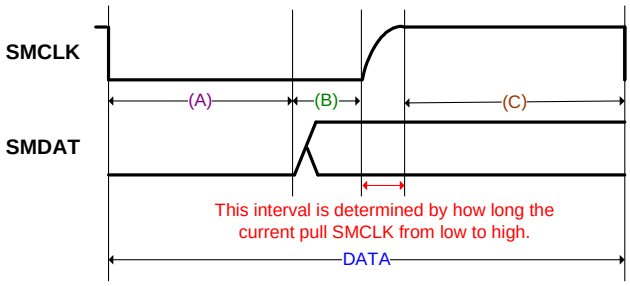
The interface of the SMBus slave is switched to SMCLK2/SMDAT2.



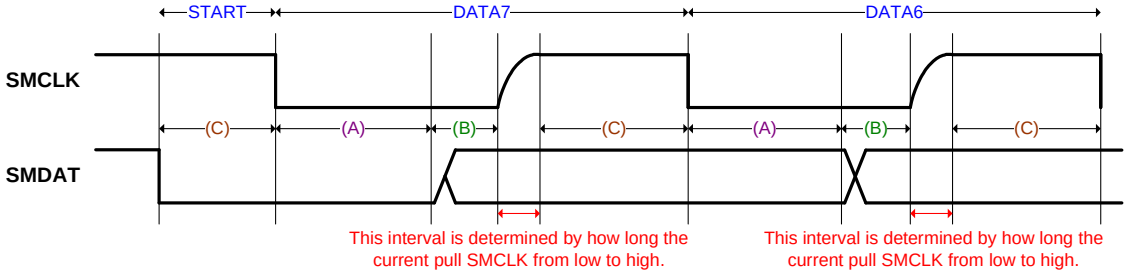
The interface of the SMBus slave is switched to SMCLK3/SMDAT3.

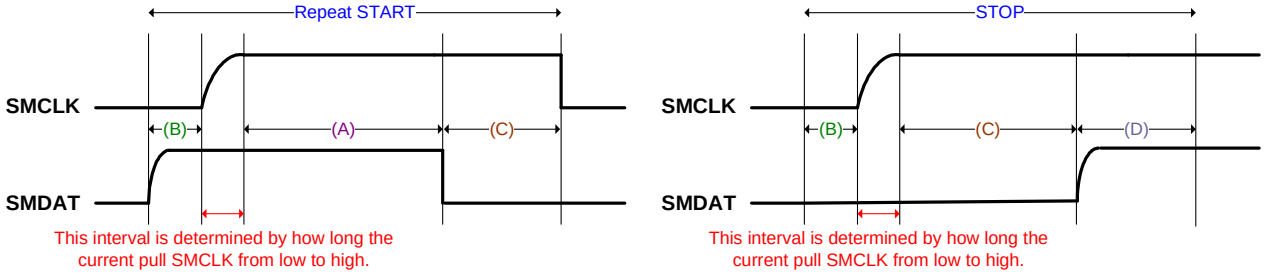
7.7.3.7 SMBus Waveform

Figure 7-21. SMBus Waveform versus SMBus Timing Registers



(A): ~=(VALUE_OF_4P7USREG / Freq_EC)
(B): ~=(VALUE_OF_250NSREG / Freq_EC)
(C): ~=(VALUE_OF_4P0USREG / Freq_EC)
(D): ~=(VALUE_OF_300NSREG / Freq_EC)
where VALUE_OF_4P7USREG consists of 4P7USH and 4P7USL.
VALUE_OF_4P0USREG consists of 4P0USH and 4P0USL.





7.7.4 EC Interface Registers

The SMBus I/O registers are listed below. The base address for SMBus is 1C00h.
A, B, C, and D are for channel A, B, C, and D respectively.

Table 7-16. EC View Register Map, SMBus

7	0	Offset
Host Status (HOSTA)(A,B,C,D)		00h,11h,29h,35h
Host Control (HOCTL)(A,B,C,D)		01h,12h,2Ah,36h
Host Command (HOCMD)(A,B,C,D)		02h,13h,2Bh,37h
Transmit Slave Address (TRASLA)(A,B,C,D)		03h,14h,2Ch,38h
Host Data 0 (D0REG)(A,B,C,D)		04h,15h,2Dh,39h
Host Data 1 (D1REG)(A,B,C,D)		05h,16h,2Eh,3Ah
Host Block Data Byte (HOBDB)(A,B,C,D)		06h,17h,2Fh,3Bh
Packet Error Check (PECERC)(A,B,C,D)		07h,18h,30h,3Ch
Receive Slave Address (RESLADR) (A)		08h
Slave Data (SLDA) (A)		09h
SMBus Pin Control (SMBPCTL)(A,B,C,D)		0Ah,1Bh,31h,3Dh
Slave Status (SLSTA) (A)		0Bh
Slave Interrupt Control (SICR) (A)		0Ch
Notify Device Address (NDADR) (A)		0Dh
Notify Data Low Byte (NDLB) (A)		0Eh
Notify Data High Byte (NDHB) (A)		0Fh
Host Control2 (HOCTL2)(A,B,C,D)		10h,21h,32h,3Eh
4.7 μs Low Register (4P7USL)		22h
4.0 μs High Register (4P0USH)		23h
300 ns Register (300NS)		24h
250 ns Register (250NS)		25h
25 ms Register (25MS)		26h
45.3 μs Low Register (45P3USL)		27h
45.3 μs High Register (45P3USH)		28h
4.7 μs and 4.0 μs High Register (4P7A4P0H)		33h
Slave Interface Select Register (SLVISEL)		34h

7.7.4.1 Host Status Register (HOSTA)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the source of the interrupt (Master Interface).

Address Offset: **Channel A: 00h**
Channel B: 11h
Channel C: 29h
Channel D: 35h

Bit	R/W	Default	Description
7	R/WC	0b	**Byte Done Status (BDS)** This bit will be set to 1 when the host controller has received a byte (for Block Read commands and I2C-compatible cycles) or if it has completed the transmission of a byte (for Block Write commands and I2C-compatible cycles).
6	R/WC	0b	**Time-out Error (TMOE)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when 25ms time-out error occurs.
5	R/WC	0b	**Not Response ACK (NACK)** 0: This bit is cleared by writing a 1 to its position. 1: This bit is set when the device does not respond ACK.
4	R/WC	0b	**Fail (FAIL)** 0: This bit is cleared by writing a 1 to the bit position. 1: Reading this bit will return 1 if KILL is set and a processing transmission is successfully killed.
3	R/WC	0b	**Bus Error (BSER)** 0: This bit is cleared by writing a 1 to the bit position. 1: The source of the interrupt is that the SMBus has lost arbitration.
2	R/WC	0b	**Device Error (DVER)** 0: This bit is cleared by writing a 1 to this bit's position. 1: This bit is set in one of the following conditions: (1) Illegal Command Field. (2) 25ms Time-out Error.
1	R/WC	0b	**Finish Interrupt (FINTR)** This bit will be set by termination of a command. 0: This bit is cleared by writing 1 to this position. 1: The source of the interrupt is the stop condition detected.
0	R	0b	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.7.4.2 Host Control Register (HOCTL)

Address Offset: **Channel A: 01h**
Channel B: 12h
Channel C: 2Ah
Channel D: 36h

Bit	R/W	Default	Description
7	R/W	0b	**PEC Enable (PEC_EN)** 0: The transaction without the PEC (Packet Error Checking) phase0 appended 1: The transaction with the PEC phase appended.
6	W	0b	**Start (SRT)** 0: This bit will always return 0 on reads. 1: When this bit is set, the SMBus host controller will perform the requested transaction.
5	W	0b	**Last Byte (LABY)** This bit is used for Block Read command and I2C-compatible read cycle. Read returns 1 if the next byte is the last byte to be received for the block read command and I2C-compatible read cycle. The firmware shall write 1 to this bit when the next byte will be the last byte to be received for the block read command and I2C-compatible cycle.
4-2	R/W	000b	**SMBus Command (SMCD)** These bits indicate which command will be performed. Bit 0 of the Transmit Slave Address Register determines if this is a read or write command. 000:Quick Command 001:Send Byte/ Receive Byte 010:Write Byte/ Read Byte 011:Write Word/ Read Word 100:Process Call 101:Block Read/ Block Write 110:I2C Block Read 111:Extend Command
1	R/W	0b	**Kill (KILL)** 0: Normal SMBus Host controller functionality. 1: When this bit is set, kill the current host transaction. This bit, once set, has to be cleared by software to allow the SMBus Host controller to function normally.
0	R/W	0b	**Host Interrupt Enable (INTREN)** 0: Disable. 1: Enable the generation of an interrupt for the master interface

7.7.4.3 Host Command Register (HOCMD)

Address Offset: **Channel A: 02h**
Channel B: 13h
Channel C: 2Bh
Channel D: 37h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCREG)** These bits are transmitted in the command field of the SMBus protocol.

7.7.4.4 Transmit Slave Address Register (TRASLA)

Address Offset: **Channel A: 03h**
Channel B: 14h
Channel C: 2Ch
Channel D: 38h

Bit	R/W	Default	Description
7-1	R/W	00h	**Address (ADR)** Address of the targeted slave.
0	R/W	0b	**Direction (DIR)** Direction of the host transfer. 0: Write 1: Read

7.7.4.5 Data 0 Register (D0REG)

Address Offset: **Channel A: 04h**
Channel B: 15h
Channel C: 2Dh
Channel D: 39h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data 0 (D0)** These bits contain the data sent in the DATA0 field of the SMBus protocol. For block write commands, this register reflects the number (from 1 to 32) of bytes to transfer.

7.7.4.6 Data 1 Register (D1REG)

Address Offset: **Channel A: 05h**
Channel B: 16h
Channel C: 2Eh
Channel D: 3Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Data 1 (D1)** These bits contain the data sent in the DATA1 field of the SMBus protocol.

7.7.4.7 Host Block Data Byte Register (HOBDB)

Address Offset: **Channel A: 06h**
Channel B: 17h
Channel C: 2Fh
Channel D: 3Bh

Bit	R/W	Default	Description
7-0	R/W	00h	**Block Data (BLDT)** For a block write command, data is sent from this register. On block read command, the received data is stored in this register.

7.7.4.8 Packet Error Check Register (PECERC)

Address Offset: **Channel A: 07h**
Channel B: 18h
Channel C: 30h
Channel D: 3Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**PEC Data (PECD)** These bits are written with the 8-bit CRC value that is used as the SMBus PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBus into this register and is then read by software.

7.7.4.9 Receive Slave Address Register (RESLADR)

Address Offset: **08h (Only for Channel A)**

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	00h	**Slave Address (SADR)** These bits are the slave address decoded for read and write cycles.

7.7.4.10 Slave Data Register (SLDA)

Address Offset: **09h (Only for Channel A)**

Bit	R/W	Default	Description
7-0	R/W	00h	**Slave Data Byte0 (SDB0)** This register stores the data received from the external master.

7.7.4.11 SMBus Pin Control Register (SMBPCTL)

Address Offset: **Channel A: 0Ah**
Channel B: 1Bh
Channel C: 31h
Channel D: 3Dh

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	R/W	1b	**SMDAT Control (SDACTL)** 0: The SMDAT0/1/2/3 pin will be driven low regardless of the other SMBus logic. 1: The SMDAT0/1/2/3 pin will not be driven low. The other SMBus logic controls this pin.
2	R/W	1b	**SMCLK Control (SCLCTL)** 0: The SMCLK0/1/2/3 pin will be driven low regardless of the other SMBus logic. 1: The SMCLK0/1/2/3 pin will not be driven low. The other SMBus logic controls this pin.
1	R	-	**SMDAT Current State (SMBDCS)** This bit returns the value of the SMDAT0/1/2/3 pin. 0: Low 1: High
0	R	-	**SMCLK Current State (SMBCS)** This bit returns the value of the SMCLK0/1/2/3 pin. 0: Low 1: High

7.7.4.12 Slave Status Register (SLSTA)

Software can read this register to know the source of the interrupt (Slave Interface).

Address Offset: 0Bh (Only for Channel A)

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	R	0b	**Read Cycle Status (RCS)** Direction of the slave transfer. 0: Write. 1: Read.
2	R/WC	0b	**Slave Timeout Status (STS)** 0: Cleared by writing a 1 to this bit. 1: Timeout status occurs.
1	R/WC	0b	**Slave Data Status (SDS)** 0: Cleared by writing a 1 to this bit. 1: Slave Data Register is waiting for read or write. When this bit is set and the Read Cycle Status (RCS) bit is low, the software shall read the data from the Slave Data Register. When this bit is set and the Read Cycle Status (RCS) bit is high, the software shall write the data to the Slave Data Register.
0	R/WC	0b	**Host Notify Status (HONOST)** This bit will be set to a 1 when a Host Notify Command has been completely received. Software can read this bit to determine that the source of the interrupt is the reception of the Host Notify Command.

7.7.4.13 Slave Interrupt Control Register (SICR)

Address Offset: 0Ch (Only for Channel A)

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	0b	**Slave Interrupt Enable (SITEN)** 0: Disable. 1: Enable the generation of an interrupt for the slave interface.
0	R/W	0b	**Host Notify Interrupt Enable (HONOIN)** 0: Disable. 1: Enable the generation of an interrupt when Host Notify Status is set and it dose not affect the setting of the Host Notify Status bit.

7.7.4.14 Notify Device Address Register (NDADR)

Address Offset: 0Dh (Only for Channel A)

Bit	R/W	Default	Description
7-1	R	00h	**Device Address (DVADR)** These bits contain the 7-bit device address received during the Host Notify protocol of the SMBus 2.0 Specification.
0	-	0b	**Reserved**

7.7.4.15 Notify Data Low Byte Register (NDLB)

Address Offset: 0Eh (Only for Channel A)

Bit	R/W	Default	Description
7-0	R	00h	**Data Low Byte (DALB)** These bits contain the first (low) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.7.4.16 Notify Data High Byte Register (NDHB)

Address Offset: 0Fh (Only for Channel A)

Bit	R/W	Default	Description
7-0	R	00h	**Data High Byte (DAHB)** These bits contain the second (high) byte of data received during the Host Notify protocol of the SMBus 2.0 Specification.

7.7.4.17 Host Control Register 2 (HOCTL2)

Address Offset: Channel A: 10h
Channel B: 21h
Channel C: 32h
Channel D: 3Eh

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5	W	0b	**SMBus Slave Enable (SLVEN)** 0: Disable the SMBus Slave Device. 1: Enable the SMBus Slave Device. The SMBus Host Controller is disabled when this bit is set.
4	-	-	**Reserved**
3	R/W	0b	**I2C Switch Direction Enable (I2C_SW_EN)** 0: Disable I2C Switch Direction. 1: Enable I2C Switch Direction.
2	R/W	0b	**I2C Switch Direction Wait (I2C_SW_WAIT)** 0: Disable I2C Switch Direction Wait. 1: Enable I2C Switch Direction Wait.
1	R/W	0b	**I2C Enable (I2C_EN)** 0: SMBus behavior. 1: Enable to communicate with I2C device and support I2C-compatible cycles. When this bit is set, the SMBus logic will instead be set to communicate with I2C devices and support I2C-compatible cycles. This forces the following changes: (1) The Process Call command will skip the Command code. (2) The Block Write command will skip sending the Byte Count. (3) The Extend command can be used to support I2C-compatible cycles.
0	R/W	0b	**SMBus Host Enable (SMHEN)** 0: Disable the SMBus Host Controller. 1: The SMBus Host interface is enabled to execute commands.

7.7.4.18 Slave Interface Select Register (SLVISELR)

Address Offset: 34h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**SMBus Slave Interface Select (SLVISEL)** These bits are to decide which interface the slave is located at. 00: Slave interface is located at SMCLK0/SMDAT0. 01: Slave interface is located at SMCLK1/SMDAT1. 10: Slave interface is located at SMCLK2/SMDAT2. 11: Slave interface is located at SMCLK3/SMDAT3.

7.7.4.19 4.7 μs Low Register (4P7USL)

The following registers (22h-28h, 33h) define the SMCLK0/1/2/3 and SMDAT0/1/2/3 timing.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.7 μs Low Register (4P7USL)** This 4.7 μs Low Register and 4.7 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.7 μs counter. The 4.7 μs is (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.20 4.0 μs Low Register (4P0USL)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.0 μs Low Register (4P0USL)** This 4.0 μs Low Register and 4.0 μs high bit (in the 4.7 μs and 4.0 μs High Register) define the count number for the 4.0 μs counter. The 4.0 μs is (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.21 300 ns Register (300NSREG)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	00h	**300ns Register (300NS)** This field defines the SMDAT0/1/2/3 hold time. This byte is the count number of the counter for 300 ns. The 300 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.22 250 ns Register (250NSREG)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	**250ns Register (250NS)** This field defines the SMDAT0/1/2/3 setup time. This byte is the count number of the counter for 250 ns. The 250 ns is calculated by (count number / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.23 25 ms Register (25MSREG)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	00h	**25 ms Register (25MS)** This field defines the SMCLK0/1/2/3 clock low timeout. This byte is the count number of the counter for 25 ms. The 25 ms is calculated by (count number *1.024 kHz).

7.7.4.24 45.3 μs Low Register (45P3USLREG)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs Low Register (45P3USLOW)** This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK0/1/2/3 high periodic (maximal). (45.3μs + 4.7μs=50μs) This byte is the count number bits [7:0] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.25 45.3 μs High Register (45P3USHREG)

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs High Register (45P3USHGH)** This 45.3 μs Low Register, 45.3 μs High Register, 4.7us Low Register and 4.7us high bit (in the 4.7μs And 4.0 μs High Register) define the SMCLK0/1/2/3 high periodic (maximal). (45.3 μs + 4.7μs=50μs). This byte is the count number bits [15:8] of the counter for 45.3 μs. The 45.3 μs is calculated by (count number[15:0] / FreqEC). (FreqEC is listed in Table 10-2 on page 352)

7.7.4.26 4.7 μs And 4.0 μs High Register (4p7A4P0H)

Address Offset: 33h

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**4.0 μs High Bit (4P0USH)** This bit is bit 8 of the count number for the 4.0 μs counter. This 4.0 μs Low Register and 4.0μs High Bit define the count number for the 4.0 μs counter.
0	R/W	0b	**4.7 μs High Bit (4P7USH)** This bit is bit 8 of the count number for the 4.7 μs counter. This 4.7 μs Low Register and 4.7μs High Bit define the count number for the 4.7 μs counter.

7.8 PS/2 Interface

7.8.1 Overview

The PS/2 device uses a two-wire bi-directional interface for data transmission. The device consists of three identical channels. Each of the three channels provides two signals (CLK and DATA line) to communicate with the auxiliary device. The PS/2 interface also connects the CLK line and DATA line to the WUC (WU10-WU17) to wake-up the 8032 when these lines are toggled.

CLK line and DATA line are the same as PS2CLKn and PS2DATn (n=0,1 or 2) pins. Refer to Table 5-6 on page 20 for the details.

7.8.2 Features

- Supports three PS/2 channels.
- Supports hardware/software mode selection.
- Three interrupt features are available: Start Interrupt, Transaction Done Interrupt, and Software Mode Interrupt (INT18, INT19 and INT20).

7.8.3 Functional Description

The PS/2 Interface has two operation methods: Hardware mode and software mode. When the hardware mode is enabled, the PS/2 interface can perform automatic reception or transmission depending on the TRMS bit in the PSCTL register. When the hardware mode is disabled (software mode is enabled), the PS/2 CLK line and DATA line are controlled by the firmware via the CCLK bit and CDAT bit in the PSCTL register. The following sections will describe how to use the PS/2 interface.

7.8.3.1 Hardware Mode Selected

Receive Mode
Here are the steps the host shall follow to receive data from a PS/2 device.

1. Enable the hardware mode, select the receive mode, and release the CLK line and DATA line (Write 07h to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register has to be set to 1 because when the data transmission is completed, the data in PS/2 Data Register needs to be read.)

After these steps, the PS/2 interface is ready to receive data. When the data transmission is completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register and the received data can be read from the PS/2 Data Register. The PS/2 CLK line will be held low until the PS/2 Data Register is read.

Transmit Mode
Here are the steps the host shall follow to send data to a PS/2 device.
1. Enable the hardware mode, select the transmit mode, and pull the CLK line low and DATA line high (Write 0Dh to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register has to be set to 1 because when the data transmission is completed, the data in PS/2 Status Register needs to be read.)
3. Write the data to be transmitted to the PS/2 Data Register.
4. Pull the DATA line low (Write 0Ch to the PS/2 Control Register).
5. Pull the CLK line high (Write 0Eh to the PS/2 Control Register).

After these steps, the PS/2 interface is ready to transmit data. When the data transmission is completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register. The CLK line will be held low until the PS/2 Status Register is read.

Input Signal Debounce
This PS/2 Interface performs a debounce operation on the CLK input signal before determining its logical value. When this operation is enabled (DCEN bit in the PS/2 Control Register is set to 1), the CLK input signal has to be stable for at least 4 clock cycles.

7.8.3.2 Software Mode Selected

Software Control PS/2 CLK line and DATA line
When the Software Mode is selected (PSHE=0 in PS/2 Control Register), the software can control the PS/2 CLK line and DATA line. The CCLK bit and CDAT bit in the PS/2 Control Register control the CLK line and DATA line. When one of these bits is cleared, the relevant pin is held low. When one of these bits is set, the relevant pin is pulled high.

Software Control the Interrupt
When the PS/2 Hardware Enable bit is cleared (PSHE=0 in PS/2 Control Register) and the Software Mode Interrupt Enable bit is set (SMIE=1 in PS/2 Interrupt Control Register), the software can control the PS/2 interrupt. The interrupt is set high when the CCLK bit in PS/2 Control Register is set high. If such an interrupt is not desired, clear the Software Mode Interrupt Enable bit (SMIE=0 in PS/2 Interrupt Control Register).

7.8.4 EC Interface Registers

The PS/2 interface registers are listed below. The base address for PS/2 is 1700h.

Table 7-17. EC View Register Map, PS/2

7	0	Offset
PS/2 Control Register 1 (PSCTL1)		00h
PS/2 Control Register 2 (PSCTL2)		01h
PS/2 Control Register 3 (PSCTL3)		02h
PS/2 Interrupt Control Register 1 (PSINT1)		04h
PS/2 Interrupt Control Register 2 (PSINT2)		05h
PS/2 Interrupt Control Register 3 (PSINT3)		06h
PS/2 Status Register 1 (PSSTS1)		08h
PS/2 Status Register 2 (PSSTS2)		09h
PS/2 Status Register 3 (PSSTS3)		0Ah
PS/2 Data Register 1 (PSDAT1)		0Ch
PS/2 Data Register 2 (PSDAT2)		0Dh
PS/2 Data Register 3 (PSDAT3)		0Eh

7.8.4.1 PS/2 Control Register 1-3 (PSCTL1-3)

This register controls the operation of the PS/2 interface. PS/2 Control Register 1-3 are for channel 1-3 respectively.

Address Offset: 00h~02h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Debounce Circuit Enable (DCEN)** 0: The debounce circuit is disabled. 1: The debounce circuit is enabled.
3	R/W	0b	**Transmit / Receive Mode Selection (TRMS)** 0: Receive mode is selected. 1: Transmit mode is selected.
2	R/W	0b	**PS/2 Hardware Enable (PSHE)** When this bit is set to 1, the PS/2 channel can perform automatic reception or transmission. When this bit is 0, the channel's CLK and DATA lines are controlled by the CCLK and CDAT bits in this register. 0: PS/2 hardware mode is disabled (Software mode is enabled). 1: PS/2 hardware mode is enabled.
1	R/W	0b	**Control CLK Line (CCLK)** This bit can control the CLK line. 0: The CLK line is held low. 1: The CLK line is pulled high.
0	R/W	1b	**Control DATA Line (CDAT)** This bit can control the DATA line. 0: The DATA line is held low. 1: The DATA line is pulled high.

7.8.4.2 PS/2 Interrupt Control Register 1-3 (PSINT1-3)

This register enables or disables various interrupts sources. PS/2 Interrupt Control Register 1-3 are for channel 1-3 respectively.

Address Offset: 04h~06h

Bit	R/W	Default	Description
7-3	-	00000b	**Reserved**
2	R/W	0b	**Transaction Done Interrupt Enable (TDIE)** Enable or disable the interrupt generation when the Transaction Done status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
1	R/W	0b	**Start Interrupt Enable (SIE)** Enable or disable the interrupt generation when the Start status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
0	R/W	0b	**Software Mode Interrupt Enable (SMIE)** Enable or disable the interrupt generation when the PS/2 hardware is disabled. The CCLK bit in PSCTL register can control the interrupt output when this bit is set to 1 and PS/2 hardware is disabled. 0: Disable the interrupt. 1: Enable the interrupt.

7.8.4.3 PS/2 Status Register 1-3 (PSSTS1-3)

This register contains the status information on the data transfer on the PS/2. Status Register 1-3 are for channel 1-3 respectively.

Address Offset: 08h~0Ah

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R	0b	**Frame Error (FER)** This bit is 1 when the stop bit in a received frame was detected low.
4	R	0b	**Parity Error (PER)** This bit is 1 when a parity error condition occurs.
3	R	0b	**Transaction Done Status (TDS)** This bit is 1 when a PS/2 data transfer is done.
2	R	0b	**Start Status (SS)** This bit is 1 when a start bit is detected.
1	R	-	**CLK Line Status (CLS)** Reading this bit returns the current status of the PS/2 CLK line.
0	R	-	**DATA Line Status (DLS)** Reading this bit returns the current status of the PS/2 DATA line.

7.8.4.4 PS/2 Data Register 1-3 (PSDAT1-3)

In receive mode, this register holds the data received from the PS/2 device. In transmit mode, the data in this register is transmitted to the PS/2 device. Data Register 1-3 are for channel 1-3 respectively.

Address Offset: 0Ch~0Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Data (DAT)** Holds the data received from the PS/2 device in the receive mode or the data which will be transmitted in the transmit mode.

7.9 Digital To Analog Converter (DAC)

7.9.1 Overview

The DAC interface is used as a communication interface between the embedded controller and DAC.

7.9.2 Feature

- Supports 6-channel D/A converter
- 8-bit resolution
- Independent enable signals for each channel
- Power-down function

7.9.3 Functional Description

The DAC interface has six channels. Each channel generates an output in the range of 0V to AVCC with eight-bit resolution. When a DAC channel is enabled, its output is defined by the value written to its DACDAT register. DACDAT 0-5 control channel 0-5 respectively. The 0V output is obtained for a value of 00h in the DACDAT register. The AVCC output is obtained for a value of FFh in the DACDAT register. In power-down mode (POWDNx=1 in DAC Power Down Register), the DAC output is 0V.

DAC analog circuit has less power consumption if it is power-down. POWDNx bit in DAC Power Down Register controls this and it's cleared during EC domain reset.
The firmware should clear POWDN bit in the DAC Power Down Register before entering Idle/Doze/Sleep mode.

7.9.4 EC Interface Registers

The DAC interface registers are listed below. The base address for DAC is 1A00h.

Table 7-18. EC View Register Map, DAC

7	0	Offset
DAC Power Down Register (DACPDREG)		01h
DAC Data Channel 0 (DACDAT0)		02h
DAC Data Channel 1 (DACDAT1)		03h
DAC Data Channel 2 (DACDAT2)		04h
DAC Data Channel 3 (DACDAT3)		05h
DAC Data Channel 4 (DACDAT4)		06h
DAC Data Channel 5 (DACDAT5)		07h

7.9.4.1 DAC Power Down Register (DACPDREG)

When the bit in this register is set, the respective DAC channels will be power-down.

Address Offset: 01h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5	R/W	1b	**DAC Channel 5 Power Down (POWDN5)** 0: The DAC channel 5 is not power-down. 1: The DAC channel 5 is power-down.
4	R/W	1b	**DAC Channel 4 Power Down (POWDN4)** 0: The DAC channel 4 is not power-down. 1: The DAC channel 4 is power-down.
3	R/W	1b	**DAC Channel 3 Power Down (POWDN3)** 0: The DAC channel 3 is not power-down. 1: The DAC channel 3 is power-down.
2	R/W	1b	**DAC Channel 2 Power Down (POWDN2)** 0: The DAC channel 2 is not power-down. 1: The DAC channel 2 is power-down.
1	R/W	1b	**DAC Channel 1 Power Down (POWDN1)** 0: The DAC channel 1 is not power-down. 1: The DAC channel 1 is power-down.
0	R/W	1b	**DAC Channel 0 Power Down (POWDN0)** 0: The DAC channel 0 is not power-down. 1: The DAC channel 0 is power-down.

7.9.4.2 DAC Data Channel 0~5 Register (DACDAT0~5)

The data in these registers will be loaded into channel 0~5.

Address Offset: Channel 0: 02h
Channel 1: 03h
Channel 2: 04h
Channel 3: 05h
Channel 4: 06h
Channel 5: 07h

Bit	R/W	Default	Description
7-0	R/W	-	**DAC Data Register (DACDAT)** 8 bit data will be loaded to the DAC for D/A operation.

7.10 Analog to Digital Converter (ADC)

7.10.1 Overview

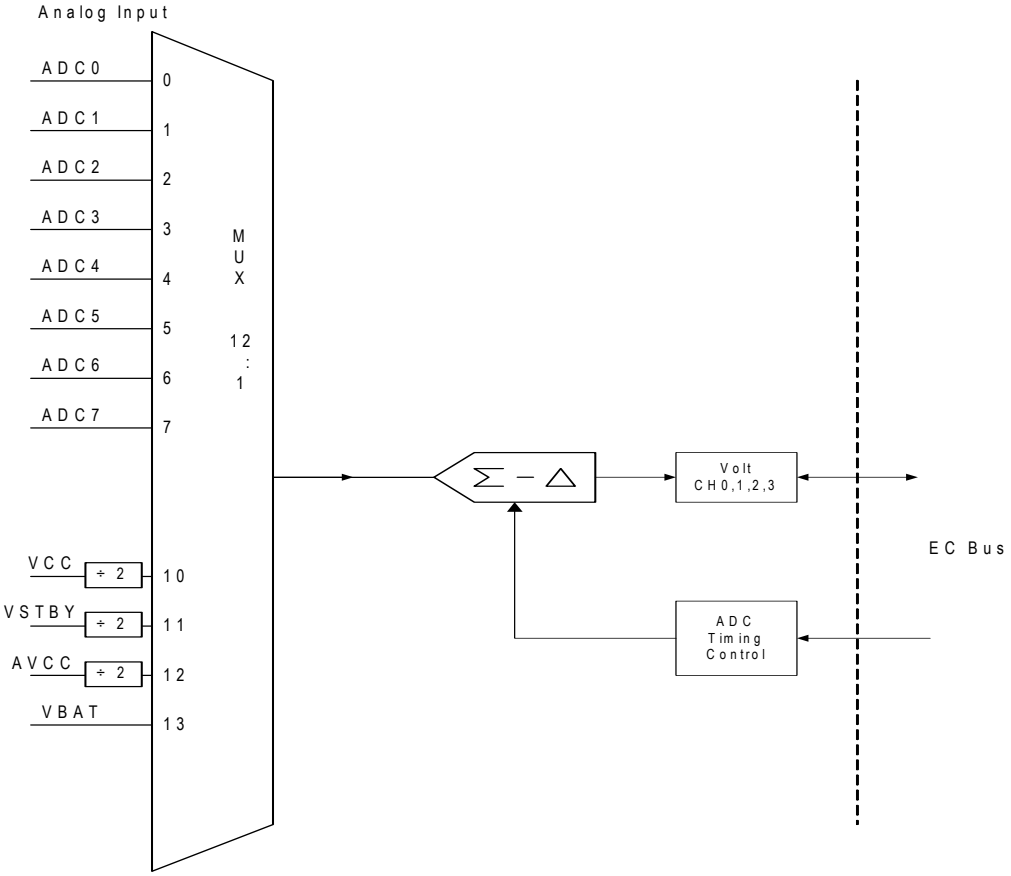
The ADC(analog to digital converter) provides an accurate method for measuring slow changing voltages. The module can measure the channel up to twelve-voltage with 10-bit resolution.

7.10.2 Features

- Supports 10-bit resolution after software calibration and 0 to 3V input voltage range
- Supports an digital low pass filter for spike smoothing
- Supports four-voltage buffers
- Supports fast AD conversion of 12 channels within 100 ms
- Supports programmable conversion-start delay to guarantee input setting time
- Polling or interrupt-driven interface

7.10.3 Functional Description

Figure 7-22. ADC Channels Control Diagram



7.10.3.1 ADC General Description

Inputs
The ADC has 12 inputs (ADC0-7, ADC10~13) divided into two groups described as the following:
• External Voltage (ADC0-7):
These are for DC voltage sources.

• Internal Voltage (ADC10-13):
These are connected to the internal supply voltages of the device (VCC, VSTBY AVCC and VBAT).
The input voltages of ADC10-12 are divided by 2 before being input to analog multiplexer while ADC13 is not divided by 2.

A/D Converter
The sigma-delta high-resolution A/D converter receives the selected input with a 16 to 1 analog multiplier and converts it. The result of the conversion is 14-bit signed integer (2's complement) and it is a 10-bit, unsigned integer for voltage inputs after software calibration process.

For the software calibration flow, refer to section 7.10.5 ADC Programming Guide.

ADC Cycle
The ADC has four output buffers: These are for the voltage channel. The buffer for voltage measurement channels holds the current data until the next same volt channel measurement is completed after one ADC cycle is finished. An ADC cycle includes measurements of all four channels. The first measurement is a voltage channel 0 and followed by voltage channel 1, 2, 3. After an A/D conversion is completed for a certain channel, its related bit in the Data Valid (DATVAL bit in VCH0CTL, VCH1CTL, VCH2CTL and VCH3CTL register) flag is set that represents the channel of data is available and EC can read out.

Channel Conversion Time
If channel delay uses a default value, which means VOLDLY is delayed 256 k units, SCLKDIV factor in ADCCTL register is also set by default, and DFILEN is set to 1, the one channel conversion time is about 3.6msec. If DFILEN is set to 0, the one channel conversion time is about 780usec.

Interrupt to INTC
ADC interrupt (INT8) will be active if end-of-cycle, voltage channel 0 data valid, voltage channel 1 data valid, voltage channel 2 data valid or voltage channel 3 data valid is true. See also INTECEN, INTDVEN0, INTDVEN1, INTDVEN2 and INTDVEN3.

ADC Configuration

Table 7-19. ADC Configuration

Configuration	DFILEN	FIRHIACC	SDIVSRC	Note
FIR Filter Enabled, High Accuracy	1	1	0/1	
FIR Filter Enabled, Low Accuracy	1	0	1	
FIR Filter Disabled	0	X	0/1	X means “don’t-care”
Invalid Configuration	All other combinations are invalid.			

7.10.3.2 Voltage Measurement and Automatic Hardware Calibration

The ADC converts the un-calibrated input voltage signal into a 14-bit singed integer (2's complement) in data buffer VCHiDATL and VCHiDATM when AHCE (Automatic Hardware Calibration Enable) is cleared(default), and converted into a 10-bit unsigned integer in data buffer VCHiDATL and VCHiDATM when AHCE(Automatic Hardware Calibration Enable) is set. The automatic hardware calibration is used for the alternative of the software calibration flow. The input signal should be applied related to the AGND pin and should range from 0V to 3V.
The following should explain the input voltage based on the reading from the Voltage/Channel Data result

(VCHiDATL field in VCHiDATM register for voltage).

Example (Refer to the bottom of Figure 7-23 on page 259 for the details:
The un-calibrated input data is 14-bit singed integer (2's complement) in data buffer VCHiDATx.
An input signal equal to 3.0V is about 0FFFh.
An input signal equal to 1.5V is about 0000h.
An input signal equal to 0.0V is about 3000h.
After software calibration flow, it is a 10-bit unsigned integer:
3.0V (about 0FFFh) is calibrated as 3FFh.
1.5V (about 0000h) is calibrated as 200h.
0.0V (about 3000h) is calibrated as 000h.

Changing the input selection for a new measurement channel (voltage), the software needs to set a delay time to prevent the result of an unintended ADC operation. The ADC waits for a programmable delay time between the selection of the input to be measured and the beginning of the A/D conversion.

7.10.3.3 ADC Operation

Reset
The ADC is disabled, and all interrupt is masked and all event status bits reset. The selected input for all four-voltage channels is disabled (Bit4-0 of the VCHiCTL register is set to 0Fh).

ADC Clock
The ADC clock is generated by dividing the EC clock by a factor defined in SCLKDIV in ADCCTL register. The ADC clock has to be at a frequency of 0.5 MHz. SCLKDIV has to be programmed before enabling the ADC.

Initializing the ADC
The ADC has to be initialized before ADC is enabled (ADCEN in the ADCCFG register is set to 1). The followings need to be done before the ADC is enabled.

1. Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on)
2. ADCEN bit in ADCCFG register is cleared.
3. Programming (SCLKDIV factor in ADCCTL register).
4. Voltage Channel Delay.
5. Channel Select in VCHiCTL register
6. Hardware voltage calibration information G and O needs to be done by setting calibration active via KDCTL register.

Enabling the ADC
After the ADC is enabled, the voltage channel is measured as long as the ADCEN is set 1 and when the voltage channel is selected. The measurement operations may be enabled or disabled individually.

Disabling the ADC
ADC analog circuit has less power consumption if it is disabled. ADCEN bit in ADCCFG register controls this and it's cleared at EC Domain Reset.
The firmware should clear ADCEN bit before entering Idle/Doze/Sleep mode.

7.10.4 EC Interface Registers

The ADC control/status and data out registers set interfaces with the EC through the EC Dedicated bus. These registers are mapped in the address space of the EC. The registers are listed below and the base address is 1900h.

Table 7-20. EC View Register Map, ADC

7	0	Offset
ADC Status (ADCSTS)		00h
ADC Configuration (ADCCFG)		01h
ADC Clock Control (ADCCTL)		02h
Voltage Channel 0 Channel Control (VCH0CTL)		04h
Calibration Data Control Register (KDCTL)		05h
Voltage Channel 1 Control (VCH1CTL)		06h
Voltage Channel 1 Data Buffer LSB (VCH1DATL)		07h
Voltage Channel 1 Data Buffer MSB (VCH1DATM)		08h
Voltage Channel 2 Control (VCH2CTL)		09h
Voltage Channel 2 Data Buffer LSB (VCH2DATL)		0ah
Voltage Channel 2 Data Buffer MSB (VCH2DATM)		0bh
Voltage Channel 3 Control (VCH3CTL)		0ch
Voltage Channel 3 Data Buffer LSB (VCH3DATL)		0dh
Voltage Channel 3 Data Buffer MSB (VCH3DATM)		0eh
Voltage High Scale Calibration Data Buffer LSB (VHSCDBL)		14h
Voltage High Scale Calibration Data Buffer MSB (VHSCDBM)		15h
Voltage Channel 0 Data Buffer LSB (VCH0DATL)		18h
Voltage Channel 0 Data Buffer MSB (VCH0DATM)		19h
Voltage High Scale Gain-error Calibration Data Buffer LSB (VHSGCDBL)		1Ch
Voltage High Scale Gain-error Calibration Data Buffer MSB (VHSGCDBM)		1Dh

For a summary of the abbreviations used for register type, see “Register Abbreviations and Access Rules”

7.10.4.1 ADC Status Register (ADCSTS)

This register indicates the global status of the ADC module. ADCSTS is cleared (00h) on VSTBY Power-Up reset; on other resets, bit 2 is unchanged and other bits are cleared.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1b	**Filter High Accuracy (FIRHIACC)** 0: Digital filter operation at low accuracy 1: Digital filter operation at high accuracy See also Table 7-19. ADC Configuration on page 247.
6	-	0b	**Reserved**
5	R/W	00b	**Clock Source Select (SDIVSRC)** This bit provides selection of the clock source of ADC clock. See also SCLKDIV field in ADCCTRL register. 0: Select EC Clock (frequency = FreqEC) 1: Select PLL Clock (frequency = FreqPLL) FreqPLL/FreqEC is listed in Table 10-2 on page 352. See also Table 7-19. ADC Configuration on page 247.
4	-	0b	**Reserved**
3	R/W	0b	**Analog Accuracy Initialization Bit (AINITB)** Write 1 to this bit and write 0 to this bit immediately once and only once during the firmware initialization and do not write 1 again after initialization since IT8502 takes much power consumption if this bit is set as 1. Writing steps about this bit should be done before ADCEN bit is set in ADCCFG register. 1: Start ADC accuracy initialization. 0: Stop ADC accuracy initialization.
2	R/W	0b	**ADC Power Statement (ADCPS)** This bit remains zero when ADC power is in a normal state. When ADC power shuts down or failure occurs, the software must program this bit to one. The program has to be waited at least 200usec for ADC internal initialization after power on. 0: Indicate the ADC power in a normal state. 1: Indicate the ADC power in a shut-down or failure state.
1	R/WC	0b	**Data Overflow Event (DOVE)** Measurement data from the previous cycle was overwritten with data From the current cycle before being read. In the event of a data overflow, the DATVAL bit remains set and new data is placed in Channel Data Buffer register. This bit is cleared by writing 1 to it; writing 0 is ignored. 0: No overflow (default) 1: Overflow
0	R/WC	0b	**End-of-Cycle Event (EOCE)** End of ADC cycle; all enabled measurements (up to four) are completed. For each of the enabled channels, the DATVAL bit is set to 1 and the data stored in Channel Data Buffer register respectively. 0: Cycle in progress (default) 1: End of ADC cycle

7.10.4.2 ADC Configuration Register (ADCCFG)

This register controls the operation and global configuration of the ADC module.

Address Offset: 01h

Bit	R/W	Default	Description
7-6		10b	**Reserved**
5	R/W	0b	**Digital Filter Enable (DFILEN)** Enables the digital filter operation for spike smoothing on ADC output signal. Setting this bit to 1 enables the digital low pass filter to prevent unwanted signal changes based on the ADC conversion and the smoothing data is read on the VCHxDAT register. 0: Disabled digital filter operation(default) 1: Enabled digital filter operation on ADC output signal when ADCEN is set 1. If ADCEN is cleared, this bit can be ignored. See also Table 7-19. ADC Configuration on page 247.
4-3	-	-	**Reserved**
2	R/W	0b	**Interrupt from End-of-Cycle Event Enable (INTECEN)** Enables an ADC interrupt generated by End-of ADC-cycle event (EOCEV in ADCSTS register). 0: Disabled (default) 1: Enabled interrupt by EOCEV event
1	R/W	0b	**Reserved**
0	R/W	0b	**ADC Module Enable (ADCEN)** Controls ADC operation or not 0: ADC disabled (default), power-down 1: ADC enabled

7.10.4.3 ADC Clock Control Register (ADCCTL)

This register controls the EC clock to ADC clock division.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	15h	**Select Clock Division Factor (SCLKDIV)** Divide the EC clock into the ADC clock. The EC clock is different from the ADC clock. ADC Clock Frequency = (EC Clock Frequency) / (SCLKDIV + 1) EC clock frequency is listed in Table 10-2 on page 352. If DFILEN is cleared, SCLKDIV has to be equal to or greater than 3h. If DFILEN is set, SCLKDIV has to be equal to or greater than 15h. It is recommended to use the default SCLKDIV value for a good performance.

7.10.4.4 Voltage Channel 0 Control Register (VCH0CTL)

This register both controls the operation and indicates the status of the Voltage channel.

Address Offset: 04h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The VCH0DATx is available for reading when DATAVAL is set. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. 0: No valid data in VCH0DATx register (default) 1: End of conversion – new data is available in VCH0DATx
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt generated by Data valid event of voltage channel 0. 0: Disabled (default) 1: Enabled – ADC Interrupt from local DATVAL
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. The channel selection has to be programmed before the channel is measured. **Bits** 43210 Description 00000: Channel 0 00001: Channel 1 .... 01010: Channel 10 .... 01101: Channel 13 Others: Reserved 11111: Channel Disabled (default)

7.10.4.5 Calibration Data Control Register (KDCTL)

This register both controls the operation and indicates the status of the Calibration channel.

Address Offset: 05h

B it	R/W	Default	Description
7	R/W	0b	**Automatic Hardware Calibration Enable(AHCE)** 0: Disable automatic hardware calibration, and the un-calibrated data(14bits signed) is stored in VCHiDATx (default). 1: Enable automatic hardware calibration, and the calibrated data(10bits unsigned) is stored in VCHiDATx .
6	R/WC	0b	**Reserved**
5	R/WC	0b	**High-Scaler Calibration Data Valid (HCDATVAL)** The data may be read when this bit is set 1. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. If gain error calibration is selected, the valid data is for Gain Error Calibration; otherwise, it is for Offset Calibration. 0: No new valid data in volt Calibration data register (default). 1: End of volt Calibration – new data is available in data buffer.
4	R/WC	0b	**Gain_Error Calibration Data Valid (GCDATVAL)** The data may be read when this bit is set 1. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. When this bit is set, the valid data is for Gain Error Calibration. 0: No new valid data in High-Scaler Calibration data register (default). 1: End of High-scaler Calibration – new data is available in data buffer.
3	R/W	0b	**Reserved**
2	R/W	0b	**Reserved**
1	R/W	0b	**Volt High Scale Calibration Enable (VHSCKE)** When GECKE is cleared to 0, set this bit to 1 to enable the Volt High Scale (3volts) Calibration operation for volt ADC channel (AHCE bit has to be cleared.) To initialize one ADC calibration operation, calibration data will be stored on Voltage High Scale Calibration Data Buffer when ADC calibration data has been done (DATVAL=1), and this bit will be cleared to zero automatically. 0: Disabled calibration operation(default) 1: Enabled calibration operation only when GECKE is cleared to 0.
0	R/W	0b	**Gain_Error Calibration Enable (GECKE)** Enables the Gain_Error Calibration operation for volt ADC channel (AHCE bit has to be clear). Set this bit to 1 to initialize one ADC gain_error calibration operation, and calibration data will be stored on Voltage Gain_Error Calibration Data Buffer when ADC calibration data has been done(GCDATVAL=1), and this bit will be cleared to zero automatically. 0: Disabled calibration operation(default) 1: Enabled gain error calibration operation

7.10.4.6 Voltage Channel 1 Control Register (VCH1CTL)

This register both controls the operation and indicates the status of Voltage Channel 1.

Address Offset: 06h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH1DATx register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 1. 0: Disabled (default) 1: Enabled – ADC Interrupt from local DATVAL
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input is selected for measurement. Channel selected has to be done before beginning to measure the channel. **Bits** 4 3 2 1 0 Description 0 0 0 0 0: Channel 0 0 0 0 0 1: Channel 1 .... 0 1 0 1 0: Channel 10 .... 0 1 1 0 1: Channel 13 Others: Reserved 1 1 1 1 1: Channel Disabled (default)

7.10.4.7 Volt Channel 1 Data Buffer LSB (VCH1DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.8 Volt Channel 1 Data Buffer MSB (VCH1DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 1.

Address Offset: 08h

Bit	R/W	Default	Description
7-6		-	**Reserved**
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 1. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.9 Voltage Channel 2 Control Register (VCH2CTL)

This register both controls the operation and indicates the status of Voltage Channel 2.

Address Offset: 09h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.10.4.10 Volt Channel 2 Data Buffer LSB (VCH2DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 2.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.11 Volt Channel 2 Data Buffer MSB (VCH2DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 2.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-6		-	**Reserved**
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 2. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.12 Voltage Channel 3 Control Register (VCHN3CTL)

This register both controls the operation and indicates the status of Voltage Channel 3.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.10.4.13 Volt Channel 3 Data Buffer LSB (VCH3DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 3.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.14 Volt Channel 3 Data Buffer MSB (VCH3DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 3.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-6		-	**Reserved**
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 3. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.15 Volt High Scale Calibration Data Buffer LSB (VHSCDBL)

This register (buffer) holds the calibration data(LSB 8bits) measured by the internal voltage channel.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R	-	**Volt Calibration Data (VCKD7-0)** Volt calibration data is measured by the internal voltage channel. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.16 Volt High Scale Calibration Data Buffer MSB (VHSCDBM)

This register (buffer) holds the calibration data(MSB 4bits) measured by the internal voltage channel.

Address Offset: 15h

Bit	R/W	Default	Description
7-6	-	00h	**Reserved**
5-0	R	-	**Volt Calibration Data (VCKD13-8)** Volt calibration data is measured by the internal voltage channel. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.17 Voltage Channel 0 Data Buffer LSB (VCH0DATL)

This register (buffer) holds the data (LSB 7-0) measured by the Voltage Channel 0.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R	-	**Voltage Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.18 Voltage Channel 0 Data Buffer MSB (VCH0DATM)

This register (buffer) holds the data (MSB 6 bits) measured by the Temperature Channel.

Address Offset: 19h

Bit	R/W	Default	Description
7-6	-	00h	**Reserved**
5-0	R	-	**Voltage Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 0. The data may be available only when DATVAL is set. DATVAL has to be cleared after read data.

7.10.4.19 Volt High Scale Gain-Error Calibration Data Buffer LSB (VHSGCDBL)

This register (buffer) holds the gain-error calibration data(LSB 8bits) measured by the internal voltage channel.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R	-	**Volt Gain-Error Data (VGED7-0)** Volt gain-error data is measured by the internal voltage channel. The data may be read only when the DATVAL is set.

7.10.4.20 Volt High Scale Gain-Error Calibration Data Buffer MSB (VHSGCDBM)

This register (buffer) holds the gain-error calibration data(MSB 6bits) measured by the internal voltage channel.

Address Offset: 1Dh

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
5-0	R	-	**Volt Gain-Error Data (VGED13-8)** Volt gain-error data is measured by the internal voltage channel. The data may be read only when the DATVAL is set.

7.10.5 ADC Programming Guide

Table 7-21. Detail Step of ADC Channel Conversion

Action	Step	Description
Determine Offset and Gain_Error during initialization	1	Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on) Case1: AHCE = 0 (hardware calibration disable, use software calibration) Clear AHCE@KDCTL reg goto step 2 Case2: AHCE = 1 (hardware calibration enable) Set AHCE@KDCTL reg , DFILEN =1 goto step 9 (skip step 3 to 8)
	2	Enable digital filter by setting DFILEN@ADCCFG = 1
	3	Set high scale offset calibration bit by setting VHSCKE@KDCTL = 1
	4	Start ADC conversion by setting ADCEN@ADCCFG = 1
	5	Waiting for HCDATVAL@KDCTL = 1 If true, get Offset Data **O** by reading VHSCDBM and VHSCDBL **O**[13:0] = {VHSCDBM[5:0], VHSCDBL[7:0]}
	6	Start Gain_Error calibration by setting GECKE@KDCTL = 1
	7	Waiting for GCDATVAL@KDCTL = 1 If true, get Gain_Error Data **G** by reading VHSGCDBM and VHSGCDBL **G**[13:0] = {VHSGCDBM[5:0], VHSGCDBL[7:0]}
	8	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0
ADC channel conversion	9	Enable VCHnCTL for measuring desired channels; n = 0,1, 2, or 3
	10	For example; To measure ADC0 voltage on voltage buffer 1 Set SELIN@VCH1CTL = 0
	11	Start ADC channel conversion by setting ADCEN@ADCCFG =1
	12	Waiting for DATVAL@VCH1CTL = 1 CASE1 : AHCE =0 (disable) If true, get ADC0 output data **R** by reading VCH1DATM and VCH1DATAL **R**[13:0] = {VCH1DTM[5:0], VCH1DATL[7:0]} CASE1 : AHCE =1 (enable) If true, get ADC0 output data **D** by reading VCH1DATM and VCH1DATAL **D**[9:0] = {VCH1DTM[1:0], VCH1DATL[7:0]}
	13	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0
	14	Follow to make a software calibration then go to step 8 next time.

Figure 7-23. ADC Software Calibration Flow

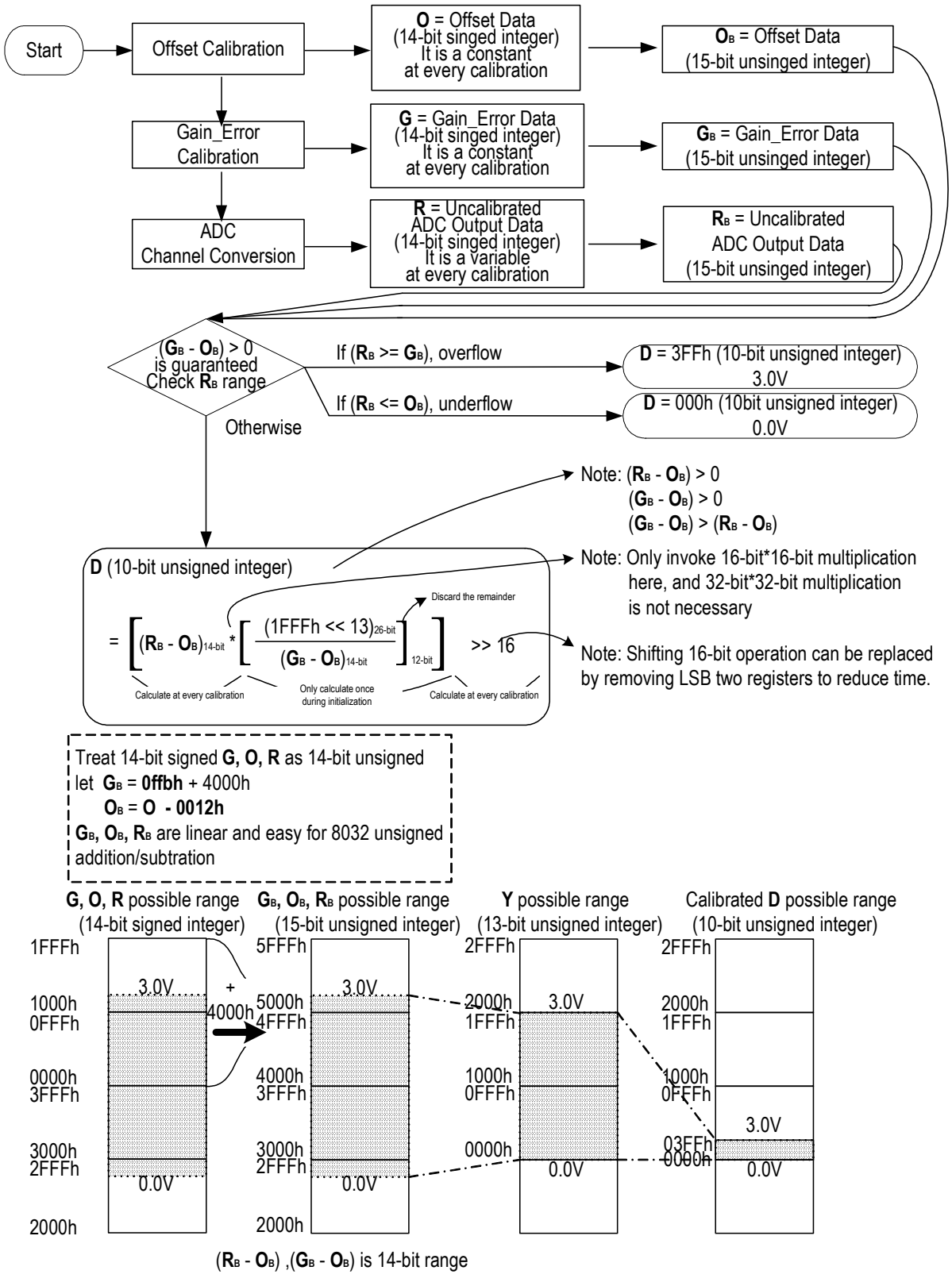


Figure 7-24. ADC Software Calibration Flow in a Special Case

Another quick way in a special case:

If **D** is used to be compared with a threshold value, this threshold can be calculated first to be mapped into the data space of G_B, O_B, R_B during initialization, and the multiplication and division operation invoked to calibrate R_B can be omitted. There are only one multiplication and one division to calculate R_{BL} during initialization.

Threshold Low Boundary $$R_{BL}{}_{15\text{-bit}} = \left[\frac{(G_B - O_B)_{14\text{-bit}} * (D << 3)_{13\text{-bit}}}{1FFFh_{\ 13\text{-bit}}} \right]_{14\text{-bit}} + O_{B}{}_{15\text{-bit}}$$

Threshold High Boundary $$R_{BH}{}_{15\text{-bit}} = R_{BL} + (2 << 3) - 1 = R_{BL} + 7$$

Then uncalibrated R_B which satisfies $R_{BL} <= R_B <= R_{BL}$ should be mapped into calibrated **D**
That is, normally 8 possible R_B values will be mapped into calibrated **D**

Example:

G_B = 5020h
O_B = 3010h
Threshold voltage = 2.0V, Target **D** = 3FFh * 2.0 / 3.0 = 2AAh
Then

$$R_{BL} = \left[\frac{(5020h - 3020h) * (2AAh << 3)}{1FFFh} \right] + 3010h = 456Bh$$

$$R_{BH} = R_{BL} + 7$$

Final

Calibrated ADC Output < 2.0V	if R_B < 456Bh
Calibrated ADC Output <= 2.0V	if R_B <= (456Bh + 7)
Calibrated ADC Output > 2.0V	if R_B > (456Bh + 7)
Calibrated ADC Output >= 2.0V	if R_B >= 456Bh

7.11 PWM

7.11.1 Overview

The PWM module generates eight 8-bit PWM outputs; each PWM output may have a different duty cycle. The fan speed is controlled by software.

7.11.2 Features

- Supports eight PWM outputs
- Supports two fan tachometer inputs

7.11.3 Functional Description

7.11.3.1 General Description

Figure 7-25. PWM Diagram

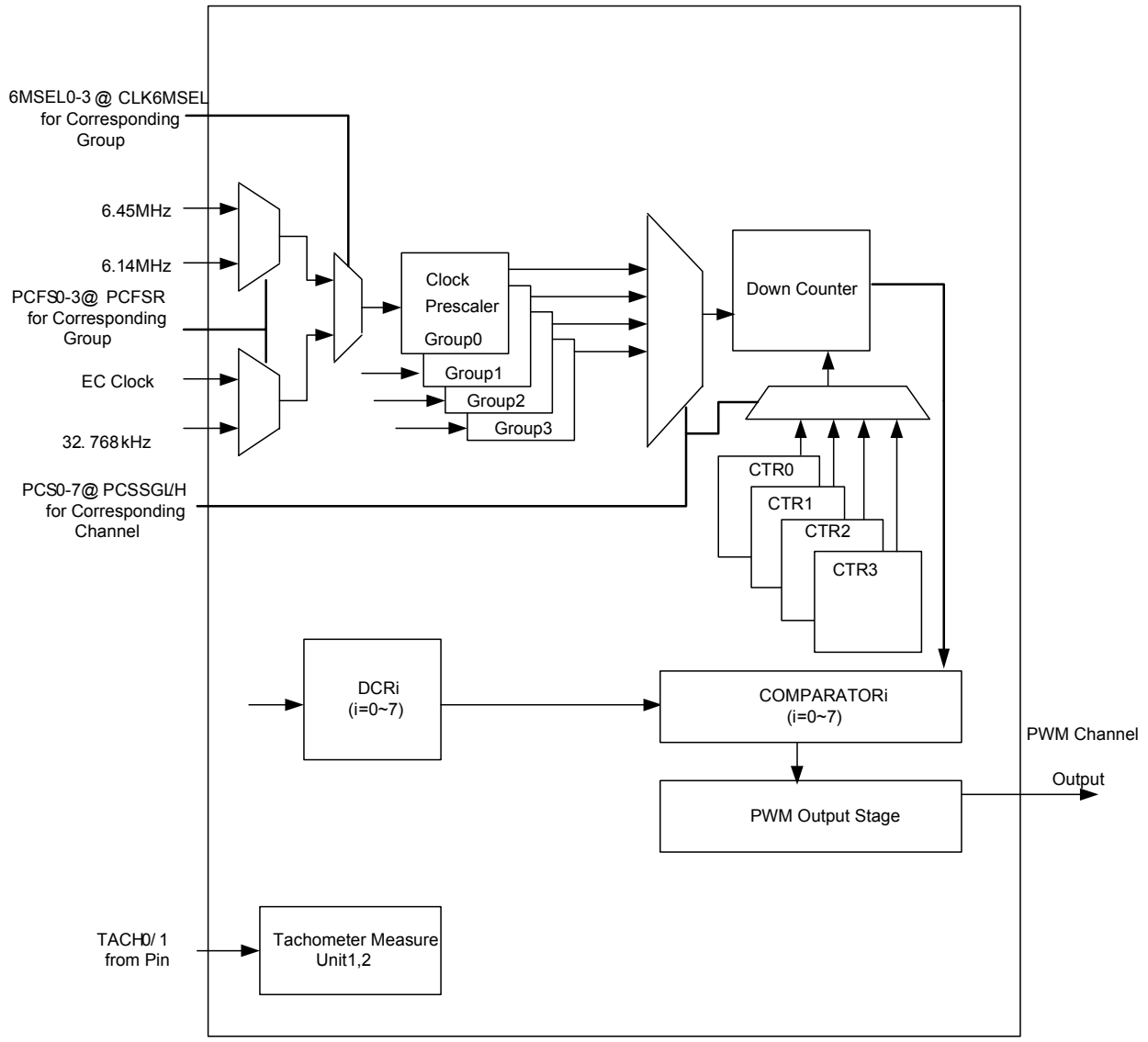
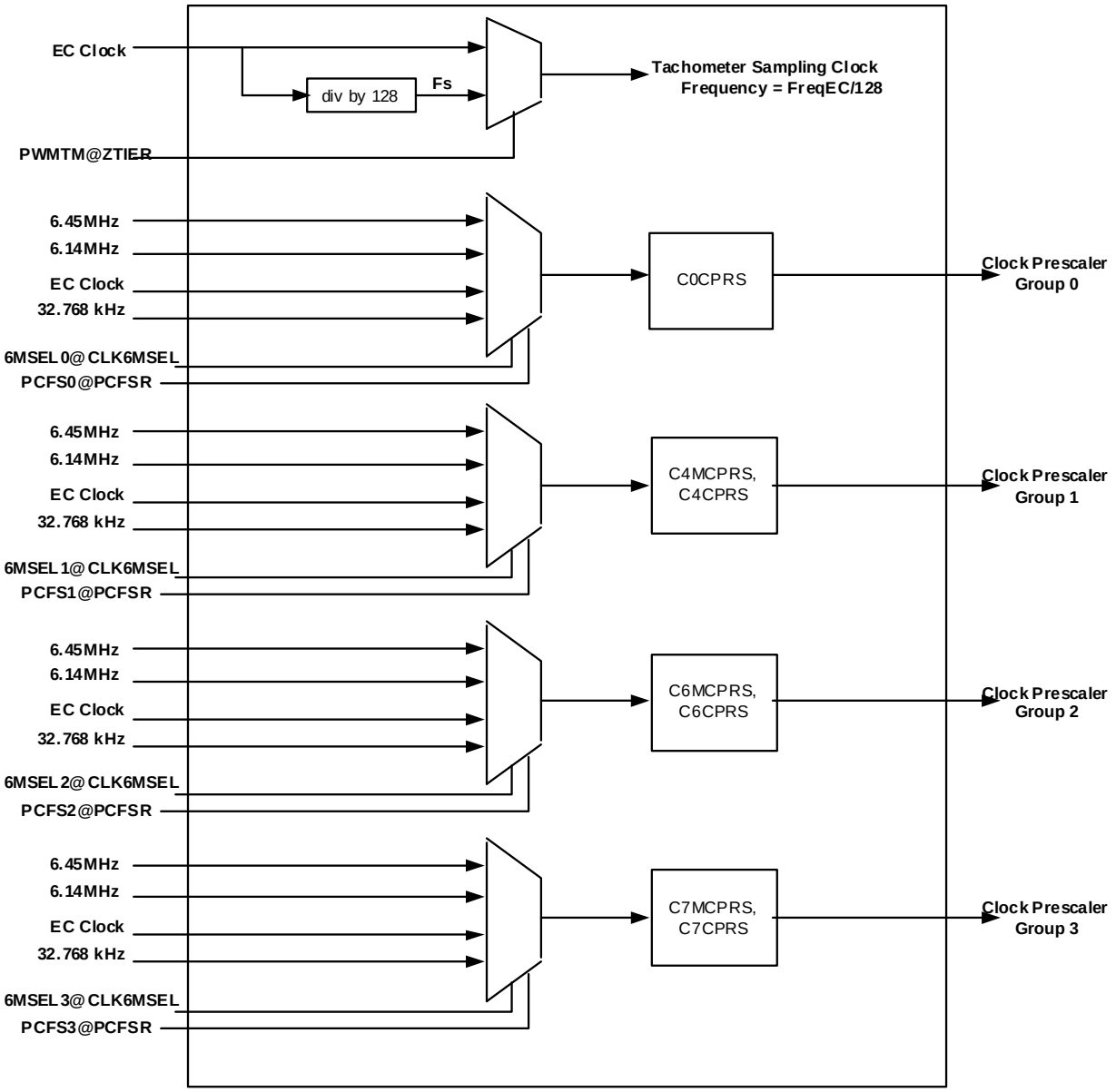


Figure 7-26. PWM Clock Tree



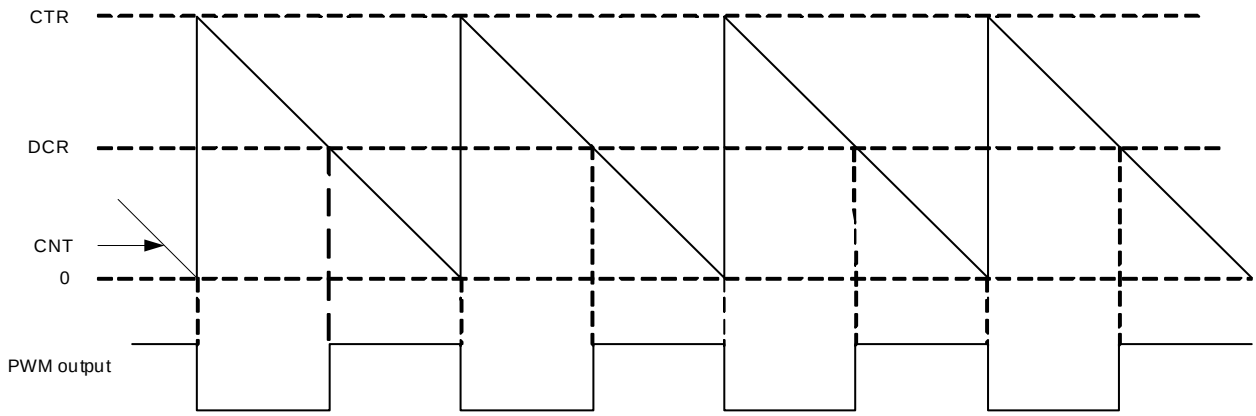
The PWM uses the 32.768 kHz Clock, EC Clock, 6.14 MHz Clock, or 6.45 MHz Clock as a reference for its PWM output. The prescaler divider values in CiCRPS register which divides the PWM input clock into its working clock respectively. Each channel can select their prescaler divider by {PCSSGH, PCSSGL} register. The prescaler divider C0CRPS register has 8-bit counter value; and the {CiMCRPS, CiCRPS}(i=4,6,7) has 16-bit counter value. The PWM provides eight 8-bit PWM outputs, which are PWM0 to PWM7. Each PWM output is controlled by its Duty Cycle registers (DCRi, i =0 to 7). All PWM output is controlled by a Cycle Time register (CTR).

When PWM working clock is enabled, the PWM cycle output is high when the value in the DCRi register is greater than the value in CTR down-counter. When the value of DCRi register is not greater than the value in CTR down-counter, the PWMi cycle output is on LOW and PWMi cycle output polarity can be inversed by INVPi register.

When the value in CTR counter down-counter reaches 0, the value in CTR counter will be reloaded then start down-counter until the PWM working clock is disabled.

Cycle Time and Duty Cycle

Figure 7-27. PWM Output Waveform



The PWM module supports duty cycles ranging from 0% to 100%.
The PWMi output signal cycle time is:

n(CiCPRS + 1) x (CTR + 1) x T clk

Where:

• T clk is the period of PWM input clock = (1 / 32.768 kHz) or (1 / FreqEC), which is selected by PCFS3-0 in PCSGR regiser. (FreqEC is listed in Table 10-2 on page 352)
• The PWMi output signal duty cycle (in %, when INVPi is 0) is:
(DCRi) / (CTR + 1) x 100.

In the following cases, the PWMi output is hold at a state(low or high):
•PWMi output is still low when the content of DCRi is greater than the CTR value.
•PWMi output is still high when the content of DCRi is equal to the CTR value.
•PWMi output is still low when the content of DCRi =0 & INVPi = 0 is in PWMPOL register.

PWM Inhibit Mode

The PWM is in an inhibit mode when PCCE in ZTIER Register is 0. In this mode, the PWM input clock is disabled (stopped). The PWMi signal is 0 when INVPi bit is 0; it is 1 when INVPi bit is 1. It is recommended the PRSC and CTR registers should be updated in a PWM inhibit mode.

7.11.3.2 Manual Fan Control Mode

In manual mode, the software may monitor the fan Tachometer Reading Registers to control the fan speed by programming the duty cycle of the driving PWM (FiMPDCR) register.

The contents of the Tachometer Reading Register is still updated according to the sampling counter that samples the tachometer input (TACH0 pin for FAN1 of the local sensor zone and TACH1 pin for FAN2 of the remote sensor zone). The sampling rate (fs) is FreqEC / 128. (FreqEC is listed in Table 10-2 on page 352)

Fan Speed (R.P.M.) = 60 / (1/fs sec * {FnTMRR, FnTLRR} * P)
n denotes 1 or 2
P denotes the numbers of square pulses per revolution.
And {FnTMRR, FnTLRR} = 0000h denotes Fan Speed is zero.

7.11.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 1800h.

Table 7-22. EC View Register Map, PWM

7	0	Offset
Channel 0 Clock Prescaler Register (C0CPRS)		00h
Cycle Time 0 (CTR0)		01h
PWM Duty Cycle (DCR0-7)		02h-09h
PWM Polarity (PWMPOL)		0Ah
Prescaler Clock Frequency Select Register (PCFSR)		0Bh
Prescaler Clock Source Select Group Low (PCSSGL)		0Ch
Prescaler Clock Source Select Group High (PCSSGH)		0Dh
Prescaler Clock Source Gating Register (PCSGR)		0Fh
Fan 1 Tachometer LSB Reading (F1TLRR)		1Eh
Fan 1 Tachometer MSB Reading (F1TMRR)		1Fh
Fan 2 Tachometer LSB Reading (F2TLRR)		20h
Fan 2 Tachometer MSB Reading (F2TMRR)		21h
Zone Interrupt Status Control (ZINTSCR)		22h
PWM Clock Control Register (ZTIER)		23h
Channel 4 Clock Prescaler Register (C4CPRS)		27h
Channel 4 Clock Prescaler MSB Register (C4MCPRS)		28h
Channel 6 Clock Prescaler Register (C6CPRS)		2Bh
Channel 6 Clock Prescaler MSB Register (C6MCPRS)		2Ch
Channel 7 Clock Prescaler Register (C7CPRS)		2Dh
Channel 7 Clock Prescaler MSB Register (C7MCPRS)		2Eh
PWM Clock 6MHz Select Register(CLK6MSEL)		40h
Cycle Time 1 (CTR1)		41h
Cycle Time 2 (CTR2)		42h
Cycle Time 3 (CTR3)		43h

For a summary of the abbreviations used for register types, see “Register Abbreviations and Access Rules”

7.11.4.1 Channel 0 Clock Prescaler Register (C0CPRS)

This register controls the cycle time and the minimal pulse width of channel 0~3.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV)** PWM input clock is divided by the number of (C0CPRS+ 1). For example, the value of 01h results in a divide by 2. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.11.4.2 Cycle Time Register 0 (CTR0)

This register controls the cycle time 0 and duty cycle steps.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 0 (CTV0)** The Prescaler output clock is divided by the number of (CTR0 + 1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.11.4.3 Cycle Time Register 1 (CTR1)

This register controls the cycle time 1 and duty cycle steps.

Address Offset: 41h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 1 (CTV1)** The Prescaler output clock is divided by the number of (CTR1 + 1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divide by 256. After writing data to the register, system will be changed to the 4-CTR mode. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.11.4.4 Cycle Time Register 2 (CTR2)

This register controls the cycle time 2 and duty cycle steps.

Address Offset: 42h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 2 (CTV2)** The function of this register is the same as that of CTR1.

7.11.4.5 Cycle Time Register 3 (CTR3)

This register controls the cycle time 2 and duty cycle steps.

Address Offset: 43h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value 3 (CTV3)** The function of this register is the same as that of CTR1.

7.11.4.6 PWM Duty Cycle Register 0 to 7(DCRi)

This register (DCRi; I=0 to 7) controls the duty cycle of PWMi output signal.

Address Offset: 02h(ch0), 03h(ch1), 04h(ch2), 05h(ch3), 06h(ch4), 07h(ch5), 08h(ch6), 09h(ch7);

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value (DCV)** DCRi register decides the number of clocks for which PWMi is high when INVPi bit is 0 in PWMPOL register. The PWMi Duty Cycle output = (DCRi)/(CTR+1) If the DCRi value > CTR value, PWMi signal is still low. If DCRi value = CTR value, PWMi signal is still high. When Inverse PWMi bit is 1, the value of PWMi is inversed.

7.11.4.7 PWM Polarity Register (PWMPOL)

This register controls the polarity of PWM0 to PWM7.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Inverse PWM Outputs (INVP7-0)** Bit 7 to 0 control the polarity of PWM7 to PWM0 respectively. 0: Non-inverting. 1: Inverting.

7.11.4.8 Prescaler Clock Frequency Select Register (PCFSR)

This register Bit 3~0 is used to select prescaler clock frequency for four channel group 3~0. Each of them includes 1 set prescaler registers. See the following table.

Channel Group	Prescaler Channels
0	C0CPRS
1	C4MCPRS,C4CPRS
2	C6MCPRS,C6CPRS
3	C7MCPRS,C7CPRS

Address Offset: 0Bh

Bit	R/W	Default	Description
5-4	-	-	**Reserved**
3-0	R/W	0000b	**Prescaler Clock Frequency Select (PCFS3-0)** The clock source of the prescaler of group 0 consists of G6MSEL0 and PCFS0 bit. G6MSEL0 bit is in CLK6MSEL register. PCFS0 bit is in this register. {G6MSEL0, PCFS0}: 00b: Select 32.768 kHz. 01b: Select FreqEC (EC Clock). 10b: Select FreqEC*2/3 (6.14 MHz) 11b: Select FreqPLL/5 (6.45 MHz, available only if PLLFREQ == 0011b) (FreqEC and FreqPLL are listed in Table 10-2 on page 352) So are group 1, 2 and 3.

7.11.4.9 Prescaler Clock Source Select Group Low (PCSSGL)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-6	R/W	00b	**Prescaler Clock Select 3 (PCS3)** The bits select prescaler clock for channel 3. The bits 7-6 are the same as bit 1-0.
5-4	R/W	00b	**Prescaler Clock Select 2 (PCS2)** The bits select prescaler clock for channel 2. The bits 5-4 are the same as bit 1-0.
3-2	R/W	00b	**Prescaler Clock Select 1 (PCS1)** The bits select prescaler clock for channel 1. The bits 3-2 are the same as bit 1-0.
1-0	R/W	00b	**Prescaler Clock Select 0 (PCS0)** Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.11.4.10 Prescaler Clock Source Select Group High (PCSSGH)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock sources.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	R/W	01b	**Prescaler Clock Select 7 (PCS7)** The bits select prescaler clock for channel 7. The bits 7-6 are the same as bit 1-0.
5-4	R/W	01b	**Prescaler Clock Select 6 (PCS6)** The bits select prescaler clock for channel 6. The bits 5-4 are the same as bit 1-0.
3-2	R/W	01b	**Prescaler Clock Select 5 (PCS5)** The bits select prescaler clock for channel 5. The bits 3-2 are the same as bit 1-0.
1-0	R/W	01b	**Prescaler Clock Select 4 (PCS4)** The bits select prescaler clock for channel 4. Default as below： 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR0 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR0 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR0 After writing data to CTR1,CTR2 or CTR3 register 00: select prescaler clock divided by C0CPRS and select CTR0 01: select prescaler clock divided by {C4MCPRS,C4CPRS} and select CTR1 10: select prescaler clock divided by {C6MCPRS,C6CPRS} and select CTR2 11: select prescaler clock divided by {C7MCPRS,C7CPRS} and select CTR3

7.11.4.11 Prescaler Clock Source Gating Register (PCSGR)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Clock Source Gating (PCSG)** Bits 7-0 are used to gate prescaler clock source for PWM channels 7-0 respectively. 0: no gating clock source 1: gating clock source; PWM channel output is 0 when INVP bit is set to 0 respectively

7.11.4.12 Fan 1 Tachometer LSB Reading Register (F1TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 1 corresponds to TACH0 (tachometer input of fan1).
Reading F1TLRR and F1TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bit 7-0 denotes LSB Tachometer speed.

7.11.4.13 Fan 1 Tachometer MSB Reading Register (F1TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 1 corresponds to TACH0.

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bits 7-0 denotes MSB Tachometer speed.

7.11.4.14 Fan 2 Tachometer LSB Reading Register (F2TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 2 corresponds to TACH1 (tachometer input of fan2)..
Reading F2TLRR and F2TMRR registers should be in pairs to get the correct 16-bit tachometer value.
Reading these two registers via D2EC/I2EC is not guaranteed to get the correct value.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bits 7-0 denotes the LSB Tachometer speed.

7.11.4.15 Fan 2 Tachometer MSB Reading Register (F2TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16-bit binary digits. Fan 2 corresponds to TACH1.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bits 7-0 denotes MSB Tachometer speed.

7.11.4.16 Zone Interrupt Status Control Register (ZINTSCR)

Address Offset: 22h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5	R/W	0b	**TACH1 Data-valid Interrupt Enable(T1DIE)** 1: Enable interrupt to R8032 when fan1 tachometer data is valid. 0: Disable interrupt to R8032 when fan1 tachometer data is valid.
4	R/WC	0b	**TACH1 Data-valid Interrupt Clear(T1DIC)** Write one to clear the Interrupt status, which is caused when fan 1 tachometer data is valid; writing zero is ignored.
3	R	0b	**TACH1 Data-valid Interrupt Status(T1DIS)** 1: Fan1 tachometer data-valid event occurs. 0: No fan1 tachometer data-valid event occurs.
2	R/W	0b	**TACH2 Data-valid Interrupt Enable(T2DIE)** 1: Enable interrupt to R8032 when fan 2 tachometer data is valid. 0: Disable interrupt to R8032 when fan 2 tachometer data is valid.
1	R/WC	0b	**TACH2 Data-valid Interrupt Clear(T2DIC)** Write one to clear Interrupt status, which is caused when fan 2 tachometer data is valid; writing zero is ignored.
0	R	0b	**TACH2 Data-valid Interrupt Status(T2DIS)** 1: Fan2 tachometer data-valid event occurs. 0: No fan2 tachometer data-valid event occurs.

7.11.4.17 PWM Clock Control Register (ZTIER)

Address Offset: 23h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	-	-	**Reserved**
5-2	-	0b	**Reserved**
1	R/W	0b	**PWM Clock Counter Enable (PCCE)** 1: Enable PWMs clock counter. Set this bit to 1 after all other registers have been set. 0: Disable PWMs clock counter
0	R/W	0b	**PWM Test Mode (PWMTM)** 1: PWM switches to a test mode 0: PWM works on a normal mode

7.11.4.18 Channel 4 Clock Prescaler Register (C4CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C4MCPRS defines the high byte.

7.11.4.19 Channel 4 Clock Prescaler MSB Register (C4MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.11.4.20 Channel 6 Clock Prescaler Register (C6CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Bh

	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C6MCPRS defines the high byte.

7.11.4.21 Channel 6 Clock Prescaler MSB Register (C6MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.11.4.22 Channel 7 Clock Prescaler Register (C7CPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C7MCPRS defines the high byte.

7.11.4.23 Channel 7 Clock Prescaler MSB Register (C7MCPRS)

This register controls the cycle time and the minimal pulse width of PWM channel.
The setting of the prescaler channel is based on the value of PCSSGL and PCSSGH registers.

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00h	**Prescaler Divider Value (PSDV15-8)** Refer to the previous register for the details.

7.11.4.24 PWM Clock 6MHz Select Register (CLK6MSEL)

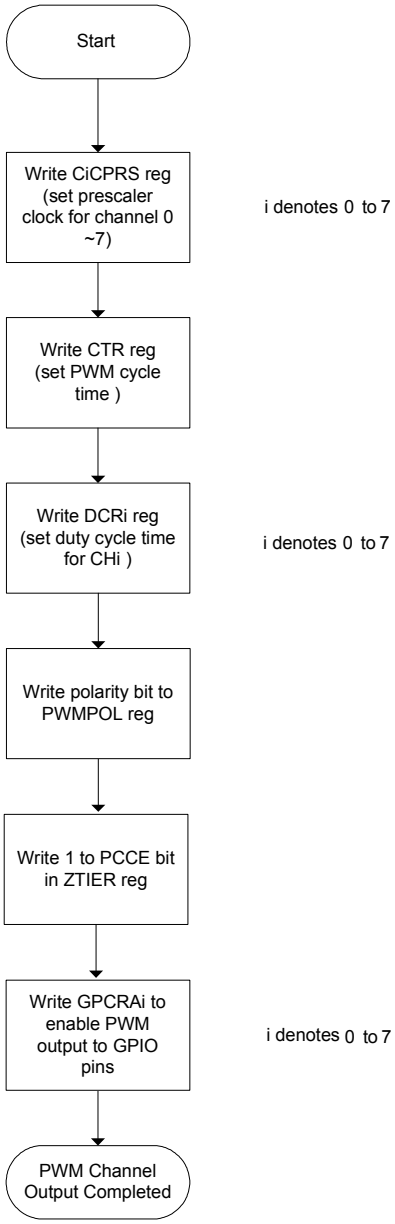
This register controls the group clock.

Address Offset: 40h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R	0b	**Cycle Time Register Mode (CTRMODE)** 0: 1 cycle time mode. 1: 4 cycle time mode. After writing data to CTR1, CTR2, or CTR3, the bit will be set to 1 and system will be changed to the 4-CTR mode.
3-0	R/W	0000b	**Clock Group 6MHz Selection (G6MSEL3-0)** Refer to PCFS3-0 field in PCFSR register.

7.11.5 PWM Programming Guide

Figure 7-28. Program Flow Chart for PWM Channel Output



7.12 8-bit Timer (TMR)

7.12.1 Overview

This module is an on-chip 8-bit timer (TMA0, TMA1, TMB0, and TMB1) with four channels operating on the basis of an 8-bit counter. The 8-bit timer module can be used as a multi-function timer in a variety of applications, such as generation of counter reset, interrupt requests, and pulse output with an arbitrary duty cycle using a compare-match signal with registers.

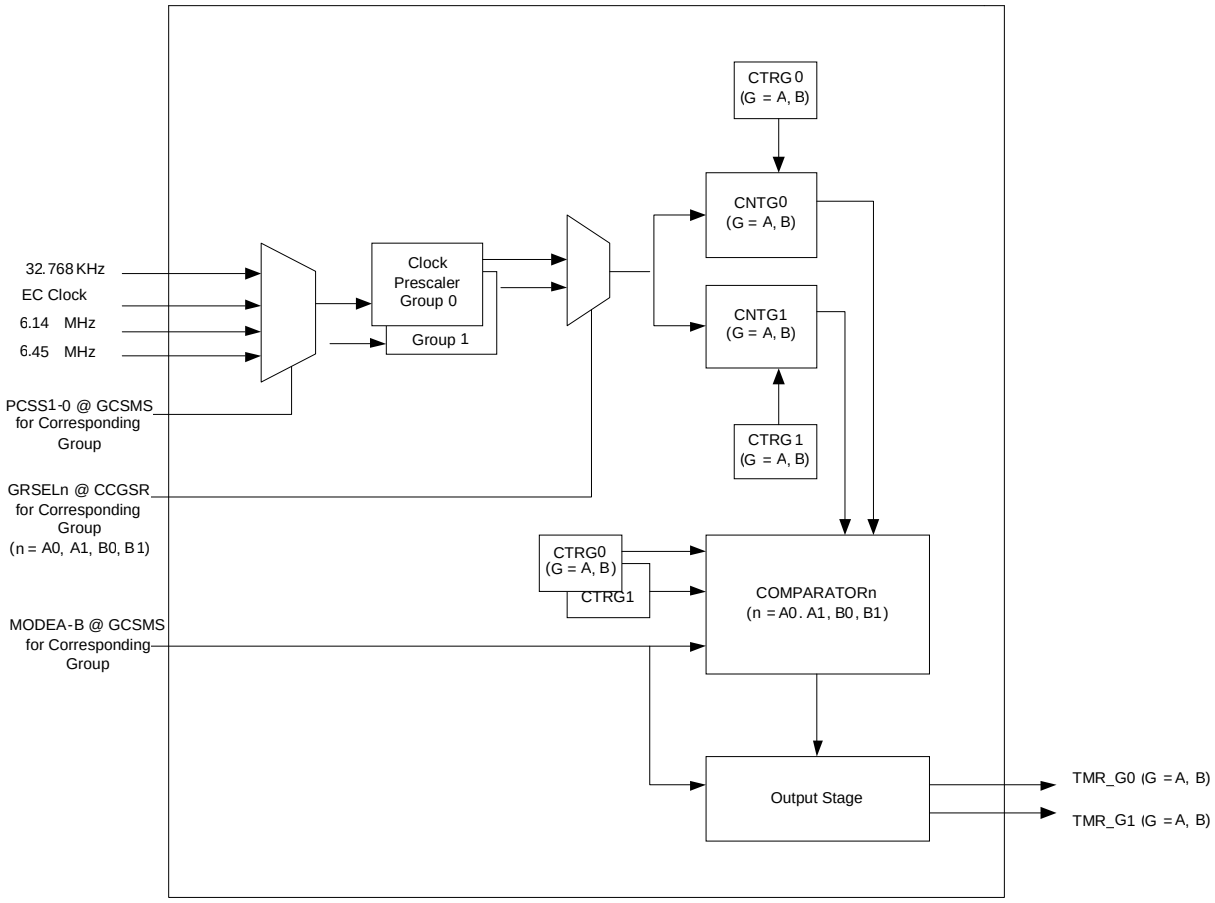
7.12.2 Features

- Supports four channels.
- Supports four Counters, Cycle Time registers and Duty Cycle registers for each channel.
- Supports four clock sources and two clock prescalers.
- Supports 8-bit pulse mode, 16-bit pulse mode, and toggle mode.
- Supports interrupt enable and interrupt disable for cycle time match and duty cycle match respectively.

7.12.3 Functional Description

7.12.3.1 General Description

Figure 7-29. TMR Block Diagram



The TMR uses the 32.768 kHz Clock, EC Clock, 6.14 MHz Clock or 6.45 MHz Clock as a reference for its TMR output. The prescaler divider values in PRSC register divides the TMR intput clock into its working clock respectively. Each channel can select their prescaler divider by CCGSR register. The TMR provides four TMR

outputs, TMRA0, TMRA1, TMRB0, and TMRB1. Each TMR output is controlled by its Duty Cycle registers and Cycle Time register.

TMR module consists of three modes, 8-bit mode, 16-bit mode, and toggle mode.

7.12.3.2 TMR Counter (CNT)

Each CNT is an 8-bit up-counter. CNT_A0 and CNT_A1 (or CNT_B0 and CNT_B1) comprise a single 16-bit counter in toggle mode or 16-bit pulse mode. CNT can be cleared by writing data to Duty Cycle register or by compare-match Cycle Time signal. Note that CNT is disabled when DCR is 00h and CNT is initialized to 00h.

7.12.3.3 TMR Duty Cycle (DCR)

DCR is an 8-bit readable/writable register. DCR_A0 and DCR_A1 (or DCR_B0 and DCR_B1) comprise a single 16-bit register in toggle mode or 16-bit pulse mode. DCR is continually compared with the value in CNT. When a match is detected, the corresponding TMR output polarity will be changed and the corresponding interrupt will be set if the interrupt is enabled. DCR is initialized to 00h.

7.12.3.4 TMR Cycle Time (CTR)

CTR is an 8-bit readable/writable register. CTR_A0 and CTR_A1 (or CTR_B0 and CTR_B1) comprise a single 16-bit register in toggle mode or 16-bit pulse mode. CTR is continually compared with the value in CNT. When a match is detected, the corresponding TMR output polarity will be changed and the corresponding interrupt will be set if the interrupt is enabled and the value in CNT will be changed to 00h. CTR is initialized to H'FF.

7.12.3.5 TMR Mode

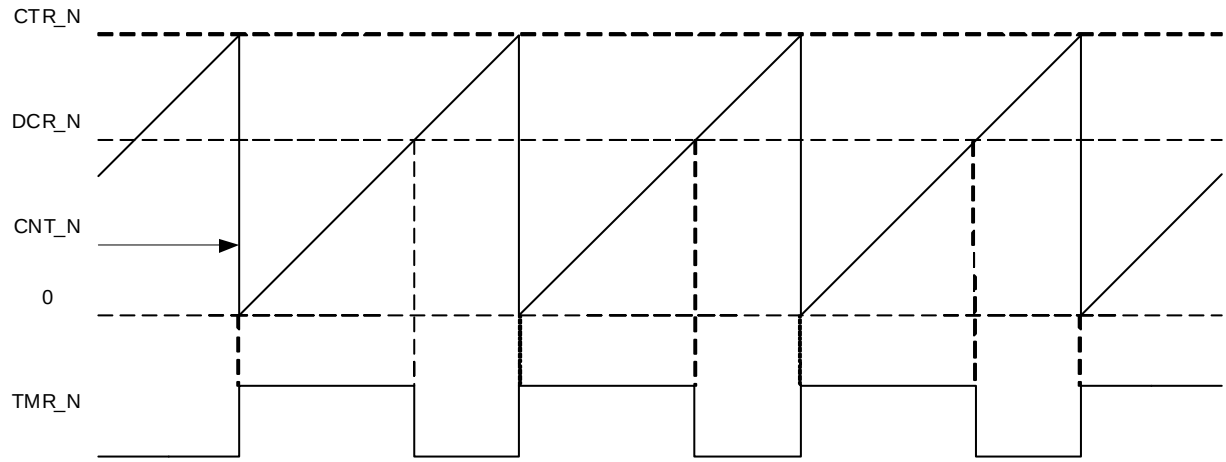
8-bit Pulse Mode
In 8-bit pulse mode, each TMR_N output is controlled by its Duty Cycle register and Cycle Time register.(N = A0, A1, B0, and B1)

When the TMR working clock is enabled, the TMR_N output is high when the value in the DCR_N register is greater than the value in the counter. When the value of DCR_N register is not greater than the value in the counter, the TMR_N cycle output is low. When the value in the counter reaches the value in the CTR_N register, the counter will be reset then start counting until the TMR working clock is disabled.

The TMR_N output signal cycle time is:
Tclk × PRSCi × (CTR_N + 1)
Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC), (1/ 6.14 MHz), or (1/ 6.45 MHz), which is selected by PCCS1-0 in GCSMS register.

The TMR_N output signal duty cycle (in %) is:
(DCR_N) / (CTR_N + 1) × 100

Figure 7-30. 8-bit Mode Waveform of Channel N



16-bit pulse mode

In 16-bit pulse mode, TMR output is controlled by the cascading of two Duty Cycle registers and two Cycle Time registers.

Operation of a 16-bit counter can be performed by using CNT_G1 as the upper half and CNT_G0 as the lower half, and operation of 16-bit Duty Cycle register (DCR_G) and 16-bit Cycle Time register (CTR_G) is performed in the same way as that of 16-bit counter (CNT_G). (G = A, B)

When the TMR working clock is enabled, the TMR_G1 output is high when the value in the DCR_G register is greater than the value in the CNT_G register. When the value of the DCR_G register is not greater than the value in the CNT_G register, the TMR_G1 output is low. When the value in the CNT_G register reaches the value in the CTR_G register, the CNT_G counter will be reset then start counting until the TMR working clock is disabled. But TMR_G0 output is always low in 16-bit pulse mode.

The TMR_G1 output signal cycle time is:

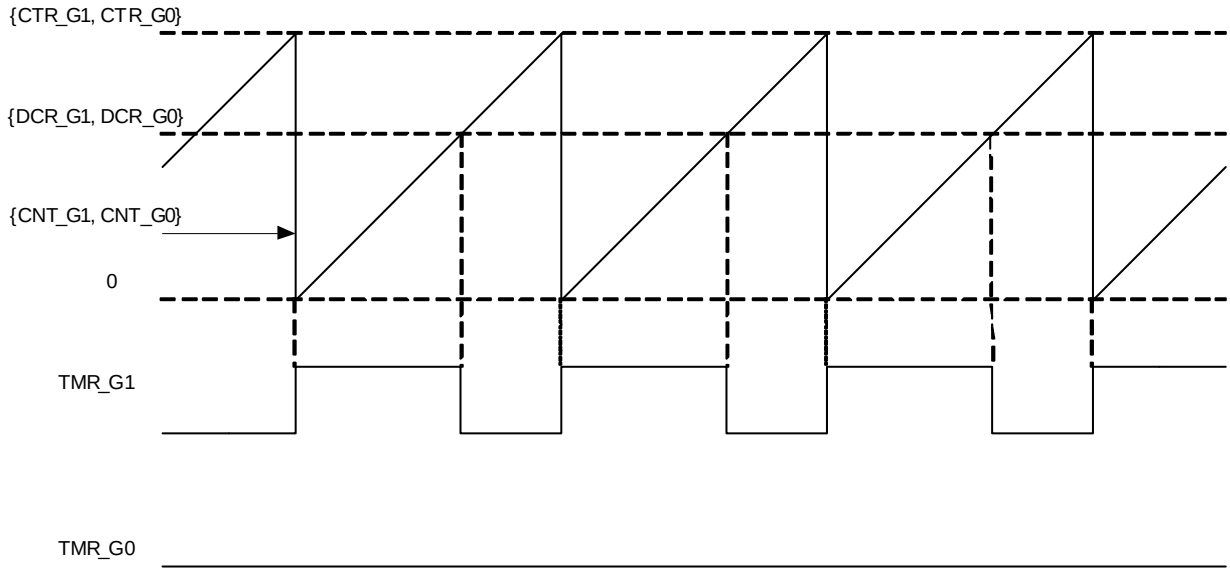
Tclk × PRSCi × (CTR_G + 1)

Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC), (1/ 6.14 MHz), or (1/ 6.45 MHz), which is selected by PCCS1-0 in GCSMS register.

The TMR_G1 output signal duty cycle (in %) is:

(DCR_G) / (CTR_G + 1) × 100

Figure 7-31. 16-bit Mode Waveform of Group G



Toggle mode

The Counter, Duty Cycle register, and Cycle Time register are cascaded in the same way as that in 16-bit pulse mode.

When TMR working clock is enabled, the TMR_G1 output polarity will be changed at the moment that the value in the CNT_G counter reaches the value in the DCR_G register and the TMR_G0 output polarity will be changed at the moment that the value in the CNT_G counter reaches the value in the CTR_G register. When the value in the CNT_G register reaches the value in the CTR_G register, the CNT_G counter will be reset then start counting until the TMR working clock is disabled.

The TMR_G1 and TMR_G0 output signal cycle time is:

Tclk × PRSCi × (CTR_G + 1)

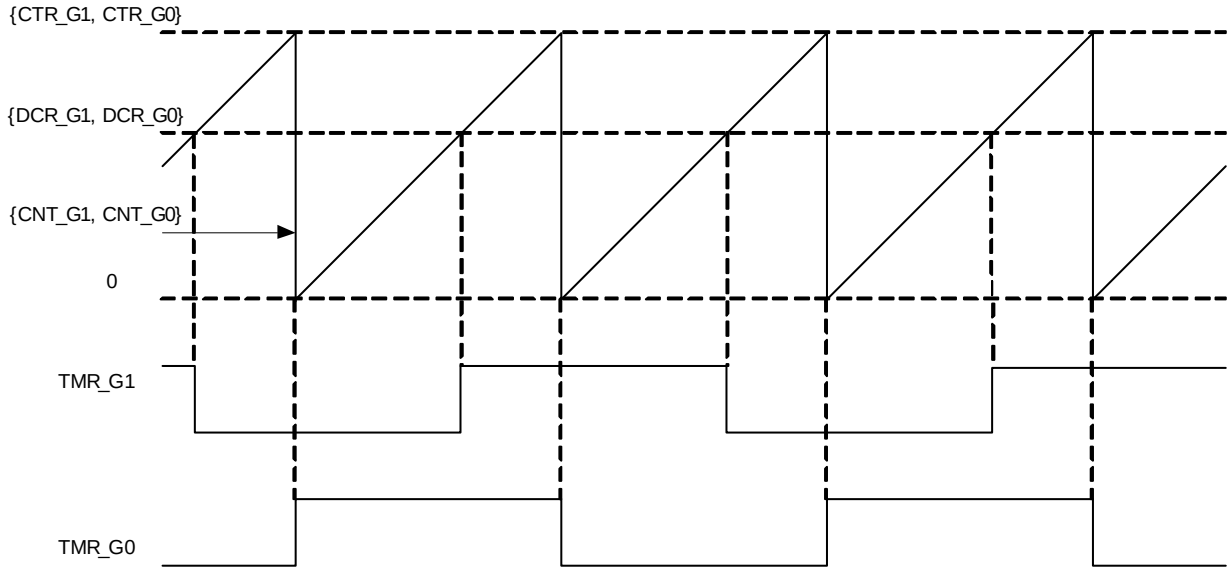
Where Tclk is the period of TMR intput clock = (1/ 32.768 kHz), (1/ FreqEC), (1/ 6.14 MHz), or (1/ 6.45 MHz), which is selected by PCCS1-0 in GCSMS register.

The TMR_G1 and TMR_G0 output signal duty cycle (in %) is 50 %.

The phase differential of TMR_G1 and TMR_G0 (in %) is:

(DCR_G) / (CTR_G + 1) × 100

Figure 7-32. 16-bit Mode Waveform of Group N



7.12.3.6 TMR Interrupt

Each TMR output can generate two types of interrupts, Cycle Time compare-match interrupt and Duty Cycle compare-match interrupt. Each interrupt source can be enabled or disabled independently by interrupt enable bits in TMRIE register. Independent signals are sent to the interrupt controller for each interrupt.

For the following three TMR modes, each of the four interrupts, TMRINTA0, TMRINTA1, TMRINTB0, TMRINTB1, has its own specific interrupt sources.

CTR_A = CTR_A1 * 100h + CTR_A0
DCR_A = DCR_A1 * 100h + DCR_A0
CTR_B = CTR_B1 * 100h + CTR_B0
DCR_B = DCR_B1 * 100h + DCR_B0

8-bit Pulse Mode

TMRINTA0: CTR_A0 compare-match and DCR_A0 compare-match sources.
TMRINTA1: CTR_A1 compare-match and DCR_A1 compare-match sources.
TMRINTB0: CTR_B0 compare-match and DCR_B0 compare-match sources.
TMRINTB1: CTR_B1 compare-match and DCR_B1 compare-match sources.

16-bit Pulse Mode

TMRINTA0: No interrupt.
TMRINTA1: CTR_A compare-match and DCR_A compare-match sources.
TMRINTB0: No interrupt.
TMRINTB1: CTR_B compare-match and DCR_B compare-match sources.

Toggle mode

TMRINTA0: CTR_A compare-match source.
TMRINTA1: DCR_A compare match source.
TMRINTB0: CTR_B compare-match source.
TMRINTB1: DCR_B compare match source.

7.12.4 EC Interface Registers

These registers are mapped in the address space of EC. The registers are listed below and the base address is 2900h.

Table 7-23. EC View Register Map, TMR

7	0	Offset
TMR Prescaler Register (PRSC)		00h
Group Clock Source and Mode Select Register (GCSMS)		01h
A0 Cycle Time Register (CTR_A0)		02h
A1 Cycle Time Register (CTR_A1)		03h
B0 Cycle Time Register (CTR_B0)		04h
B1 Cycle Time Register (CTR_B1)		05h
A0 Duty Cycle Register (DCR_A0)		06h
A1 Duty Cycle Register (DCR_A1)		07h
B0 Duty Cycle Register (DCR_B0)		08h
B1 Duty Cycle Register (DCR_B1)		09h
Channel Clock Group Select Register (CCGSR)		0Ah
TMR Clock Enable Register (TMRCE)		0Bh
TMR Interrupt Enable Register (TMRIE)		0Ch

For a summary of the abbreviations of register types, refer to “Register Abbreviations and Access Rules”

7.12.4.1 TMR Prescaler Register (PRSC)

This register controls the cycle time and the minimal pulse width of TMR channel.

Address Offset: 00h

Bit	R/W	Default	Description
7-4	R/W	0000b	**TMR Prescaler Divider Value 1 (PRSC1)** PWM input clock is divided by the number of PRSC1. 0000: clk disabled. 1000: clk/128. 0001: clk. 1001: clk/256. 0010: clk/2. 1010: clk/512. 0011: clk/4. 1011: clk/1024. 0100: clk/8. 1100: clk/2048. 0101: clk/16. 1101: clk/4096. 0110: clk/32. 1110: clk/8192. 0111: clk/64. 1111: clk/16384. Where clk is the clock source selected by PCSS1 field in GCSMS register.
3-0	R/W	0000b	**TMR Prescaler Divider Value 0 (PRSC0)** Bit 3-0 are the same as bit 7-4

7.12.4.2 Group Clock Source and Mode Select Register (GCSMS)

This register selects the clock source and mode.

Address Offset: 01h

Bit	R/W	Default	Description
7-6	R/W	00b	**Group B Mode (MODEB)** Select the mode of TMB0 and TMB1. 00: 8-bit pulse mode. 01: 16-bit pulse mode. 10: Toggle mode. 11: The same as 10.
5-4	R/W	00b	**Group A Mode (MODEA)** Select the mode of TMA0 and TMA1. Bit 5-4 are the same as bit 7-6.
3-2	R/W	00b	**Prescaler 1 Clock Source Select (PCSS1)** 00b: Select 32.768 kHz. 01b: Select FreqEC (EC Clock). 10b: Select FreqEC*2/3 (6.14 MHz) 11b: Select FreqPLL/5 (6.45 MHz, available only if PLLFREQ == 0011b) (FreqEC and FreqPLL are listed in Table 10-2 on page 352)
1-0	R/W	00b	**Prescaler 0 Clock Source Select (PCSS0)** Bit 1-0 are the same as bit 3-2

7.12.4.3 A0 Cycle Time Register (CTR_A0)

This register controls the cycle time of channel A0.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value A0 (CTVA0)** The Prescaler output clock is divided by the number of (CTR_A0 +1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divided by 256.

7.12.4.4 A1 Cycle Time Register (CTR_A1)

This register controls the cycle time of channel A1.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value A1 (CTVA1)** The function of this register is the same as that of CTR_A0.

7.12.4.5 B0 Cycle Time Register (CTR_B0)

This register controls the cycle time of channel B0.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value B0 (CTVB0)** The function of this register is the same as that of CTR_A0.

7.12.4.6 B1 Cycle Time Register (CTR_B1)

This register controls the cycle time of channel B1.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value B1 (CTVB1)** The function of this register is the same as that of CTR_A0.

7.12.4.7 A0 Duty Cycle Register (DCR_A0)

This register controls the duty cycle of channel A0.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value A0 (DCVA0)** DCR_A0 register decides the number of clocks for the waveform of the corresponding TMR output.

7.12.4.8 A1 Duty Cycle Register (DCR_A1)

This register controls the duty cycle of channel A1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value A1 (DCVA1)** The function of this register is the same as that of DCR_A0.

7.12.4.9 B0 Duty Cycle Register (DCR_B0)

This register controls the duty cycle of channel B0.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value B0 (DCVB0)** The function of this register is the same as that of DCR_A0.

7.12.4.10 B1 Duty Cycle Register (DCR_B1)

This register controls the duty cycle of channel B1.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value B1 (DCVB1)** The function of this register is the same as that of DCR_A0.

7.12.4.11 Channel Clock Group Select Register (CCGSR)

This register selects the clock group of TMR output.

Address Offset: 0Ah

Bit	R/W	Default	Description
7	R	0b	**TMR B1 Reading Register (RDB1)** Read Channel B1 if TMR output pins are used by other modules.
6	R	0b	**TMR B0 Reading Register (RDB0)** Bit 6 is the same as bit 7.
5	R	0b	**TMR A1 Reading Register (RDA1)** Bit 5 is the same as bit 7.
4	R	0b	**TMR A0 Reading Register (RDA0)** Bit 4 is the same as bit 7.
3	R/W	0b	**TMR B1 Clock Group Select Register (GRSELB1)** Select the clock group of channel B1. 0: Select Clock PRSC0. 1: Select Clock PRSC1.
2	R/W	0b	**TMR B0 Clock Group Select Register (GRSELB0)** Bit 2 is the same as bit 3 In the 16-bit pulse mode or toggle mode, this bit is of no use and the clock group of TMR B0 will be the same as TMR B1.
1	R/W	0b	**TMR A1 Clock Group Select Register (GRSELA1)** Bit 1 is the same as bit 3.
0	R/W	0b	**TMR A0 Clock Group Select Register (GRSELA0)** Bit 0 is the same as bit 3. In the 16-bit pulse mode or toggle mode, this bit is of no use and the clock group of TMR A0 will be the same as TMR A1.

7.12.4.12 TMR Clock Enable Register (TMRCE)

This register selects the clock group of TMR output.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1	R/W	0b	**TMR Clock Enable Register (CLKEN)** 1: Enable TMR clock counter. Set this bit to 1 after all other registers have been set. 0: Disable TMR clock counter.
0	R/W	0b	**TMR Test Mode (TMRTM)** 1: The mode of TMR is switched to a test mode. 0: TMR works in a normal mode.

7.12.4.13 TMR Interrupt Enable Register (TMRIE)

This register controls the interrupt enable of all TMR channels.

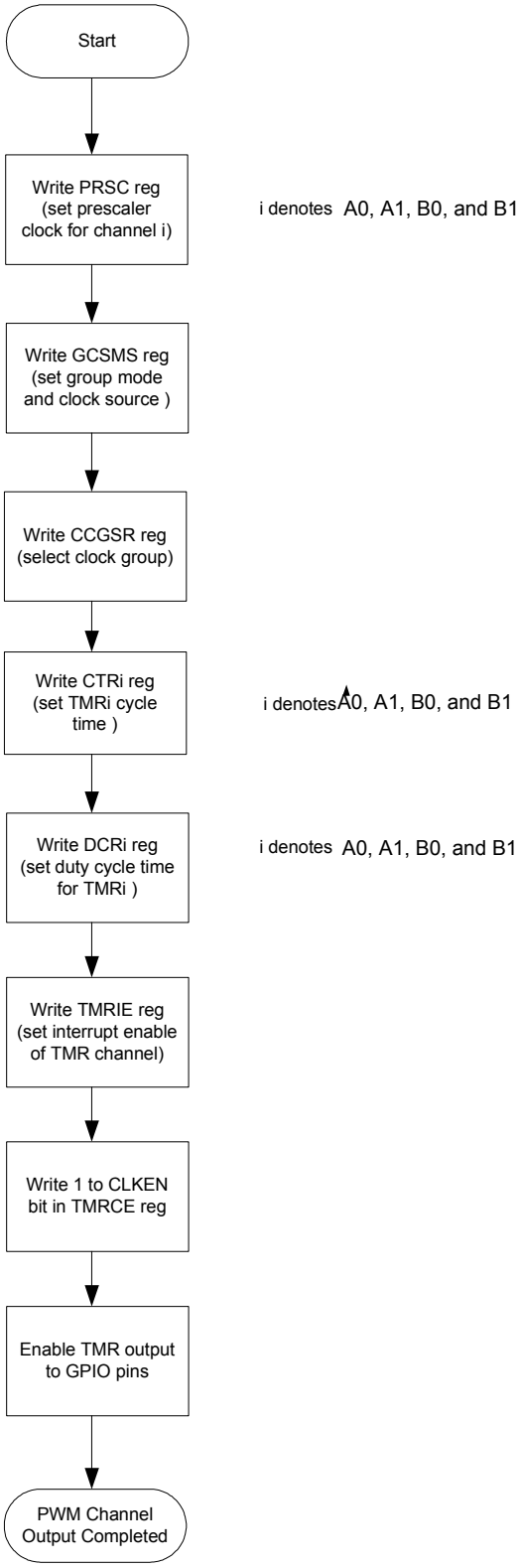
Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0b	**TMR B1 Duty Cycle Interrupt Enable Register (B1DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable **In toggle mode:** This bit controls the duty cycle compare-match interrupt enable.
6	R/W	0b	**TMR B1 Cycle Time Interrupt Enable Register (B1CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In toggle mode:** This bit is of no use.
5	R/W	0b	**TMR B0 Duty Cycle Interrupt Enable Register (B0DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use. **In toggle mode:** This bit is of no use.
4	R/W	0b	**TMR B0 Cycle Time Interrupt enable Register (B0CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** The bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** The bit is of no use. **In toggle mode:** The bit controls the cycle time compare-match interrupt enable.
3	R/W	0b	**TMR A1 Duty Cycle Interrupt enable Register (A1DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable **In toggle mode:** This bit controls the duty cycle compare-match interrupt enable.

Bit	R/W	Default	Description
2	R/W	0b	**TMR A1 Cycle Time Interrupt enable Register (A1CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In toggle mode:** This bit is of no use.
1	R/W	0b	**TMR A0 Duty Cycle Interrupt enable Register (A0DCRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the duty cycle compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use **In toggle mode:** This bit is of no use.
0	R/W	0b	**TMR A0 Cycle Time Interrupt enable Register (A0CTRIE)** 0: Disable 1: Enable **In 8-bit pulse mode:** This bit controls the cycle time compare-match interrupt enable. **In 16-bit pulse mode:** This bit is of no use. **In toggle mode:** This bit controls the cycle time compare-match interrupt enable.

7.12.5 TMR Programming Guide

Figure 7-33. Program Flow Chart for TMR Channel Output



7.13 EC Access to Host Controlled Modules (EC2I Bridge)

7.13.1 Overview

The module enables EC access to PNPCFG and SWUC modules. It can access the host domain modules with host on alternate usage or take control of it and prevent any host from accessing that module.

7.13.2 Features

- Supports lock bit to prevent conflicts in host-controlled module.
- Supports Super I/O I-Bus arbitration
- Supports Super I/O access lock violation indication

7.13.3 Functional Description

The EC2I bridge enables the EC to access the Host Controlled module registers (e.g., host configuration module(PNPCFG) and SWUC), using the I-Bus which is arbitrated by I-Bus Arbiter to prevent I-Bus grant from fighting between EC and the host side. The bridge provides a lock bit to control the access of the Host Controlled modules. When the related lock bit is cleared, the host is allowed to access to the Host Controlled modules registers. When the related lock bit is set, the host is not allowed to access to the Host Controlled module registers (i.e., write operations are ignored and read operations return the unknown). Whenever the host accesses to the locked register, a violation flag is set on the respective bit in the SIOLV register.
EC should access the Host Controlled modules only after preventing host accessing to the module (using lock bits). The I-Bus arbiter arbitrates I-Bus usage between the host and EC. If an LPC transaction has started prior to the beginning of EC transaction, EC waiting for the completion of the LPC transaction. If EC transaction starts prior to LPC transaction, the LPC translation needs to wait for the completion of EC transaction.
EC firmware may access the Host Controlled modules only when VSTBY is on and VCC is on and LPCCLK is active.

EC Read Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write 1 to CRIB bit in IBCTL register.
6. Read the CRIB bit in IBCTL until it returns 0.
7. Read the data from IHD register.

EC Write Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write the data to IHD register, which begins a write transaction.
6. Read the CWIB bit in IBCTL until it returns 0, which represents that a write transaction has been finished.

For minimal conflict between host and EC in the use of Host Controlled modules, refer to the followings.

Notice for Read/Write Operation
1. The host is allowed to access the Host Controlled module only when the corresponding lock bit is cleared.

7.13.4 EC Interface Registers

The following set of registers is accessible only by the EC. The registers are maintained by VSTBY. The registers are listed below and the base address is 1200h.

Table 7-24. EC View Register Map, EC2I

7	0	Offset
Indirect Host I/O Address.(IHIOA)		00h
Indirect Host Data (IHD)		01h
Lock Super I/O Host Access (LSIOHA)		02h
Super I/O Access Lock Violation (SIOLV)		03h
EC to I-Bus Modules Access Enable (IBMAE)		04h
I-Bus Control (IBCTL)		05h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.13.4.1 Indirect Host I/O Address Register (IHIOA)

This register defines the host I/O address for read or write transactions initiated by EC from/to the Host Controlled modules. The I/O address is an offset from the LSB bits of the address of the host controlled module. The accessed module is selected using EC to I-Bus Modules Access Enable Register (IBMAE).

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host I/O Offset (IHIOO)** These bits indicate the offsets within the device range are allowed.

7.13.4.2 Indirect Host Data Register (IHD)

This register holds host data for read or write transactions initiated by EC from/to the Host Controlled modules.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Indirect Host Data (IHDA)**

7.13.4.3 Lock Super I/O Host Access Register (LSIOHA)

This register controls locking of host access to the Host Controlled modules.

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	-	0b	**Reserved**
0	R/W	0b	**Lock PNPCFG Registers Host Access (LKCFG)** 0: Host access to the PNPCFG Registers is enabled. 1: Host access to the PNPCFG Registers is disabled.

7.13.4.4 Super I/O Access Lock Violation Register (SIOLV)

This register provides an error indication when a host lock violation occurs on Host Controlled modules access.

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	-	0b	**Reserved**
0	R/WC	0b	**PNPCFG Register Lock Violation (CFGLV)** 0: There is no lock violation when the host accesses PNPCFG registers. 1: when the host accesses PNPCFG register but LKCFG bit in LSIOHA register is set, this bit is set to indicate a violation and can be write-1-clear.

7.13.4.5 EC to I-Bus Modules Access Enable Register (IBMAE)

This register enables EC access to the Host Controlled modules. Only one of the bits in this register may be set at a time.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**Mobile System Wake-Up Control (SWUC) Access Enable (SWUCAE)** 0: EC access to the SWUC Registers is disabled. 1: EC access to the SWUC Registers is enabled.
1	-	-	**Reserved**
0	R/W	0b	**PNPCFG Register EC Access Enable (CFGAE)** 0: EC access to the PNPCFG Registers is disabled. 1: EC access to the PNPCFG Registers is enabled.

7.13.4.6 I-Bus Control Register (IBCTL)

This register allows EC to the I-Bus Bridge operation.

Address Offset: 05h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	-	-	**Reserved**
2	R	0b	**EC Write to I-Bus (CWIB)** Read: 1: EC write-access is still processing with IHD register. 0: It's completed.
1	R/W	0b	**EC Read from I-Bus (CRIB)** Write: See also CSAE bit definition. Read: 1: EC read-access is still processing. 0: It's completed and IHD register is available.
0	R/W	0b	**EC to I-Bus Access Enabled (CSAE)** 0: EC access to the I-Bus is disabled (default). 1: EC access to the I-Bus is enabled. The module to be accessed is selected in the IBMAE register. If 1 is written to both CSAE and CRIB, this access is a read-action. If 1 is written to CSAE and 0 to CRIB, this access is a write-action. If 0 is written to CSAE, the internal state machine of accessing is stopped.

7.13.5 EC2I Programming Guide

The read/write cycles PNPCFG and SWUC modules via EC2I are only valid when VCC is supplied. It means that such cycles may be executed after every VCC power-on.

Figure 7-34. Program Flow Chart for EC2I Read

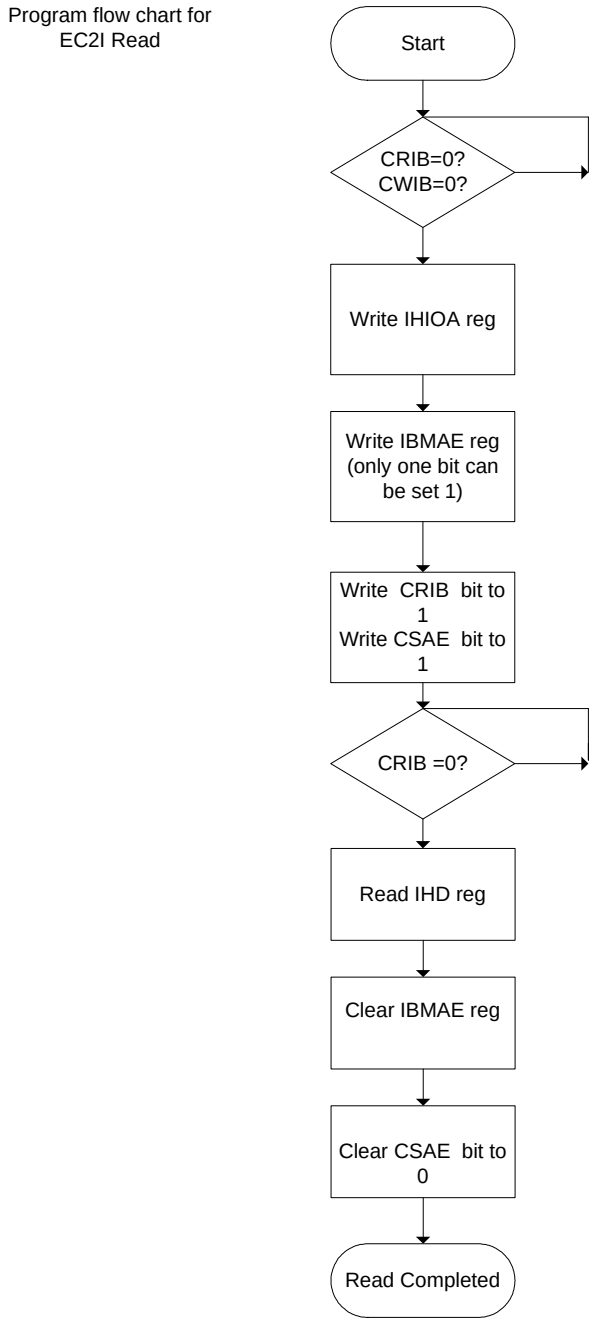
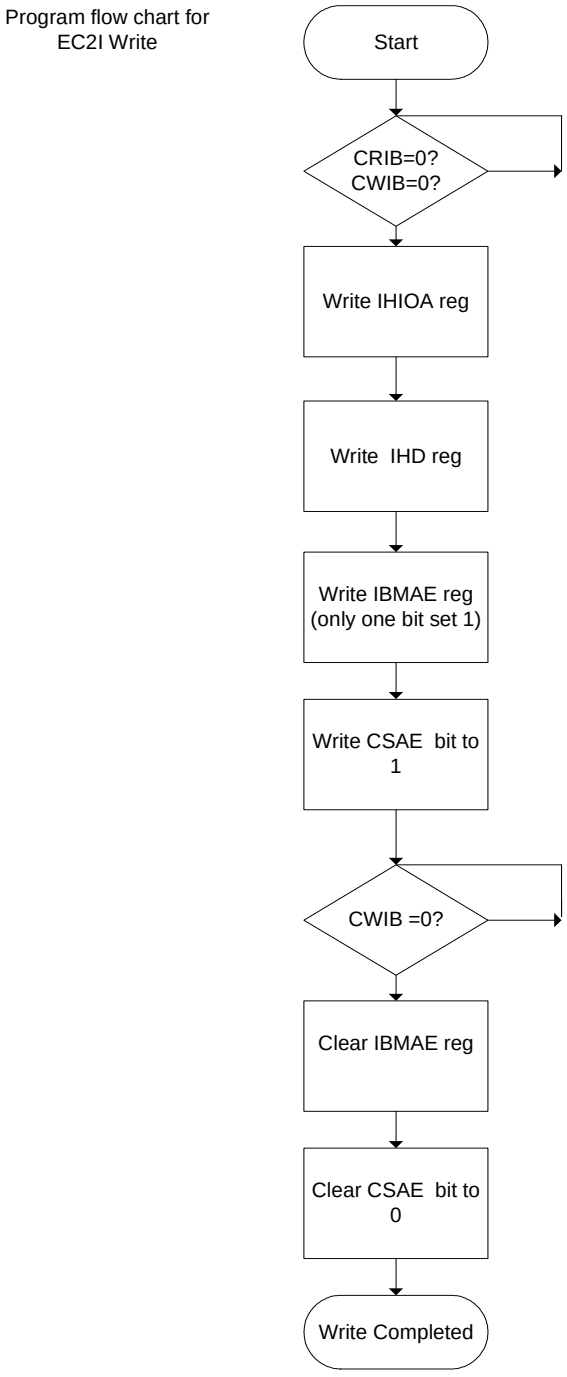


Figure 7-35. Program Flow Chart for EC2I Write



7.14 External Timer and External Watchdog (ETWD)

7.14.1 Overview

Besides the internal timer 0, 1, 2 and WDT inside the 8032, there are external timer 1 with WDT and external Timer 2 without WDT outside the 8032. External Timer 1 with WDT and External Timer 2 without WDT are based on 32.768 k Clock and still work when EC is in Idle/Doze/Sleep mode. The external timers are recommended to replace internal timer for periodical wakeup task.

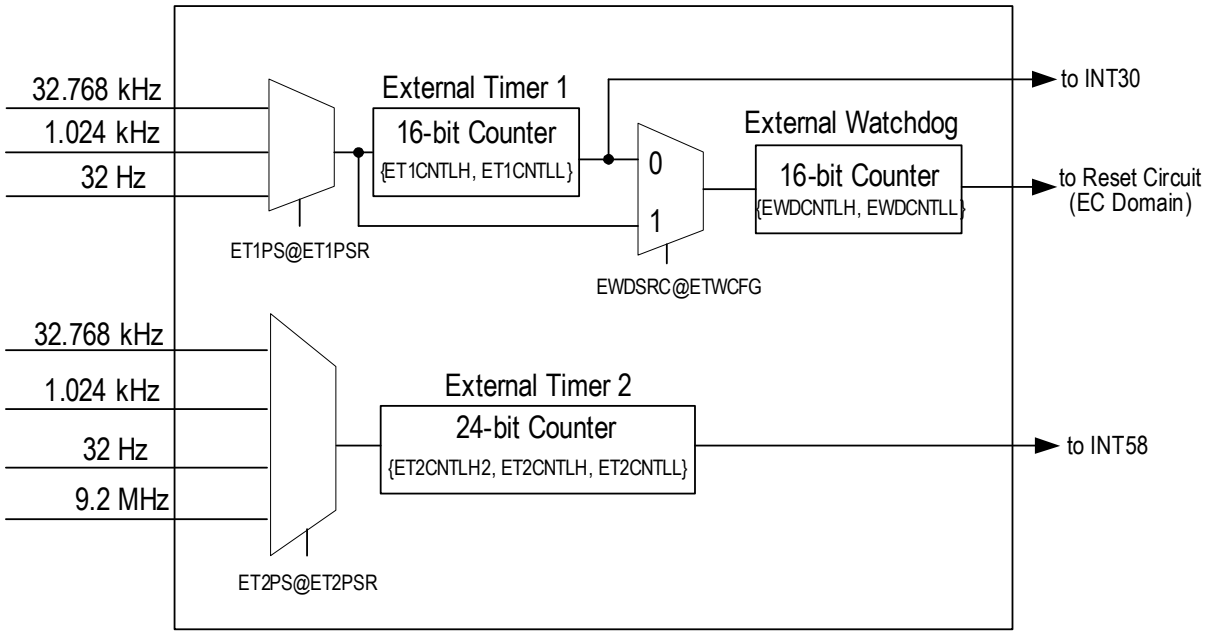
External Timer 1 with WDT has less power consumption than internal Timer/WDT due to the low frequency.

ETWD module cannot count external signal sources from pins. If the firmware wants to count external signal sources from pins, refer to TMRI0, TMRI1, TACH0 and TACH1. TMRI0/TMRI1 are used as Timer1/2 sources of 8032 and TACH0/1 are tachometer inputs of PWM.

7.14.2 Features

- 32.768 kHz, 1.024 kHz and 32 Hz prescaler for External Timer 1
- 32.768 kHz, 1.024 kHz, 32 Hz, and 9.2 MHz prescaler for External Timer 2
- 16-bit count-down External Timer 1
- 24-bit count-down External Timer 2
- 16-bit count-down External WDT

Figure 7-36. Simplified Diagram



7.14.3 Functional Description

7.14.3.1 External Timer Operation

The External Timer 1 is a 16-bit counter down timer, and the External Timer 2 is a 24-bit count-down timer. Its clock source is based on 32.768 k Clock and can be selected by a prescaler defined at ET1PS/ET2PS field in ET1PSR/ET2PSR register.

The count number of External Timer 1 is defined in ET1CNTLH and ET1CNTLL registers, and that of External Timer 2 is defined in ET2CNTLH2, ET2CNTLH, and ET2CNTLL registers. External Timer 1/2 is stopped after reset and started after writing data to ET1CNTLL/ET2CNTLL register and never stops until reset. It asserts an interrupt to INTC (INT30 for External Timer 1; INT58 for External Timer 2) when it counts to zero every time.

The External Timer 1/2 re-starts when
- it counts to zero periodically.
- data is written to ET1CNTLL/ET2CNTLL register.
- 1 is written to ET1RST/ET2RST bit in ETWCTRL register.

External Timer 1/2 asserts periodical interrupt to EC 8032 via INT30/INT58 of INTC.

7.14.3.2 External WDT Operation

External WDT is a 16-bit counter down timer. Its clock source is either External Timer 1 output or the same clock source of External Timer 1, and it is controlled by EWDSRC bit in ETWCFG register.
The count number is defined in EWDCNTLH and EWDCNTLL registers. External WDT is stopped after reset and started after writing data to EWDCNTLL register and can be stopped by setting EWDSCEN bit and EWDSCMS bit in ETWCTRL register. It asserts an External Watchdog Reset to EC domain when it counts to zero. External WDT requires starting External Timer 1 regardless of EWDSRC field in ETWCFG register. External WDT cannot be started until External Timer 1 is started.

The External WDT re-starts when it is touched by the firmware.
There are two following ways to touch (re-start) External WDT:
- Writing data to EWDCNTLL register (if LEWDCNTL bit in ETWCFG register is not set)
- Writing 5Ch to EWDKEYR register, called key-match

External WDT asserts an External Watchdog Reset to EC domain when
- it counts to zero.
- data except 5Ch is written to EWDKEYR register.

7.14.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 1F00h.

Table 7-25. EC View Register Map, ETWD

7 — 0	Offset
External Timer 1/WDT Configuration Register (ETWCFG)	01h
External Timer 1 Prescaler Register (ET1PSR)	02h
External Timer 1 Counter High Byte (ET1CNTLHR)	03h
External Timer 1 Counter Low Byte (ET1CNTLLR)	04h
External Timer 2 Prescaler Register (ET2PSR)	0Ah
External Timer 2 Counter High Byte (ET2CNTLHR)	0Bh
External Timer 2 Counter Low Byte (ET2CNTLLR)	0Ch
External Timer 2 Counter High Byte 2 (ET2CNTLH2R)	0Eh
External Timer/WDT Control Register (ETWCTRL)	05h
External WDT Counter High Byte (EWDCNTLHR)	09h
External WDT Counter Low Byte (EWDCNTLLR)	06h
External WDT Key Register (EWDKEYR)	07h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.14.4.1 External Timer 1/WDT Configuration Register (ETWCFG)

Address Offset: 01h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	0b	**External WDT Stop Mode (EWDSM)** 1: Stop counting WDT when LPC memory/FWH cycles are processing. 0: Otherwise
5	R/W	0b	**External WDT Key Enabled (EWDKEYEN)** 1: Enable the key match function to touch the WDT. 0: Otherwise.
4	R/W	0b	**External WDT Clock Source (EWDSRC)** 1: Select clock after prescaler of the external timer 1. 0: Select clock from the output of the external timer 1.
3	R/W	0b	**Lock EWDCNTLx Register (LEWDCNTL)** 1: Writing to EWDCNTL is ignored. 0: Writing to EWDCNTL is allowed.
2	R/W	0b	**Lock ET1CNTLx Registers (LET1CNTL)** 1: Writing to ET1CNTL is ignored. 0: Writing to ET1CNTL is allowed.
1	R/W	0b	**Lock ET1PS Register (LET1PS)** 1: Writing to ET1PS is ignored. 0: Writing to ET1PS is allowed.
0	R/W	0b	**Lock ETWCFG Register (LETWCFG)** 1: Writing to ETWCFG itself is ignored, and this bit can't be cleared until reset. 0: Writing to ETWCFG itself is allowed.

7.14.4.2 External Timer 1 Prescaler Register (ET1PSR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**External Timer 1 Prescaler Select (ET1PS)** These bits control the clock input source to the external timer 1. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: Reserved Note the prescaler will not output clock until data is written to ET1CNTLLR register.

7.14.4.3 External Timer 1 Counter High Byte (ET1CNTLHR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 1 Counter High Byte (ET1CNTLH)** Define the count number of high byte of the 16-bit count-down timer.

7.14.4.4 External Timer 1 Counter Low Byte (ET1CNTLLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 1 Counter Low Byte (ET1CNTLL)** Define the count number of low byte of the 16-bit count-down timer. The external timer 1 starts or re-starts after writing this register.

7.14.4.5 External Timer 2 Prescaler Register (ET2PSR)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	R/W	00b	**External Timer 2 Prescaler Select (ET2PS)** These bits control the clock input source to the external timer 2. 00b: 32.768 kHz 01b: 1.024 kHz 10b: 32 Hz 11b: 9.2 MHz Note the prescaler will not output clock until data is written to ET2CNTLLR register.

7.14.4.6 External Timer 2 Counter High Byte (ET2CNTLHR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte (ET2CNTLH)** Define the count number of high byte of the 24-bit count-down timer.

7.14.4.7 External Timer 2 Counter Low Byte (ET2CNTLLR)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter Low Byte (ET2CNTLL)** Define the count number of low byte of the 24-bit count-down timer. The external timer 2 starts or re-starts after writing this register.

7.14.4.8 External Timer 2 Counter High Byte 2 (ET2CNTLH2R)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer 2 Counter High Byte 2 (ET2CNTLH2)** Define the count number of high byte 2 of the 24-bit count-down timer.

7.14.4.9 External Timer/WDT Control Register (ETWCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R/W	0b	**External WDT Stop Count Enable (EWDSCEN)** 1: External WDT is stopped counting. 0: Otherwise. This bit cannot be set until EWDSCMS bit is set to 1.
4	R/W	0b	**External WDT Stop Count Mode Select (EWDSCMS)** 1: External WDT can be stopped by setting EWDSCEN bit. 0: External WDT cannot be stopped. Writing data to this bit is ignored after writing data to EWDCNTLL register, and this bit cannot be cleared until being reset.
3	R	0b	**External Timer 2 Terminal Count (ET2TC)** 1: Indicates the external timer 2 has counted down to zero, and it is cleared after reading it. 0: Otherwise. Writing to this bit is ignored.
2	W	-	**External Timer 2 Reset (ET2RST)** Writing 1 forces the external timer 2 to re-start. Writing 0 is ignored. Read always returns zero.
1	R	0b	**External Timer 1 Terminal Count (ET1TC)** 1: Indicates the external timer 1 has counted down to zero, and it is cleared after reading it. 0: Otherwise Writing to this bit is ignored.
0	W	-	**External Timer 1 Reset (ET1RST)** Writing 1 forces the external timer 1 to re-start. Writing 0 is ignored. Read always returns zero.

7.14.4.10 External WDT Counter High Byte (EWDCNTLHR)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**External WDT Counter High Byte (EWDCNTL)** Define the count number of high byte of the 16-bit count-down WDT.

7.14.4.11 External WDT Low Counter (EWDCNTLLR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0Fh	**External WDT Low Counter (EWDCNTL)** Define the count number of 16-bit count-down WDT.

7.14.4.12 External WDT Key Register (EWDKEYR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	W	-	**External WDT Key (EWDKEY)** External WDT is re-started (touched) if 5Ch is written to this register. Writing with other values causes an External Watchdog Reset. This function is enabled by EDWKEYEN bit. Read returns unpredictable value.

7.15 General Control (GCTRL)

7.15.1 Overview

This module controls EC function that doesn't belong to the specified module.

7.15.2 Features

- By module reset

7.15.3 Functional Description

Wait Next Clock Rising:
When writing 0 WNCKR register, the R8032TT will be paused and wait for a low to high transition of the internal 65.536 kHz clock. This may be useful to get a delay.

For a loop that writing 0 to WNCKR register for N times, the delay value will be
((N-1) / 65.536 kHz) to (N / 65.536 kHz)

e.g.
Consecutively writing 0 to WNCKR register for 33 times get 0.5ms delay with –2.3% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 66 times get 1ms delay with –0.8% ~ +0.7% tolerance.
Consecutively writing 0 to WNCKR register for 132 times get 2ms delay with –0.05% ~ +0.7% tolerance.

7.15.4 EC Interface Registers

The following set of the registers is accessible only by EC. They are listed below and the base address is 2000h.

Table 7-26. EC View Register Map, GCTRL

7	0	Offset
Chip ID Byte 1 (ECHIPID1)		00h
Chip ID Byte 2 (ECHIPID2)		01h
Chip Version (ECHIPVER)		02h
Reserved		03h
Identify Input Register (IDR)		04h
Reserved		05h
Reset Status (RSTS)		06h
Reset Control 1 (RSTC1)		07h
Reset Control 2 (RSTC2)		08h
Reset Control 3 (RSTC3)		09h
Reset Control 4 (RSTC4)		11h
Reset Control DMM (RSTDMMC)		10h
Base Address Select (BADRSEL)		0Ah
Wait Next Clock Rising (WNCKR)		0Bh
Oscillator Control Register (OSCTRL)		0Ch
Special Control 1 (SPCTRL1)		0Dh
Reset Control Host Side (RSTCH)		0Eh
Generate IRQ (GENIRQ)		0Fh

For a summary of the abbreviations used for the register type, see "Register Abbreviations and Access Rules".

7.15.4.1 Chip ID Byte 1 (ECHIPID1)

The content of this EC side register is the same as that of the CHIPID1 register in the host side.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	85h	**Chip ID Byte 1 (ECHIPID1)** This register contains the Chip ID byte 1.

7.15.4.2 Chip ID Byte 2 (ECHIPID2)

The content of this EC side register is the same as that of the CHIPID2 register in the host side.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R	02h	**Chip ID Byte 2 (ECHIPID2)** This register contains the Chip ID byte 2.

7.15.4.3 Chip Version (ECHIPVER)

This register contains revision ID of this chip.
The content of this EC side register is the same as that of the CHIPVER register in the host side.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R	71h	**Chip Version (ECHIPVER)**

7.15.4.4 Identify Input Register (IDR)

Address Offset: 04h

Bit	R/W	Default	Description
7	R	-	**Identify Input 7 (ID7)**
6	R	-	**Identify Input 6 (ID6)**
5	R	-	**Identify Input 5 (ID5)**
4	R	-	**Identify Input 4 (ID4)**
3	R	-	**Identify Input 3 (ID3)**
2	R	-	**Identify Input 2 (ID2)**
1	R	-	**Identify Input 1 (ID1)**
0	R	-	**Identify Input 0 (ID0)**

7.15.4.5 Reset Status (RSTS)

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R/W	10b	**VCC Detector Option (VCCDO)** 10b: The VCC power status is detected by internal circuit. 00b: The VCC power status is treated as power-off. 01b: The VCC power status is treated as power-on. otherwise: reserved No matter which option is selected, the VCC power status is always recognized as power off if LPCPD# input is level low. The VCC power status is used as internal “power good” signal to prevent current leakage while VCC is off. The current VCC power status can be read from VCCPO bit in SWCTL1 register in section 6.4.5.1 on page 102. Intentionally toggling this field when VCC is supplied can reset logic VCC domain in EC.
5	-	-	**Reserved**
4	-	-	**Reserved**
3	R/W	1b	**Host Global Reset (HGRST)** 0: The reset source of PNPCFG is RSTPNP bit in RSTCH register and WRST#. 1: The reset source of PNPCFG are RSTPNP bit in RSTCH register, internal VCC status controlled by VCCDO bit in RSTS register, LPCPD#, LPCRST# and WRST#.
2	R/W	1b	**Global Reset (GRST)** This bit controls whether to reset EC domain globally during Internal/External Watchdog Reset. 0: Only reset 8032, and each module can be reset by RSTC register 1: Reset all the EC domain
1-0	R	-	**Last Reset Source (LRS)** If this register field is used, it is required to read this field once and only one time after reset. 00b, 01b: VSTBY Power-Up Reset or Warm Reset 10b: Internal Watchdog Reset 11b: External Watchdog Reset

7.15.4.6 Reset Control 1 (RSTC1)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).
Refer to VCCDO field in RSTS register to reset logic in VCC domain in EC.

Address Offset: 07h

Bit	R/W	Default	Description
7	W	-	**Reset SMFI (RSMFI)**
6	W	-	**Reset INTC (RINTC)**
5	W	-	**Reset EC2I (REC2I)**
4	W	-	**Reset KBC (RKBC)**
3	W	-	**Reset SWUC (RSWUC)**
2	W	-	**Reset PMC (RPMC)**
1	W	-	**Reset GPIO (RGPIO)**
0	W	-	**Reset PWM (RPWM)**

7.15.4.7 Reset Control 2 (RSTC2)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 08h

Bit	R/W	Default	Description
7	W	-	**Reset ADC (RADC)**
6	W	-	**Reset DAC (RDAC)**
5	W	-	**Reset WUC (RWUC)**
4	W	-	**Reset KBS (RKBS)**
3	-	-	**Reserved**
2	W	-	**Reset EGPC (REXGPIO)**
1	-	-	**Reserved**
0	-	-	**Reserved**

7.15.4.8 Reset Control 3 (RSTC3)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 09h

Bit	R/W	Default	Description
7	-	-	**Reserved**
6	W	-	**Reset PS/2 Channel 3 (RPS23)**
5	W	-	**Reset PS/2 Channel 2 (RPS22)**
4	W	-	**Reset PS/2 Channel 1 (RPS21)** To reset the logic of PS/2 shared with all channels, write 1111b to bit 7-4 at the same time and writing 0111b is reserved.
3	W	-	**Reset SMBus Channel D (RSMBD)**
2	W	-	**Reset SMBus Channel C (RSMBC)**
1	W	-	**Reset SMBus Channel B (RSMBB)**
0	W	-	**Reset SMBus Channel A (RSMBA)** To reset the logic of SMBus shared with all channels, write 1111b to bit 3-0 at the same time and writing 0111b is reserved.

7.15.4.9 Reset Control 4 (RSTC4)

Write 1 to the selected bit(s) to possibly reset corresponding module(s).

Address Offset: 11h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	-	-	**Reserved**
3	W	-	**Reset TMR (TMR)**
2	W	-	**Reserved**
1	W	-	**Reset UART1 (RUART1)**
0	W	-	**Reset SPI (RSPI)**

7.15.4.10 Reset Control DMM (RSTDMMC)

Determine whether a double-mapping module belongs to the host or EC side.

Address Offset: 10h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	-	-	**Reserved**
3	R/W	0b	**UART1 SIDE (UART1SD)** 1: UART1 belongs to the EC side. 0: UART1 belongs to the host side and it will be reset during Host Domain Hardware/Software reset. See also section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 206.
2	-	-	**Reserved**
1	R/W	1b	**SSPI SIDE (SSPISD)** 1: SSPI belongs to the EC side. 0: SSPI belongs to the host side and it will be reset during Host Domain Hardware/Software reset. See also section 7.6.3.5 Auto Clock Gating (AUTOCG) on page 206.
0	-	-	**Reserved**

7.15.4.11 Base Address Select (BADRSEL)

Address Offset: 0Ah

Bit	R/W	Default	Description
7-2	-	-	**Reserved**
1-0	R/W	00b	**Base Address (BADDR1-0)** 00b: The register pair to access PNPCFG is 002Eh and 002Fh. 01b: The register pair to access PNPCFG is 004Eh and 004Fh. 10b: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR. 11b: Reserved.

7.15.4.12 Wait Next Clock Rising (WNCKR)

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	W	-	**Wait Next 65K Rising (WN65K)** Writing 00h to this register and the R8032TT program counter will be paused until the next low to high transition of 65.536 kHz clock. Writing other values is reserved.

7.15.4.13 Oscillator Control Register (OSCTRL)

Address Offset: 0Ch

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	-	-	**Reserved**
3-1	-	-	**Reserved**
0	R/W	1b	**Oscillator Enable (OSCEN)** 1b: 32.768 kHz oscillator will keep running if VBS/VSTBY power = on/off 0b: 32.768 kHz oscillator in this case

7.15.4.14 Special Control 1 (SPCTRL1)

Address Offset: 0Dh

Bit	R/W	Default	Description
7	R/W	0b	**P80L Enable (P80LEN)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VBS power and only reset by VBS Power-Up Reset. Refer to section 7.17.3.1 **P80L** on page 308. 1b: Enable P80L function. 0b: Otherwise
6	R/W	0b	**Accept Port 80h Cycle (ACP80)** This bit will be set if 1 is written and cleared if 1 is written or there is a VCC on->off transition. This bit is supplied by the VBS power and only reset by VBS Power-Up Reset. Refer to section Refer to section 7.17.3.1 **P80L** on page 308. 1b: The host LPC I/O cycle with address 80h will be accepted by EC. If P80LEN is set, enabling this bit to guarantee LPC I/O port 80h data can be latched even though there is a transaction cycle to BRAM or EC2I->RTC in EC side. 0b: Otherwise
5-2	-	-	**Reserved**
1-0	R/W	00b	**I2EC Control (I2ECCTRL)** 00b: I2EC is disabled. 10b: I2EC is read-only. 11b: I2EC is read-write. 01b: Reserved Refer to section 7.20.3.2 EC Memory Snoop (ECMS) on page 332.

7.15.4.15 Reset Control Host Side (RSTCH)

Address Offset: 0Eh

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2	W	-	**Reset PNPCFG (RSTPNP)**
1-0	-	-	**Reserved**

7.15.4.16 Generate IRQ (GENIRQ)

Address Offset: 0Fh

Bit	R/W	Default	Description
7-4	-	-	**Reserved**
3-0	W	-	**Generate IRQ Number (GENIRQNUM)** Writing to this field will generate SERIRQ with a specified number. This field is valid only when it is between 1-12 or 14-15.

7.16 External GPIO Controller (EGPC)

7.16.1 Overview

This module controls the external GPIO (General Purpose I/O Port) chip. It can maintain bi-directional communication with the 4 external IT8301.

7.16.2 Features

- Communicate with 4 IT8301 chip
  (IT8301 is a 48-pin GPIO chip)
- Each IT8301 supports 38 GPIO ports

7.16.3 Functional Description

This module uses a three-wire bidirectional interface for data transmission. When writing the data to the External GPIO Data Register, this module will start to transmit the data (the contents of the External GPIO Data Register) to the targeted register of the external GPIO chip (the targeted register can be assigned in the External GPIO Address Register). When reading the External GPIO Data Register, the contents of the targeted register of the external GPIO chip can be read.

Because of the serial nature of the interface, the time of accessing the external GPIO chip may be longer than the time that the 8032 CPU read/write the External GPIO Controller registers. We have two methods to handle this condition.

(1). A dedicated channel ready signal (internal signal) for the 8032 CPU

The channel ready signal (internal signal) is used to inform the 8032 CPU whether the data transfer process is ended or not. When the Channel Ready Enable bit in the External GPIO Control Register is set, the channel ready signal will not be asserted until the data transfer process is ended. When the Channel Ready Enable bit is cleared, the channel ready signal is always set high no matter the data transfer process is ended or not.

(2). Enable the cycle done interrupt

If the Channel Ready Enable bit in the External GPIO Control Register is cleared, the firmware must enable the Cycle Done Interrupt Enable bit in the External GPIO Control Register to know that the data transfer process is ended or not. When writing the data to the External GPIO Data Register, this module will start to transmit the data to the targeted register of the external GPIO chip. When the transfer process is ended, the Cycle Done Status bit in the External GPIO Status Register is set and the Cycle Done Interrupt is asserted. When firmware first reads the External GPIO Data Register, this module will start to receive data from the targeted register of the external GPIO chip. When the transfer process is ended, the Cycle Done Status bit in the External GPIO Status Register is set and the Cycle Done Interrupt is asserted. Then the firmware can read again the External GPIO Data Register to get the updated data.

7.16.4 EC Interface Registers

The EGPC registers are listed below. The base address is 2100h.

Table 7-25. EC View Register Map, EGPC

7	0	Offset
External GPIO Address Register (EADDR)		00h
External GPIO Data Register (EDAT)		01h
External GPIO Control Register (ECNT)		02h
External GPIO Status Register (ESTS)		03h

7.16.4.1 External GPIO Address Register (EADDR)

Address Offset: 00h

Bit	R/W	Default	Description
7-2	R/W	00h	**Address (AD)** The 6-bit address of the targeted register of the external GPIO chip.
1-0	R/W	00h	**Chip Selection (CS)** These bits will be transmitted as external chip selection

7.16.4.2 External GPIO Data Register (EDAT).

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data (DATA)** When writing to this register, the contents of this register are sent to the targeted register of the external GPIO chip. When reading this register, the contents of the targeted register of the external GPIO chip can be read.

7.16.4.3 External GPIO Control Register (ECNT).

Address Offset: 02h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4-2	R/W	100b	**Transmitted Data Bits (TMB)** Define the number of the data bits that will be transmitted to (or received from) the data register of the external GPIO chip. 000: 1 bit 001: 2 bits 010: 3 bits 011: 4 bits 100: 5 bits 101: 6 bits 110: 7 bits 111: 8 bits
1	R/W	0b	**Cycle Done Interrupt Enable (CDIE)** Enable or disable the interrupt generation when the Cycle Done status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
0	R/W	1b	**Channel Ready Enable (CREN)** The channel ready signal (internal signal) is used to inform the 8032 CPU that the data transfer process is ended or not. When this bit is set, the channel ready signal will not be asserted until the data transfer process is ended. When this bit is cleared, the channel ready signal is always set high no matter the data transfer process is ended or not. 0: Disabled. 1: Enabled.

7.16.4.4 External GPIO Status Register (ESTS).

Address Offset: 03h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R	-	**Cycle Done Status (CDS)** This bit is set when the data transfer was done.

7.17 Battery-backed SRAM (BRAM)

7.17.1 Overview

This module provides 192 bytes of battery-backed memory area and power-switching circuit.

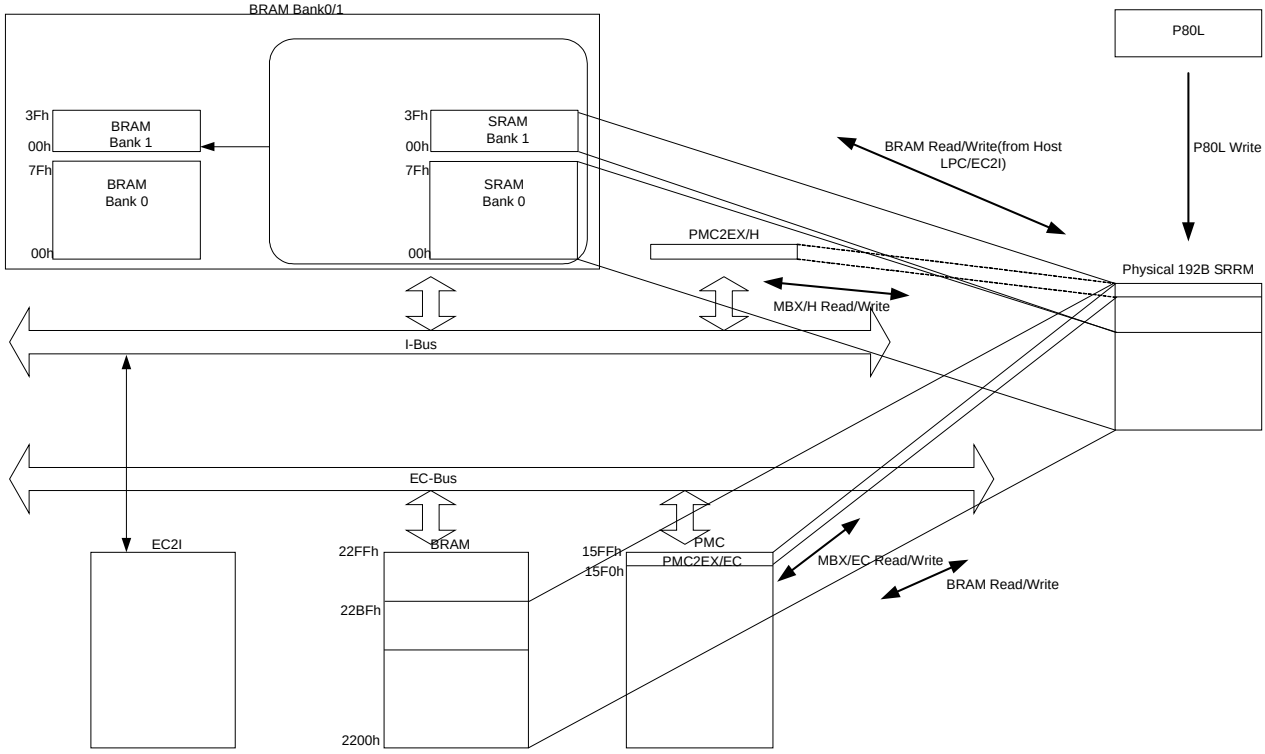
7.17.2 Features

- 192 bytes of battery-backed SRAM shared with the host side
- Power-switching circuit

7.17.3 Functional Description

This module provides 192 bytes of battery-backed SRAM for data-saving function shared with the host side.

Figure 7-37. BRAM Mapping Diagram



7.17.3.1 P80L

If this function is enabled by P80LEN bit in SPCTRL1 register, LPC I/O port 80h written data will be latched into SRAM of BRAM bank 1.

The data may fail to latch data if there is a transaction cycle to BRAM or EC2I->RTC in the EC side at the same time unless ACP80 bit in SPCTRL1 register is set, which guarantees written data is latched into SRAM by issuing Long Wait Sync on host LPC bus.

The destination address range in BRAM Bank 1 is determined by P80LB, P80LE register in the host side, which constructs a queue.
P80LB: It indicates the start index of the queue. Readable/Writable.
P80LE: It indicates the end index of the queue.Readable/Writable.

P80LC: It indicates the current index of the queue. Read-only.
These three registers are supplied by VBS power and not affected by VCC status.

Whenever written data is latched, P80LC increases one. If it reaches P80LE (queue end), it will wrap back to P80LB (queue begin).

7.17.4 Host Interface Registers

The registers of BRAM can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.

The BRAM resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The BRAM logical device number is 10h (LDN=10h).

These registers are listed below.

Table 7-27. Host View Register Map, BRAM

7 … 0	Offset
BRAM Index Register of Bank 0 (RIRB0)	Legacy 70h
BRAM Data Register of Bank 0 (RDRB0)	Legacy 71h
BRAM Index Register of Bank 1 (RIRB1)	Legacy 72h
BRAM Data Register of Bank 1 (RDRB1)	Legacy 73h

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)
Legacy 72h represents (I/O Port Base Address 1) + (Offset 0h)
Legacy 73h represents (I/O Port Base Address 1) + (Offset 1h)
See also Table 6-3 on page 42.

Table 7-28. Host View Register Map via Index-Data I/O Pair, BRAM Bank 0

7 … 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT127)	7Fh

Table 7-29. Host View Register Map via Index-Data I/O Pair, BRAM Bank 1

7 … 0	Offset
SRAM Byte n Registers (SBT128)	00h
…	…
SRAM Byte n Registers (SBT191)	3Fh

7.17.5 EC Interface Registers

The registers of the battery-backed SRAM are listed below. The base address is 2200h.

Table 7-30. EC View Register Map, BRAM

7 … 0	Offset
SRAM Byte n Registers (SBT0)	00h
…	…
SRAM Byte n Registers (SBT191)	BFh

7.17.5.1 SRAM Byte n Registers (SBTn, n= 0-191).

Address Offset: 00h – BFh for byte 0 – byte 191

Bit	R/W	Default	Description
7-0	R/W	-	**SRAM Data (SD)** When data is written to this register, it will be saved in the corresponding memory space. When this register is read, the contents of the corresponding memory space can be read. For example, when data is written to the SRAM Byte 0 Register, it will be saved in the memory space 2200h. When the SRAM Byte 63 Register is read, the data saved in the memory space 223Fh can be read.

7.18 Serial Peripheral Interface (SSPI)

7.18.1 Overview

The SPI device uses 3-wire bi-directional or 4-wire interface for data transmission. The 4-wire device consists four signals, SSCE#, SSCK, SMOSI, and SMISO, for data transmission, and the 3-wire device consists three signals, SSCE#, SSCK, SMISO, for data transmission. The SPI interface consists of one channel which can be selected to connect to the 3-wire or 4-wire device.

7.18.2 Features

- Supports one SPI channel.
- Supports both Host and EC side.
- Supports eight frequency dividers of SSCK. (2, 4, 6, 8, 10, 12, 14, 16)
- Supports 8-bit transmission and 1-bit transmission.
- Supports blocking and non-blocking selection.
- Supports Interrupt enable and Interrupt disable in the non-blocking selection.
- Supports 3-wire SPI device and 4-wire SPI device.
- Supports four clock modes.
- Supports BUSY pin.

7.18.3 Functional Description

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. The interfacne supplies the synchronous clock (SSCK) for the serial interface and initiates the data transfer.

The device responds by sending (or receiving) the requested data. The device uses the interface clock to serially shift data out (or in) while the interface shifts the data in (or out).

7.18.3.1 Data Transmissions

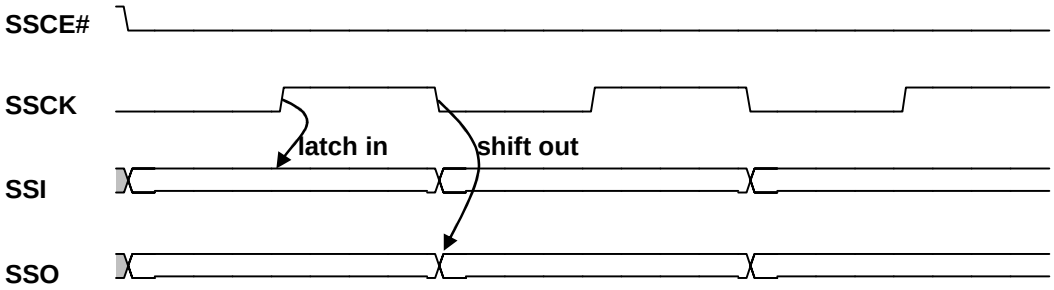
8-bit Transmission
The interface supports 8-cycle SSCK for data transmission. It is available for 1-byte transaction devices. (default)

N-bit Transmission (N = 1 ~ 7)
The interface supports N-cycle SSCK for data transmission. It is available for non-1-byte transaction devices.

7.18.3.2 SPI Mode

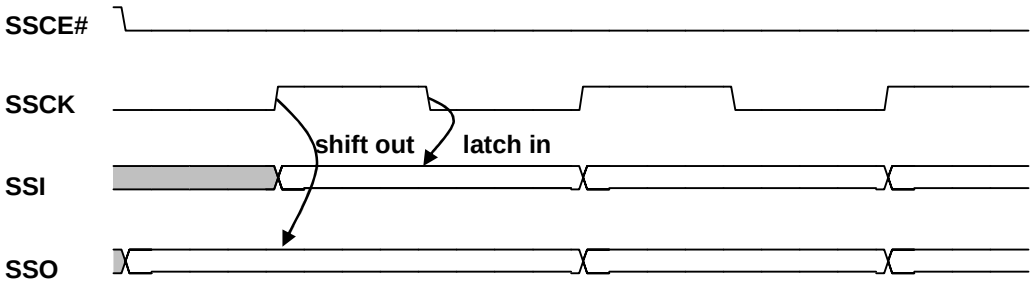
Mode 0
SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-38. SPI Mode 0 Waveform



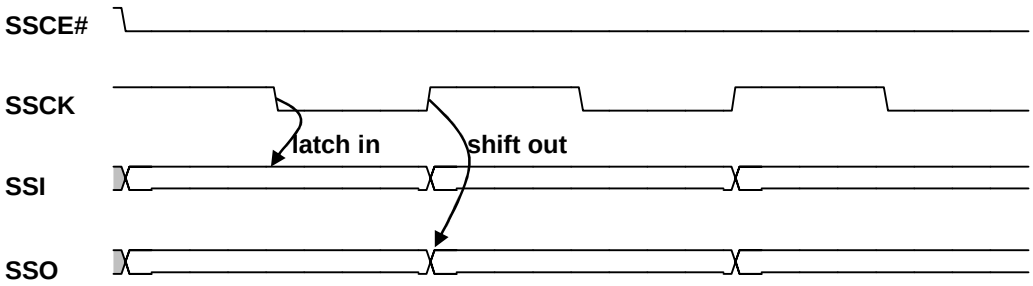
Mode 1
SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-39. SPI Mode 1 Waveform



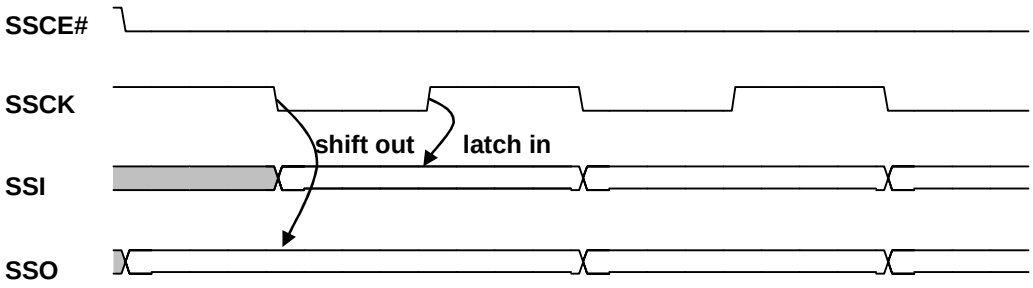
Mode 2
SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge.

Figure 7-40. SPI Mode 2 Waveform



Mode 3
SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.

Figure 7-41. SPI Mode 3 Waveform



7.18.3.3 Blocking and Non-blocking mode

- Blocking mode:

After starting the read cycle or write cycle to the SPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the bus will be blocked until this read/write command is finished.

If the SPI function is controlled by the EC side, 8032 instruction will be halted until this read/write command is finished.

If the SPI function is controlled by the host side, the LPC bus will return the long-wait sync pattern until this read/write command is finished.

It means that the interrupt and the polling are not needed.

- Non-blocking mode

After starting the read cycle or write cycle to the SSPI module (writing 1 to CH0START or CH1START bit in SPISTS register), the processor receives an interrupt signal or polls bit 2 of SPISTS register to determine if this read/write command will be terminated .

7.18.4 Host Interface Registers

The registers of SSPI can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The SSPI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers.
The SSPI logical device number is 13h (LDN=13h).
These registers are listed below:

Table 7-316. Host View Register Map, SSPI

7 — 0		Offset
SPI Data Register (SPIDATA)		00h
SPI Control Register 1 (SPICTRL1)	Bank 0	01h
SPI Control Register 2 (SPICTRL2)		02h
SPI Control Register 3 (SPICTRL3)	Bank 1	01h
SPI Start and End Status Register (SPISTS)		03h

All registers are double mapped into the host and EC side, however, the SSPI function should be controlled by a side only.

7.18.5 EC Interface Registers

The register map of EC interface is listed below. The base address for SSPI is 2600h.

Table 7-327. EC View Register Map, SSPI

7	0	Offset
SPI Data Register (SPIDATA)		00h
SPI Control Register 1 (SPICTRL1)		01h
SPI Control Register 2 (SPICTRL2)		02h
SPI Control Register 3 (SPICTRL3)		04h
SPI Start and End Status Register (SPISTS)		03h

7.18.5.1 SPI Data Register (SPIDATA)

In the read mode, the register holds the shift data from the SPI device. In the write mode, the interface shift the data out to the SPI device.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**SPI Data (DATA)** Receive Data from the SPI device or Transmit Data to the SPI device.

7.18.5.2 SPI Control Register 1 (SPICTRL1)

This register controls the SPI operation mode.

Address Offset: Host: 01h (Bank 0) / EC: 01h

Bit	R/W	Default	Description
7	R/W	0b	**Chip Select Polarity (CHPOL)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 0. Otherwise, the bit indicates both the chip select polarity of device 0 and device 1 0: Active low 1: Active high
6-5	R/W	00b	**Bit 6:Clock Polarity (CLPOL)** 0: SSCK is low in the idle mode. 1: SSCK is high in the idle mode. **Bit 5:Clock Phase (CLPHS)** 0: Latch data on the first SSCK edge. 1: Latch data on the second SSCK edge. **Mode 0:** SSCK is low in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge. **Mode 1:** SSCK is low in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 2:** SSCK is high in the idle mode. Data is sampled on the falling edge, and shifted on the rising edge. **Mode 3:** SSCK is high in the idle mode. Data is sampled on the rising edge, and shifted on the falling edge.
4-2	R/W	000b	**SSCK Frequency (SCKFREQ)** **000b:** 1/2 FreqEC **001b:** 1/4 FreqEC **010b:** 1/6 FreqEC **011b:** 1/8 FreqEC **100b:** 1/10 FreqEC **101b:** 1/12 FreqEC **110b:** 1/14 FreqEC **111b:** 1/16 FreqEC (FreqEC is listed in Table 10-2 on page 352)
1	R/W	0b	**Interrupt Enable (INTREN)** 0: Disable 1: Enable
0	R/W	0b	**Device0 3-Wire Mode (3WIRECH0)** 0: Disable (4-wire) 1: Enable (3-wire)

7.18.5.3 SPI Control Register 2 (SPICTRL2)

This register controls the SPI operation mode.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0b	**Host Side Bank (HBANK)** The bit is only available in host side. 0: bank 0 1: bank 1
6	R/W	0b	**Device Busy Polarity (DEVBUSYPOL)** The bit indicates the state of the device busy signal when the device is not busy.
5-3	R/W	000b	**Byte Width (BYTEWIDTH)** 000b: 8-bit transmission 001b: 1-bit transmission 010b: 2-bit transmission 011b: 3-bit transmission 100b: 4-bit transmission 101b: 5-bit transmission 110b: 6-bit transmission 111b: 7-bit transmission
3	R/W	0b	**Byte Width (BYTEWIDTH)** 0: 8-bit transmission 1: 1-bit transmission
2	R/W	0b	**Channel Read/Write Cycle (CHRW)** 0: Write cycle 1: Read cycle
1	R/W	0b	**Block Select (BLKSEL)** 0: Non-blocking selection 1: Blocking selection
0	R/W	0b	**Device1 3-Wire Mode (3WIRECH1)** 0: Disable (4-wire) 1: Enable (3-wire)

7.18.5.4 SPI Start and End Status Register (SPISTS)

This register reports the status of the SPI and controls the start and end signal.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W1C	0b	**Wait Busy Start Signal (WAITBUSYSTART)** Write 1 to start the Wait Busy function after a write command or a read command. Read 0b.
6	R	-	**Device Busy Signal (DEVBUSY)** The bit indicates the device busy signal.
5	R/W1C	0b	**SPI Transmission End (TRANEND)** Write 1 to end the SPI transmission. Read 0b.
4	R/W1C	0b	**Channel 0 Start Signal (CH0START)** Write 1 to start the data transmission of device 0. Read 0b.
3	R/W1C	0b	**Channel 1 Start Signal (CH1START)** Write 1 to start the data transmission of device 1. Read 0b.
2	R	0b	**Transfer In Progress (TRANIP)** This bit indicates the SPI is in the transmission state. 0: Data transfer is not in progress. 1: Data transfer is in progress.
1	R/W1C	0b	**Transfer End Flag(TRANENDIF)** This bit indicates SPI transmission ends. The bit will be 1 when writing 1 to TRANEND bit. Write 1 to clear this bit and terminate data transmission.
0	R	0b	**SPI Busy (SPIBUSY)** This bit indicates whether the SPI interface is busy or not. 0: SPI idle 1: SPI busy

7.18.5.5 SPI Control Register 3 (SPICTRL3)

This register controls the SPI operation mode.

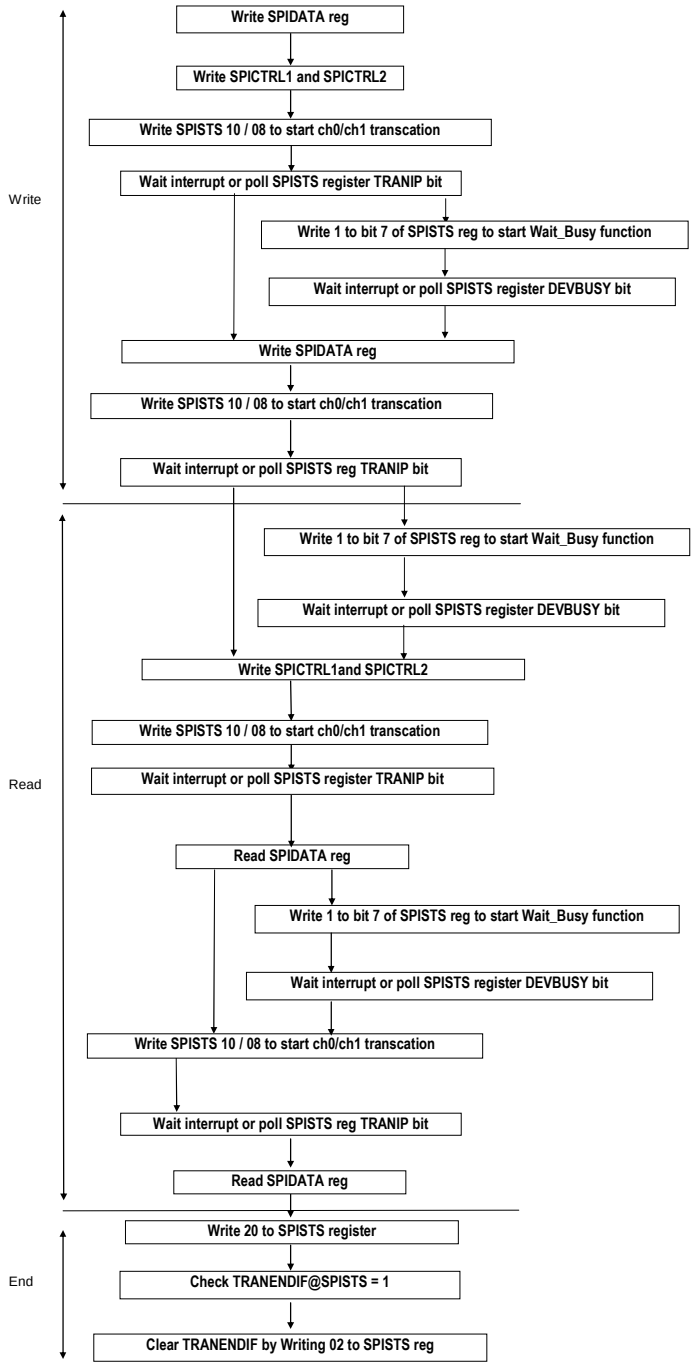
Address Offset: Host: 01h (Bank 1) / EC: 04h

Bit	R/W	Default	Description
7-4	R	-	**Reserved**
3	R/W	0b	**Device Busy Mode(DEVBUSYMODE)** 0: Without device busy pin. 1: Wth device busy pin.
2	R/W	0b	**Chip Select Polarity Select (CSPOLSEL)** 0: The chip select polarity of device 1 and device 0 is the same. 1: The chip select polarity of device 1 and device 0 is different.
1	R/W	0b	**Chip Select Polarity 1 (CHPOL1)** If CSPOLSEL is set to 1, the bit indicates the chip select polarity of device 1. 0: Active low 1: Active high
0	R/W	0b	**No BUSY Clock (BUSYNOCLK)** 0: Generate SSPI clock when waiting for the device busy signal. 1: Do not generate SSPI clock when waiting for the device busy signal.

7.18.6 Programming Guide

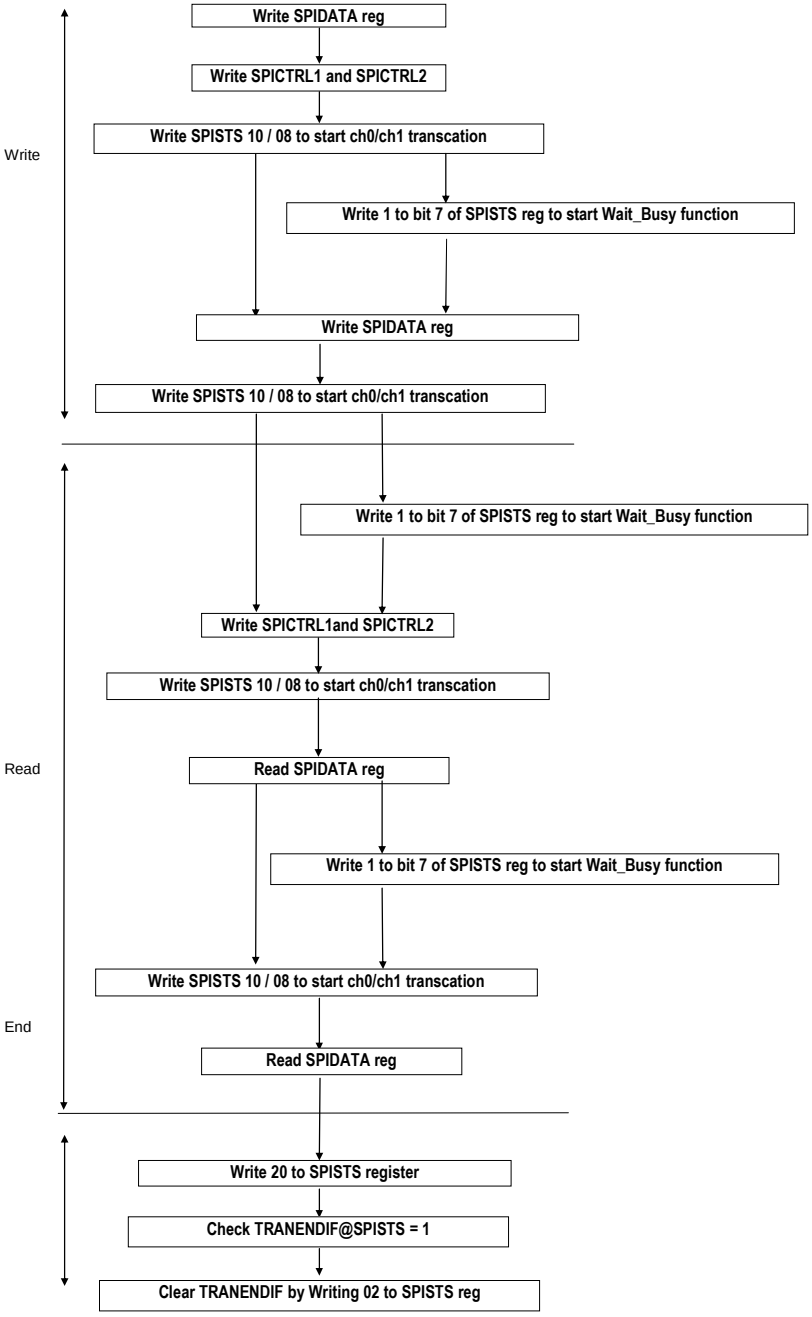
Write 16-bit data to SPI device 0/1 and read 16-bit data from SPI device 0/1.

Figure 7-42. Program Flow Chart for SSPI Non-blocking



Write 16-bit data to SPI device 0/1 and read 16-bit data from SPI device 0/1.

Figure 7-43. Program Flow Chart for SSPI Blocking



7.19 Serial Port (UART)

7.19.1 Overview

Besides the internal UART inside the 8032, there is an external UART1 outside the 8032.
UART1 can be accessed by software in the host or EC side, however, the UART1 function should be controlled by a side only.

The UART1 module is 16550 compatible. This module performs the serial to parallel conversion for the received data, and parallel to serial conversion for the transmitted data.

7.19.2 Features

- Programmable FIFO or character mode
- The 16-byte FIFO buffer is on the transmitter and receiver in the FIFO mode
- Add or delete standard asynchronous communication bits (start, stop and parity) to or from serial data.
- The programmable baud rate generator allows the division of input clock by 1 to 2^16-1 and generates the internal 16X clock.
- Modem control function (CTS#, RTS#, DTR#, DSR#, RI#, DCD#)
- Fully programmable serial-interface characteristics: 5, 6, 7 or 8-bit character
- Even, odd, forced 0/1 or no parity bit generation and detection
- 1, 1½, or 2 stop bits generation
- Baud rate up to 115.2K
- Baud rate up to 230.4K/460.8K if high speed mode enabled
- False start bit detection

7.19.3 Functional Description

UART contains a programmable baud rate generator that is capable of dividing the input clock by a number from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts. Besides, if the High Speed Baud Rate Select (HHS) or EC High Speed Select (ECHS) is activated, the highest baud rate can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator.

7.19.4 Host Interface Registers

The registers of UART1 can be treated as Host Interface Registers or EC Interface Registers. This section lists the host interface registers. These registers can only be accessed by the host processor.
The UART resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The UART logical device number is 01h ; 02h (LDN=01h for UART1).
These registers are listed below:

Table 7-33. Host/EC View Register Map, UART

			Index
Receiver Buffer Register (RBR)	if DLAB=0	R	00h
Interrupt Enable Register (IER)	if DLAB=0	R/W	01h
Interrupt Identification Register (IIR)		R	02h
Line Control Register (LCR)		R/W	03h
Modem Control Register (MCR)		R/W	04h
Divisor Latch LSB Register (DLL)	if DLAB=1	R/W	00h
Divisor Latch MSB Register (DLM)	if DLAB=1	R/W	01h
Line Status Register (LSR)		R/W	05h
Modem Status Register (MSR)		R/W	06h
Scratch Pad Register (SCR)		R/W	07h
Transmitter Holding Register (THR)		W	00h
FIFO Control Register (FCR)		W	02h
EC Serial Port Mode Register (ECSPMR)	EC View	R/W	08h

All registers are double mapped into the host and EC side except that ECSPMR is only for EC side; however, the UART function should be controlled by a side only.

7.19.5 EC Interface Registers

The register map of EC interface is the the same as Host interface registers. The base address for UART1 is 2700h.

7.19.5.1 Receiver Buffer Register (RBR)

This register receives and holds the entering data. It contains a non-accessible shift register that converts the incoming serial data stream to a parallel 8-bit word.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R	00h	**Receiver Buffer Register (URBR)** This register receives and holds the entering data.

7.19.5.2 Transmitter Holding Register (THR)

This register holds and transmits the data via a non-accessible shift register. It converts the outgoing parallel data to a serial stream before transmission.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	W	-	**Transmitter Holding Register (THR)** This register holds and transmits the data via a non-accessible shift register.

7.19.5.3 Interrupt Enable Register (IER)

IER is used to enable (or disable) four active high interrupts that activate the interrupt outputs with its lower four bits, bit 0-bit 3.

Address Offset: 01h

Bit	R/W	Default	Description
7-4	R	0h	**Reserved** These bits are always “0”.
3	R/W	-	**Enable Modem Status Interrupt (EMSI)** Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit state.
2	R/W	-	**Enable Receiver Line Status Interrupt (ERLSI)** Set this bit high to enable the receiver line status interrupt, which is caused when overrun, parity, framing or break occurs.
1	R/W	-	**Enable Transmitter Holding Register Empty Interrupt (ETHREI)** Set this bit high to enable the transmitter holding register empty interrupt.
0	R/W	-	**Enable Received Data Available Interrupt (ERDVI)** Set this bit high to enable the received data available interrupt (and time-out interrupt in the FIFO mode).

7.19.5.4 Interrupt Identification Register (IIR)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	R	00b	**Interrupt Identification Register Bit 7, Bit 6 (IIR7, IIR6)** These bits are set when FCR[0] is equal to 1.
5-4	R	00b	**Reserved** Always logic 0.
3	R	0b	**Interrupt Identification Register Bit 3 (IIR3)** In the non-FIFO mode, this bit is logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.
2-1	R	00b	**Interrupt Identification Register Bit 2, Bit 1 (IIR2, IIR1)** These bits are used to identify the highest priority pending interrupt.
0	R	1b	**Interrupt Identification Register Bit 0 (IIR0)** This bit is used to indicate a pending interrupt in either a hard-wired prioritized or a polled environment with a logic 0 state. When the condition takes place, IIR contents may be used as a pointer to the appropriate interrupt service routine.

Table 7-34. Interrupt Control Functions

IIR				Interrupt Set and Reset Functions			
Bit3	**Bit2**	**Bit1**	**Bit0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	0	1	-	None	None	-
0	1	1	0	1st	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	2nd	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or FIFO drops below the Trigger Level
1	1	0	0	2nd	Character Timeout Identification	There is at least one character in the FIFO but no character has been input to the FIFO or read from it for the last four Char times.	Reading the Receiver Buffer Register
0	0	1	0	3rd	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if the source of interrupt is THRE) or Writing into the THR
0	0	0	0	4th	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

7.19.5.5 FIFO Control Register (FCR)

This register is used to enable, and clear the FIFO, and set the RCVR FIFO trigger level.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	W	00b	**FIFO Control Register Bit 7, Bit 6 (FCR7,FCR6)** These bits set the trigger level for the RCVR FIFO interrupt. **FCR7 FCR6 RCVR FIFO Trigger Level** 0 0 1 byte 0 1 4 bytes 1 0 8 bytes 1 1 14 bytes
5-4	W	00b	**Reserved**
3	W	0b	**Reserved** This bit does not affect the serial channel operation. RXRDY and TXRDY functions are not available on this controller.
2	W	0b	**XMIT FIFO Reset (XFRST)** This self-clearing bit clears all contents of XMIT FIFO and resets its related counter to 0.
1	W	0b	**RCVR FIFO Reset (RFRST)** Set this self-clearing bit to logic “1” to clear all contents of RCVR FIFO and resets its related counter to 0 (except the shift register).
0	W	0b	**FIFO Enable (FEN)** XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs will be disabled and cleared when this bit is cleared to low. This bit has to be a logic “1” if the other bits of the FCR are written or they will not be properly programmed. When this register is changed to the non-FIFO mode, all contents will be cleared.

7.19.5.6 Divisor Latch LSB (DLL)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLL)** This register stores the low byte of the divisor.

7.19.5.7 Divisor Latch MSB (DLM)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Divisor Latch LSB (DLM)** This register stores the high byte of the divisor.

Table 7-35. Baud Rate Using 1.8432MHz Clock

Desired Baud Rate	Divisor Used	Percent Error Difference[1]	High Speed Bit[2]
50	2304	-	X
75	1536	-	X
110	1047	0.1247	X
134.5	857	0.0409	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.5916	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	-	X
57600	2	-	X
115200	1	-	X
230400	32770	-	1
460800	32769	-	1

Note[1]: The percent error difference, which is between the desired and the actual value, for all baud rates is 0.0986% except where the baud rates are indicated otherwise.
Note[2]: The high speed bit indicates whether the HHS bit or ECHS bit is set to high or not.

7.19.5.8 Scratch Pad Register (SCR)

There are two 8-bit Divisor Latches (DLL and DLM), which store the divisor in a 16-bit binary format. They are loaded during initialization to generate a desired Baud Rate.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	-	**Scratch Pad Register (SCR)** This 8-bit register does not control the operation of UART in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general-purpose data.

7.19.5.9 Line Control Register (LCR)

LCR controls the format of the data character and provides the information of the serial line.

Address Offset: 03h

Bit	R/W	Default	Description
7	R/W	-	**Divisor Latch Access Bit (DLAB)** This bit has to be set high to access the Divisor Latches of the baud rate generator during read or write operation and set low to access the Data Register (RBR and THR) or the Interrupt Enable Register.
6	R/W	-	**Break Control (BREAK)** This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will remain until a low level resets this bit, enabling the serial port to alert the terminal in a communication system.
5	R/W	-	**Stick Parity Bit (SP)** When this bit and Parity Enable (PEN) bit are high at the same time, the parity bit is transmitted and then detected by the receiver. On the contrary, the parity bit is detected by Even Parity Select (EPS) bit to force the parity to a known state and to check the parity bit in a known state.
4	R/W	-	**Even Parity Select (EPS)** When the parity is enabled (Parity Enable=1), EPS=0 selects odd parity, and EPS=1 selects even parity.
3	R/W	-	**Parity Enable (PEN)** A parity bit, between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when this bit is high.
2	R/W	-	**Stop Bit Select (STB)** Specify the number of stop bits in each serial character, which is summarized below: **STB — Word Length — No. of Stop Bit** 0 — - — 1 bit 1 — 5 — 1.5 bits 1 — 6 — 2 bits 1 — 7 — 2 bits 1 — 8 — 2 bits **Note:** The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.
1-0	R/W	-	**Word Length Select Bit 1, Bit 0 (WLS1, WLS0)** Specify the number of bits in each serial character, which is encoded below: **WLS1 — WLS0 — Word Length** 0 — 0 — 5 bits 0 — 1 — 6 bits 1 — 0 — 7 bits 1 — 1 — 8 bits

7.19.5.10 Modem Control Register (MCR)

Address Offset: 04h

Bit	R/W	Default	Description
7-5	R	000b	**Reserved** Bit 7-5 are always low.
4	R/W	0b	**Loop** This bit provides a loopback feature for the diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State. Shift Register output Loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected, and the four are forced to inactive high. The transmitted data are immediately received, allowing the processor to verify the data paths of transmitting and receiving of the serial channel.
3	R/W	0b	**OUT2** The Output 2 bit enables the serial port interrupt output by a logic 1.
2	-	0b	**OUT1** This bit does not have an output pin and can only be read or written by the processor.
1	R/W	0b	**Request To Send (RTS)** This bit controls the Request to Send (RTS#), which is in an inverse logic state with it.
0	R/W	0b	**Data Terminal Ready (DTR)** This bit controls the Data Terminal Ready (DTR#), which is in an inverse logic state with it.

7.19.5.11 Line Status Register (LSR)

Address Offset: 05h

Bit	R/W	Default	Description
7	R/W	0b	**Error In RCVR FIFO (ERF)** In the 16550 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads LSR if there are no subsequent errors in the FIFO.
6	R	1b	**Transmitter Empty (TEMT)** This read-only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty; otherwise, this bit is “0”. It has the same function in the FIFO mode.
5	R	1b	**Transmitter Holding Register Empty (THRE)** This read-only bit indicates that the THR is empty, and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to XMIT FIFO.
4	R/W	0b	**Break Interrupt (BI)** This bit indicates that the last received character is a break character. The break interrupt status bit will be asserted only when the last received character, parity bits and stop bits are all break bits. When any of these error conditions is detected (LSR[1] to LSR[4]), a Receiver Line Status interrupt (priority 1) will be produced in IIR with IER[2] previously enabled.
3	RC	0b	**Framing Error (FE)** When this bit is a logic 1, it indicates that the stop bit in the received character is not valid. It is reset low when the CPU reads the contents of LSR.
2	RC	0b	**Parity Error (PE)** This bit Indicates the parity error (PE) with a logic “1”, representing that the received data character does not have the correct even or odd parity as bit 3 of LCR (Parity Enable) is set to “1”. It will be reset to “0” whenever LSR is read by CPU.
1	RC	0b	**Overrun Error (OE)** Overrun Error (OE) bit is set as a logic “1” after RBR has been overwritten by the next character before it is read by CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when CPU reads LSR.
0	R/W	0b	**Data Ready (DR)** A logic “1” indicates a character has been received by RBR. A logic “0” indicates all data in the RBR or RCVR FIFO have been read.

7.19.5.12 Modem Status Register (MSR)

This 8-bit register provides the current state of the control lines from modems or peripheral devices. In addition to this current state information, bit 7-4 can provide the change information when a modem control input changes the state. It will be reset to low when the processor reads MSR.

Address Offset: 06h

Bit	R/W	Default	Description
7	R	0b	**Data Carrier Detect (DCD#)** This bit indicates the complement status of Data Carrier Detect input. If bit 4 of MCR is 1, this bit is equivalent to OUT2 of MCR.
6	R	0b	**Ring Indicator (RI#)** This bit indicates the complement to the RI# input. If bit 4 of MCR is 1, this bit is equivalent to OUT1 in MCR.
5	R	0b	**Data Set Ready (DSR#)** This bit indicates the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (bit 5 of MCR is 1), this bit is equivalent to DTR# in the MCR.
4	R	0b	**Clear to Send (CTS#)** This bit indicates the complement of CTS# input. If the serial channel is in the loop mode (bit 4 of MCR is 1), this bit is equivalent to RTS# in MCR.
3	R/W	0b	**Delta Data Carrier Detect (DDCD)** This bit indicates that the DCD# input state has been changed since the last time it is read by the processor.
2	R/W	0b	**Trailing Edge of Ring Indicator (TERI)** This bit indicates that RI input state to the serial channel has been changed from a low to high state since the last time it is read by the processor. The change of logic 1 doesn't activate TERI.
1	R/W	0b	**Delta Data Set Ready (DDSR)** A logic "1" indicates that DSR# input state to the serial channel has been changed since the last time it is read by the processor.
0	R/W	0b	**Delta Clear to Send (DCTS)** This bit indicates the CTS# input state to the serial channel has been changed since the last time it is read by the processor.

7.19.5.13 EC Serial Port Mode Register (ECSPMR)

Address Offset: 08h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved** Bit 7-2 are always low.
1	R/W	0b	**EC High Speed Select (ECHS)** This bit indicates that the supported baud rate of UART1 can be up to 230.4K and 460.8K, which are determined by the divisor of the baud rate generator. (From EC Side) 0: Not selected 1: Selected
0	-	0b	**Reserved** This bit is always low.

7.19.6 Programming Guide

Each serial channel is programmed by control registers whose contents define the character length, number of stop bits, parity, baud and modem interface. Although the control registers can be written in any order, IER

should be the last because it controls whether the interrupt is enabled. After the port is programmed, these registers can still be updated whenever the port is not transferring data.

7.19.6.1 Programming Sequence

UART module in Intelligent Peripheral Controller is compatible with standard 16550. The following is the programming sequence for standard 16550 compatible component register.

For access RBR/THR:
1. Set bit 7 of the LCR register to “0”.
2. Access RBR/THR.

For Access IER:
1. Set bit 7 of the LCR register to “0”.
2. Access IER.

For Access DLL/DLM:
1. Set bit 7 of the LCR register to “1”.
2. Access DLL/DLM.

7.19.7 Software Reset

This method allows returning to a completely known state without a system reset. It consists of writing the required data to LCR, DLL, DLM and MCR. LSR and RBR has to be read before enabling interrupts in order to clear any residual data or status bits that may be invalid for the subsequent operations.

If UART function is controlled by the EC side, it can be done by writing 1 to the corresponding bit in RSTC4 register, too.

7.19.8 Clock Input Operation

The input frequency of the Serial Channel is FreqEC/5, not exactly 1.8432 MHz.
FreqEC is listed in Table 10-2 on page 352.

7.19.9 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When bit 0 of FCR and bit 0 of IER are set to 1, RCVR FIFO and receiver interrupts are enabled. RCVR interrupt occurs under the following conditions:

A. The received data available interrupt and the IIR receive data available indication will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level.

B. The receiver line status interrupt has higher priority than the received data available interrupt.

C. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever a time-out interrupt occurs.

RCVR FIFO time-out Interrupt: By enabling RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

A. It will occur only if there is at least one character in FIFO whenever the period between the most recent received serial character and the most recent processor read from the FIFO is longer than the period of four consecutive character-time.

B. The time-out timer will be reset after receiving a new character or after the processor reads RCVR FIFO whenever any time-out interrupts occur. The timer will be reset when the processor reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting bit 0 of FCR and bit 1 of IER to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt will occur as follows:

A. The transmitter interrupt will occur when XMIT FIFO is empty, and it will be reset if THR is written or IIR is read.
B. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following conditions occurs:
THRE=1 and there are not at least two bytes in the transmitter FIFO at the same time since the last THRE=1. The transmitter interrupt will be issued immediately after the bit 0 of FCR is changed. Once it is enabled, the THRE indication is delayed for 1 character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation (Bit 0 of FCR is 1, and bit 0, 1, 2, 3 of IER or all are 0.)
Either one or both XMIT and RCVR can be in this operation mode in which the program will check RCVR and XMIT status via the LSR as described below:

LSR[7]: RCVR FIFO error indication.
LSR[6]: XMIT FIFO and Shift register empty.
LSR[5]: The XMIT FIFO empty indication.
LSR[4] – LSR[1]: Specify that errors have occurred, and the character error status is handled in the same way as in the interrupt mode. IIR is not affected since IER(2)=0.
LSR[0]: This bit is high whenever RCVR FIFO contains at least one byte. There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode.

7.19.10 High Speed Baud Rate Activation

When the high speed baud rate select bit is set to 1 from host side (High Speed Baud Rate Select ; HHS) or EC side (EC High Speed Select ; ECHS), the highest baud rate of UART1 can be up to 230.4K or 460.8K, which are determined by the divisor of the baud rate generator.

If HHS or ECHS is set to 1 and the divisor is 32770, the baud rate is 230.4K.
If HHS or ECHS is set to 1 and the divisor is 32769, the baud rate is 460.8K.

7.20 Debugger (DBGR)

7.20.1 Overview

This EC side module provides three 18-bit 8032 ROM trigger addresses and issues an INT0# and EC Memory Snoop (ECMS).

7.20.2 Features

- 3 trigger addresses
- EC Memory Snoop (ECMS = I2EC + D2EC)

7.20.3 Functional Description

7.20.3.1 ROM Address Match Interrupt

The trigger address, where an instruction is constructed by one, two or three bytes, has to be the first byte of each instruction.

INT0RM is set when the trigger address matches the 8032 program counter except that the trigger address is equal to zero.

If Parallel Port cable is detected by internal hardware strap, this function is disabled.

Note that DBGR module is clock-gated in default and cannot work until 0 is written to DBGRCG bit in the CGCTRL3R register.

7.20.3.2 EC Memory Snoop (ECMS)

ECMS is available through one of the two ways:

1. I2EC (I-bus to EC Memory)
Local machine snoops EC memory through the LPC I/O cycle.

2. D2EC (DBGR to EC Memory)
Remote machine snoops EC memory through EPP cycle.

I2EC/D2EC utility is provided by ITE.
I2EC is not enabled until its controlled register in the EC side register is written.
I2EC can be configured as read-only for all targets.
If D2EC is enabled by the utility, I2EC will be disabled until reset.
I2EC/D2EC will not affect any register content of read-clear registers.
The writing action of I2EC/D2EC to F/F based register is okay, however, the result of writing to non-F/F based register is not expected. Such registers may be write-clear, or writing to start internal state-machine, etc.
If D2EC is enabled, PLL will not be power-down in the Sleep mode.

Table 7-36. I2EC/D2EC Accessible Target

	I2EC	D2EC
uC SFR (except Acc reg.)	R	R
uC SFR - Acc reg.	R	R/W
uC External Memory (except DMM)	R/W controlled by I2ECCTRL field in SPCTRL1 reg.	R/W
uC External Memory – DMM	Not Accessible	R

Note: DMM denotes double-mapping module.

7.20.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 2500h.

Table 7-37. EC View Register Map, DBGR

7	0	Offset
Trigger 1 Address Low Byte Register (BKA1L)		10h
Trigger 1 Address Middle Byte Register (BKA1M)		11h
Trigger 1 Address High Byte Register (BKA1H)		12h
Trigger 2 Address Low Byte Register (BKA1L)		13h
Trigger 2 Address Middle Byte Register (BKA1M)		14h
Trigger 2 Address High Byte Register (BKA1H)		15h
Trigger 3 Address Low Byte Register (BKA1L)		16h
Trigger 3 Address Middle Byte Register (BKA1M)		17h
Trigger 3 Address High Byte Register (BKA1H)		18h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”.

7.20.4.1 Trigger 1 Address Low Byte Register (BKA1L)

Address Offset: 10h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 1 Address (BK1A7-0)**

7.20.4.2 Trigger 1 Address Middle Byte Register (BKA1M)

Address Offset: 11h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 1 Address (BK1A15-8)**

7.20.4.3 Trigger 1 Address High Byte Register (BKA1H)

Address Offset: 12h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	W	00b	**Trigger 1 Address (BK1A17-16)**

7.20.4.4 Trigger 2 Address Low Byte Register (BKA2L)

Address Offset: 13h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 2 Address (BK2A7-0)**

7.20.4.5 Trigger 2 Address Middle Byte Register (BKA2M)

Address Offset: 14h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 2 Address (BK2A15-8)**

7.20.4.6 Trigger 2 Address High Byte Register (BKA2H)

Address Offset: 15h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	W	00b	**Trigger 2 Address (BK2A17-16)**

7.20.4.7 Trigger 3 Address Low Byte Register (BKA3L)

Address Offset: 16h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 3 Address (BK3A7-0)**

7.20.4.8 Trigger 3 Address Middle Byte Register (BKA3M)

Address Offset: 17h

Bit	R/W	Default	Description
7-0	W	00h	**Trigger 3 Address (BK3A15-8)**

7.20.4.9 Trigger 3 Address High Byte Register (BKA3H)

Address Offset: 18h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1-0	W	00b	**Trigger 3 Address (BK3A17-16)**

7.21 Parallel Port (PP)

7.21.1 Overview

IT8502 supports IEEE 1284 parallel port interface to allow in-system programming regardless of running firmware code.

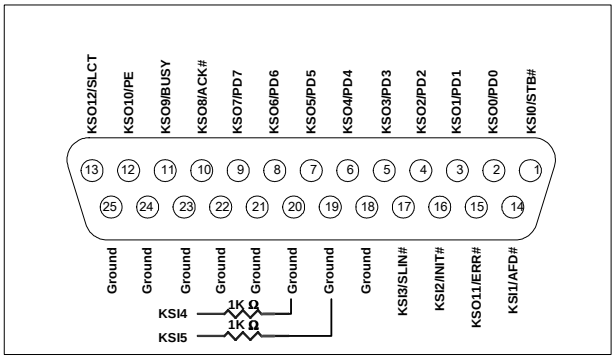
7.21.2 Features

- ISP via parallel port interface on existed KBS connector
- Fast flash programming with software provided by ITE
- Programming software supports EPP/SPP mode

7.21.3 Functional Description

7.21.3.1 KBS Connection with Parallel Port Connector

Figure 7-44. Parallel Port Female 25-Pin Connector



7.21.3.2 In-System Programming Operation

In-system programming takes place when VSTBY is supplied (other power is don't-care) and both EC chip and the flash are soldered on PCB. Parallel port interface occupies the same interface pins as KBS to use the existing KBS connector.

IT8502 enters in-system programming mode if it detects parallel port signals when VSTBY power on pulled high. It can be disabled by OVRPPK/OVRPPEN bit in the KSICTRLR register

If Parallel Port cable is detected by internal hardware strap, the following functions will be disabled.

1. ROM Address Match Interrupt
2. Internal/External Watchdog

8. Register List

9. DC Characteristics

Operating Conditions

VSTBY/VCC……. .....3.3V±0.3V
AVCC……. .....3.3V±0.15V
VBAT…….....2.3V to 3.3V
Operating Temperature (Ta) ..... -25°C to +85°C

Absolute Maximum Ratings

Applied Voltage of VSTBY, VCC, AVCC, VBAT…….....-0.3V to +3.6V
Input Voltage of 3.3V Interface..... -0.3V to VCC+0.3V
Storage Temperature..... -40°C to +125°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
V_{IL}	Input Low Voltage	-0.3V	—	VCC x 0.3	VCC=3.0 - 3.6V
V_{IH}	Input High Voltage	VCC x 0.7	—	VCC+ 0.3V	VCC=3.0 - 3.6V
V_{IH}	Input High Voltage (5V tolerant pad)	VCC x 0.7	—	6.3V	VCC=3.0 - 3.6V
V_{OL}	Output Low Voltage	—	—	0.4	I_{OL}= -2, -4, -6, -8mA
V_{OH}	Output High Voltage	2.4	—	—	I_{OH}= 2, 4, 6, 8mA
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.9	1.2	—	
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—	2.1	2.5	
I_{IL}	Input leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	40KΩ	75KΩ	190KΩ	V_I= 0V
R_{pd}	Input Pull-Down resistance	40KΩ	75KΩ	190KΩ	V_I= VCC
Cin	Input Capacitance	—	2.8pF	—	
Cout	Output Capacitance	2.7pF	—	4.9pF	
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	

Table 9-1. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
I_{SLEEP}	VSTBY supply current	—	250 μA	—	Internal pull are disabled VIL = GND VIH = VSTBY No load
I_{BAT}	VBAT supply current	—	TBD	TBD	VSTBY and VCC are not supplied

10. AC Characteristics

Figure 10-1. VSTBY Power-on Reset Timing

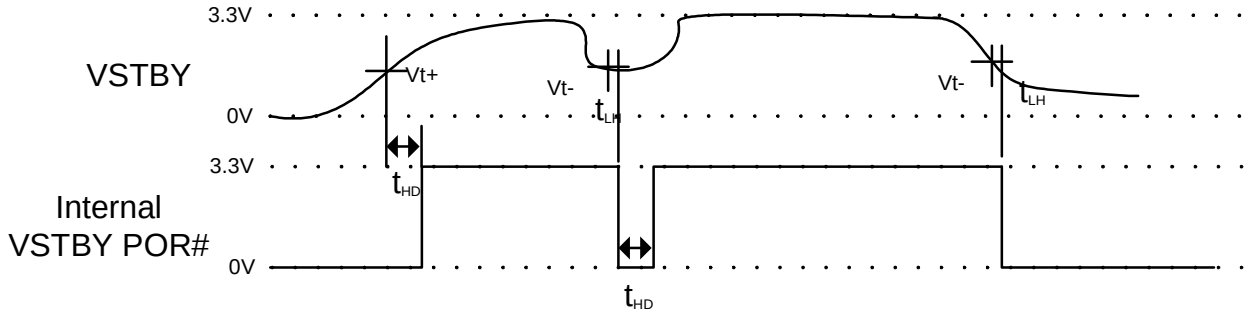


Table 10-1. VSTBY Power-on Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vt+	Level Detection Positive Going Threshold Voltage	—	2.89	—	V
Vt-	Level Detection Negative Going Threshold Voltage	—	2.65	—	V
t_{HD}	Internal VSTBY POR Going High Delay	—	500	—	µs
t_{LH}	Minimum Hold Time after VSTBY < Vt- and before Internal VSTBY POR Going Low	—	10	—	µs

Figure 10-2. Reset Timing

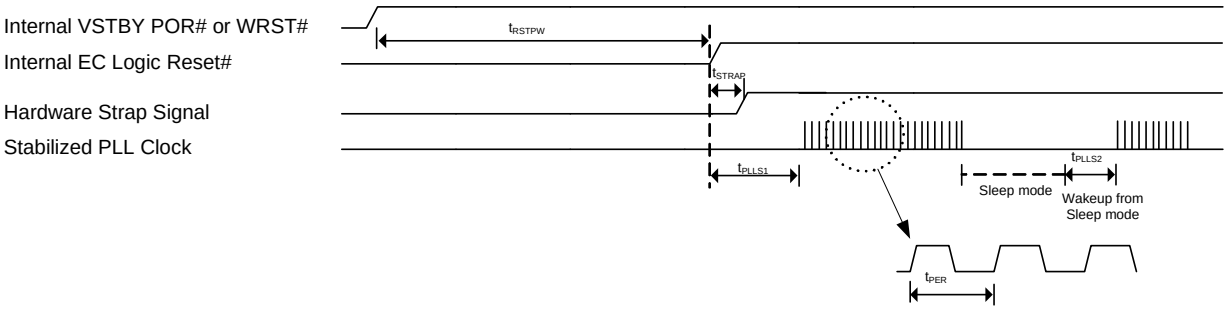


Table 10-2. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 kHz)
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t_{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t_{PER}	PLL clock period	—	$1/_{FreqPLL}$	—	ns
FreqPLL	PLL clock frequency if PLLFREQ = 0011b	—	32.3	—	MHz
	PLL clock frequency if PLLFREQ = 0101b	—	46.0	—	MHz
	PLL clock frequency if PLLFREQ = 0111b	—	64.5	—	MHz
FreqEC	EC clock frequency	—	9.2	—	MHz

Figure 10-3. Warm Reset Timing

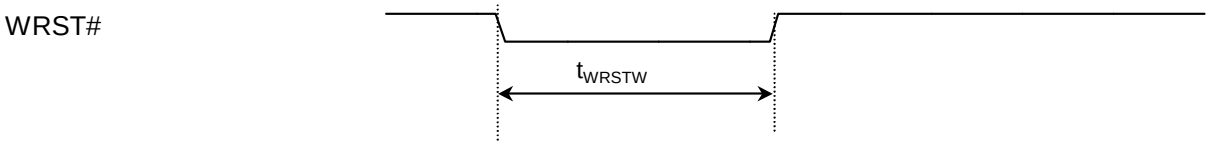


Table 10-3. Warm Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	µs

Figure 10-4. Wakeup from Doze Mode Timing

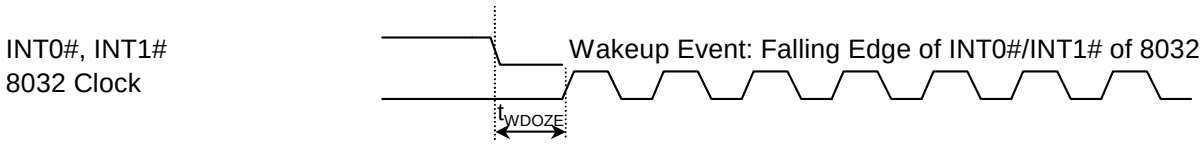


Table 10-4. Wakeup from Doze Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDOZE}	Doze wakeup time from falling edge of INT0#/INT1# to rising edge of first 8032 clock.	—	—	2 / (EC Clock Freq)	—

Figure 10-5. Wake Up from Sleep Mode Timing

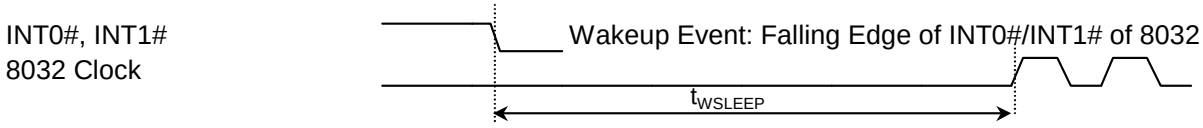


Table 10-5. Wake Up from Sleep Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WSLEEP}	Sleep wakeup time from falling edge of INT0#/INT1# to rising edge of first 8032 clock.	—	—	4.2	ms

Figure 10-6. Asynchronous External Wakeup/Interrupt Source Edge Detected Timing

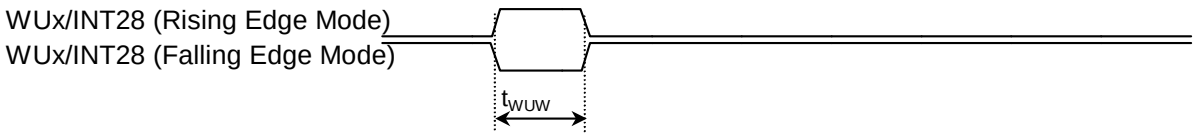


Table 10-6. Asynchronous External Wakeup/Interrupt Source Edge Detected AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{wuw}	Wakeup source pulse width	—	1	—	ns

Figure 10-7. LPC and SERIRQ Timing

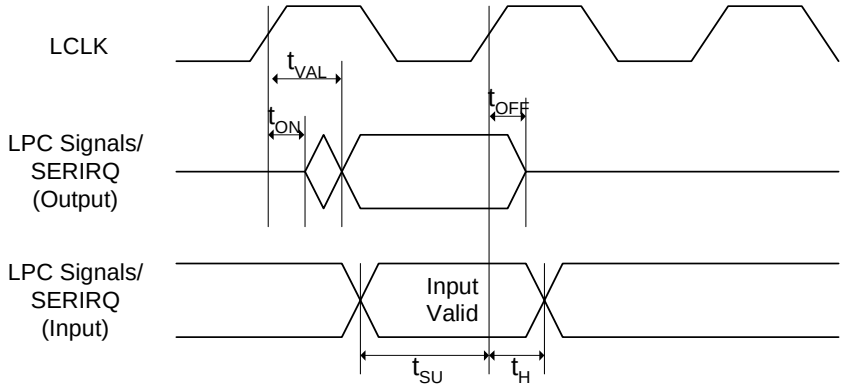


Table 10-7. LPC and SERIRQ AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ON}	Float to Active Delay	3	—	—	ns
t_{VAL}	Output Valid Delay	—	—	12	ns
t_{OFF}	Active to Float Delay	—	—	20	ns
t_{SU}	Input Setup Time	7	—	—	ns
t_H	Input Hold Time	0	—	—	ns

Figure 10-8. SWUC Wake Up Timing

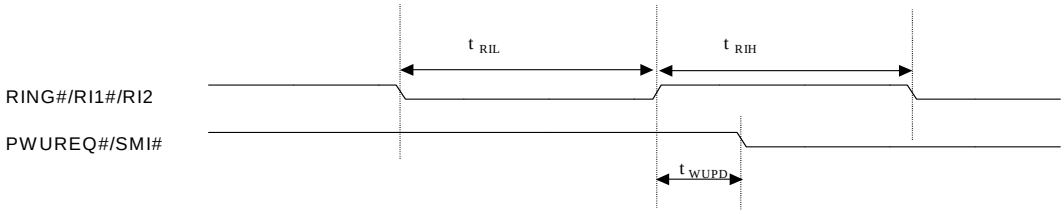


Table 10-8. SWUC Wake Up AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RIL}	RING#, RI1# , RI2# Low Time	10	—	—	ns
t_{RIh}	RING#, RI1# , RI2# High Time	10	—	—	ns
t_{WUPD}	Wake Up propagation delay time	—	20	—	ns

Figure 10-9. Serial Flash (FSPI) Cycle Timing

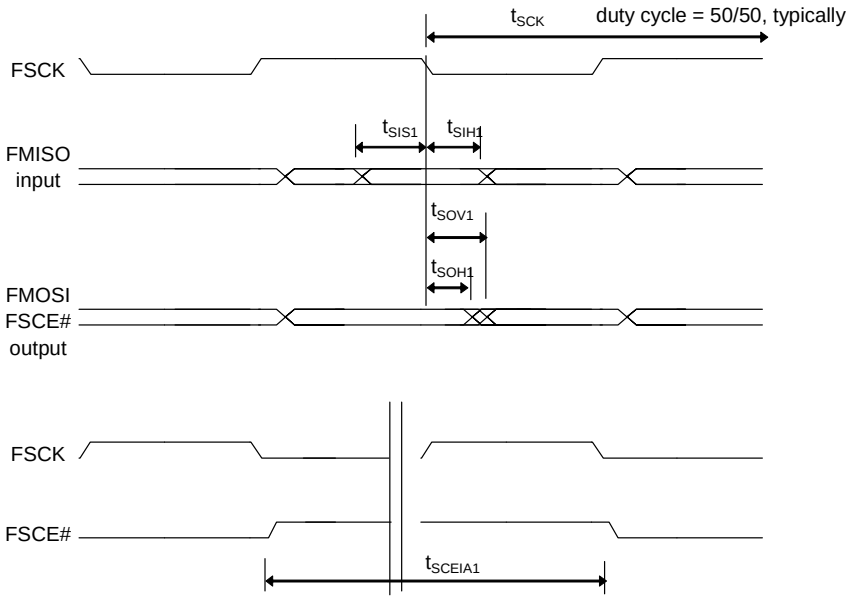


Table 10-9. Serial Flash (FSPI) Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCK}	FSCK period	—	$1/_{FreqPLL}$	—	ns
t_{SIS1}	Input setup time	3	—	—	ns
t_{SIH1}	Input hold time	3	—	—	ns
t_{SOV1}	Clock low to output valid	—	—	5	ns
t_{SOH1}	Output hold time	0	—	—	ns
t_{SCEIA1}	FSCE# high time	(SCEMINHW + 1) * t_{SCK}	—	—	ns

Figure 10-10. PWM Output Timing

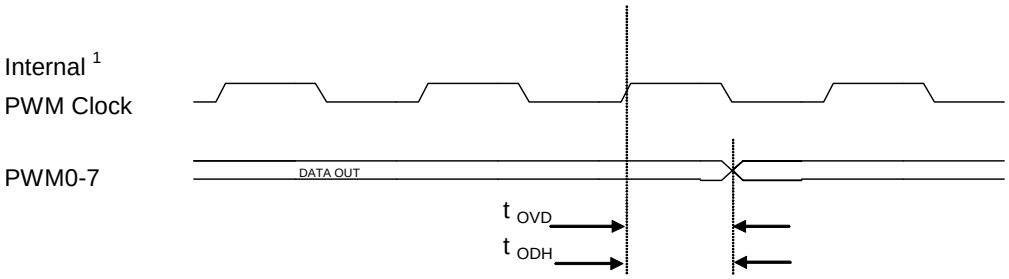


Table 10-10. PWM Output AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{OVD}	PWM output valid delay time	—	—	0.5	T^{NOTE1}
t_{ODH}	PWM output hold time	0	—	—	ns

Note 1: T is one time unit and its length is equal to the EC clock period X C0CPRS +1 (ns) for CH0~3, or X

C4CPRS +1 (ns) for CH4~7.

Figure 10-11. PMC SMI#/SCI# Timing

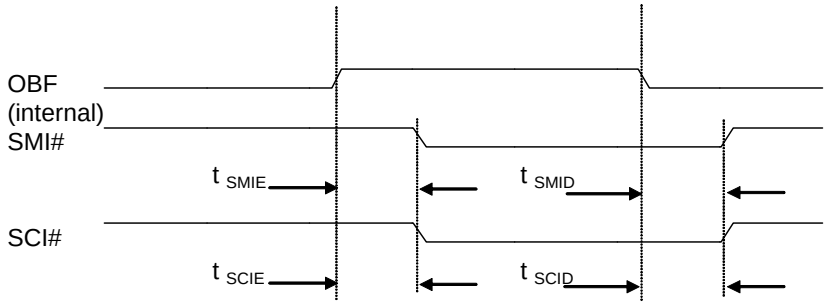


Table 10-11. PMC SMI#/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SMIE}	OBF asserted to SMI# asserted time	—	10	—	ns
t_{SMID}	OBF de-asserted to SMI# de-asserted time	—	5	—	ns
t_{SCIE}	OBF asserted to SCI# asserted time	—	10	—	ns
t_{SCID}	OBF de-asserted to SCI# de-asserted time	—	5	—	ns

Figure 10-12. PMC IBF/SCI# Timing

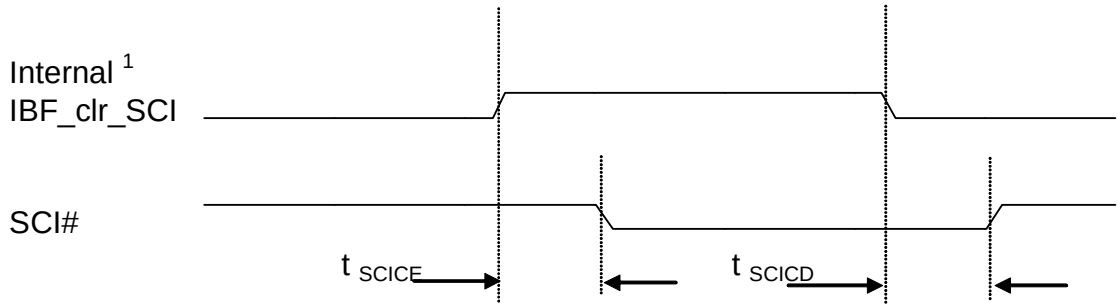


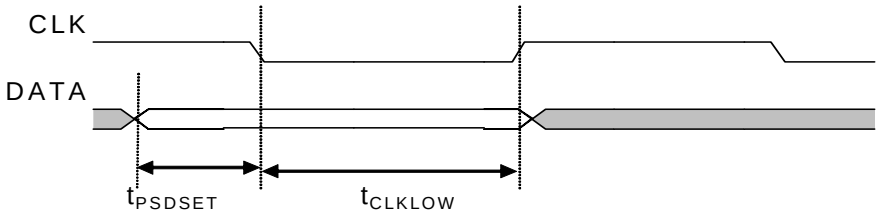
Table 10-12. PMC IBF/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCICE}	IBF_clr_SCI asserted to SCI# asserted time	—	70	—	ns
t_{SCICD}	IBF_clr_SCI de-asserted to SCI# de-asserted time	—	40	—	ns

Note 1: IBF_clr_SCI means the invert signal of IBF, IBF_clr_SCI set to one when EC read PMDI or PMDISCI.

Figure 10-13. PS/2 Receive/Transmit Timing

Receive:



Transmit:

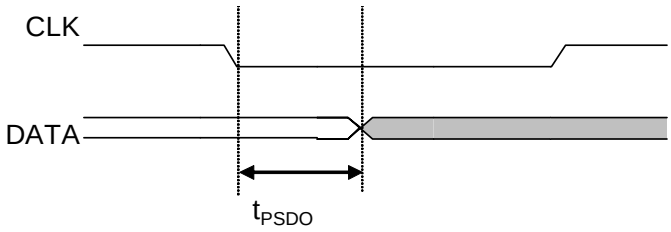


Table 10-13. PS/2 Receive/Transmit AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PSDSET}	DATA line input set up time	1	—	—	ns
t_{CLKLOW}	CLK line low time	1	—	—	µs
t_{PSDO}	DATA line output data time	—	—	1	µs

Figure 10-14. SMBus Timing

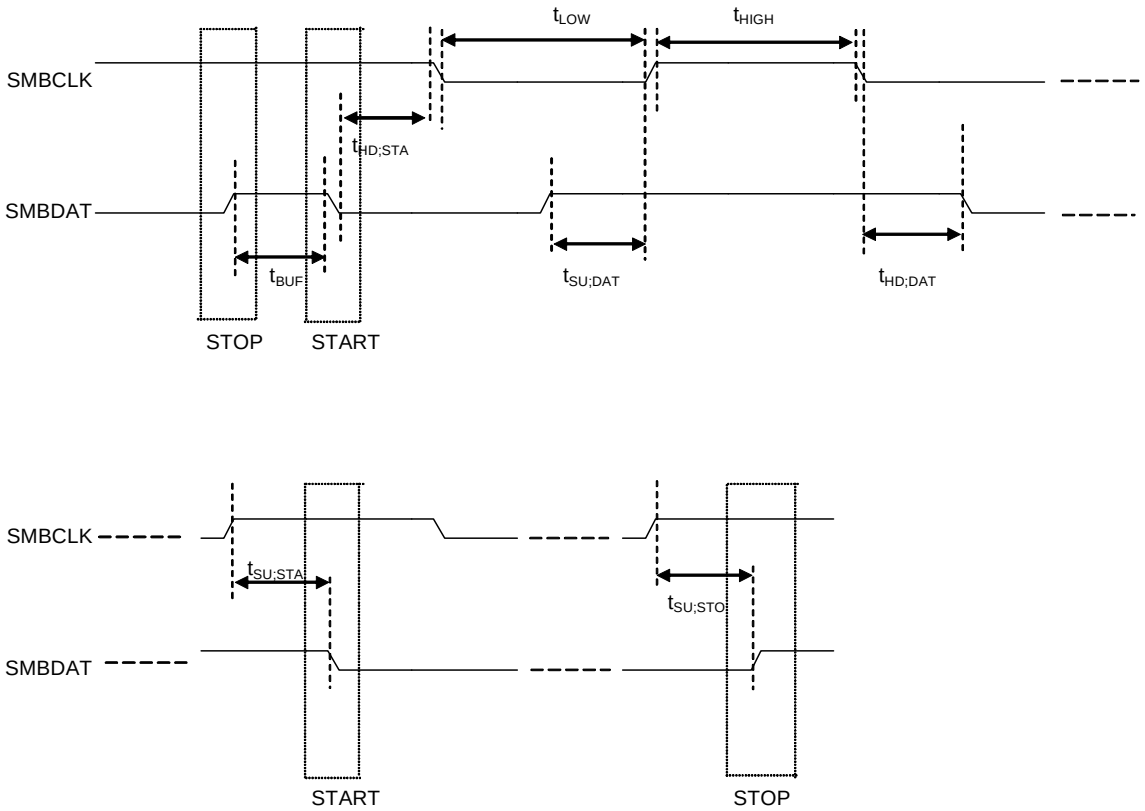
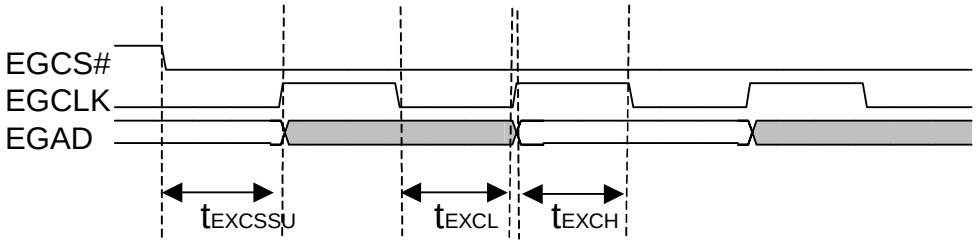


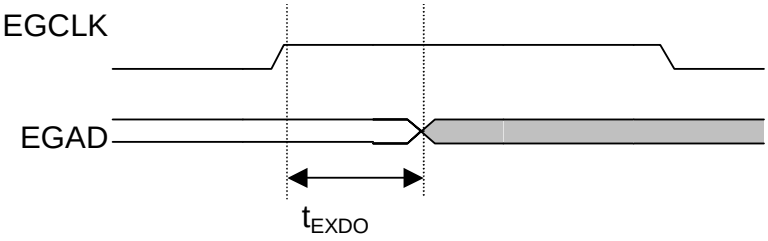
Table 10-14. SMBus AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Bus free time between Stop and Start condition	4.7	—	—	µs
$t_{HD;STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	4.0	—	—	µs
t_{LOW}	Clock low period	4.7	—	—	µs
t_{HIGH}	Clock high period	4.0	—	50	µs
$t_{SU;DAT}$	Data setup time	250	—	—	ns
$t_{HD;DAT}$	Data hold time	300	—	—	ns
$t_{SU;STA}$	Repeated Start condition setup time	4.7	—	—	µs
$t_{SU;STO}$	Stop condition setup time	4.0	—	—	µs

Figure 10-15. External GPIO Controller Data Timing



Transmit:



Receive:

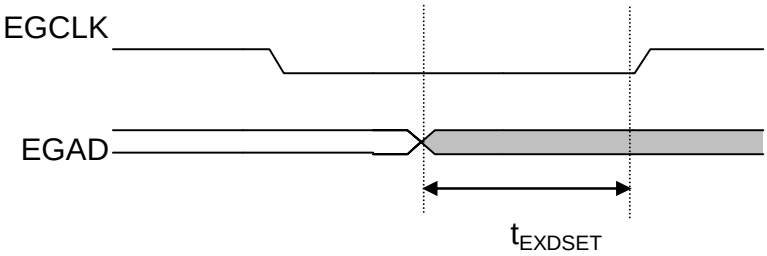


Table 10-15. External GPIO Controller Interface AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{EXCSSU}	EGCS# line input set up time	30	—	—	ns
t_{EXCL}	EGCLK line low time	—	1/FreqEC	—	ns
t_{EXCH}	EGCLK line high time	—	1/FreqEC	—	ns
t_{EXDO}	EGAD line output data time	—	—	50	ns
t_{EXDSET}	EGAD line input set up time	1	—	—	ns

Figure 10-16. Serial Peripheral Interface (SSPI) Timing

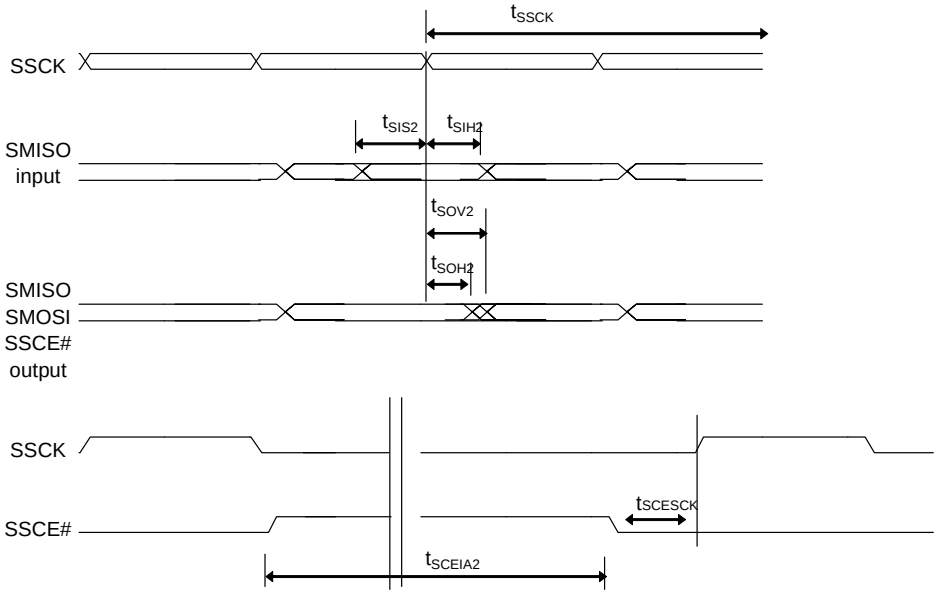


Table 10-16. Serial Peripheral Interface (SSPI) AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SSCK}	SSCK period	2/ FreqEC	—	16/ FreqEC	ns
t_{SIS2}	Input setup time	5	—	—	ns
t_{SIH2}	Input hold time	5	—	—	ns
t_{SOV2}	Clock edge to output valid	—	—	5	ns
t_{SOH2}	Output hold time	0	—	—	ns
t_{SCEIA2}	SSCE# inactive time	1/ FreqEC	—	—	ns
$t_{SCESSCK}$	From SSCE# active edge to first SSCK active edge	—	2/ FreqEC	—	ns

Figure 10-17. Serial Port (UART) Timing

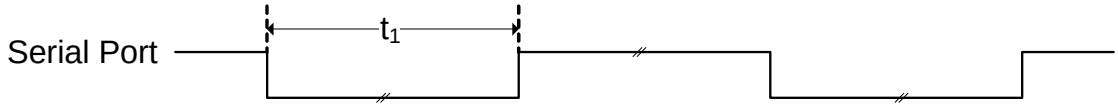


Table 10-17. Serial Port (UART) AC Table

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in UART	Transmitter	t_{BTN} – Tclk Note1	t_{BTN} + Tclk Note1	ns
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	ns

Note 1: tBTN is the nominal bit time in Serial Port (UART). It is determined by setting the Baud Rate Divisor registers. Tclk equals to 1/ FreqEC.Tclk equals to 1/ FreqEC.

11. Analog Device Characteristics

Table 11-1. ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Resolution	—	—	10	—	Bit
Integral Non-linearity Error (INL)	ADC0-9	—	—	±4	LSB
Differential Non-linearity Error (DNL)	ADC0-9	—	—	±4	LSB
Offset Error	ADC0-9	—	—	±4	LSB
Gain Error	ADC0-9	—	—	±4	LSB
External Input Accuracy	ADC0-9	—	—	±4	LSB
ADC Input Voltage Range	—	0	—	3	V
ADC Input Leakage Current	ADC0-9: 0 ≦ Vin ≦ AVCC	—	±1	—	μA
ADC Input Resistance	—	4	—	—	MΩ
ADC Input Capacitance	—	—	—	8	pF
ADC Clock Frequency	—	—	0.5	—	MHz
Voltage Conversion Delay	—	16	512	1000	μs
Voltage Conversion Time	—	—	3.6	—	ms

Note: This table is for “FIR filter enabled, high accuracy” configuration only.

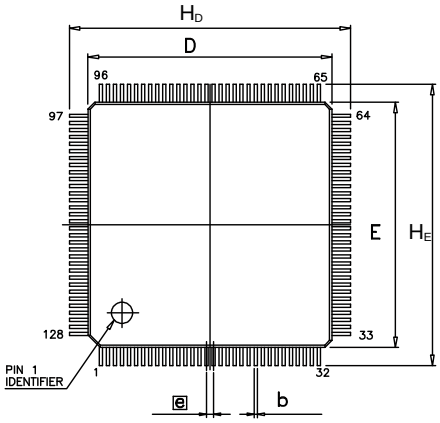
Table 11-2. DAC Characteristics

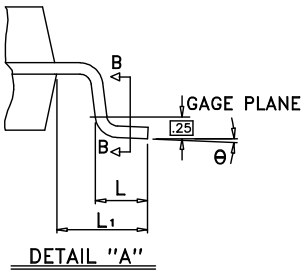
Parameter	Condition	Min.	Typ.	Max.	Unit
Resolution	—	—	8	—	Bit
Integral Non-linearity Error (INL)	AVCC = 3.3V	—	—	±1	LSB
Differential Non-linearity Error (DNL)	AVCC = 3.3V	—	—	±1	LSB
Offset Error	AVCC = 3.3V	—	—	±1	LSB
Gain Error	AVCC = 3.3V	—	—	±1	LSB
DAC Output Voltage Range	—	0	—	AVCC	V
DAC settling time	C_{load} = 50pF	—	—	1	μs
DAC Output Resistance	0 ≦ Vout ≦ AVCC	3	—	800	Ω
DAC Output Capacitance	—	—	6.5	—	pF

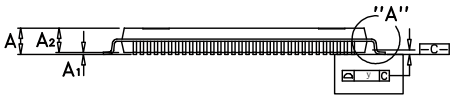
Note: C_{load} = (DAC Output Capacitance) + (External Load Capacitance)

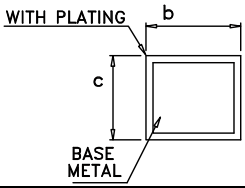
12. Package Information

LQFP 128L Outline Dimensions unit: inches/mm









Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A_1	0.002	-	-	0.05	-	-
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.547	0.551	0.555	13.90	14.00	14.10
e	0.016 BSC			0.40 BSC		
H_D	0.624	0.630	0.636	15.85	16.00	16.15
H_E	0.624	0.630	0.636	15.85	16.00	16.15
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1. Dimensions D and E do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
   Total in excess of the b dimension at maximum material condition.
   Dambar cannot be located on the lower radius of the foot.
3. Controlling dimension : Millimeter
4. Reference document : JEDEC MS-026

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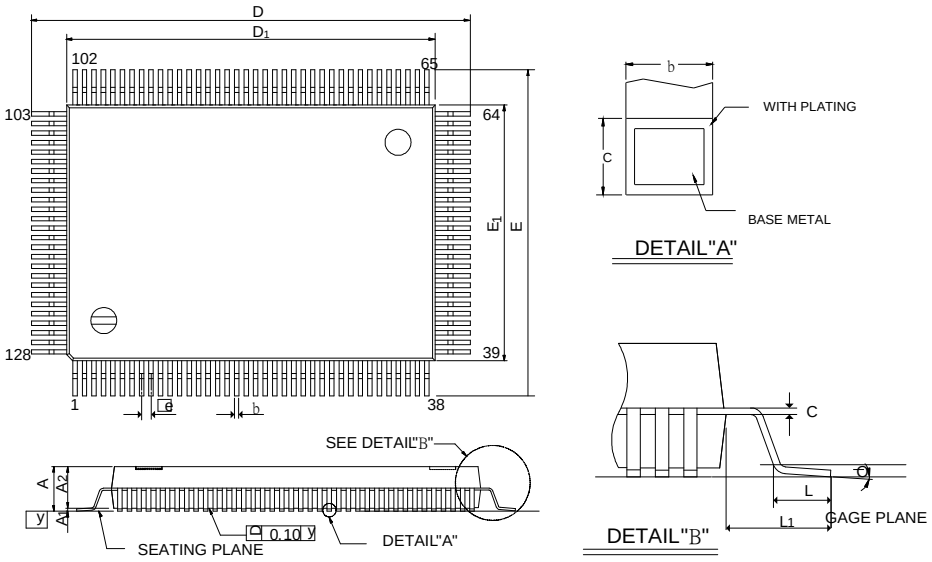
QFP 128L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.25	-	-
A_2	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.50 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

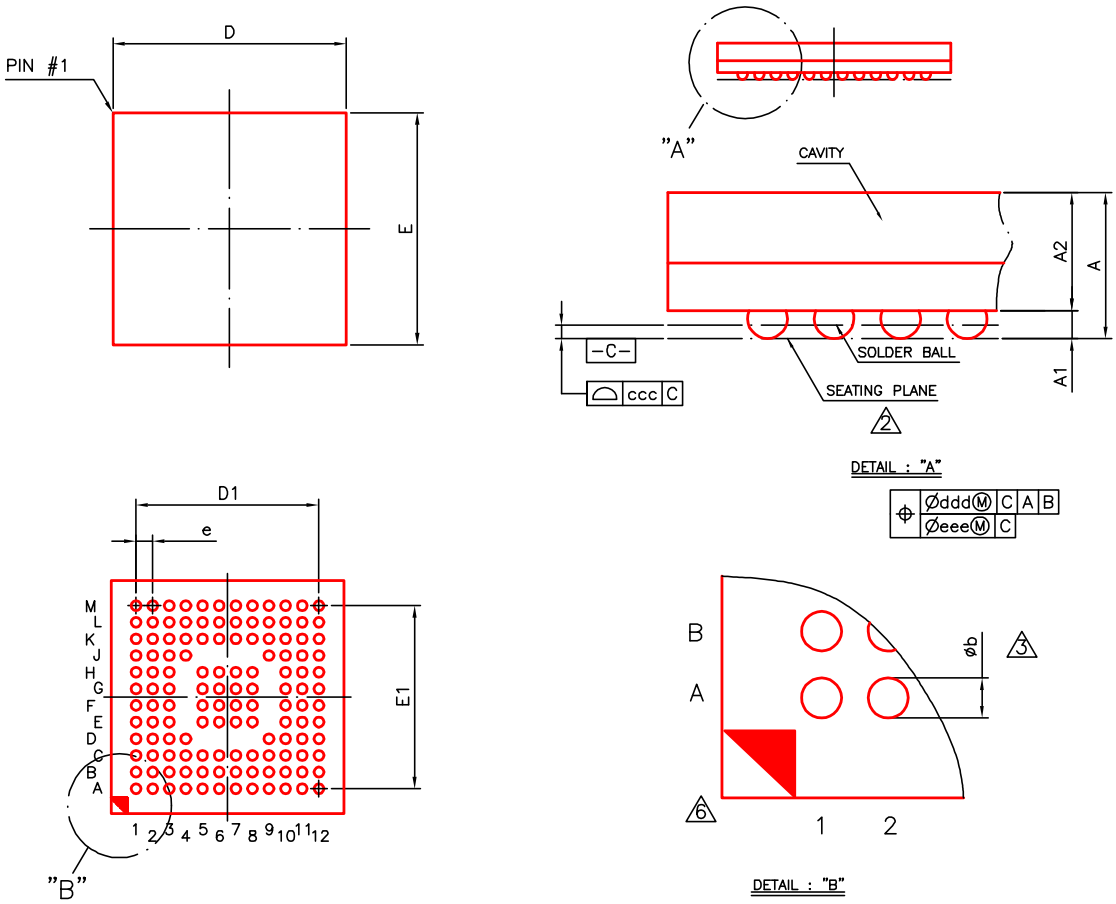
Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion. But mold mismatch is included
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension : Millimeter

DI-QFP128(14*20)v2

TFBGA 128 Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	--	--	0.047	--	--	1.20
A_1	0.006	0.008	0.010	0.16	0.21	0.26
A_2	0.033	0.035	0.037	0.84	0.89	0.94
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
D1	--	0.217	--	--	5.50	--
E1	--	0.217	--	--	5.50	--
e	--	0.020	--	--	0.50	--
b	0.010	0.012	0.014	0.25	0.30	0.35
ccc	0.003			0.08		
ddd	0.006			0.15		
eee	0.003			0.08		
MD/ME	12/12			12/12		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-207
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

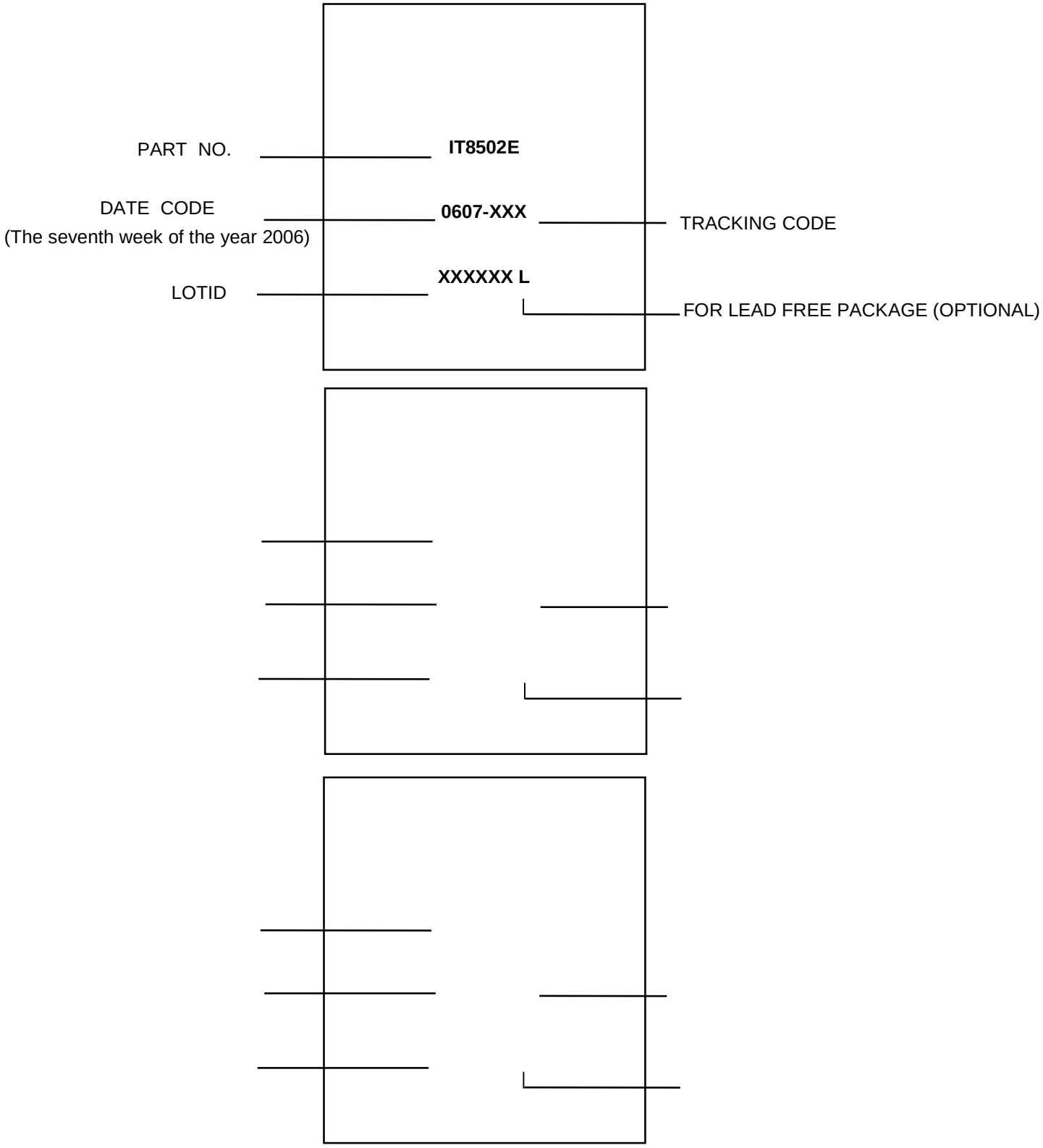
DI-TFBGA128(7*7)v0

13. Ordering Information

Part No.	Package
IT8502E	LQFP 128L
IT8502F	QFP 128L
IT8502G	TFBGA 128

ITE also provides RoHS compliant component. Please mark "-L" at the end of the Part No. when the parts ordered are RoHS compliant.

14. Top Marking Information



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2005)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.

(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.

(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.

(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.

(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).

(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.

(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.

(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.

(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.

(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.

(c) Buyer will not return any goods without first obtaining a customer return order number.

(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.

(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.

(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.