聯陽半導體
ITE Tech. Inc.

IT8510E/TE/G

Embedded Controller

Preliminary Specification 0.7.2

ITE TECH. INC.

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Revision History

Section	Revision	Page No.
6	• In section 6.2.2.4, the value of Chip Version (CHIPVER) was changed.	48
6	• In section 6.3.4.1 FBIU Configuration Register (FBCFG), OVRSHBM and OVRBADDR fields were added.	76
6	• In section 6.3.4.2 Flash Programming Configuration Register (FPCFG), HSPD field was added.	77
7	• In section 7.4.3.5 Keyboard Scan In Control Register (KSICTRLR), OVRPPEN field was added.	174
7	• In section 7.5.3.1 General Control Register (GCR), GFLE field was added.	176
7	• In section 7.11.4.5 Prescaler Clock Frequency Select Register (PCFSR), its table was revised.	222
7	• In section 7.14.4.10, Chip Version (ECHIPVER) was added	247
4, 11	• TFBGA package information was added.	263
12	• In section 12 Ordering Information, lead-free information was added.	267

CONTENTS

FIGURES

TABLES

1. Features

- **8032 Embedded Controller**
  - Twin Turbo version
  - 1 instruction at 1 machine cycle
  - Maximum 10 MHz for EC domain and 8032
  - Instruction set compatible with standard 8051

- **LPC Bus Interface**
  - Compatible with the LPC specification v1.1
  - Supports I/O read/write
  - Supports Memory read/write
  - Supports FWH read/write
  - Serial IRQ

- **External Flash Interface**
  - Up to 4M bytes Flash space shared by the host and EC side
  - 8-bit data bus

- **SM Bus Controller**
  - SM Bus spec. 2.0
  - SM Bus host and slave

- **System Wake Up Control**
  - Modem RI# wake up
  - Telephone RING# wake up
  - IRQ/SMI routing

- **EC Wake Up Control**
  - 32 external/internal wake up events

- **Interrupt Controller**
  - 32 interrupt events to EC
  - Fixed priority

- **Timer / Watch Dog Timer**
  - 3 16-bit multi-function timers inside 8032, which is based on EC clock
  - 1 watch dog timer inside 8032, which is based on EC clock
  - 1 external timer in ETWD module, which is based on RTC clock
  - 1 external WDT in ETWD module, which is based on RTC clock

- **UART**
  - Full duplex UART

- **ACPI Power Management Channel**
  - 2 Power Management channels
  - Compatible and enhanced mode

- **RTC**
  - Supports 2 lockable memory areas
  - Supports power-switch circuit
  - Supports two alarms

- **GPIO**
  - Supports 71-bit GPIO
  - Programmable pull up/pull down
  - Schmitt trigger for input

- **KBC Interface**
  - 8042 style KBC interface
  - Legacy IRQ1 and IRQ12
  - Fast A20G and KB reset

- **ADC**
  - 14 ADC channels (10 external)
  - 10-bit ADC resolution (accuracy ±4LSB)
  - Digital filter for noise reduction
  - Conversion time for 14 channels within 100 ms

- **DAC**
  - 4 DAC channels
  - 8-bit DAC

- **PWM with SmartAuto Fan Control**
  - 8 PWM channels
  - SmartAuto Fan control
  - Base clock frequency is 32.768KHz
  - 2 Tachometers for measuring fan speed

- **PS/2 Interface**
  - 4 PS/2 interface
  - Hardware/Software mode selection

- **KB Matrix Scan**
  - Hardware keyboard scan
  - 16x8 keyboard matrix scan

- **In-System Programming**
  - ISP via parallel port interface on existing KBS connector
  - Fast flash programming with software provided by ITE

- **Power Consumption**
  - Standby with Sleep mode current: 50 μA

- **Package**
  - 176 pin LQFP

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2. General Description

The IT8510 is a highly integrated embedded controller with system functions suitable for mobile system applications. The IT8510 directly interfaces to the LPC bus and provides ACPI embedded controller function, keyboard controller (KBC) and matrix scan, external flash interface for system BIOS and EC code, PWM, ADC and SmartAuto Fan control for hardware monitor, PS/2 interface for external keyboard/mouse devices, RTC and system wake up functions for system power management. It also supports the external flash (or EPROM) to be shared by the host and EC side.

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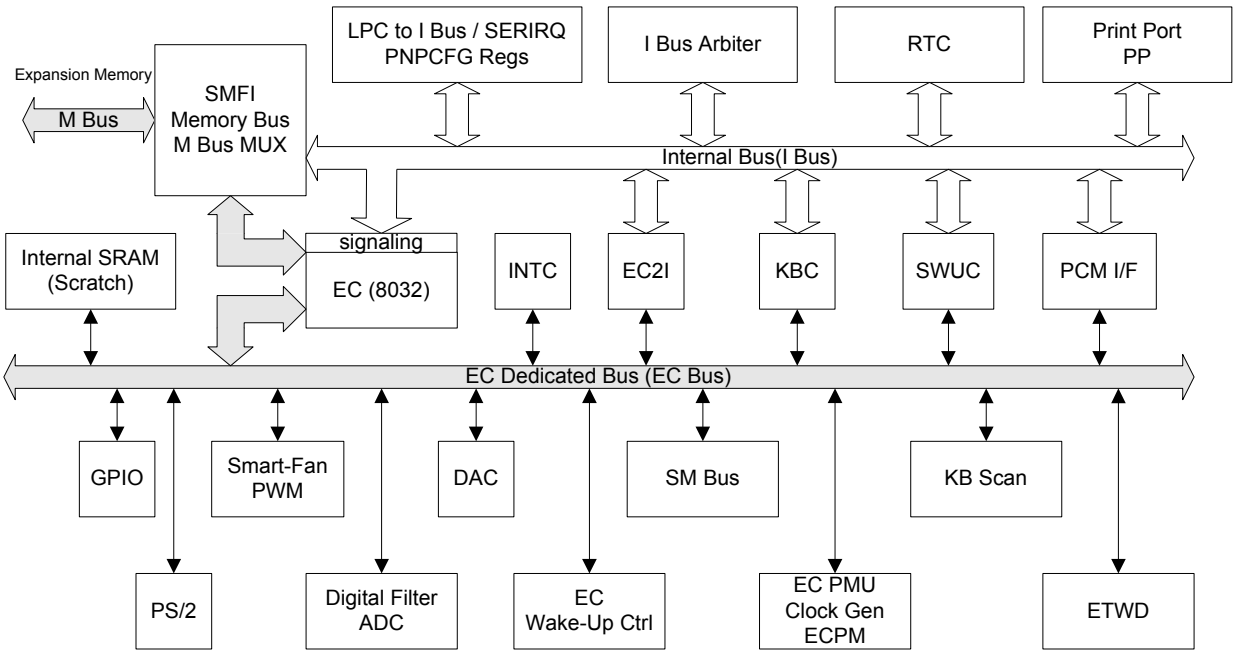
3. System Block Diagram

3.1 Block Diagram



- **Host Domain:**
  LPC, PNPCFG, RTC logic device, host parts of SMFI/SWUC/KBC/PMC logical devices and host parts of EC2I.
- **EC Domain:**
  EC 8032, INTC, WUC KB Scan, GPIO, ECPM, SMB, PS/2, DAC, ADC, PWM, HWS, ETWD, PP, EC2I, EC parts of SMFI/SWUC/KBC/PMC and EC parts of EC2I.

3.2 Host/EC Mapped Memory Space

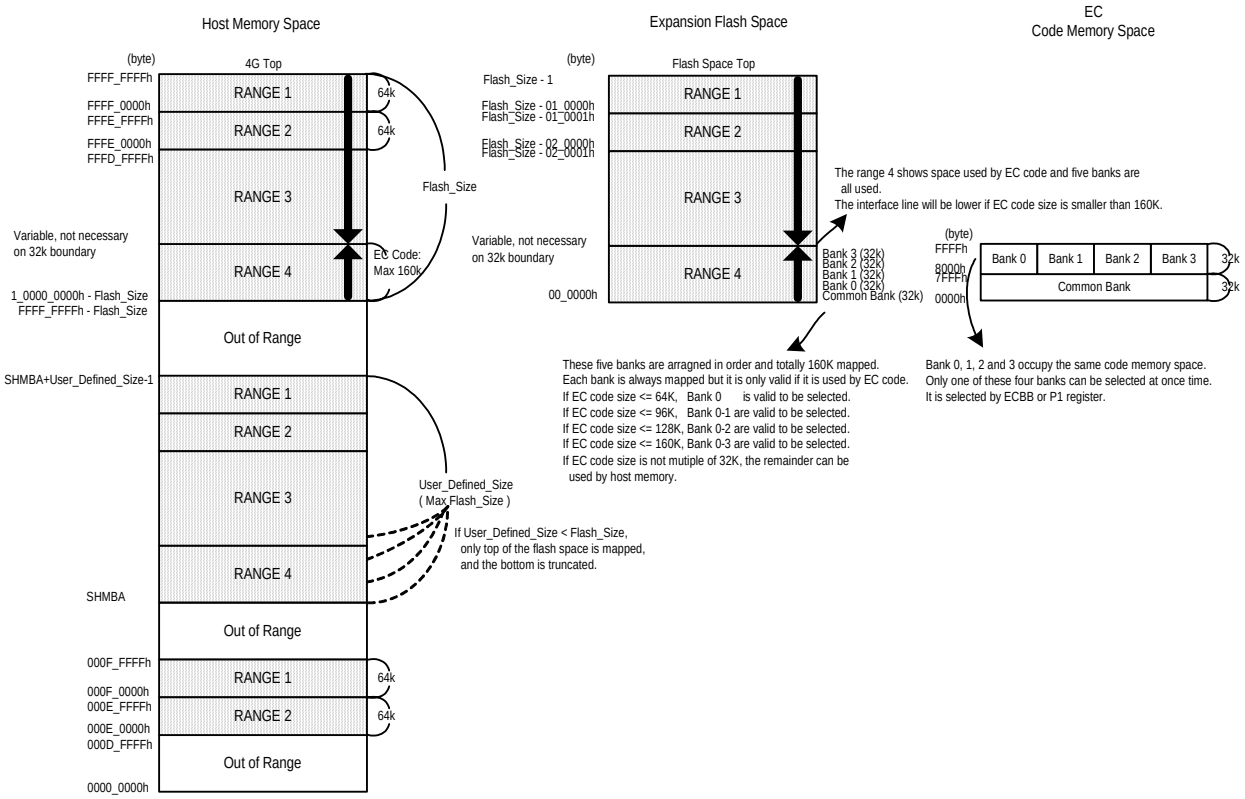


Figure 3-1. Host/Flash and EC/Flash Mapping (General)

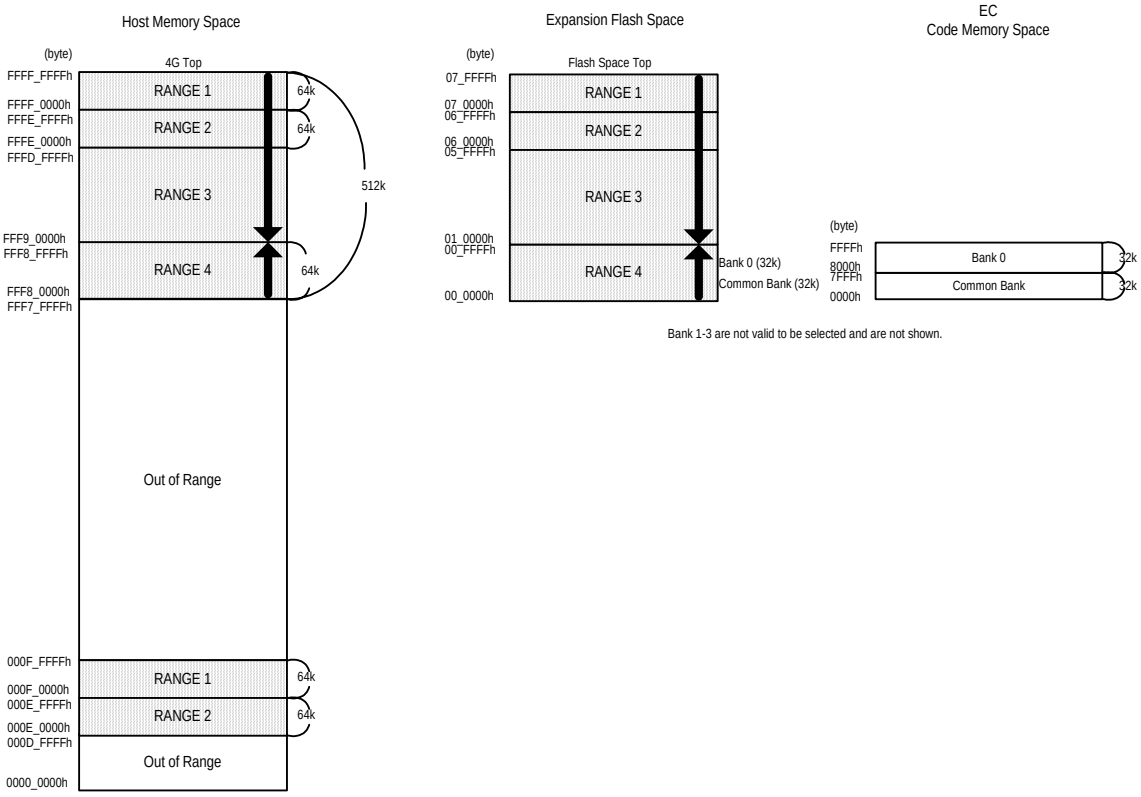


Figure 3-2. Host/Flash and EC/Flash Mapping (Flash Size = 512k, EC Code = 64k, No User-Defined, a specific example)

The flash memory space is shared between the host side and EC side, and it is shown in Figure 3-1. An example of 512k flash size, 64k EC code size and no user-defined is shown in Figure 3-2.

The host memory 4G byte top is always mapped into the top of flash space and the host processor fetches the first instruction after reset at FFFF_FFF0h in the host memory, which is 16 bytes below the uppermost flash space.

The bottom of EC code is always mapped into the bottom of flash space and EC R8032TT micro-controller fetches the first instruction after reset at 00_0000h in the EC code memory, which is 1 byte in the lowermost flash space.

The interface line of host memory and EC code is variable and not necessary on 32k boundary.

Table 3-1. Host/Flash Mapping

Host Memory Space on LPC Bus (byte)	Mapped Expansion Flash Space (byte)	Size (byte)	Mapping Condition
(1_0000_0000h–Flash_Size)~ FFFF_FFFFh	00_0000h~ (Flash_Size-1)	Flash_Size	Always
SHMBA ~ (SHMBA+User_Defined_Size-1)	(Flash_Size-User_Defined_Size)~ (Flash_Size-1)	User_Defined_Size (<= Flash_Size)	USRMEM=1
000F_0000h ~ 000F_FFFFh	(Flash_Size-01_0000h)~ (Flash_Size-1)	64k	Always
000E_0000h ~ 000E_FFFFh	(Flash_Size-02_0000h)~ (Flash_Size-01_0001h)	64k	BIOSEXTS=1
Note: The host side can map all flash range regardless of EC code space. Note: All host mappings are controlled by LPCMEN and FWHEN bit in SHMC register. Note: Flash Size is defined in FMSSR register, and it may be 128k, 256k, 512k, 1M, 2M and the maximum 4M bytes. Note: User_Defined_Size is defined in SHMUSZ register.			

Table 3-2. EC/Flash Mapping

EC Code Memory Space (byte)	Mapped Flash Address Range (byte)	Size (byte)	Mapping Condition	Bank Selected Condition
Bank 3: 8000h ~ FFFFh	02_0000h ~ 02_7FFFh	32k	Always	ECBB=11
Bank 2: 8000h ~ FFFFh	01_8000h ~ 01_FFFFh	32k	Always	ECBB=10
Bank 1: 8000h ~ FFFFh	01_0000h ~ 01_7FFFh	32k	Always	ECBB=01
Bank 0: 8000h ~ FFFFh	00_8000h ~ 00_FFFFh	32k	Always	ECBB=00
Common Bank: 0000h ~ 7FFFh	00_0000h ~ 00_7FFFh	32k	Always	Always
Note: EC code can use the maximum 160k by banking. **Note:** All EC code memory space is mapped to both EC and host side at the same time. The EC size is not necessary on 32k boundary. **Note:** If BSO=1, ECBB is replaced with P1 register of 8032. ECBB means ECBB field in FECBSR register. BSO means BSO bit in FPCFG register.				

Table 3-3. Flash Read/Write Protection Controlled by EC Side

Flash Address Range (byte)	Read Control Register Bits	Write Control Register Bits	Note
38_0000h ~ 3F_FFFFh	ORP56 ~ 63 in SMECORPR9	ORP56 ~ 63 in SMECOWPR9	Each bit controls 64K bytes
30_0000h ~ 37_FFFFh	ORP48 ~ 55 in SMECORPR8	ORP48 ~ 55 in SMECOWPR8	
28_0000h ~ 2F_FFFFh	ORP40 ~ 47 in SMECORPR7	ORP40 ~ 47 in SMECOWPR7	
20_0000h ~ 27_FFFFh	ORP32 ~ 39 in SMECORPR6	ORP32 ~ 39 in SMECOWPR6	
18_0000h ~ 1F_FFFFh	ORP24 ~ 31 in SMECORPR5	ORP24 ~ 31 in SMECOWPR5	
10_0000h ~ 17_FFFFh	ORP16 ~ 23 in SMECORPR4	ORP16 ~ 23 in SMECOWPR4	
08_0000h ~ 0F_FFFFh	ORP8 ~ 15 in SMECORPR3	ORP8 ~ 15 in SMECOWPR3	
02_0000h ~ 07_FFFFh	ORP2 ~ 7 in SMECORPR2	ORP2 ~ 7 in SMECOWPR2	
01_0000h ~ 01_FFFFh	ORPLA8~15 in SMECORPR1	ORPLA8 ~ 15 in SMECOWPR1	Each bit controls 8K bytes
00_0000h ~ 00_FFFFh	ORPLA0 ~ 7 in SMECORPR0	ORPLA0 ~ 7 in SMECOWPR0	
		All ranges are write-control by HOSTWA, too.	

Table 3-4. Flash Read/Write Protection Controlled by Host Side

Flash Address Range (byte)	Read Control Register Bits	Write Control Register Bits	Note
30_0000h ~ 3F_FFFFh	HRP in SMHAPR4	HRW in SMHAPR4	Each index controls 64K bytes
20_0000h ~ 2F_FFFFh	HRP in SMHAPR3	HRW in SMHAPR3	
10_0000h ~ 1F_FFFFh	HRP in SMHAPR2	HRW in SMHAPR2	
00_0000h ~ 0F_FFFFh	HRP in SMHAPR1	HRW in SMHAPR1	

3.3 EC Mapped Memory Space

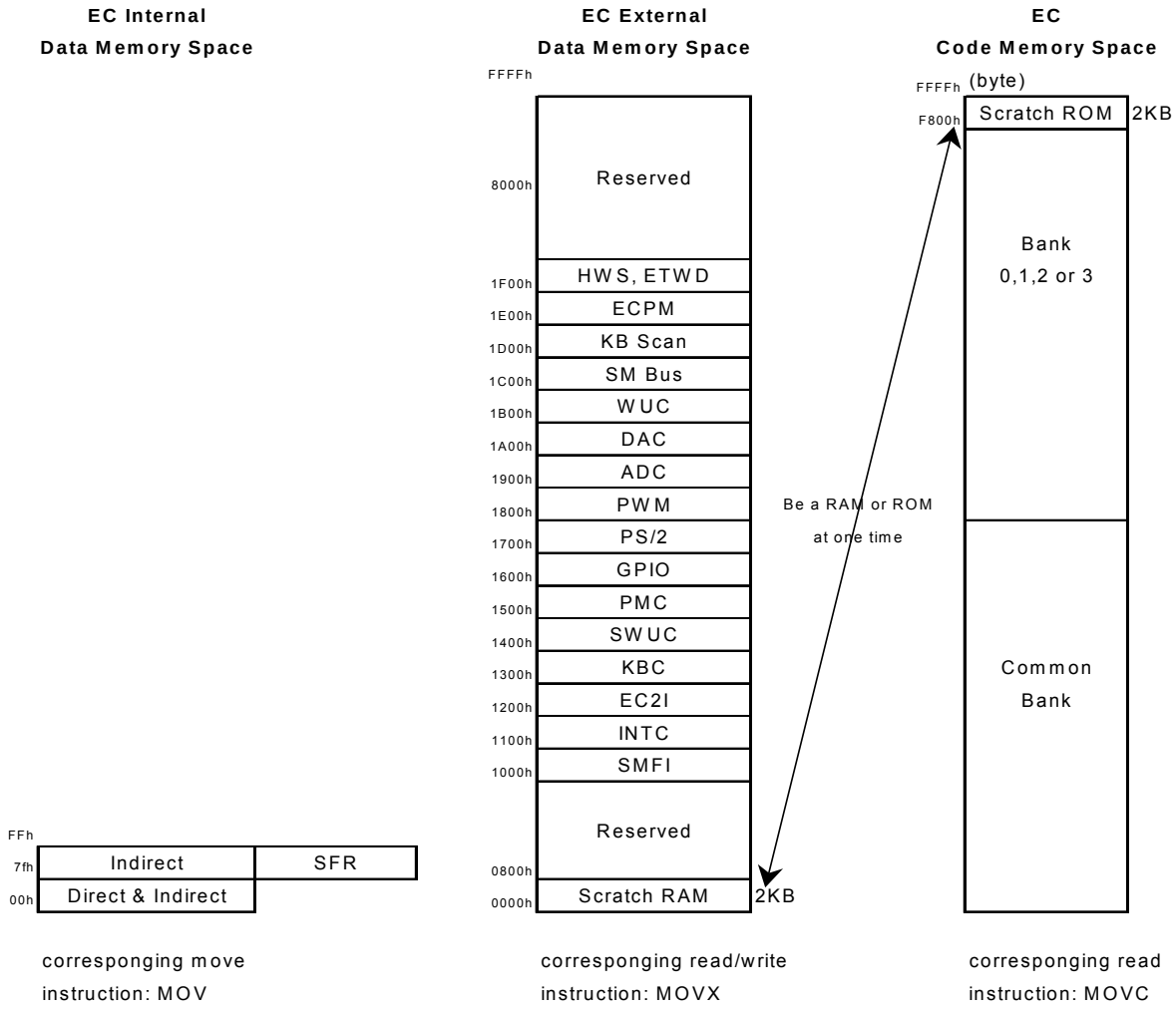


Figure 3-3. EC 8032 Data/Code Memory Map

There is an internal Scratch SRAM which can be located at data space or code space but cannot be located at both spaces at the same time. Where it is located depends on Scratch SRAM Map Control bit (SSMC) in FBCFG register. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.
The EC code space is 64k bytes and physically occupies the maximum 160 k bytes at the bottom of the flash space. Refer to Figure 3-1 on page 6 for the details.

3.4 Register Abbreviation

The register abbreviations and access rules are listed as follows:

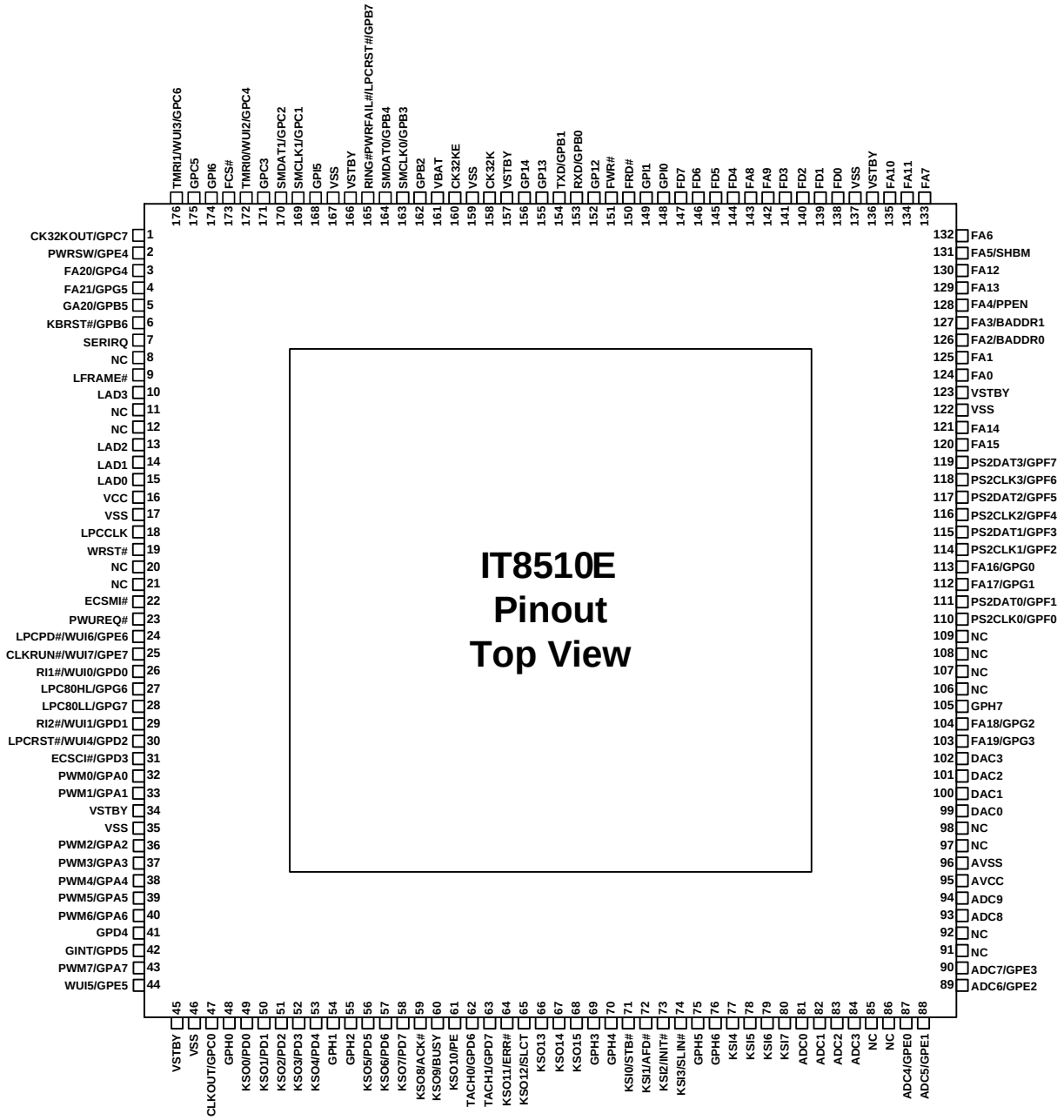
R **READ ONLY**. If a register is read only, writing to this register has no effect.
W **WRITE ONLY**. If a register is write only, reading to this register returns all zero.
R/W **READ/WRITE**. A register with this attribute can be read and written.
RC **READ CLEAR**. If a register is read clear, reading to this register clears the register to '0'.
R/WC **READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, writing 1 clears the corresponding bit and writing 0 has no effect.

BFNAME@REGNAME This abbreviation may be shown in figures to represent one bit in a register or one field in a register.

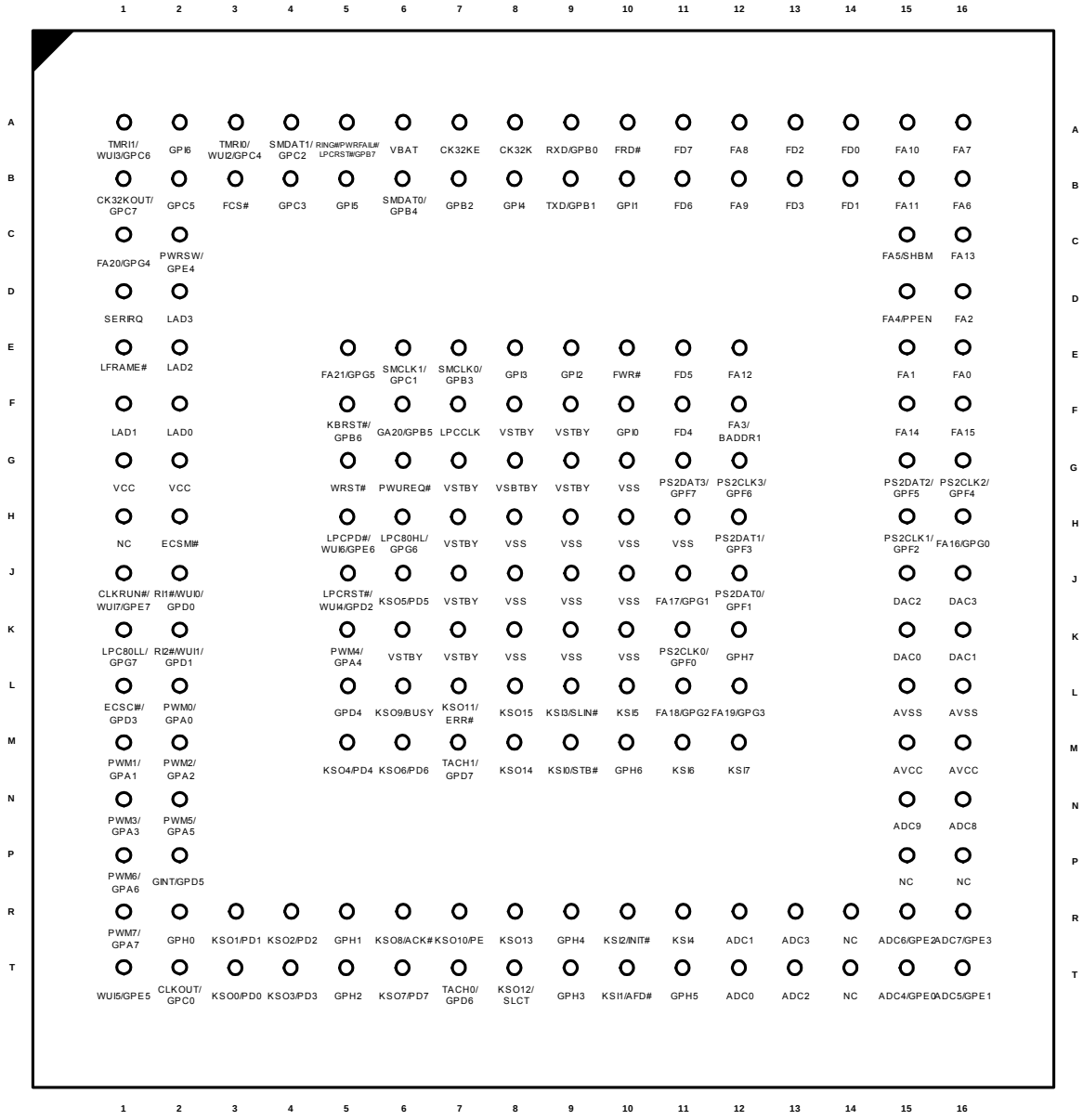
The used radix indicator suffixes in this specification are listed below

Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

4. Pin Configuration



IT8510G Top View



IT8510G Bottom View

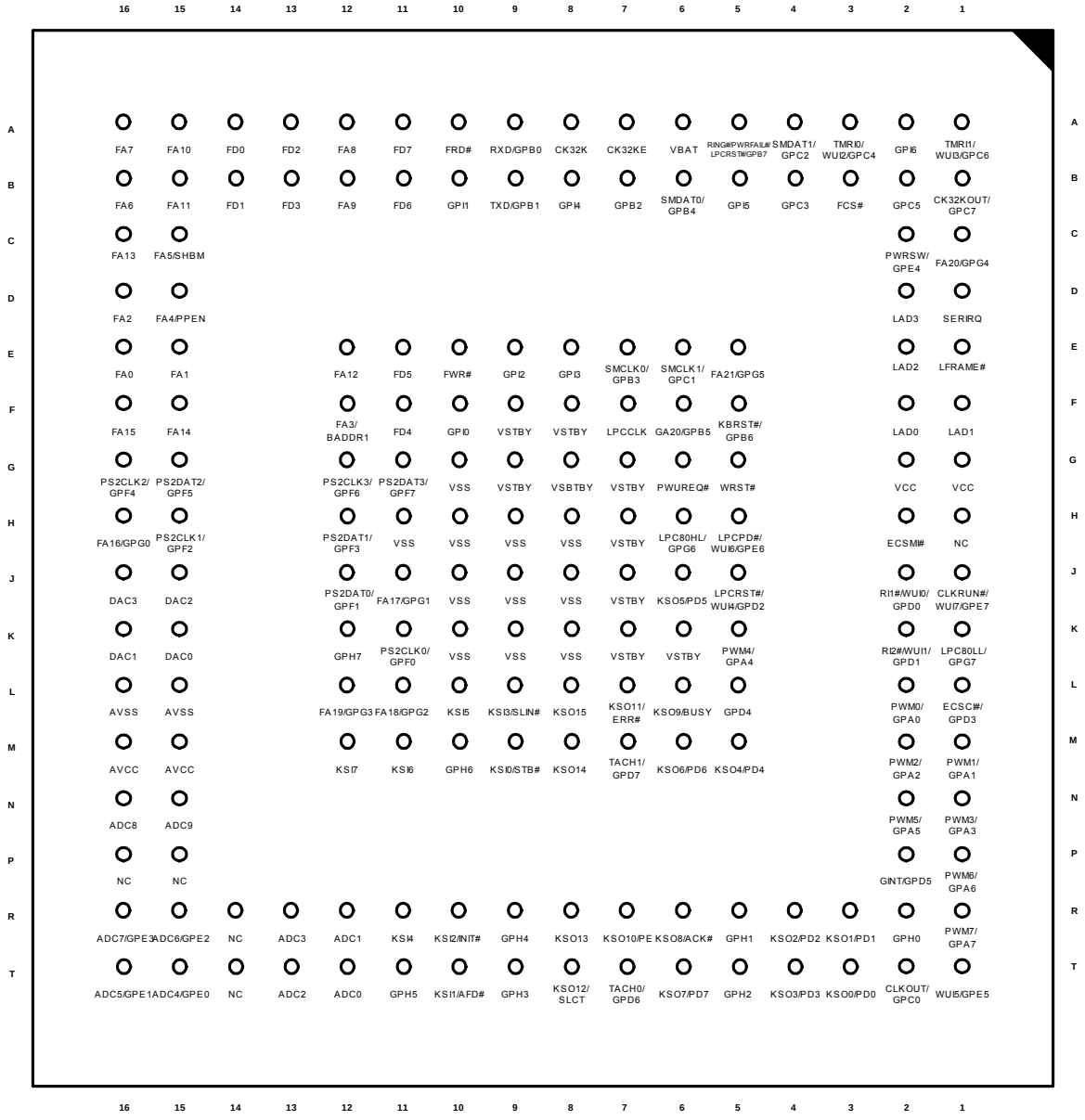


Table 4-1. Pins Listed in Numeric Order (176-pin LQFP)[u5]

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CK32KOUT/GPC7	45	VSTBY	89	ADC6/GPE2	133	FA7
2	PWRSW/GPE4	46	VSS	90	ADC7/GPE3	134	FA11
3	FA20/GPG4	47	CLKOUT/GPC0	91	NC	135	FA10
4	FA21/GPG5	48	GPH0	92	NC	136	VSTBY
5	GA20/GPB5	49	KSO0/PD0	93	ADC8	137	VSS
6	KBRST#/GPB6	50	KSO1/PD1	94	ADC9	138	FD0
7	SERIRQ	51	KSO2/PD2	95	AVCC	139	FD1
8	NC	52	KSO3/PD3	96	AVSS	140	FD2
9	LFRAME#	53	KSO4/PD4	97	NC	141	FD3
10	LAD3	54	GPH1	98	NC	142	FA9
11	NC	55	GPH2	99	DAC0	143	FA8
12	NC	56	KSO5/PD5	100	DAC1	144	FD4
13	LAD2	57	KSO6/PD6	101	DAC2	145	FD5
14	LAD1	58	KSO7/PD7	102	DAC3	146	FD6
15	LAD0	59	KSO8/ACK#	103	FA19/GPG3	147	FD7
16	VCC	60	KSO9/BUSY	104	FA18/GPG2	148	GPI0
17	VSS	61	KSO10/PE	105	GPH7	149	GPI1
18	LPCCLK	62	TACH0/GPD6	106	NC	150	FRD#
19	WRST#	63	TACH1/GPD7	107	NC	151	FWR#
20	NC	64	KSO11/ERR#	108	NC	152	GPI2
21	NC	65	KSO12/SLCT	109	NC	153	RXD/GPB0
22	ECSMI#	66	KSO13	110	PS2CLK0/GPF0	154	TXD/GPB1
23	PWUREQ#	67	KSO14	111	PS2DAT0/GPF1	155	GPI3
24	LPCPD#/WUI6/GPE6	68	KSO15	112	FA17/GPG1	156	GPI4
25	CLKRUN#/WUI7/GPE7	69	GPH3	113	FA16/GPG0	157	VSTBY
26	RI1#/WUI0/GPD0	70	GPH4	114	PS2CLK1/GPF2	158	CK32K
27	LPC80HL/GPG6	71	KSI0/STB#	115	PS2DAT1/GPF3	159	VSS
28	LPC80LL/GPG7	72	KSI1/AFD#	116	PS2CLK2/GPF4	160	CK32KE
29	RI2#/WUI1/GPD1	73	KSI2/INIT#	117	PS2DAT2/GPF5	161	VBAT
30	LPCRST#/WUI4/GPD2	74	KSI3/SLIN#	118	PS2CLK3/GPF6	162	GPB2
31	ECSCI#/GPD3	75	GPH5	119	PS2DAT3/GPF7	163	SMCLK0/GPB3
32	PWM0/GPA0	76	GPH6	120	FA15	164	SMDAT0/GPB4
33	PWM1/GPA1	77	KSI4	121	FA14	165	RING#/PWRFAIL#/LPCRST#/GPB7
34	VSTBY	78	KSI5	122	VSS	166	VSTBY
35	VSS	79	KSI6	123	VSTBY	167	VSS
36	PWM2/GPA2	80	KSI7	124	FA0	168	GPI5
37	PWM3/GPA3	81	ADC0	125	FA1	169	SMCLK1/GPC1
38	PWM4/GPA4	82	ADC1	126	FA2/BADDR0	170	SMDAT1/GPC2
39	PWM5/GPA5	83	ADC2	127	FA3/BADDR1	171	GPC3
40	PWM6/GPA6	84	ADC3	128	FA4/PPEN	172	TMRI0/WUI2/GPC4
41	GPD4	85	NC	129	FA13	173	FCS#
42	GINT/GPD5	86	NC	130	FA12	174	GPI6
43	PWM7/GPA7	87	ADC4/GPE0	131	FA5/SHBM	175	GPC5
44	WUI5/GPE5	88	ADC5/GPE1	132	FA6	176	TMRI1/WUI3/GPC6

Table 4-2. Pins Listed in Numeric Order (176-pin TFBGA)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	TMRI1/WUI3/GPC6	E15	FA1	J1	CLKRUN#/WUI7/GPE7	M6	KSO6/PD6
A10	FRD#	E16	FA0	J10	VSS	M7	TACH1/GPD7
A11	FD7	E2	LAD2	J11	FA17/GPG1	M8	KSO14
A12	FA8	E5	FA21/GPG5	J12	PS2DAT0/GPF1	M9	KSI0/STB#
A13	FD2	E6	SMCLK1/GPC1	J15	DAC2	N1	PWM3/GPA3
A14	FD0	E7	SMCLK0/GPB3	J16	DAC3	N15	ADC9
A15	FA10	E8	GPI3	J2	RI1#/WUI0/GOD0	N16	ADC8
A16	FA7	E9	GPI2	J5	LPCRST#/WUI4/GPD2	N2	PWM5/GPA5
A2	GPI6	F1	LAD1	J6	KSO5/PD5	P1	PWM6/GPA6
A3	TMRI0/WUI2/GPC4	F10	GPI0	J7	VSTBY	P15	NC
A4	SMDAT1/GPC2	F11	FD4	J8	VSS	P16	NC
A5	RING#/PWRFAIL/#/LPCRST#/GPB7	F12	FA3/BADDR1	J9	VSS	P2	GINT/GPD5
A6	VBAT	F15	FA14	K1	LPC80LL/GPG7	R1	PWM7/GPA7
A7	CK32KE	F16	FA15	K10	VSS	R10	KSI2/INT#
A8	CK32KE	F2	LAD0	K11	PS2CLK0/GPF0	R11	KSI4
A9	RXD/GPB0	F5	KBRST#/GPB6	K12	GPH7	R12	ADC1
B1	CK32KOUT/GPC7	F6	GA20/GPB5	K15	DAC0	R13	ADC3
B10	GPI1	F7	LPCCLK	K16	DAC1	R14	NC
B11	FD6	F8	VSTBY	K2	RI2#/WUI1/GPD1	R15	ADC6/GPE2
B12	FA9	F9	VSTBY	K5	PWM4/GPA4	R16	ADC7/GPE3
B13	FD3	G1	VCC	K6	VSTBY	R2	GPH0
B14	FD1	G10	VSS	K7	VSTBY	R3	KSO1/PD1
B15	FA11	G11	PS2DAT3/GPF7	K8	VSS	R4	KSO2/PD2
B16	FA6	G12	PS2CLK3/GPF6	K9	VSS	R5	GPH1
B2	GPC5	G15	PS2DAT2/GPF5	L1	ECSCI#/GPD3	R6	KSO8/ACK#
B3	FCS#	G16	PS2CLK2/GPF4	L10	KSI5	R7	KSO10/PE
B4	GPC3	G2	VCC	L11	FA18/GPG2	R8	KSO13
B5	GPI5	G5	WRST#	L12	FA19/GPG3	R9	GPH4
B6	SMDAT0/GPB4	G6	PWUREQ#	L15	AVSS	T1	WUI5/GPE5
B7	GPB2	G7	VSTBY	L16	AVSS	T10	KSI1/AFD#
B8	GPI4	G8	VSTBY	L2	PWM0/GPA0	T11	GPH5
B9	TXD/GPB1	G9	VSTBY	L5	GPD4	T12	ADC0
C1	FA20/GPG4	H1	NC	L6	KSO9/BUSY	T13	ADC2
C15	FA5/SHBM	H10	VSS	L7	KSO11/ERR#	T14	NC
C16	FA13	H11	VSS	L8	KSO15	T15	ADC4/GPE0
C2	PWRSW/GPE4	H12	PS2DAT1/GPF3	L9	KSI3/SLIN#	T16	ADC5/GPE1
D1	SERIRQ	H15	PS2CLK1/GPF2	M1	PWM1/GPA1	T2	CLKOUT/GPC0
D15	FA4/PPEN	H16	FA16/GPG0	M10	GPH6	T3	KSO0/PD0
D16	FA2	H2	ECSMI#	M11	KSI6	T4	KSO3/PD3
D2	LAD3	H5	LPCPD#/WUI6/GPE6	M12	KSI7	T5	GPH2
E1	LFRAME#	H6	LPC80HL/GPG6	M15	AVCC	T6	KSO7/PD7
E10	FWR#	H7	VSTBY	M16	AVCC	T7	TACH0/GPD6
E11	FD5	H8	VSS	M2	PWM2/GPA2	T8	KSO12/SLCT
E12	FA12	H9	VSS	M5	KSO4/PD4	T9	GPH3

Table 4-3. Pins Listed in Alphabetical Order (176-pin LQFP/TFBGA)

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
ADC0	81/T12	FA9	142/B12	KSI5	78/L10	PS2DAT1/GPF3	115/H12
ADC1	82/R12	FCS#	173/B3	KSI6	79/M11	PS2DAT2/GPF5	117/G15
ADC2	83/T13	FD0	138/A14	KSI7	80/M12	PS2DAT3/GPF7	119/G11
ADC3	84/R13	FD1	139/B14	KSO0/PD0	49/T3	PWM0/GPA0	32/L2
ADC4/GPE0	87/T15	FD2	140/A13	KSO1/PD1	50/R3	PWM1/GPA1	33/M1
ADC5/GPE1	88/T16	FD3	141/B13	KSO10/PE	61/R7	PWM2/GPA2	36/M2
ADC6/GPE2	89/R15	FD4	144/F11	KSO11/ERR#	64/L7	PWM3/GPA3	37/N1
ADC7/GPE3	90/R16	FD5	145/E11	KSO12/SLCT	65/T8	PWM4/GPA4	38/K5
ADC8	93/N16	FD6	146/B11	KSO13	66/R8	PWM5/GPA5	39/N2
ADC9	94/N15	FD7	147/A11	KSO14	67/M8	PWM6/GPA6	40/P1
AVCC	95/ M15,M16	FRD#	150/A10	KSO15	68/L8	PWM7/GPA7	43/R1
AVSS	96/ L15,L16	FWR#	151/E10	KSO2/PD2	51/R4	PWRSW/GPE4	2/C2
CK32K	158/A8	GA20/GPB5	5/F6	KSO3/PD3	52/T4	PWUREQ#	23/G6
CK32KE	160/A7	GINT/GPD5	42/P2	KSO4/PD4	53/M5	RI1#/WUI0/GPD0	26/J2
CK32KOUT/GPC7	1/B1	GPB2	162/B7	KSO5/PD5	56/J6	RI2#/WUI1/GPD1	29/K2
CLKOUT/GPC0	47/T2	GPC3	171/B4	KSO6/PD6	57/M6	RING#/PWRFAIL#/ LPCRST#/GPB7	165/A5
CLKRUN#/WUI7 /GPE7	25/J1	GPC5	175/B2	KSO7/PD7	58/T7	RXD/GPB0	153/A9
DAC0	99/K15	GPD4	41/L5	KSO8/ACK#	59/R6	SERIRQ	7/D1
DAC1	100/K16	GPH0	48/R2	KSO9/BUSY	60/L6	SMCLK0/GPB3	163/E7
DAC2	101/J15	GPH1	54/R5	LAD0	15/F2	SMCLK1/GPC1	169/E6
DAC3	102/J16	GPH2	55/T5	LAD1	14/F1	SMDAT0/GPB4	164/B6
ECSCI#/GPD3	31/L1	GPH3	69/T9	LAD2	13/E2	SMDAT1/GPC2	170/A4
ECSMI#	22/H2	GPH4	70/R9	LAD3	10/D2	TACH0/GPD6	62/T7
FA0	124/E16	GPH5	75/T11	LFRAME#	9/E1	TACH1/GPD7	63/M7
FA1	125/E15	GPH6	76/M10	LPC80HL/GPG6	27/H6	TMRI0/WUI2/GPC4	172/A3
FA10	135/A15	GPH7	105/K12	LPC80LL/GPG7	28/K1	TMRI1/WUI3/GPC6	176/A1
FA11	134/B15	GPI0	148/F10	LPCCLK	18/F7	TXD/GPB1	154/B9
FA12	130/E12	GPI1	149/B10	LPCPD#/WUI6/GPE6	24/H5	VBAT	161/A6
FA13	129/C16	GPI2	152/E9	LPCRST#/WUI4/ GPD2	30/J5	VCC	16/ G1,G2
FA14	121/F15	GPI3	155/E8	NC	91/P16	VSS	122,137, 159,167, 17,35,46 /G10,H10,H11,H8,H9,J10 ,J8,J9,K10,K8,K9
FA15	120/F16	GPI4	156/B8	NC	92/P15		
FA16/GPG0	113/H16	GPI5	168/B5	NC	21/H1		
FA17/GPG1	112/J11	GPI6	174/A2	NC	85/T14		
FA18/GPG2	104/L11	GPJ0	8/	NC	86/R14		
FA19/GPG3	103/L12	GPJ1	11/	NC	98, 106-109		
FA2/BADDR0	126/D16	GPJ2	12/				
FA20/GPG4	3/C1	GPJ3	20/			VSTBY	123,136, 166,34,4 5/F9,G7, G8,G9,H 7,J7,K6, K7
FA21/GPG5	4/E5	GPJ4	21/				
FA3/BADDR1	127/F12	KBRST#/GPB 6	6/F5				
FA4/PPEN	128/D15	KSI0/STB#	71/M9	PS2CLK0/GPF0	110/K11		
FA5/SHBM	131/C15	KSI1/AFD#	72/T10	PS2CLK1/GPF2	114/H15		
FA6	132/B16	KSI2/INIT#	73/R10	PS2CLK2/GPF4	116/G16	VSTBY	157/F8
FA7	133/A16	KSI3/SLIN#	74/L9	PS2CLK3/GPF6	118/G12	WRST#	19/G5
FA8	143/A12	KSI4	77/R11	PS2DAT0/GPF1	111/J12	WUI5/GPE5	44/T1

5. Pin Descriptions

5.1 Pin Descriptions

Table 5-1. Pin Descriptions of LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V CMOS I/F, 5V tolerant)			
165 or 30	**LPCRST#**	IK	***LPC Hardware Reset*** LPC hardware reset will reset LPC interface and host side modules. The source is determined by EC side register bit LPCRSTEN. This pin can be omitted if external LPC reset is not required.
18	**LPCCLK**	PI	***LPC Clock*** 33 MHz clock for LPC domain functions.
10, 13-15	**LAD[3:0]**	PIO	***LPC Address Data***
9	**LFRAME#**	PI	***LPC LFRAME# Signal***
24	**LPCPD#**	IO2	***LPC LPCPD# Signal***
25	**CLKRUN#**	IO6	***LPC CLKRUN# Signal***
7	**SERIRQ**	PIO	***SERIRQ Signal***
22	**ECSMI#**	O8	***EC SMI# Signal*** This is SMI# signal driven by SWUC module.
31	**ECSCI#**	O8	***EC SCI# Signal*** This is SCI# signal driven by PMC module.
5	**GA20**	IO2	***Gate A20 Signal*** This is GA20 signal driven by SWUC module.
6	**KBRST#**	IO2	***KB Reset Signal*** This is KBRST# signal driven by SWUC module.
19	**WRST#**	IK	***Warm Reset*** For EC domain function reset after power up.
23	**PWUREQ#**	O2	***System Power On Request*** This is PWUREQ# signal driven by SWUC module.
27	**LPC80HL**	O4	***LPC I/O Port 80, High-nibble LAD Latch*** An active high signal to latch Port 80 high-nibble for the debug purpose.
28	**LPC80LL**	O4	***LPC I/O Port 80, Low-nibble LAD Latch*** An active high signal to latch Port 80 low-nibble for the debug purpose.

Table 5-2. Pin Descriptions of External Flash Interface

Pin(s) No.	Signal	Attribute	Description
Flash Interface (3.3V CMOS I/F, 5V tolerant)			
120-121, 129-130, 134-135, 142-143, 133-131, 128-124	**FA[15:0]**	O4	***Flash Address [15:0]*** These are dedicated external Flash address pins. In addition to being the Flash address output, FA[5:2] serve as hardware strap pins described below. FA[5] : SHBM, shared BIOS mode enable. FA[4] : PPEN, enable in-system programming via parallel port interface FA[3] : BADDR[1], used in PNPCFG base address. FA[2] : BADDR[0], used in PNPCFG base address.
3-4, 103-104, 112-113	**FA[21:16]**	IOK4	***Flash Address [21:16]/Alternate GPIO*** These pins can be used as GPIO pins depending on the external Flash size.
147-144, 141-138	**FD[7:0]**	IOK4	***Flash Data [7:0]*** Flash data bus.
150	**FRD#**	O4	***Flash Read*** Flash read control.
151	**FWR#**	O4	***Flash Write*** Flash write control.
173	**FCS#**	O4	***Flash Chip Select*** FCS# is the external Flash chip select.

Table 5-3. Pin Descriptions of Keyboard Matrix Scan Interface

Pin(s) No.	Signal	Attribute	Description
KB Matrix Interface (3.3V CMOS I/F, 5V tolerant)			
68-64, 61-56, 53-49	**KSO[15:0]**	O8	***Keyboard Scan Output*** Keyboard matrix scan output.
80-77, 74-71	**KSI[7:0]**	IK	***Keyboard Scan Input*** Keyboard matrix scan input for switch based keyboard.

Table 5-4. Pin Descriptions of SM Bus Interface

Pin(s) No.	Signal	Attribute	Description
SM Bus Interface (3.3V CMOS I/F, 5V tolerant)			
169, 163	**SMCLK[1:0]**	IOK2	***SM Bus CLK*** 2 SM bus interface provided. SMCLK0-1 correspond to channel A and B, respectively.
170, 164	**SMDAT[1:0]**	IOK2	***SM Bus Data*** 2 SM bus interface provided. SMDAT0-1 correspond to channel A and B, respectively.

Table 5-5. Pin Descriptions of PS/2 Interface

Pin(s) No.	Signal	Attribute	Description
PS/2 Interface (3.3V CMOS I/F, 5V tolerant)			
118, 116, 114, 110,	**PS2CLK[3:0]**	IOK8	***PS/2 CLK*** 4 sets of PS/2 interface, alternate function of GPIO. PS2CLK0-3 correspond to channel 1-4, respectively.
119, 117 115, 111	**PS2DAT[3:0]**	IOK8	***PS/2 Data*** 4 sets of PS/2 interface, alternate function of GPIO. PS2DAT0-3 correspond to channel 1-4, respectively.

Table 5-6. Pin Descriptions of PWM Interface

Signal	Pin(s) No.	Attribute	Description
PWM Interface (3.3V CMOS I/F, 5V tolerant)			
43, 40-36, 33-32	**PWM[7:0]**	IOK8	***Pulse Width Modulation Output*** Two of the eight PWM outputs can be selected as SmartAuto fan control if enabled. Others are general-purpose PWM signals. PWM0-7 correspond to channel 0-7, respectively.
63-62	**TACH[1:0]**	IOK2	***Tachometer Input*** TACH[1:0] are tachometer inputs from external fans. They are used for measuring the external fan speed.
176,172	**TMRI[1:0]**	IOK2	***Counter Input*** TMRI[1:0] are timer/counter input signals connected to timer2 and timer1 of 8032. Notice that the frequency must be slower than 8032 clock to be sampled.

Table 5-7. Pin Descriptions of Wake Up Control Interface

Pin(s) No.	Signal	Attribute	Description
Wake Up Control Interface (3.3V CMOS I/F, 5V tolerant)			
25-24, 44, 30, 176, 172, 29, 26	**WUI[7:0]**	IOK2-8	***EC Wake Up Input*** Supplied by VSTBY, used for EC wake up.
2	**PWRSW**	IOK2	***Power Switch Input*** Supplied by VSTBY, used to indicate the status of power switch.
29,26	**RI[2:1]#**	IOK4	***Ring Indicator Input*** Supplied by VSTBY, used for system wake up.
165	**RING#**	IOK2	***Telephone Line Ring Input*** Supplied by VSTBY, used for system wake up.

Table 5-8. Pin Descriptions of UART Interface

Pin(s) No.	Signal	Attribute	Description
UART Interface (3.3V CMOS I/F, 5V tolerant)			
154	**TXD**	IOK2	***UART TX Output*** UART TX Output from 8032
153	**RXD**	IOK2	***UART RX Input*** UART RX Input from 8032

Table 5-9. Pin Descriptions of Parallel Port Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface (3.3V CMOS I/F)			
65	**SLCT**	O8	***Printer Select***
61	**PE**	O8	***Printer Paper End***
60	**BUSY**	O8	***Printer Busy***
59	**ACK#**	O8	***Printer Acknowledge***
74	**SLIN#**	IK	***Printer Select Input***
73	**INIT#**	IK	***Printer Initialize***
64	**ERR#**	O8	***Printer Error***
72	**AFD#**	IK	***Printer Auto Line Feed***
71	**STB#**	IK	***Printer Strobe***
58-56,53-49	**PD[7:0]**	O8	***Parallel Port Data[7:0]***

Table 5-10. Pin Descriptions of GPIO Interface

Pin(s) No.	Signal	Attribute	Description
GPIO Interface (3.3V CMOS I/F, 5V tolerant)			
A: 43, 40-36, 33-32 B: 165 6-5, 164-162, 154-153 C: 1, 176-175, 172-169, 47 D: 63-62, 42-41, 31-29, 26 E: 25-24, 44, 2, 90-87 F: 119-114, 111-110 G: 28-27, 4-3, 103-104, 112-113 H: 105, 76-75, 70-69, 55-54, 48 I: 174, 168, 156-155, 152, 149-148	**GPA[7:0], GPB[7:0], GPC[7:0], GPD[7:0], GPE[7:0], GPF[7:0], GPG[7:0], GPH[7:0], GPI[6:0]**	IOK Refer to Table 7-13 on page 179 for output driving capability	***GPIO Signals*** The 71 GPIO pins are divided into 9 groups. Each of them contains 8 GPIO pins. Some GPIO pins have alternative function. GPI5 may be used by power supply control and it is only reset by VSTBY Power-Up Reset and Watchdog Reset.
42	**GINT**	IK	***General Purpose Interrupt*** General Purpose Interrupt directly input to INT28 of INTC.

Table 5-11. Pin Descriptions of Hardware Strap

Pin(s) No.	Signal	Attribute	Description
Hardware Strap (3.3V CMOS I/F, 5V tolerant)			
131	**SHBM**	I	***Share Host BIOS Memory Configuration*** Sampled at VSTBY power up reset. No pull resistor: disable shared memory with host BIOS External 10K ohm pull up resistor: enable shared memory with host BIOS
128	**PPEN**	I	***Parallel Port Enable*** Sampled at VSTBY power up reset. No pull resistor: Normal. External 10K ohm pull up resistor: KBS interface pins are switched to parallel port interface for in-system programming.
127,126	**BADDR[1:0]**	I	***I/O Base Address Configuration*** Sampled at VSTBY power up reset. No pull resistor: The register pair to access PNPCFG is 002Eh and 002Fh. 10K ohm external pull-up resistor on BADDR0: The register pair to access PNPCFG is 004Eh and 004Fh. 10K ohm external pull-up resistor on BADDR1: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Table 5-12. Pin Descriptions of NC

Pin(s) No.	Signal	Attribute	Description
NC (3.3V CMOS I/F, 5V tolerant)			
8, 11, 12, 85, 86, 91, 92, 97, 98,106-109	**NC**	-	***NC*** Don't connect it to any nets, or tie to digital ground. For IT8510G, it's recommend to reserve test pads on PCB for pin H1, R14, T14, P15 and P16.

Table 5-13. Pin Descriptions of ADC Input Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface (3.3V CMOS I/F)			
84-81	**ADC[3:0]**	AI	***ADC Input*** Dedicated ADC input pins.
90-87	**ADC[7:4]**	AIO2	***ADC Input/Alternate GPIO*** These 4 ADC inputs can be used as GPIO pins depending on the ADC channels required.
93	**ADC[8]**	AI	***ADC Input***
94	**ADC[9]**	AI	***ADC Input***

Table 5-14. Pin Descriptions of DAC Output Interface

Pin(s) No.	Signal	Attribute	Description
DAC Interface (3.3V CMOS I/F)			
102-99	**DAC[3:0]**	O	***DAC Output***

Table 5-15. Pin Descriptions of Clock

Pin(s) No.	Signal	Attribute	Description
Clock Interface (3.3V CMOS I/F)			
158	**CK32K**	OSCI	***32.768K Hz Crystal X1*** It is connected to internal crystal oscillator.
160	**CK32KE**	OSCIO	***32.768K Hz Crystal X2*** It is connected to internal crystal oscillator.
1	**CK32KOUT**	O4	***32.768K Hz Oscillator Output*** 32.768 KHz clock output.
47	**CLKOUT**	O2	***EC Clock Output*** EC domain clock output.

Table 5-16. Pin Descriptions of Power/Ground Signals

Pin(s) No.	Signal	Attribute	Description
Power Ground Signals			
167, 159, 137, 122, 46, 35, 17	**VSS**	I	***Ground*** Digital ground.
16	**VCC**	I	***System Power Supply of 3.3V*** The power supply of LPC and related functions, which is main power of system.
166, 157, 136, 123, 45, 34	**VSTBY**	I	***Standby Power Supply of 3.3V*** The power supply of EC domain functions, which is standby power of system. Note that the power of PLL is sourced by pin 157 only. (pin F8 for IT8510G)
161	**VBAT**	I	***Battery Power Supply of 3.3V*** The power supply for RTC, 32.768KHz oscillator and some system wake up function. Internal VBS power is supplied by VSTBY when it is valid and is supplied by VBAT when VSTBY is not supplied. If VBAT is not used, tie this pin to ground.
96	**AVSS**	I	***Analog Ground for Analog Component***
95	**AVCC**	I	***Analog VCC for Analog Component***

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
IKD: Schmitt Trigger Input PAD (integrated one pull-down resistor).
PIU: PCI Bus Specified Input PAD (integrated one pull-up resistor).
OSCI: Oscillator Input PAD.
O2: 2 mA Output PAD.
O4: 4 mA Output PAD.
O6: 6 mA Output PAD.
O8: 8 mA Output PAD.
PIO: PCI Bus Specified Bidirectional PAD.
OSCIO: Oscillator Bidirectional PAD.
AIO2: 2 mA Bidirectional PAD with Analog Input PAD.
IOK2: 2 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK4: 4 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK6: 6 mA Bidirectional PAD with Schmitt Trigger Input PAD.
IOK8: 8 mA Bidirectional PAD with Schmitt Trigger Input PAD.

5.2 Chip Power Planes and Power States

Table 5-17. Power States

Power State	VCC pin	VSTBY/AVCC pin	VBAT pin	Internal VBS
Active	Supplied	Supplied	Supplied or Not	Switched from VSTBY
Active with Power Saving	Supplied	Supplied EC is in Idle, Doze or Sleep Mode	Supplied or Not	Switched from VSTBY
Standby	Not Supplied	Supplied	Supplied or Not	Switched from VSTBY
Standby with Power Saving	Not Supplied	Supplied EC is in Idle, Doze or Sleep Mode	Supplied or Not	Switched from VSTBY
Power Fail	Not Supplied	Not Supplied	Supplied	Switched from VBS
Battery Fail	Not Supplied	Not Supplied	Not Supplied	Not Supplied

Note:

(1) The AVCC should be derived from VSTBY.
(2) All other combinations of VCC / VSTBY / VBAT are invalid.
(3) In Power Saving mode, 8032 program counter is stopped and no instruction will be executed no matter EC Clock is running or not.
(4) VBS is the battery-backed power. When VSTBY is valid, VBS is supplied by VSTBY. When VSTBY is not valid, VBS is supplied by VBAT.

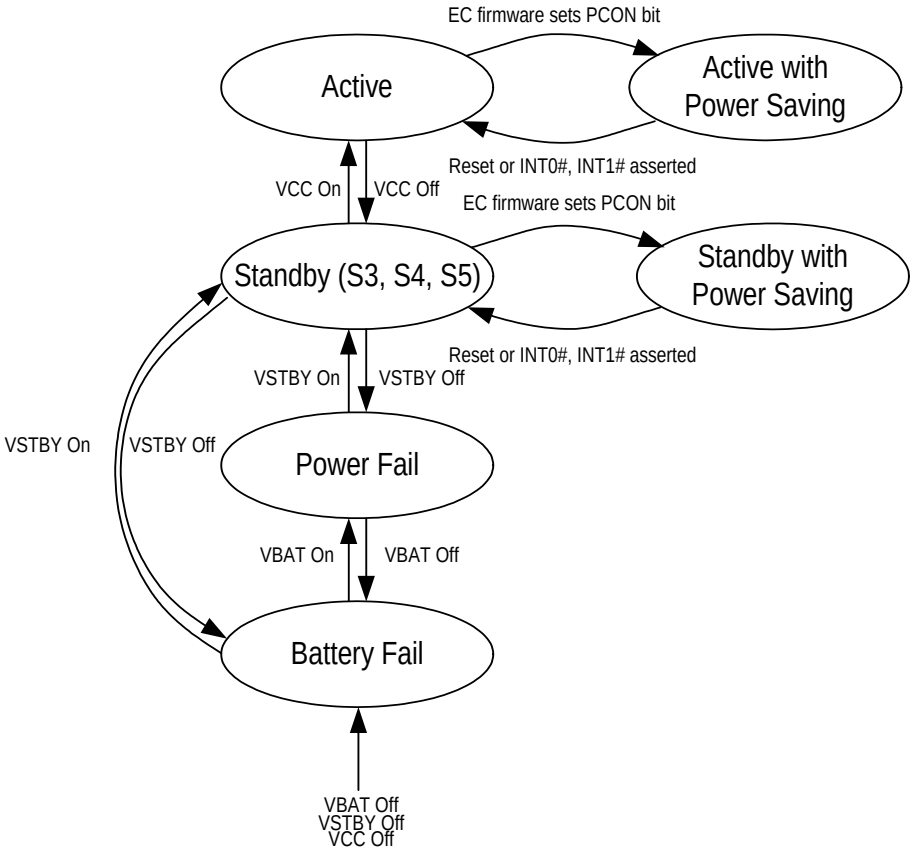


Figure 5-1. Power State Transitions

5.3 Pin Power Planes and States

Table 5-18. Quick Table of Power Plane for Pins

Power Plane	Pins No.
VCC	7-18
VSTBY	1-6, 19-157, 162-176
VBS	158-161

In the following tables of this section, Standby means that the VCC is not valid but VSTBY is supplied (S3, S4 or S5) and EC is in normal operation. Standby with Sleep means that 8032 and most of its functions are out of work due to PLL power-down while VSTBY is still supplied. Power Fail means only battery-backed power is supplied.

The abbreviations used in the following tables are described below:
H means EC drives high or driven high.
L means EC drives low or driven to low or output pin power off.
Z means EC tri-stated the I/O pin or output pin with enable.
RUN means that Output or I/O pins are in normal operation.
Driven means that the input pin is driven by connected chip or logic.
STOP means that the output pin keeps its logical level before the clock is stopped.
OFF means I/O pin power off.

Note that reset sources of 'Reset Finish' columns depend on Reset Types and Applied Module Table and it means the reset is finished when its corresponding power plane is supplied.
Note that GPIO pins listed in different functional tables except GPIO table indicate their pin status of corresponding alternative function.

Table 5-19. Pin States of LPC Bus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
LPCRST# (Y)	VSTBY	Driven	L	L	L
LPCCLK	VCC	Driven	L	L	L
LAD[3:0]	VCC	RUN	OFF	OFF	OFF
LFRAME#	VCC	Driven	L	L	L
SERIRQ	VCC	Z	OFF	OFF	OFF
LPCPD# (Y)	VSTBY	Driven	L	L	L
CLKRUN# (Y)	VSTBY	Driven	OFF	L	OFF
ECSMI#	VSTBY	RUN	RUN	Z	OFF
ECSCI# (Y)	VSTBY	Driven	RUN	Z	OFF
GA20 (Y)	VSTBY	Driven	RUN	STOP	OFF
KBRST# (Y)	VSTBY	H	RUN	STOP	OFF
WRST#	VSTBY	Driven	Driven	Driven	L
PWUREQ#	VSTBY	Z	RUN	STOP	OFF
LPC80HL (Y)	VSTBY	Driven	L	L	OFF
LPC80LL (Y)	VSTBY	Driven	L	L	OFF

Table 5-20. Pin States of External Flash Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
FA[15:0]	VSTBY	RUN	RUN	AFSTBY=1: Z with pull-down AFSTBY=0 STOP	OFF
FA16 (Y) FA17 (Y) FA18 (Y) FA19 (Y) FA20 (Y) FA21 (Y)	VSTBY	L (pull-down)	RUN	AFSTBY=1: Z with pull-down AFSTBY=0 STOP	OFF
FD[7:0]	VSTBY	RUN	RUN	AFSTBY=1: Z with pull-down AFSTBY=0: STOP	OFF
FRD#	VSTBY	L	RUN	L	OFF
FWR#	VSTBY	H	RUN	H	OFF
FCS#	VSTBY	L	RUN	AFSTBY=1: H AFSTBY=0: L	OFF

Table 5-21. Pin States of Keyboard Matrix Scan Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
KSO[15:0]	VSTBY	L	RUN	STOP	OFF
KSI[7:0]	VSTBY	Driven	Driven	Driven	L

Table 5-22. Pin States of SM Bus Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
SMCLK0 (Y) SMCLK1 (Y)	VSTBY	Driven	RUN	Z	OFF
SMDAT0 (Y) SMDAT1 (Y)	VSTBY	Driven	RUN	Z	OFF

Table 5-23. Pin States of PS/2 Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PS2CLK0 (Y) PS2CLK1 (Y) PS2CLK2 (Y) PS2CLK3 (Y)	VSTBY	Driven	RUN	Z	OFF
PS2DAT0 (Y) PS2DAT1 (Y) PS2DAT2 (Y) PS2DAT3 (Y)	VSTBY	Driven	RUN	Z	OFF

Table 5-24. Pin States of PWM Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
PWM0 (Y) PWM1 (Y) PWM2 (Y) PWM3 (Y) PWM4 (Y) PWM5 (Y) PWM6 (Y) PWM7 (Y)	VSTBY	Driven	RUN	STOP	OFF
TACH0 (Y) TACH1 (Y)	VSTBY	Driven	Driven	Driven	OFF
TMRI0 (Y) TMRI1 (Y)	VSTBY	Driven	Driven	Driven	OFF

Table 5-25. Pin States of Wake Up Control Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
WUI0 (Y) WUI1 (Y) WUI2 (Y) WUI3 (Y) WUI4 (Y) WUI5 (Y) WUI6 (Y) WUI7 (Y)	VSTBY	Driven	Driven	Driven	OFF
PWRSW (Y)	VSTBY	Driven	Driven	Driven	OFF
RI1# (Y) RI2# (Y)	VSTBY	Driven	Driven	Driven	OFF
RING# (Y)	VSTBY	Driven	Driven	Driven	OFF
PWRFAIL# (Y)	VSTBY	Driven	Driven	Driven	OFF

Table 5-26. Pin States of UART Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
RXD (Y)	VSTBY	Driven	Driven	Driven	OFF
TXD (Y)	VSTBY	Driven	RUN	STOP	OFF

Table 5-27. Pin States of GPIO Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
GPA0-GPI6	VSTBY	Driven	Z or by alternative function.	STOP	OFF

Table 5-28. Pin States of ADC Input Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
ADC[3:0]	AVCC	Driven	Driven	Driven	L
ADC4 (Y) ADC5 (Y) ADC6 (Y) ADC7	AVCC	Driven	Driven	Driven	L
ADC8	AVCC	Driven	RUN	RUN	L
ADC9	AVCC	Driven	Driven	Driven	L

Table 5-29. Pin States of DAC Output Interface

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
DAC[3:0]	AVCC	L	RUN	RUN	OFF

Table 5-30. Pin States of Clock

Signal (Alt Func of GPIO ?)	Power Plane	Reset Finish	Standby	Standby with Sleep	Power Fail
CK32K	VBS	Driven	RUN	RUN	RUN
CK32KE	VBS	Driven	RUN	RUN	RUN
CK32KOUT/GPC7	VSTBY	Driven	RUN	RUN	OFF
CLKOUT/GPC0	VSTBY	Driven	RUN	STOP	OFF

5.4 PWRFAIL# Interrupt to INTC

The firmware may use the PWRFAIL# to do some necessary response if VSTBY is being lost. Corresponded INT0# has higher priority than INT1#.

5.5 Reset Sources and Types

Table 5-31. Reset Sources

Reset Sources	Description
VBS Power-Up Reset	Activated after VBS is power up
VSTBY Power-Up Reset	Activated after VSTBY is power up and 10 MHz PLL is stable It takes t_{PLLS} for PLL stabling, and the external flash must be ready before VSTBY Power-Up Reset finish
VCC Power-Up Reset	Activated after VCC is power up
Warm Reset	Activated if WRST# is asserted
LPC Hardware Reset	Activated if LPCRST# is asserted
Super I/O Software Reset	Activated if SIOSWRST of PNPCFG is writing 1
Watch Dog Reset	Activated if 8032 WDT or External WDT time-out

Table 5-32. Reset Types and Applied Module

Reset Types	Sources	Applied Module
VBS Region Reset	VBS Power-Up Reset	RTC, SWUC
Host Domain Hardware Reset	Warm Reset, VCC Power-Up Reset or LPC Hardware Reset LPC Hardware Reset may be unused	LPC, PNPCFG, Logical Devices and EC2I
Host Domain Software Reset	Super I/O Software Reset	PNPCFG, Logical Devices and EC2I
EC Domain Reset	Warm Reset, VSTBY Power-Up Reset or Watch Dog Reset	EC Domain

The WRST# should be driven low for at least t_{WRSTW} before going high (Refer to Table 9-2. Warm Reset AC Table on page 253)

.

If the firmware wants to assert an EC Domain Reset, start an internal of external watchdog without clearing its counter or write invalid data to EWDKEYR register (refer to EWDKEYEN and EWDKEYR registers).
If the firmware wants to determine the source of the last EC Domain Reset, use the Reset Scratch Register (RSTSCR).

5.5.1 Relative Interrupts to INTC

- Interrupt to INTC

LPCRST# may come from pin LPCRST#/WUI4/GPD2 or RING#/PWRFAIL#/LPCRST#/GPB7, both pins have another interrupt relative alternative function. LPCRST# can be treated as an orthogonal input and LPCRST# event can be handled in the same interrupt routine of another alternative function.

5.6 Chip Power Mode and Clock Domain

Table 5-33. Clock Types

Types	Description
RTC Clock	32.768 KHz generated by internal oscillator
EC Clock	10 MHz generated by internal PLL which feds RTC Clock and applied on EC Domain. The EC Clock may be divided by CFSELR of ECPM module Default EC Clock is divided into 5 MHz, and should be programmed to 10 MHz.
LPC Clock	33 MHz or slower from LPCCLK pin and applied on Host Domain

The 8032 can enter Idle/Doze/Sleep mode to reduce some power consumption. After entering the Idle mode, timers and the Watch Dog timer of 8032 still work. After entering Doze/Sleep mode, clock of 8032 is stopped and internal timers are stopped but external timer still works. After entering Doze mode, EC domain clock is stopped and all internal timers are stopped. Also see Table 5-35 on page 33 for the details.
The way to wake up 8032 from the Idle mode is to enable internal or external interrupts, or hardware reset. The way to wake up 8032 from Doze/Sleep mode is to enable external interrupts or hardware reset. Firmware may set PLLCTRL bit before setting PD bit to enter the Sleep mode, since stopping PLL can reduce more power consumption, but it takes more time to wake up from Sleep mode due to waiting for PLL being stable. The steps to enter and exit Idle/Doze/Sleep are listed below:

(a) Set relative bits of IE register if they are cleared.
(b) Set channels of WUC which wants to wake up 8032 and disable unwanted channels.
(c) Set channels of INTC which wants to wake up 8032 and disable unwanted channels.
(d) Set PLLCTRL bit for Doze mode, or clear it for Doze mode.
(e) Set IDL bit in PCON to enter the Idle mode, or set PD bit in PCON to enter the Doze/Sleep mode.
(f) 8032 waits for an interrupt to wake up.
(g) After an interrupt is asserted, 8032 executes the corresponding interrupt routine and return the next instruction after setting PCON. Notice that 8032 will not execute the interrupt routine if PDC bit in PDCON is set before PCON is set and the interrupt is de-asserted.

The following figure describes the drivers and branches of the three clocks.
In this figure, clk_32khz represents RTC Clock; clk_src and its branches represent EC Clock; clk_ibus represents LPC Clock.

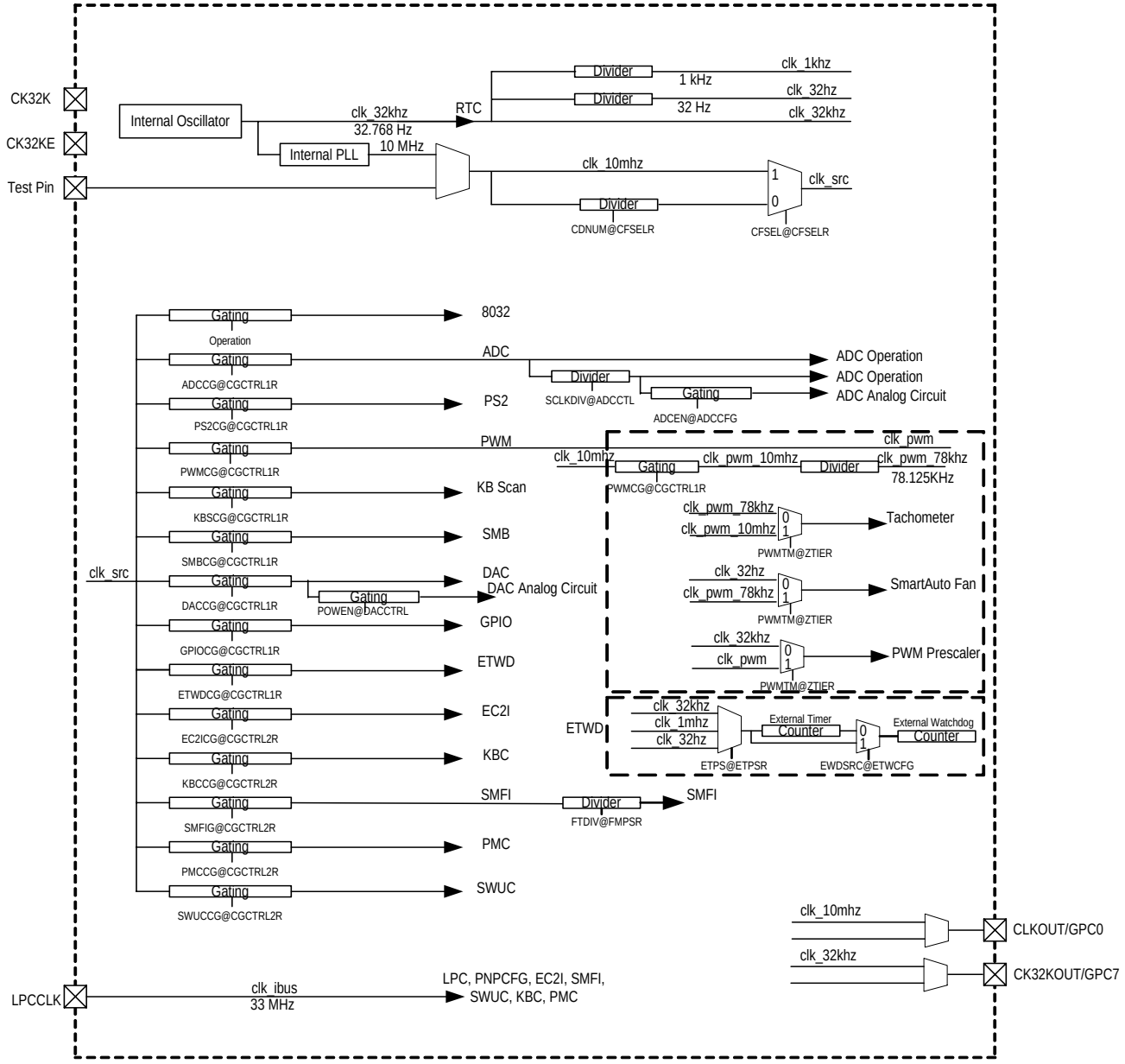


Figure 5-2. Clock Tree

Table 5-34. Power Saving by EC Clock Operation Mode

Mode	Item	Description
Normal	Enter	VSTBY is supplied and hardware reset done
	Exit	Enter other modes
	RTC Clock	On
	10 MHz PLL	On
	EC Domain Clock	Driven by PLL or divided clock (refer to CFSELR of ECPM module)
	8032 Clock	The same as EC Domain Clock
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Idle	Enter	Set IDL bit in PCON of 8032
	Exit	Interrupt from INTC, interrupt from 8032 timer, watchdog reset or hardware reset
	RTC Clock	On
	10 MHz PLL	On
	EC Domain Clock	Driven by PLL or divided clock (refer to CFSELR of ECPM module)
	8032 Clock	The same as EC Domain Clock
	Comment	Power consumption can be reduced by selectively disabling modules, refer to ECPM module.
Doze	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	RTC Clock	On
	10 MHz PLL	On, clearing PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL or divided clock (refer to CFSELR of ECPM module)
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)
Sleep	Enter	Set PD bit in PCON of 8032
	Exit	Interrupt from INTC or hardware reset
	RTC Clock	On
	10 MHz PLL	Off, setting PLLCTRL of ECPM module is required
	EC Domain Clock	Driven by PLL or divided clock (refer to CFSELR of ECPM module)
	8032 Clock	Off
	Comment	Power consumption can be reduced by selectively disabling modules (refer to ECPM module)

Note:
The PD bit in PCON register may trigger the Doze or Sleep mode of EC Domain.

Table 5-35. Module Status in Each Power State/Clock Operation

Power State and/or Clock Operation	Running Module	Stopped Module	Off Module	Note
Active *Active with Power Saving*	LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC/ RTC			List host relative modules only
Standby *Standby with Power Saving*			LPC, PNPCFG, EC2I, host parts of SMFI/ SWUC/ KBC/ PMC/ RTC	List host relative modules only
Active with Idle Mode *Standby with Idle Mode*	All other EC modules	8032 code-fetch (but internal timer/WDT are still running)		List EC modules only
Active with Doze Mode *Standby with Doze Mode*	All other EC modules	8032		List EC modules only
Active with Sleep Mode *Standby with Sleep Mode*	GPIO, WUC and its sources, INTC and its sources from running modules, SWUC wakeup logic, PWM channel outputs, KBS, ETWD, RTC	All other EC modules		List EC modules only
Power Fail	RTC		All others	List all
Battery Fail			All	List all

Note: Running module means this module works well.
Stopped module means this module is frozen because its clock is stopped.
Off module means this module is turned off due to power lost.

5.7 Pins with Pull, Schmitt-Trigger or Open-Drain Function

Table 5-36. Pins with Pull Function

Pin	Pull Function	Note
KSI[7:0]	Programmable 75k pull-up resistor	Default off
KSO[15:0]	Programmable 75k pull-up resistor	Default off
GPE4-E7 and their alternative functions	Programmable 75k pull-up resistor	GPE0-E3 have no pull function Default on/off refer to Table 7-13 on page 179 .
GPG0-G7 and their alternative functions	Programmable 75k pull-down resistor	Default on/off refer to Table 7-13 on page 179 .
All other GPIO pins and their alternative functions	Programmable 75k pull-up resistor	Default on/off refer to Table 7-13 on page 179 .
FA[21:0], FD[7:0], FCS#, FRD#, FWR#	Operational 75k pull-down resistor	Pull-down if power-saving
FA[5:2]	Operational 75k pull-down resistor	Pull-down after VSTBY power on until its pin state is sampled for hardware strap function

Note: 75k ohm is typical value. Refer to section 8 DC Characteristics on page 251 for details

Table 5-37. Pins with Schmitt-Trigger Function

Pin	Pull Function	Note
All GPIO pins except GPE0-E3 and their alternative functions	Fixed Schmitt-Trigger Input	
KSI[7:0]	Fixed Schmitt-Trigger Input	
WARMRST#	Fixed Schmitt-Trigger Input	
FD[7:0]	Fixed Schmitt-Trigger Input	

Table 5-38. Signals with Open-Drain Function

Signal	Open-Drain Function	Note
SERIRQ	Open-drain bi-directional signal	
CLKRUN#	Open-drain output signal	
KSO[15:0]	Programmable open-drain output signal	Default is push-pull
PS2CLK0, PS2DAT0 PS2CLK1, PS2DAT1 PS2CLK2, PS2DAT2 PS2CLK3, PS2DAT3	Open-drain bi-directional signal	
SMCLK0, SMDAT0 SMCLK1, SMDAT1	Open-drain bi-directional signal	
SCI#, SMI#, PWUREQ#	Open-drain output signal	
All GPIO signals except GPE0-E3 and their alternative functions	Programmable open-drain output signal	Default is push-pull

5.8 Power Consumption Consideration

- Each input pin should be driven or pulled

Input floating causes leakage current and should be prevented.
Pins can be pulled by an external pull resistor or internal pull for a pin with programmable pull.
GPE0-~GPE3 have analog inputs as their alternative function, and these four pins can prevent leakage current by switching to the alternative function, too.

- Each output-drain output pin should be pulled

If an output-drain output pin is not used and is not pulled by an external pull resistor or internal pull for a pin with programmable pull, make it drive low by the firmware.

- Each input pin which belongs to VSTBY power plane is connected or pulled up to VCC power plane

Such cases may cause leakage current when VCC is not supplied and a diode may be used to isolate leakage current from VSTBY to VCC. For example, use diodes for KBRST# and GA20 if they are connected to VCC logic of South-Bridge.

- Any pin which belongs to VSTBY power plane should not be pulled to VCC in most cases.

It may cause a leakage current path when VCC is shut down. Refer to the above consideration.

- Program GPIO ports as output mode as soon as possible

Any GPIO port used in output mode should be programmed as soon as possible since this pin may not be driven (be floating) if its default value of pull is off.

- Disable unnecessary pull in power saving mode

Prevent from driving a pin low or let a pin be driven low but its pull high function is enabled in power saving mode.
Prevent from driving a pin high or let a pin be driven high but its pull low function is enabled in power saving mode.

- Handle the connector if no cable is plugged into it

The firmware or the hardware should prevent the wire connected to the connector from no driving if no cable is plugged into the connector such as PS/2 mouse and so on.

- Disable unnecessary pull for a programmable pull pin

Pull control may be enabled for an input pin or an open-drain output pin and should be disabled for a push-pull output pin.
Pull control should be disabled if an external pull resistor exists.
External pull resistor can control the pull current precisely since the register value of the internal pull has large tolerance. Refer to section 8 DC Characteristics on page 251 for details

- Flash standby mode

Make flash enter standby mode to reduce power consumption if it is not used.
It's controlled by AFSTBY bit in FPCFG register.
It may be an EMI option.

- Prevent accessing Scratch RAM before entering power-saving mode

There is unnecessary power consumption after Scratch RAM is accessed in data space. Reading any other registers of external data memory once to prevent this condition.

- Use Doze mode rather than Idle mode

Doze mode has less power consumption than Idle mode because 8032 clock is gated (stopped) in Doze mode. Firmware design using Idle mode should be replaced with Doze mode by replacing internal timer and watchdog by external timer and watchdog.

- Use Sleep mode rather than Doze mode

Sleep mode has less power consumption than Doze mode because PLL is power-down and EC clock is stopped in Sleep mode, although most EC modules are not available.
Refer to Table 5-35 on page 33 for the details.

- Divide EC clock by module

After reset, EC clock is 5 MHz and the firmware sets to 10 MHz as normal operation. Divided EC clock makes less power consumption and it's controlled by CFSELR register.

- Gate clock by module in EC domain

All modules in EC domain are not clock gated in default but can be gated by module to get less power consumption.
It's controlled by CGCTRL1R and CGCTRL2R registers.

- Power-down ADC/DAC analog circuit if it is unnecessary

ADC/DAC analog circuits are power-down in default and should be activated only if necessary.
ADC analog circuit power-down is controlled by ADCEN bit in ADCCFG register.
DAC analog circuit power-down is controlled by POWDN bit in DACCTRL register.

- Connect LED cathode to output pin

It doesn't reduce total power consumption although it reduces power consumption of IT8510.
The advantage is to reduce the temperature of IT8510 and prevent the output pad from driving large current.

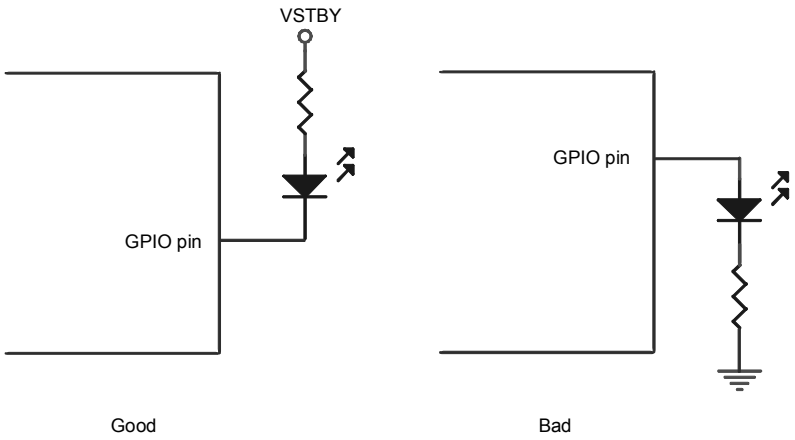


Figure 5-3. LED connection

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6. Host Domain Functions

6.1 Low Pin Count Interface

6.1.1 Overview

The Low Pin Count (LPC) is an interface for modern ISA-free system. It is defined in Intel's LPC Interface Specification, Revision 1.1. There are seven host-controlled modules that can be accessed by the host via the LPC interface. These host-controlled modules are "Logical Devices" defined in Plug and Play ISA Specification, Version 1.0a.

6.1.2 Features

- Complies with Intel's LPC Interface Specification, Revision 1.1
- Supports SERIRQ and complies with Serialized IRQ Support for PCI Systems, Revision 6.0
- Supports LPCPD#, CLKRUN#
- Supports Plug and Play ISA registers

6.1.3 Accepted LPC Cycle Type

The supported LPC cycle types are listed below:
* LPC I/O Read (16-bit address, 8-bit data)
* LPC I/O Write (16-bit address, 8-bit data)
* LPC Memory Read (32-bit address, 8-bit data)
* LPC Memory Write (32-bit address, 8-bit data)
* FWH Read (32-bit address, 8-bit data)
* FWH Write (32-bit address, 8-bit data)

I/O cycles are used to access PNPCFG and Logical Devices. Memory or FWH is used to access Flash content through SMFI module Indirect memory cycles based on I/O cycles can also access Flash. Refer to SMFI Module for details about indirect memory access.

The following table describes how LPC module responds the I/O, Memory and FWH cycles from Host side in different conditions.

Table 6-1. LPC/FWH Response

Cycle Type/Condition		Read Response	Write Response
All Cycles before 10 MHz PLL Stable		Long-Wait	Long-Wait
I/O Cycle to PNPCFG or Logical Devices		Ready	Ready
I/O Cycle but Address Out Of Range		Cycle Ignored	Cycle Ignored
I/O Cycle to Locked PNPCFG/RTC by EC2I		Returns 00h	Cycle Ignored
Indirect Memory Address NOTE 3		Ready	Ready
Memory Cycle, FWH Cycle or Indirect Memory Data		Long-Waits until Ready	Long-Waits until Ready NOTE 1
Memory Cycle, FWH Cycle or Indirect Memory Data but Address Protected by SMFI	*HERES=00**	Long-Wait	Cycle Ignored
	HERES=01	Returns 00h	Cycle Ignored
	HERES=10	Error-SYNC	Error-SYNC
	HERES=11	Long-Wait	Error-SYNC
Memory Cycle or Indirect Memory Data but Address Out of Range		Cycle Ignored	Cycle Ignored
FWH Cycle but Address Out of Range		Ready	Ready
FWH Cycle but FWH ID is unmatched NOTE 2		Cycle Ignored	Cycle Ignored
LPC Cycle or Indirect Memory Data but LPCMEN bit in SHMC register cleared		Cycle Ignored	Cycle Ignored
FWH Cycle but FWHEN bit in SHMC register cleared		Cycle Ignored	Cycle Ignored

Note 1:
After reset, IT8510 responses Long-Waits before Ready for FWH Write Cycle.

If LPC host (South-Bridge) fails to recognize Long-Wait SYNC during FWH Write Cycle, it is recommended to use Indirect Memory.

Note 2:
FWH ID is defined in FWHID field in SHMC register.

Note 3:
Indirect Memory Cycles access the flash via LPC I/O Cycle. Indirect Memory Address is combined with SMIMAR0, SMIMAR1, SMIMAR2 and SMIMAR3 registers. Indirect Memory Data is SMIMDR register.

6.1.4 Debug Port Function

LPC module implements two latch signals for Main-Board debug purpose. LPC I/O write cycles with address equal to 80h will cause the LPC module to assert LPC80HL and LPC80LL signals which provide a simple external logic to latch it in order to display on LED, even though I/O port 80h is not recognized by PNPCFG or any Logical Device. LPC80HL goes high when it is time to latch the high-nibble of the data written to port 80h, and LPC80LL means the low-nibble.

6.1.5 Serialized IRQ (SERIRQ)

IT8510 has programmable IRQ number for each logical device. Available IRQ numbers are 1, 2, 3, 4 5, 6, 7, 8, 9, 10, 11, 12, 14, and 15.

Different logical devices inside IT8510 can share the same IRQ number if they have the same IRQPS bit in IRQTP register and are configured as the same triggered mode (all level-triggered or all edge triggered) in their EC side registers.

But it is not allowed to share an IRQ number with a logical device outside IT8510. Note that edge-triggered interrupts are not suitable for sharing in most cases.

6.1.6 Relative Interrupts to INTC/WUC

- Interrupt to WUC
  If the LPC address of an I/O, LPC Memory or FWH Cycle on LPC bus is accepted, WU42 interrupt will be asserted.

6.1.7 LPCPD# and CLKRUN#

- LPCPD#
  LPCPD# is used as internal “power good” signal to indicate the status of VCC. It is recommend to be implemented.

- CKRUN#
  CLKRUN# is used to make sure that SERIRQ status is entirely translated to host side.

6.1.8 Check Items

If the IT8510 fails in LPC memory or I/O cycles at boot, check the following recommended items first.

- LPC/FWH memory cycles
  Check whether corresponding GPIO ports of necessary FA21-17 are switched to their alternative function.
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether hardware strap SHBM is enabled or set FWHEN/LPCMEN bit in SHMC register.
  Check whether the firmware doesn't change the read protection control.

- LPC I/O cycles
  Check whether LPCRST# reset source from GPD2 or GPB7 is logic low if it is in alternative function.
  Check whether LPCPD# signal from GPE6 is logic low if it is in alternative function.
  Check whether hardware strap BADDR1-0 are in correct setting.

6.2 Plug and Play Configuration (PNPCFG)

The host interface registers of PNPCFG (Plug and Play Configuration) are listed below. The base address can be configured via hardware strap BADDR1-0. Note that bit 0 of SWCBALR must be zero.
To access a register of PNPCFG, write target index to address port and access this PNPCFG register via data port. If accessing the data port without writing index to address port, the latest value written to address port is used as the index. Reading the address port register returns the last value written to it.

Table 6-2. Host View Register Map, PNPCFG

	BADDR1-0 =00b	BADDR1-0 =01b	BADDR1-0 =10b	BADDR1-0 =11b
7 0	I/O Port Address			
Address Port	2Eh	4Eh	(SWCBAHR, SWCBALR)	Reserved
Data Port	2Fh	4Fh	(SWCBAHR, SWCBALR+1)	Reserved

Note 1: SWCBALR should be on boundary = 2, which means bit 0 must be 0.
Note 2: Only use BADDR1-0=10b if the port pair is not 2Eh/2Fh or 4Eh/4Fh.

The host interface registers for Logic Device Control are listed below. The base address can be configured via the following Plug and Play Configuration Registers. Note that if a logical device is activated but with base address equal to 0000h, the host side cannot access this logical device since 0000h means I/O address range is disabled.

Table 6-3. Host View Register Map, Logical Devices

7 0	I/O Port Address
System Wake-Up Control (SWUC)	Depend on PnP SW Used Addr: (IOBAD0+00h,+02h,+06h,+07h,13h,15h) Base address boundary = 32
KBC / Mouse Interface	Unused
KBC / Keyboard Interface	Depend on PnP SW Used Addr: (IOBAD0+00h), (IOBAD1+00h) Base address boundary = none, none Legacy Address = 60h,64h
Shared Memory/Flash Interface (SMFI)	Depend on PnP SW Used Addr: (IOBAD0+0h, …+8h,+0Ch) Base address boundary = 16
Real Time Clock (RTC)	Depend on PnP SW Used Addr: (IOBAD0+0h,+1h), (IOBAD1+0h,+1h) Base address boundary = 2, 2 Legacy Address = 70h-73h
Power Management I/F Channel 1 (PM1)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 62h,66h
Power Management I/F Channel 2 (PM2)	Depend on PnP SW Used Addr: (IOBAD0+0h), (IOBAD1+0h) Base address boundary = none, none Legacy Address = 68h,6Ch

Note: The boundary number means the address must be the multiple of this number.

The host interface registers for Standard Plug and Play Configuration of PNPCFG are listed below. These registers are accessed via the Index-Data I/O ports defined in Table 6-3 on page 45. Note PNPCFG registers are not allowed to be accessed if LKCFG bit in LSIOHA register of EC2I module is set. They are divided into two parts, Super I/O Configuration Registers and Logical Device Registers.

Table 6-4. Host View Register Map via Index-Data I/O Pair, Standard Plug and Play Configuration Registers

	7 0 Register Name	Index
Super I/O Configuration Registers	Logical Device Number (LDN)	07h
	Chip ID Byte 1(CHIPID1)	20h
	Chip ID Byte 2(CHIPID2)	21h
	Chip Version (CHIPVER)	22h
	Super I/O Control (SIOCTRL)	23h
	Reserved	24h
	Super I/O IRQ Configuration (SIOIRQ)	25h
	Super I/O General Purpose (SIOGP)	26h
	Reserved	27h
	Reserved	28h
	Reserved	29h
	Reserved	2Ah
	Reserved	2Bh
	Super I/O Power Mode (SIOPWR)	2Dh
	Reserved	2Eh
Logical Device Configuration Registers Selected by LDN Register	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	DMA Channel Select 0 (DMAS0)	74h
	DMA Channel Select 0 (DMAS1)	75h
	Device Specific Logical Device Configuration 1 to 10	F0h-F9h

The IRQ numbers for Logic Device IRQ via LPC/SERIRQ are listed below. The IRQ numbers can be configured via the above Plug and Play Configuration Registers.

Table 6-5. Interrupt Request (IRQ) Number Assignment, Logical Device IRQ via SERIRQ

Logical Device	IRQ number
System Wake-Up Control (SWUC)	Depend on PnP SW
KBC / Mouse Interface	Depend on PnP SW, Legacy IRQ Num=12
KBC / Keyboard Interface	Depend on PnP SW, Legacy IRQ Num=01
Shared Memory/Flash Interface (SMFI)	Unused
Real Time Clock (RTC)	Depend on PnP SW, Legacy IRQ Num=08
Power Management I/F Channel 1 (PM1)	Depend on PnP SW, Legacy IRQ Num=01
Power Management I/F Channel 2 (PM2)	Depend on PnP SW, Legacy IRQ Num=01

6.2.1 Logical Device Assignment

Table 6-6. Logical Device Number (LDN) Assignments

LDN	Functional Block
04h	System Wake-Up Control (SWUC)
05h	KBC/Mouse Interface
06h	KBC/Keyboard Interface
0Fh	Shared Memory/Flash Interface (SMFI)
10h	Real Time Clock (RTC)
11h	Power Management I/F Channel 1 (PM1)
12h	Power Management I/F Channel 2 (PM1)

The following figure indicates the PNPCFG registers is combined with Super I/O Configuration Registers and Logical Device Configuration Registers. Logical Device Configuration Registers of a specified Logical Device is accessable only when Logical Device Number Register is filled with corresponding Logical Device Number listed in Table 6-6 on page 47 .

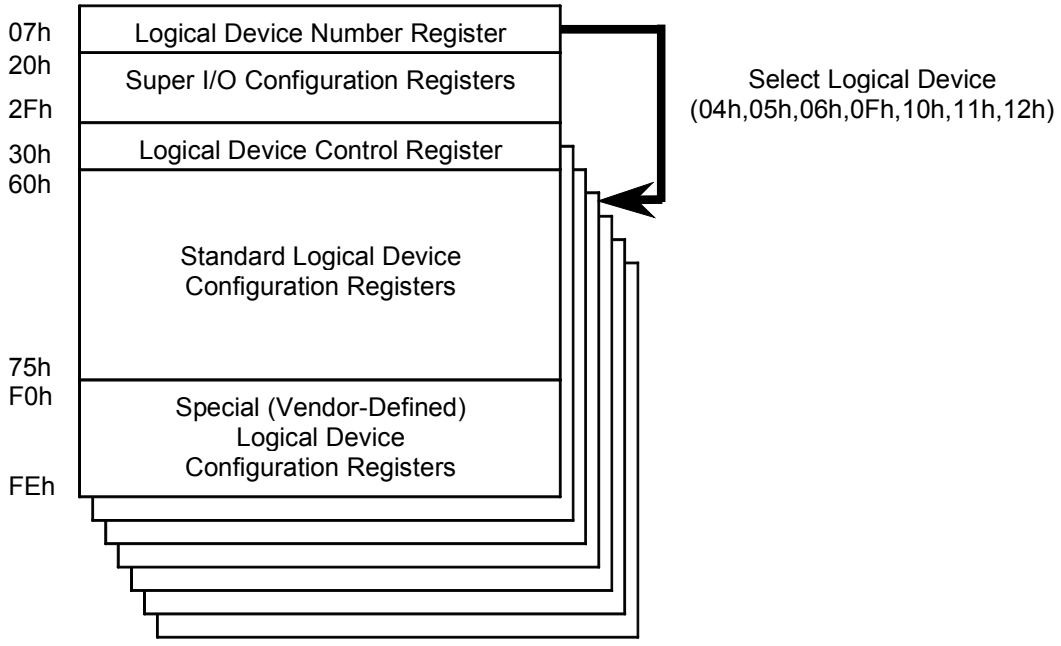


Figure 6-1. Host View Register Map via Index-Data Pair

6.2.2 Super I/O Configuration Registers

Registers with index from 07h to 2Eh contain Super I/O configuration settings.

6.2.2.1 Logical Device Number (LDN)

This register contains general Super I/O configurations.

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	04h	**Logical Device Number (LDN)** This register selects the current logical device. Valid values are 04h, 05h, 06h, 0Fh, 10h, 11h and 12h. All other values are reserved.

6.2.2.2 Chip ID Byte 1 (CHIPID1)

Index: 20h

Bit	R/W	Default	Description
7-0	R	85h	**Chip ID Byte 1 (CHIPID1)** This register contains the Chip ID byte 1.

6.2.2.3 Chip ID Byte 2 (CHIPID2)

Index: 21h

Bit	R/W	Default	Description
7-0	R	10h	**Chip ID Byte 2 (CHIPID2)** This register contains the Chip ID byte 2.

6.2.2.4 Chip Version (CHIPVER)

This register contains revision ID of this chip

Index: 22h

Bit	R/W	Default	Description
7-0	R	21h	**Chip Version (CHIPVER)**

6.2.2.5 Super I/O Control Register (SIOCTRL)

This register contains general Super I/O configurations.

Index: 23h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-4	-	0h	**Reserved**
3-2	-	0h	**Reserved**
1	W	0b	**Software Reset (SIOSWRST)** Read always returns 0. 0: No action. 1: Software Reset the logical devices.
0	R/W	1b	**Super I/O Enable (SIOEN)** 0: All Super I/O logical devices are disabled, except SWUC and SMFI. 1: Each Super I/O logical device is enabled according to its Activate register. (Index 30h)

6.2.2.6 Super I/O IRQ Configuration Register (SIOIRQ)

This register contains general Super I/O configurations.

Index: 25h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0b	**SMI# to IRQ2 Enable (SMI2IRQ2)** This bit enables using IRQ number 2 in the SERIRQ protocol as a SMI# interrupt. This bit is similar to LDACT bit in LDA register. 0: Disabled 1: Enabled
3-0	-	0h	**Reserved**

6.2.2.7 Super I/O General Purpose Register (SIOGP)

This register contains general Super I/O configurations.

Index: 26h

Bit	R/W	Default	Description
7	R/W	0b	**SIOGP Software Lock (SC6SLK)** 0: Writing to bits 0-6 of SIOGP is allowed. Other bits in this register can be cleared by Hardware and Software reset (SIOSWRST). 1: Not allowed. Bits 6-0 of this register are read-only. All bits in this register can be cleared by Hardware reset only.
6-5	R/W	00b	**General-Purpose Scratch (GPSCR)** Reading returns the value that was previously written. Note that the EC side can access whole PNPCFG registers via EC2I.
4	R/W	0b	**RTC Disabled (RTCDE)** 0: RTC is enabled according to its Activate register and SIOEN bit in SIOCTRL register. 1: Disabled
3-0	-	0h	**Reserved**

6.2.2.8 Super I/O Power Mode Register (SIOPWR)

This register is a battery-backed register used by the EC side. See also 6.4.5.2.

Index: 2Dh

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0b	**Power Supply Off (PWRSLY)** It indicates the EC side that the host requests to shut down the power in legacy mode. Refer to SCRDPSO bit in SWCTL2 register on page 94 0: No action 1: It indicates power shut down if PWRSLY is Legacy mode. **Note:** It always returns 0 when read.
0	R/W	0h	**Power Button Mode (PWRBTN)** This bit controls the power button mode in the SWUC. Refer to SCRDPBM bit in SWCTL2 register on page 94 0: Legacy 1: ACPI

6.2.3 Standard Logical Device Configuration Registers

Registers with index from 30h to F9h contain Logical Device configuration settings. LDN of the wanted logical device should be written to LDN register before accessing these registers.
This section lists a standard description of these registers. Some default values for each register and more detailed information for each logical device should be referred in each section.

6.2.3.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-1	-	0h	**Reserved**
0	R/W	0b	**Logical Device Activation Control (LDACT)** 0: Disabled The registers (Index 60h-FEh) are not accessible. Refer to SIOEN bit in SIOCTRL 1: Enabled

6.2.3.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 0.

6.2.3.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 0.

6.2.3.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register will be read-only if it is unused by a logical device.
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBA[15:8])** This register indicates selected I/O base address bits 15-8 for I/O Descriptor 1.

6.2.3.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

This register will be read-only if it is unused by a logical device
The 16-bit base address must not be 0000h and might have the boundary limit for each logical device.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	Depend on Logical Device	**I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBA[7:0])** This register indicates selected I/O base address bits 7-0 for I/O Descriptor 1.

6.2.3.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register will be read-only if it is unused by a logical device.

Index: 70h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0	**Wake-Up IRQ Enable (WKIRQEN)** Allow this logical device to trigger a wake-up event to SWUC. This bit should not be set in SWUC Logical Device since it is used to collect IRQ sources for SWUC. 0: Disabled 1: Enabled
3-0	R/W	Depend on Logical Device	**IRQ Number (IRQNUM)** Select the IRQ number (level) asserted by this logical device via SERIRQ. 00d: This logical device doesn't use IRQ. 01d-012d: IRQ1-12 are selected correspondingly. 14d-15d: IRQ14-15 are selected correspondingly. Otherwise: Invalid IRQ routing configuration.

6.2.3.7 Interrupt Request Type Select (IRQTP)

This register will be read-only if it is unused by a logical device.

Index: 71h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	Depend on Logical Device	**Interrupt Request Polarity Select (IRQPS)** This bit indicates the polarity of the interrupt request. 0: IRQ request is buffered and applied on SERIRQ. 1: IRQ request is inverted before being applied on SERIRQ. This bit should be configured before the logical device is activated.
0	R/W	Depend on Logical Device	**Interrupt Request Triggered Mode Select (IRQTMS)** This bit indicates that edge or level triggered mode is used by this logical device and should be updated by EC firmware via EC2I since the triggered mode is configured in EC side registers. This bit is just read as previously written (scratch register bit) and doesn't affect SERIRQ operation. 0: edge triggered mode 1: level triggered mode

6.2.3.8 DMA Channel Select 0 (DMAS0)

Index: 74h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 0** A value of 4 indicates that no DMA channel is active.

6.2.3.9 DMA Channel Select 0 (DMAS1)

Index: 75h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2-0	R	4h	**DMA Channel Select 1** A value of 4 indicates that no DMA channel is active.

6.2.4 System Wake-Up Control (SWUC) Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-7. Host View Register Map via Index-Data I/O Pair, SWUC Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 04h)	07h
Logical Device Control And Configuration Registers	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) -Unused	63h
Selected if LDN Register=04h	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.4.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.4.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.**

6.2.4.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.3 on page 51.** Bits 4-0 (IOBAD0[4:0]) are forced to 00000b and can't be written. It means the base address is on the 32-byte boundary.

6.2.4.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 51.**

6.2.4.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 52.**

6.2.4.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.6 on page 52.**

6.2.4.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.7 on page 52.**

6.2.5 KBC / Mouse Interface Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-8. Host View Register Map via Index-Data I/O Pair, KBC / Mouse Interface Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 05h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=05h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8]) –Unused	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0]) –Unused	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8]) –Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0]) –Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.5.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.5.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

This register is unused and read-only.

Index: 60h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.2 on page 51.**

6.2.5.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

This register is unused and read-only.

Index: 61h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.3 on page 51.**

6.2.5.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 51.**

6.2.5.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 52.**

6.2.5.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	0Ch	**Refer to section 6.2.3.6 on page 52.**

6.2.5.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.7 on page 52.**

6.2.6 KBC / Keyboard Interface Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-9. Host View Register Map via Index-Data I/O Pair, KBC / Keyboard Interface Logical Device

	7 0	Index
	Register Name	
Super I/O Control Reg	Logical Device Number (LDN = 06h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=06h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.6.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.6.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.6.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	60h	**Refer to section 6.2.3.3 on page 51.**

6.2.6.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 51.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.6.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	64h	**Refer to section 6.2.3.5 on page 52.**

6.2.6.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.6 on page 52.**

6.2.6.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.7 on page 52.**

6.2.7 Shared Memory/Flash Interface (SMFI) Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-10. Host View Register Map via Index-Data I/O Pair, SMFI Interface Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 0Fh)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=0Fh	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])-Unused	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])-Unused	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX) –Unused	70h
	Interrupt Request Type Select (IRQTP) -Unused	71h
	Shared Memory Configuration Register (SHMC)	F4h
	Shared Memory Base Address High Byte Register (SHMBAH)	F5h
	Shared Memory Base Address Low Byte Register (SHMBAL)	F6h
	Shared Memory Size Configuration Register (SHMSZ)	F7h
	LPC Memory Control (LPCMCTRL)	F8h

6.2.7.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.7.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.**

6.2.7.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.3 on page 51.** Bits 3-0 (IOBAD0[3:0]) are forced to 0000b and can't be written. It means the base address is on the 16-byte boundary.

6.2.7.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

This register is unused and read-only.

Index: 62h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.4 on page 51.**

6.2.7.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

This register is unused and read-only.

Index: 63h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.5 on page 52.**

6.2.7.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

This register is unused and read-only.

Index: 70h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.6 on page 52.**

6.2.7.7 Interrupt Request Type Select (IRQTP)

This register is unused and read-only.

Index: 71h

Bit	R/W	Default	Description
7-0	R	00h	**Refer to section 6.2.3.7 on page 52.**

6.2.7.8 Shared Memory Configuration Register (SHMC)

Index: F4h

Bit	R/W	Default	Description
7-4	R/W	0h	**BIOS FWH ID (FWHID)** These bits correspond to the 4-bit ID which is part of a FWH transaction.
3	R/W	Strap	**BIOS FWH Enable (FWHEN)** It enables this chip to respond to FWH access. 0: Disabled (default as SHBM = 0) 1: Enabled (default as SHBM = 1)
2	R/W	0b	**User-Defined Memory Space Enable (USRMEM)** It enables this chip to respond to LPC or FWH transactions to the user-defined memory space. Note: User-defined memory is specified by SHMBAH and SHMBAL registers.
1	R/W	0b	**BIOS Extended Space Enable (BIOSEXTS)** This bit expands the BIOS address space to make this chip response the Extended BIOS address range.
0	R/W	Strap	**BIOS LPC Enable (LPCMEN)** It enables this chip to respond to LPC Memory and Indirect Memory accesses. 0: Disabled (default as SHBM = 0) 1: Enabled (default as SHBM = 1)

6.2.7.9 Shared Memory Base Address High Byte Register (SHMBAH)

This register indicates the base address of the user-defined memory block mapped to the shared memory.

Index: F5h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared Memory Base Address High Byte (SHMBA[15:8])** It contains the high 8 bits of the base address of the user-defined memory block.

6.2.7.10 Shared Memory Base Address Low Byte Register (SHMBAL)

This register indicates the base address of the user-defined memory block mapped to the shared memory.

Index: F6h

Bit	R/W	Default	Description
7-0	R/W	00h	**Shared Memory Base Address Low Byte (SHMBA[7:0])** It contains the low 8 bits of the base address of the user-defined memory block.

6.2.7.11 Shared Memory Size Configuration Register (SHMSZ)

Index: F7h

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
3-0	R/W	00h	**User-Defined Memory Block Size (SHMUSZ)** It defines the size of zone window. Size = $2^{(SHMUZE + 16)}$ bytes, and maximum size = 2M bytes. **Exp:** **SHMUSZ Size** 0000b 64K 0001b 128K … 0101b 2M 0110b 4M Others Reserved

6.2.7.12 LPC Memory Control (LPCMCTRL)

Normally the M-bus grant parks on 8032 side for code fetch and switches to LPC side if memory transactions on LPC bus. To improve the host memory access performance, the M-bus grant parks on LPC side temporarily during LPC Burst Window.

LPC Burst Window starts from the time when CLPCBT counts of “Continuous” LPC memory cycles are seen by IT8510 and stops at the time when a “Non-continuous” LPC memory cycles are detected.

LPC memory cycles are “Continuous” if the Idle count between two LPC memory cycles is smaller than LPCIT clocks.

Index: F8h

Bit	R/W	Default	Description
7-6	-	-	**Reserved**
5-4	R/W	01b	**Continuous LPC Burst Threshold (CLPCBT)** Define the threshold count to start LPC Burst Window. 00b: 1 Continuous LPC cycle 01b: 5 Continuous LPC cycles 10b: 9 Continuous LPC cycles 11b: 13 Continuous LPC cycles
3-0	R/W	1000b	**LPC Idle Threshold (LPCIT)** Define the threshold count to be a “Continuous” LPC memory access. 0000b: Disable LPC Burst Otherwise: LPCIT*4 + 3 clocks (7 ~ 59 clocks) Default value is 35 clock Note LPC Burst is controlled by DLPCB bit in FPCFG register, too.

6.2.8 Real Time Clock (RTC) Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-11. Host View Register Map via Index-Data I/O Pair, RTC Logical Device

	7 Register Name 0	Index
Super I/O Control Reg	Logical Device Number (LDN = 10h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=10h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h
	RAM Lock Register (RLR)	F0h
	Date of Month Alarm Register Offset (DOMAO)	F1h
	Month Alarm Register Offset (MONAO)	F2h

6.2.8.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.** Refer to SIOEN bit in SIOCTRL and SIOEN bit in SIOCTRL Register.

6.2.8.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.**

6.2.8.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	70h	**Refer to section 6.2.3.3 on page 51.** Bit 0 (IOBAD0[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.2.8.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 51.**

6.2.8.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	72h	**Refer to section 6.2.3.5 on page 52.** Bit 0 (IOBAD0[0]) is forced to 0b and can't be written. It means the base address is on the 2-byte boundary.

6.2.8.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	08h	**Refer to section 6.2.3.6 on page 52.**

6.2.8.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.7 on page 52.**

6.2.8.8 RAM Lock Register (RLR)

Index: F0h

Bit	R/W	Default	Description
7	R/W	0b	**Block Standard RAM R/W (CMOSSRW)** 0: R/W to 38h-3Fh of the Standard RAM is allowed. 1: Not allowed. Writes are ignored and reads return FFh.
6	R/W	0b	**Block RAM Write (CMOSW)** 0: Write to Standard and Extended RAM is allowed. 1: Not allowed. Writes are ignored.
5	R/W	0b	**Block Extended RAM Write (CMOSEW)** 0: Write to bytes 00h-1Fh of the Extended RAM is allowed. 1: Not allowed. Writes are ignored.
4	R/W	0b	**Block Extended RAM Read (CMOSER)** 0: Read from bytes 00h-1Fh of the Extended RAM is allowed. 1: Not allowed. Reads return FFh.
3	R/W	0b	**Block Extended RAM R/W (CMOSERW)** 0: R/W to the Extended RAM 128 bytes is allowed. 1: Not allowed. Writes are ignored and reads return FFh
2-0	-	0h	**Reserved**

6.2.8.9 Date of Month Alarm Register Offset (DOMAO)

Index: F1h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	49h	**Date of Month Alarm Register Offset (DOMAO)** It contains the index offset of "date of month alarm".

6.2.8.10 Month Alarm Register Offset (MONAO)

Index: F2h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6-0	R/W	4Ah	**Month Alarm Register Offset (MONAO)** It contains the index offset of “month alarm”.

6.2.9 Power Management I/F Channel 1 Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-12. Host View Register Map via Index-Data I/O, PM1 Logical Device

	7 … 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 11h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=11h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.9.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.9.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can’t be written.

6.2.9.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	62h	**Refer to section 6.2.3.3 on page 51.**

6.2.9.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 51.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.9.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	66h	**Refer to section 6.2.3.5 on page 52.**

6.2.9.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
3-0	R/W	01h	**Refer to section 6.2.3.6 on page 52.**

6.2.9.7 Interrupt Request Type Select (IRQTP)

Index: 71h

Bit	R/W	Default	Description
7-2	R/W	03h	**Refer to section 6.2.3.7 on page 52.**

6.2.10 Power Management I/F Channel 2 Configuration Registers

This section lists default values for each register and more detailed information for this logical device. Some register bits will be read-only if unused.

Table 6-13. Host View Register Map via Index-Data I/O, PM2 Logical Device

	7 0 Register Name	Index
Super I/O Control Reg	Logical Device Number (LDN = 12h)	07h
Logical Device Control And Configuration Registers Selected if LDN Register=12h	Logical Device Activate Register (LDA)	30h
	I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])	60h
	I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])	61h
	I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])	62h
	I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD1[7:0])	63h
	Interrupt Request Number and Wake-Up on IRQ Enabled (IRQNUMX)	70h
	Interrupt Request Type Select (IRQTP)	71h

6.2.10.1 Logical Device Activate Register (LDA)

Index: 30h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.1 on page 51.**

6.2.10.2 I/O Port Base Address Bits [15:8] for Descriptor 0 (IOBAD0[15:8])

It contains Data Register Base Address Register.

Index: 60h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.2 on page 51.** Bits 7-3 (IOBAD0[15:11]) are forced to 00000b and can't be written.

6.2.10.3 I/O Port Base Address Bits [7:0] for Descriptor 0 (IOBAD0[7:0])

It contains Data Register Base Address Register.

Index: 61h

Bit	R/W	Default	Description
7-0	R/W	68h	**Refer to section 6.2.3.3 on page 51.**

6.2.10.4 I/O Port Base Address Bits [15:8] for Descriptor 1 (IOBAD1[15:8])

It contains Command/Status Register Base Address Register.

Index: 62h

Bit	R/W	Default	Description
7-0	R/W	00h	**Refer to section 6.2.3.4 on page 51.** Bits 7-3 (IOBAD1[15:11]) are forced to 00000b and can't be written.

6.2.10.5 I/O Port Base Address Bits [7:0] for Descriptor 1 (IOBAD0[7:0])

It contains Command/Status Register Base Address Register.

Index: 63h

Bit	R/W	Default	Description
7-0	R/W	6Ch	**Refer to section 6.2.3.5 on page 52.**

6.2.10.6 Interrupt Request Number and Wake-Up on IRQ Enable (IRQNUMX)

Index: 70h

Bit	R/W	Default	Description
7-0	R/W	01h	**Refer to section 6.2.3.6 on page 52.**

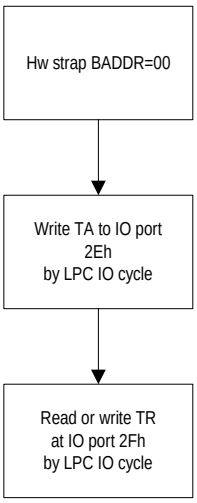
6.2.10.7 Interrupt Request Type Select (IRQTP)

Index: 71h

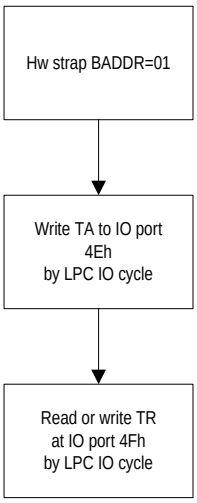
Bit	R/W	Default	Description
7-0	R/W	03h	**Refer to section 6.2.3.7 on page 52.**

6.2.11 Programming Guide

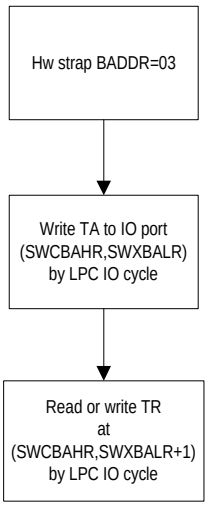
Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 1



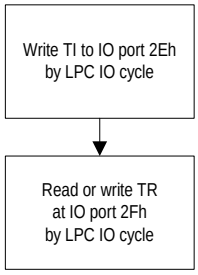
Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 2



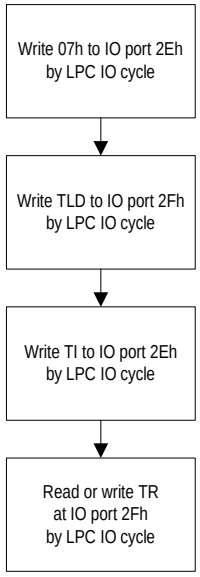
Host Side
To read or write the target register (TR)
at target address(TA) of PNPCFG
Approach 3



Host Side
To read or write the target register (TR)
at target Index (TI) of PNPCFG
TI = 00h~2Eh
(Assume BADDR=00)



Host Side
To read or write the target register (TR)
at target Index(TI) of PNPCFG
TI=30h~FEh, belongs to target logical device (TLD)
(Assume BADDR=00)



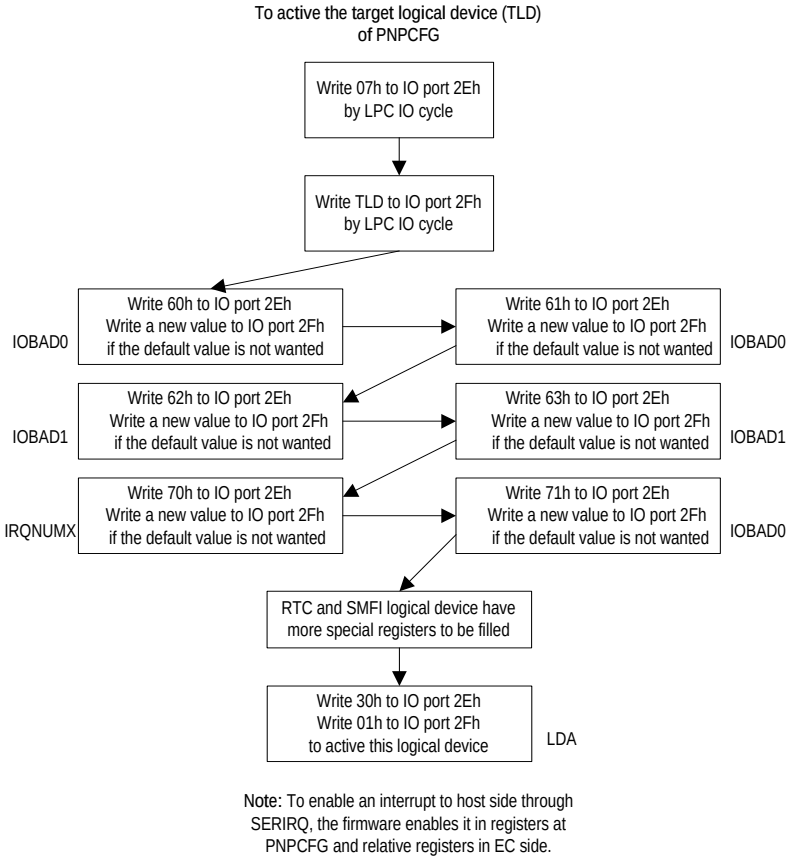


Figure 6-2. Program Flow Chart for PNPCFG

See also section 7.12.5 on page 239 for accessing PNPCFG through EC2I.

6.3 Shared Memory Flash Interface Bridge (SMFI)

6.3.1 Overview

The bridge provides the host to access the shared memory. It also provides EC code address space mapped into host domain address space, and locking mechanism for read/write protection.

6.3.2 Features

- Supports memory mapping between host domain and EC domain
- Supports read/write/erase flash operations and locking mechanism
- Supports two shared memory access paths: host and EC
- Supports two flash contents protection: different access paths and different memory block
- Supports timing control for memory device (flash)

6.3.3 Function Description

6.3.3.1 Flash Requirement

"Read Cycle Time" and "Write Cycle Time" of the flash/EPROM have to be faster than or equal to $\mathbf{t}_{FRDD}$ (Refer to Table 9-8. Flash Read Cycle AC Table).

6.3.3.2 Host to M Bus Translation

The SMFI provides an interface between the host bus and the M bus, the flash is mapped into the host memory address space for host accesses, the flash is also mapped into the EC memory address space for EC accesses.
An M bus transaction is generated by the host bus translations and has the following three types:

- 8-bit LPC Memory Read/Write
- 8-bit FWH Read/Write
- 8-bit Indirect Memory Read/Write

After the LPC address translation is done, the host memory transaction is forwarded to M-bus (flash interface) if it is accessing an unprotected region. The host side can't issue a write transaction until the firmware write 1 to HOSTWA bit SMECCS register. See also Table 3-3 on page 8 and Table 3-4 on page 8.

Note: The flash bus doesn't have the highest performance until writing 00h to MZCFG register and 08h to SMZCFG register.

6.3.3.3 Memory Mapping

The host memory addresses are mapped into the following regions shown in the following table. Some regions are always mapped and some are mapped only when the corresponding register is active. And these regions may be mapped into the same range in the flash space. See also Table 3-1 on page 8.

Table 6-14. Mapped Host Memory Address

Memory Address Range (byte)	Region Description
FFC0_0000h-FFFF_FFFFh	**386 Mode BIOS Range** This is the memory space whose maximum value is up to 4M bytes. If the flash size defined in FMSSR register is smaller than 4M bytes, the remaining space is treated as "Out of Range"
000F_0000h-000F_FFFFh	**Legacy BIOS Range** The total is 64K inside lower 1M legacy BIOS range.
000E_0000h-000E_FFFFh	**Extended Legacy BIOS Range** The total is 64K inside lower 1M legacy BIOS range.

Following memory transactions are based on LPC, FWH or I/O Cycles which are valid only when corresponding LPCMEN/FWHEN bit in SHMC register is enabled.

Legacy BIOS Range
Always handle.

Extended Legacy BIOS Range
Handle only when BIOSEXTS bit in SHMC register is active. Otherwise, transactions are ignored.

386 Mode BIOS Range
Always handle.

User-Defined Shared Memory Space
Handle only when USRMEM bit in SHMC register is active. Otherwise, transactions are ignored.

Indirect Memory Address
Indirect Memory Cycles are memory transactions based on LPC I/O Cycles.
This address specified in SMIMAR3-0 is used as follows:
Translated 32-bit host address = { SMIMAR3[7:0], SMIMAR2[7:0], SMIMAR1[7;0], SMIMAR0[7:0]}

6.3.3.4 Indirect Memory Read/Write Transaction

The following I/O mapped registers can be used to perform an M bus transaction using an LPC I/O transaction:

- **Indirect Memory Address registers (SMIMAR 3-0)**

Stand for host address bit 31 to 0.

- **Indirect Memory Data register (SMIMDR)**

Stand for read or write data bit 7 to 0.

When LPC I/O writes to IMD register, SMFI begins a flash read with SMIMAR3-0 as the addresses. IT8510 responses Long-Waits until the transaction on M-bus (flash interface) is completed.
When LPC I/O read cycle from SMIMDR register begins a flash write with using the SMIMAR3-0 as the address. The data back from SMIMDR register is used to complete the LPC I/O read cycle.
The indirect memory read/write transactions use the same memory mapping and locking mechanism as the LPC memory read/write transactions.

6.3.3.5 Locking Between Host and EC Domains

A hardware arbiter handles flash read/write translation between the host and EC side. Normally the grant is parked on the EC side and switches to the host side when the memory transaction on LPC bus (see also section 6.2.7.12 and 6.3.3.9).

If the EC side is code fetching, any host access will be deferred or aborted depending on HERES bit in SMECCS register.
If the host side is accessing, the EC side is pending to code fetch.
When the host wants to erase or program the flash, the signaling interface (Semaphore Write or KBC/PMC extended command) notifies the firmware to write 1 to HOSTWA bit in SMECCS register and relative register listed in Table 3-3 on page 8. EC 8032 should fail to code fetch due to flash busying for erasing/programming and Scratch ROM should be applied (see also section 6.3.3.8). Once the host accessing to the flash is completed, the host should indicate this to the EC, allowing EC to clear HOSTWA bit and resume normal operation. The EC can clear HOSTWA bit at any time, and prevent the host from issuing any erase or program operations.

6.3.3.6 Host Access Protection

The software can use a set of registers to control the host read/write protection functionality. The protection block can be divided into two types: 8k size and 64k size; the block's read/write protection flags may be set individuality. A Lock Protect flag may prevent read/write protection flag from changing in the future.

Once locked, the lock bit and the read/write enable bits may be restored only after host domain hardware reset. The EC can override the host settings and prevent host access to certain regions of the shared memory. The override may be set individuality for read and write. In the first 128 Kbytes of address space, each EC-controlled block is 8 Kbytes. For the rest of the memory space, the blocks are 64 Kbytes each.

See Table 3-4 on page 8 for the details.

After reset, all memory ranges are allowed host read but inhibited to write (erase/program).

6.3.3.7 Response to a Forbidden Access

A forbidden access is generated by a translated host address which is protected.
The EC responds to a forbidden access by generating an interrupt INT23 (if enabled by HERRIEN bit in SMECCS register). HWERR and HRERR in the SMECCS register indicate the forbidden access to write or read respectively .The response on the host bus is according to the HERES set in the SMECSS.

BIT(HERES):
00: Drive Long Wait for read; ignore write
01: Read back 00h; ignore write
10: Drive error SYNC for both read and write
11: Read back long sync; write back error sync

6.3.3.8 Scratch SRAM

This SRAM is scratch SRAM, which can be located at data space or code space (BUT not the same time).
Where it is located depends on Scratch SRAM Map Control (SSMC) in FBCFG register. It is called Scratch RAM when being located at data space and called Scratch ROM when being located at code space.
Scratch ROM is mapped to the top of 2KB of EC code size, that is, 62K ~ 64K.
Code space of 0K ~ 62K is always mapped into the external flash space.
Code space of 62K ~ 64K may be mapped into the external flash space or Scratch ROM.
Refer to
Figure 3-3 on page 9 for the details.

Application:
When programming flash is processing, the flash will be busy and code fetch from flash by 8032 and will be invalid and cause 8032 fail to execute instructions. It means the firmware must copy necessary instructions from code space (by MOVC instruction) to Scratch SRAM, switch Scratch SRAM to Scratch ROM, and jump to Scratch ROM before programming flash.

Flash Programming Steps:
(a) The host side communicates to EC side via KBC/PMC extended or semaphore registers
(b) EC side: Write 1 to HOSTWA bit in SMECCS register
(c) EC side: Write 0 to SMECOWPR0-9 (for example, 4-M bytes range)
(Write is allowed in host side, and read is allowed in default.)
(Refer to Table 3-3. Flash Read/Write Protection Controlled by EC Side on page 8)
(d) EC side: Copy necessary code to Scratch RAM
(e) EC side: Make the host processor enter SMM mode if necessary
(f) EC side: Switch to Scratch ROM by SSMC bit in FBCFG register
(g) EC side: Jump instruction to Scratch ROM
(h) Host side: Remove protection in the host side
(Refer to Table 3-4. Flash Read/Write Protection Controlled by Host Side on page 8)
(i) Host side: Set relative memory-write registers in South-Bridge
(j) Host side: Start flash programming
(k) End flash programming and reset EC domain if necessary.
(Refer to section 5.5 on page 29)

6.3.3.9 No-wait Mode

Normally the M-bus grant parks on the 8032 side for code fetch and switches to the LPC side if memory transactions on LPC bus. No-wait mode and Wait mode defines how M-bus grants to LPC side. IT8510 drives Long-Wait sync until flash data is ready.

No-wait mode: All is hardware implemented and flash access switch to LPC Memory/FWH access immediately if requested regardless of firmware. The firmware must enter No-wait mode before entering Idle/Doze/Sleep mode.

Table 6-15. M-bus Grant Behavior

M-bus Grant Status	Description	Register Configuration	Note
Interleave	M-bus grant parks on EC side and switches to host side (LPC) back and forth if the host side issues memory access.	To prevent entering “LPC Burst” status, assign the value of LPCIT field in LPCMCTRL register as 0000b.	
LPC Burst	Host side (LPC) owns the M-bus for a while and EC side cannot access at the same time. If host side (LPC) starts memory access, this status will be entered from “EC Occupy” status with Idle/Doze mode or Interleave status and it automatically exists when host side stops memory access.	The value of LPCIT field in LPCMCTRL register is greater than 0000b.	
Concurrent	Host side owns the M-bus and EC executes code-fetch from Scratch ROM at the same time.	SSMC bit in FBCFG register is 1b. (Scratch ROM)	Scratch RAM is not available when Scratch ROM mode.

6.3.3.10 Flash Interface

- Late Write and Early Write

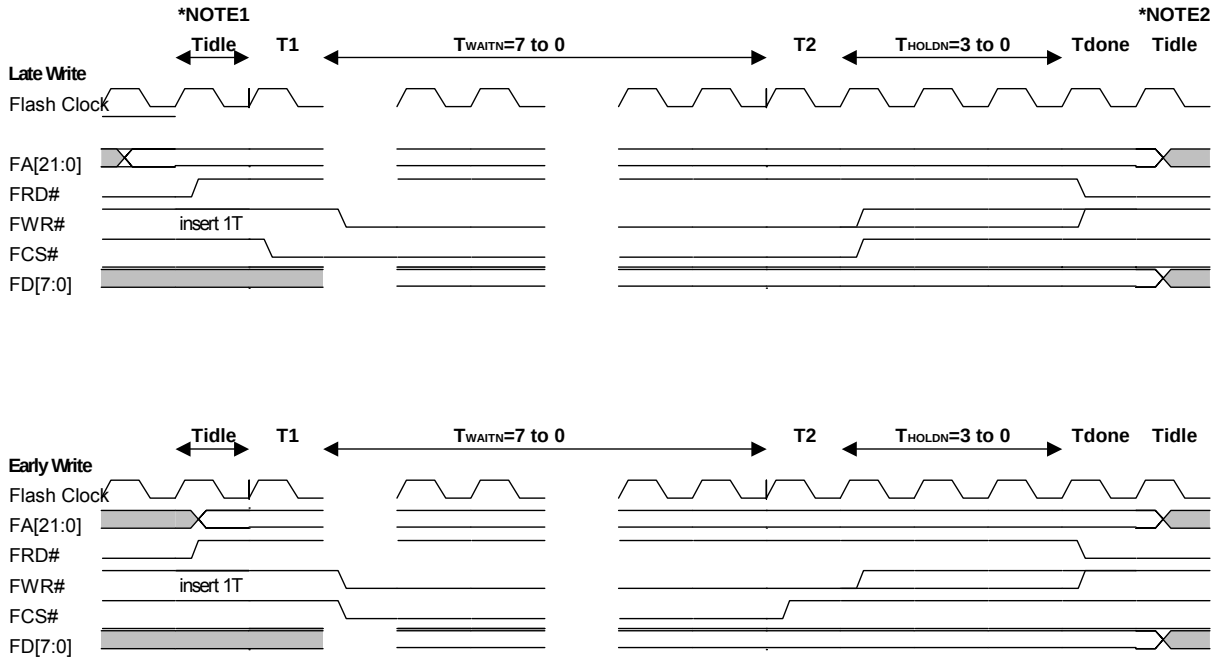


Figure 6-3. Late Write and Early Write

- Fast Read and Normal Read

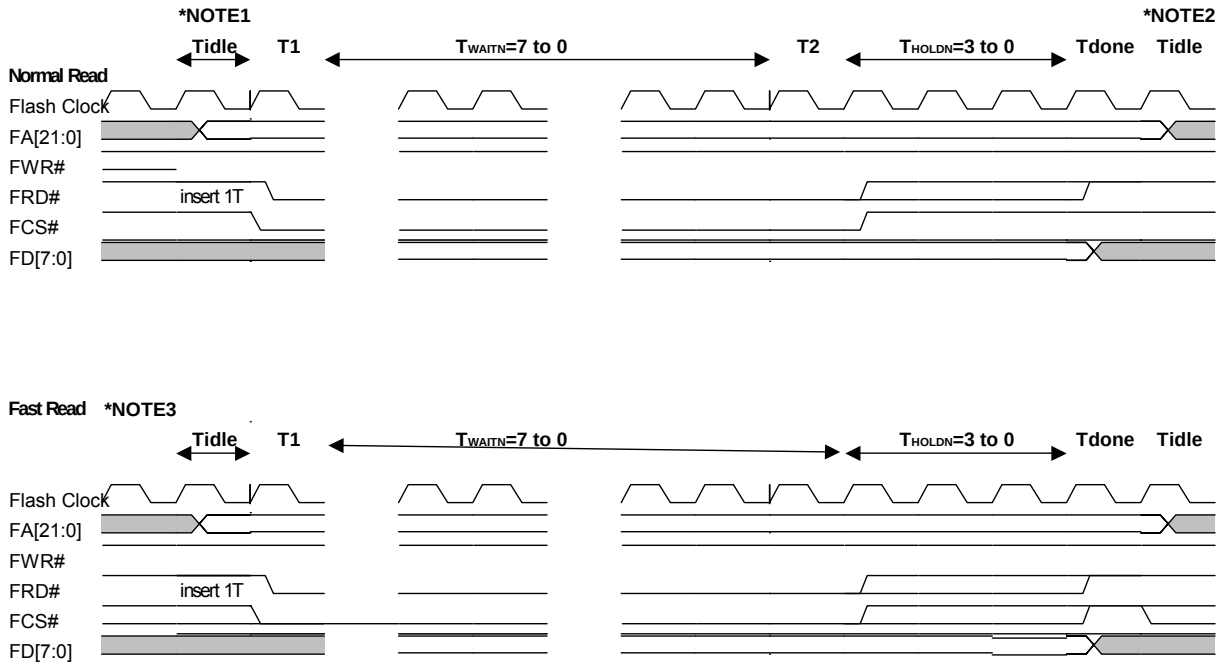


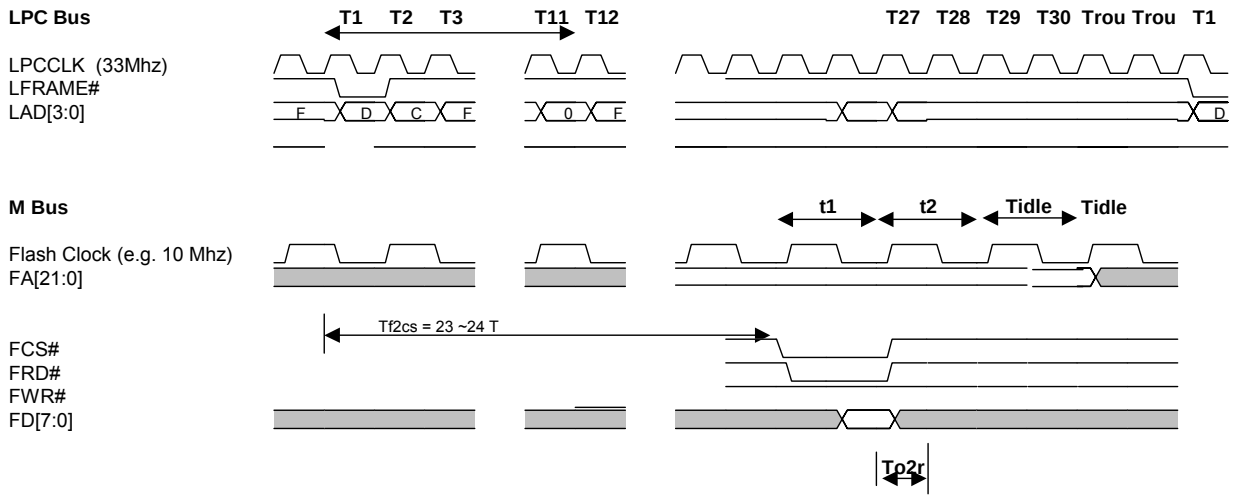
Figure 6-4. Fast Read and Normal Read

Note 1: Tidle cycle inserted when ICBBC = 1 in SMZCFG register.
Note 2: Tidle cycle inserted when ICABC = 1 in SMZCFG register.
Note 3: Fast Read cycles represent when FRE = 1 in SMZCFG register
Note 4:

Flash Clock Frequency = (EC Clock Frequency) / (FTDIV +1)
T_{WAITN} = WAITN value in MZCFG register
T_{HOLDN} = HOLDN value in MZCFG register

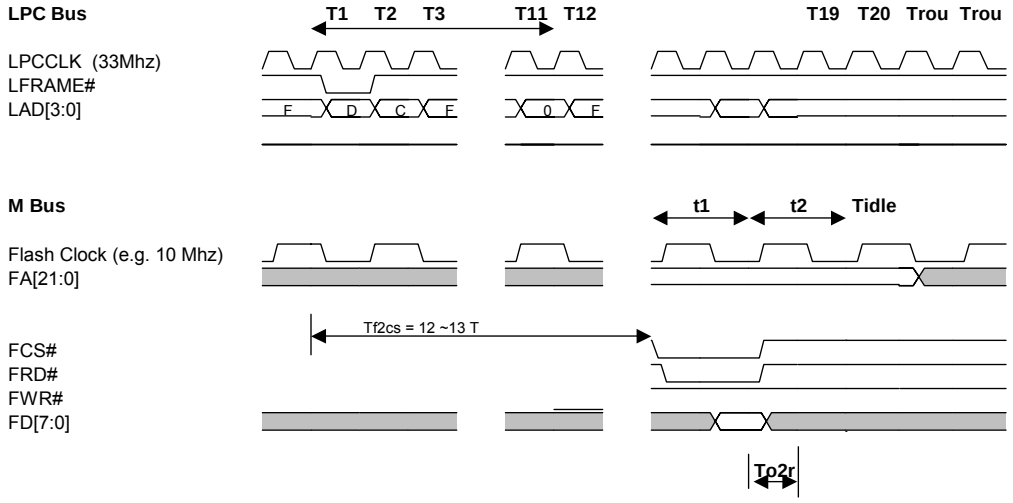
- Host Memory Read/Write Minimum Latency

The followings are the performance of host memory access, which is based on 10 MHz EC clock.
The firmware should detect the host side status by LPCRST# or others, and switch EC clock to the highest 10 MHz to get the best performance of host memory access.



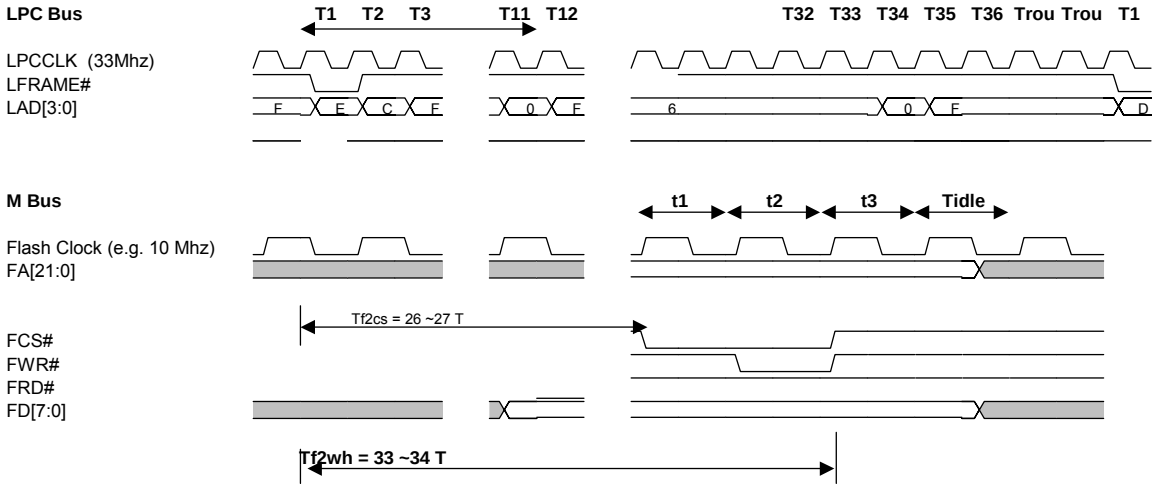
Note :
1. Tf2a denote lpc frame assert to lpc memory address ready, need 10 ~11 T (LPC Clock)
2. Tf2cs denote lpc frame assert to flash chip select active, need 23 ~24 T (LPC Clock)
3. To2r denote flash read data output to first LPC nibble read data output, need 1 ~2 T (LPC Clock)
4. Clk_fls is programmed into clk_ec (FMPSR register set to 0) ;
   Hold time/Wait time is set to 0 (FBCFG=02h; MZCFG=0h; SMZCFG=08H); in no-wait mode;

Figure 6-5. Minimum Latency Timing of Flash Memory Read Cycle



Note : 1. Tf2a denote lpc frame assert to lpc memory address ready, need 10 ~11 T (LPC Clock)
2. Tf2cs denote lpc frame assert to flash chip select active, need 12~13T (LPC Clock)
3. To2r denote flash read data output to first LPC nibble read data output, need 1 ~2 T (LPC Clock)
4. Clk_fls is programmed into clk_ec (FMPSR register set to 0) ;
Hold time/Wait time is set to 0 (FBCFG=02h; MZCFG=0h; SMZCFG=08H); in no-wait mode;

Figure 6-6. Minimum Latency Timing of Flash Memory Read Cycle in LPC Burst



Note : 1. Tf2a denote lpc frame assert to lpc memory address ready, need 10 ~11 T (LPC Clock)
2. Tf2cs denote lpc frame assert to flash chip select active, need 26 ~27 T (LPC Clock)
3. Tf2wh denote lpc frame assert to flash write go high, need 33 ~34 T (LPC Clock)
4. Clk_fls is programmed into clk_ec (FMPSR register set to 0) ;
Hold time/Wait time is set to 0 (FBCFG=02h; MZCFG=0h; SMZCFG=08H); in no-wait mode;

Figure 6-7. Minimum Latency Timing of Flash Memory Write Cycle

6.3.4 EC Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for SMFI is 1000h.

These registers are listed below.

Table 6-16. EC View Register Map, SMFI

7 — 0	Offset
FBIU Configuration (FBCFG)	00h
Flash Programming Configuration Register (FPCFG)	01h
Memory Zone Configuration (MZCFG)	02h
State Memory Zone Configuration (SMZCFG)	03h
Flash EC Code Banking Select Register (FECBSR)	05h
Flash Memory Size Select Register (FMSSR)	07h
Flash Memory Prescaler (FMPSR)	10h
Shared Memory EC Control and Status (SMECCS)	20h
Shared Memory Host Semaphore (SMHSR)	22h
Shared Memory EC Override Read Protect (SMECORPR0-5)	23h-28h
Shared Memory EC Override Read Protect (SMECORPR6-9)	11h-14h
Shared Memory EC Override Write Protect (SMECOWPR0-5)	29h-2Eh
Shared Memory EC Override Write Protect (SMECOWPR6-9)	15h-18h

6.3.4.1 FBIU Configuration Register (FBCFG)

The FBIU (Flash Bus Interface Unit) directly interfaces with the flash device. The FBIU also defines the access time to the flash base address from 00_0000h to 3F_FFFFh (4M bytes). EWR bit controls memory cycles on M-bus (flash interface).

Address Offset: 00h

Bit	R/W	Default	Description
7	-	0b	**Scratch SRAM Map Control (SSMC)** 0: Scratch RAM (data space). 1: Scratch ROM (code space).
6	-	0h	**Override Hardware Strap SHBM (OVRSHBM)** Override hardware strap SHBM and always treat its result as 1.
5	-	0h	**Override Hardware Strap BADDR1-0 (OVRBADDR)** Override hardware strap BADDR1-0 and always treat its result as 10b.
4-2	-	0h	**Reversed**
1	R/W	1b	**Reversed** Always writing 1 to this bit.
0	R/W	1b	**Early Write (EWR)** 0: Late write. 1: Early write.

6.3.4.2 Flash Programming Configuration Register (FPCFG)

This register provides general control on banking and flash standby.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	1b	**Banking Source Option (BSO)** 0: Use 8032 P1[0] and P1[1] as code banking source. 1: Use ECBB[1:0] in FECBSR register as code banking source. Using P1 as banking source has less instruction count since only "MOV" is invoked rather than "MOVX", although T2 and T2EX are used in other bits in P2.
6	R/W	1b	**Auto Flash Standby (AFSTBY)** 1: Make the flash enter the standby mode by driving FCS# high when EC is in the Idle/Doze/Sleep mode 0: Prevent the flash from entering the standby mode
5	R/W	1b	**Reserved**
4	R/W	1b	**Disable LPC Burst (DLPCB)** 0: LPC Burst mode is dependent on LPCMCTRL register in the host side. 1: LPC Burst mode is disabled. (default)
3-1	R/W	1111b	**Reserved**
0	R/W	1b	**Host Side Protection Disable(HSPD)** 0: Host side protection disabled, all read and write protection bits are ignored in SMHAPR1~4 register. 1: Host side protection enabled, all read and write protection bits can protect their memory block in SMHAPR1~4 register

6.3.4.3 Memory Zone Configuration Register (MZCFG)

The MZCFG register controls the configuration of the memory cycles on M-bus (flash interface).
Note: The flash bus doesn't have the highest performance until writing 00h to MZCFG register and 08h to SMZCFG register.

Address Offset: 02h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	1b	**Wait on Burst Read (WBR)** When set 1, one wait state (TBW) is added on a burst read cycle. 0: No TBW 1: TBW
5	R/W	0b	**Reserved**
4-3	R/W	11b	**Hold Number (HOLDN)** Number of Thold clock cycles. 4-3 Number 000 : none 001 : One 010 : Two 011 : Three(default)

Bit	R/W	Default	Description
2-0	R/W	111b	**Wait Number (WAITN)** Number of TIW clock cycles The following bits are invalid when the FRE bit in SMZCFG register is set to1. 2-0 Number 000 : none 001 : One 010 : Two 011 : Three 100 : Four 101 : Five 110 : Six 111 : Seven(default)

6.3.4.4 Static Memory Zone Configuration Register (SMZCFG)

The SMZCFG register also controls the configuration of the memory cycles on M-bus (flash interface).
Note: The flash bus doesn't have the highest performance until writing 00h to MZCFG register and 08h to SMZCFG register.

Address Offset: 03h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	R/W	0b	**Fast Read Enable (FRE)** 0: Normal read cycle takes at least two clock cycles 1: Normal read cycle takes one clock cycles
2	R/W	1b	**Idle Clock Before Bus Cycle (ICBBC)** Inserts an idle clock before the current cycle when the next cycle is in a different zone. 0: No idle cycle inserted 1: idle cycle inserted
1	R/W	1b	**Idle Clock After Bus Cycle (ICABC)** Insert an idle clock followed the current cycle when the next cycle is in a different zone. 0: No idle cycle inserted 1: Idle cycle inserted
0	-	0b	**Reserved**

6.3.4.5 Flash EC Code Banking Select Register (FECBSR)

The register is used to select EC banking area Bank 0~3 when BSO =1 in FPCFG register.

Address Offset: 05h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**EC Banking Block (ECBB)** When ECBB is set to 00, EC code uses conventional code area (maximum 64k) as code memory. Common Bank 32k-byte flash mapping range is from 00_0000h to 00_7FFFh. Bank 0 32k-byte flash mapping range is from 00_8000h to 00_FFFFh. Bank 1 32k-byte flash mapping range is from 01_0000h to 01_7FFFh. Bank 2 32k-byte flash mapping range is from 01_8000h to 01_FFFFh. Bank 3 32k-byte flash mapping range is from 02_0000h to 02_7FFFh. See also Figure 3-1 on page 6. Bits 1-0: 00: Select Common Bank + Bank 0 01: Select Common Bank + Bank 1 10: Select Common Bank + Bank 2 11: Select Common Bank + Bank 3 If A15 of 8032 code memory equals to 0, select Common Bank, otherwise select Bank 0, 1, 2 or 3.

6.3.4.6 Flash Memory Size Select Register (FMSSR)

The register provides the selection for the external flash memory size and the minimum size of the flash is defined as 128K byte.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	111111b	**Flash Memory Size Select (FMSS)** These bits select the external flash memory size and the maximum memory size is 4M bytes. **Bits** **5 4 3 2 1 0 Memory Size** 1 1 1 1 1 1: 4M 0 1 1 1 1 1: 2M 0 0 1 1 1 1: 1M 0 0 0 1 1 1: 512K 0 0 0 0 1 1: 256K 0 0 0 0 0 1: 128K Other: Reserved

6.3.4.7 Flash Memory Prescaler Register (FMPSR)

This register selects the prescaler divider ratio. The value of the register is used to divide the EC clock.

Address Offset: 10h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3-0	R/W	0h	**Prescaler Divider Value (FTDIV)** This register value divides the EC clock into flash clock Frequency. Flash Clock Frequency = (EC Clock Frequency) / (FTDIV +1) Normally the EC clock frequency is 10 MHz and may be divided by CFSELR register. The valid FTDIV range is 0 to 15.

6.3.4.8 Shared Memory EC Control and Status Register (SMECCS)

The following set of registers is accessible only by the EC. The registers are applied to VSTBY.
This register provides the flash control and status of a restricted access.

Address Offset: 20h

Bit	R/W	Default	Description
7	R/W	0b	**Host Semaphore Interrupt Enable (HSEMIE)** It enables interrupt to 8032 via INT22 of INTC. 0: Disable the host semaphore (write) interrupt to the EC. 1: The interrupt is set (level high) if HSEMW bit is set.
6	R/WC	0b	**Host Semaphore Write (HSEMW)** 0: Host has not written to HSEM3-0 field in SMHSR register. 1: Host has written to HSEM3-0 field in SMHSR register. Writing 1 to this bit to clear itself and clear internal detect logic. Writing 0 has no effect.
5	R/W	0b	**Host Write Allow (HOSTWA)** 0: The SMFI does not generate write transactions on the M bus. 1: The SMFI can generate write transactions on the M bus.
4-3	R/W	00b	**Host Error Response (HERES)** These bits control response types on read/write translation from/to a protected address. 1-0 Number 00 : Drive Long Wait for read; ignore write 01 : Read back 00h; ignore write 10 : Drive error SYNC for both read and write 11 : Read back long sync; write back error sync
2	R/W	0b	**Host Error Interrupt Enable (HERRIEN)** It enables interrupt to 8032 via INT23 of INTC. 0: Disable 1: The interrupt is set (level high) if HRERR or HWERR bit is set.
1	R/WC	0b	**Host Write Error (HWERR)** 0: No error is detected during a host-initiated write. 1: It represents the host write to a write-protected address. Writing 1 to this bit clears it to 0. Writing 0 has no effect.
0	R/WC	0b	**Host Read Error (HRERR)** 0: No error is detected during a host-initiated read. 1: It represents the host reads to a read-protected address. Writing 1 to this bit clears it to 0. Writing 0 has no effect.

6.3.4.9 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register is reset on host domain hardware reset.
This is the register the same as the one in section 6.3.5.7 but they are in different views.

Address Offset: 22h

Bit	R/W	Default	Description
7-4	R/W	0h	**EC Semaphore (CSEM3-0)** These four bits may be written by the EC and read by both the host and the EC
3-0	R	0h	**Host Semaphore (HSEM3-0)** These four bits may be written by the host and read by both the host and the EC.

6.3.4.10 Shared Memory EC Override Read Protect Registers 0-9 (SMECORPR 0-9)

SMECORPR 0-9 are 8-bit registers that permit EC to override on the host read protection bits. To allow the host to read a memory location, both the Host Read Protection bit controlled through the SMHAPR (1-2) and the associated bit in SMECORPR 0-9 should be cleared. Each bit in this register is related with a memory block. Bits in these registers may be Read Only or RW accroding to their position and the size of the EC and host boot blocks.

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect Low Address (ORPLA7-0)**

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect Low Address (ORPLA15-8)**

Address Offset: 25h

Bit	R/W	Default	Description
7-2	R/W	00h	**Override Read Protect (ORP7-2)**
1-0	-	0h	**Reserved**

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP15-8)**

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP23-16)**

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP31-24)**

Address Offset: 11h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP39-32)**

Address Offset: 12h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP47-40)**

Address Offset: 13h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP55-48)**

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R/W	00h	**Override Read Protect (ORP63-56)** ORPLA15-0 (Override Read Protect Low Addresses 15 through 0). ORP63-2 (Override Read Protect 63 through 2). Each bit affects the host's read capacity from one block. The block size is 8 Kbytes on the first low address (ORPLAi). For the other blocks, it is 64 Kbytes. The block address is intended as follows: Low Address Blocks, ORPLAi: from i*8K to (i+1)*8K-1 Other Blocks, ORPj: from j*64K to (j+1)*64K Refer to Table 3-3 on page 8 for the details. 0: no override the host read 1: Host Read for this block is disabled regardless of the setting of others. The default values make all the flash ranges readable.

6.3.4.11 Shared Memory EC Override Write Protect Registers 0-9 (SMECOWPR0-9)

SMECOWPR0-9 are 8-bit registers that permit EC to override on the host write protection bits. For the host to be able to write a memory location, both the Host Write Protection bit (controlled through the SMHAPR (1-2) and the related bit in SMECOWPR0-9 should be cleared. Each bit in this register is related with a memory block. Bits attribute in these registers may be Read Only or RW according to their positions, and all blocks and sizes.

Address Offset: 29h

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect Low Address (OWPLA7-0)**

Address Offset: 2Ah

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect Low Address (OWPLA15-8)**

Address Offset: 2Bh

Bit	R/W	Default	Description
7-2	R/W	111111b	**Override Write Protect (OWP7-2)**
1-0	-	0h	**Reserved**

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP15-8)**

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP23-16)**

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP31-24)**

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP39-32)**

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP47-40)**

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R/W	11111111b	**Override Write Protect (OWP55-48)**

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Override Write Protect (OWP63-56)** OWPLA15-0 (Override Write Protect Low Addresses 15 through 0). OWP63-2 (Override Write Protect 63 through 2). Each bit affects the host's write capacity from one block. The block size is 8 Kbytes on the first low address (OWPLAi). The other blocks are 64 Kbytes. The block address is intended as follows: Low Address Blocks, OWPLAi: from i*8K to (i+1)*8K-1 Other Blocks, OWPj: from j*64K to (j+1)*64K Refer to Table 3-3 on page 8 for the details. 0: No override the host Write Protect 1: Host Write for this block is disabled regardless of the setting of others The default values make all the flash ranges readonly.

6.3.5 Host Interface Registers

The registers of SMFI can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The SMFI resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SMFI logical device number is 0Fh (LDN=0Fh).
These registers are listed below

Table 6-17. Host View Register Map, SMFI

7	0	Offset
Shared Memory Indirect Memory Address (SMIMAR0-3)		00h-03H
Shared Memory Indirect Memory Data (SMIMDR)		04h
Shared Memory Host Access Protect (SMHAPR1-4)		07-Ah
Shared Memory Host Semaphore (SMHSR)		0Ch

6.3.5.1 Shared Memory Indirect Memory Address Register 0 (SMIMAR0)

The following set of registers is accessible only by the host. The registers are applied to VCC.
This register defines the addresses 7-0 for a read or write transaction to the memory.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR7-0)**

6.3.5.2 Shared Memory Indirect Memory Address Register 1 (SMIMAR1)

This register defines the addresses 15-8 for a read or write transaction to the memory.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR15-8)**

6.3.5.3 Shared Memory Indirect Memory Address Register 2 (SMIMAR2)

This register defines the addresses 23-16 for a read or write transaction to the memory.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR23-16)**

6.3.5.4 Shared Memory Indirect Memory Address Register 3 (SMIMAR3)

This register defines the addresses 31-24 for a read or write transaction to the memory.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Address (IMADR31-24)**

6.3.5.5 Shared Memory Indirect Memory Data Register (SMIMDR)

This register defines the Data bits 7-0 for a read or write transaction to the memory.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	-	**Indirect Memory Data (IMDA7-0)**

6.3.5.6 Shared Memory Host Access Protect Register 1-4 (SMHAPR1-4)

This register provides the read/write protection and lock control for host from host side. The content of the register hold the block size, which is 64 Kbyte. SMHAPR1 controls the first 16 blocks (0-1 Mbyte). SMHAPR2 controls the second 16 blocks (1-2 Mbyte). SMHAPR3 controls the third 16 blocks (2-3 Mbyte). SMHAPR4 controls the fourth 16 blocks (3-4 Mbyte). Refer to Table 3-4 on page 8 for the details.
A lock protect flag may be set to prevent read and write protection bit change in the feature. All bits are clear after hardware reset.

Address Offset: 07h; 08h; 09h; 0Ah

Bit	R/W	Default	Description
7-4	R/W	0h	**Host Access Protection Index (HAPI)** Holds the index number of the host block in this register. Each block is 64 Kbytes. The block index is intended in the flash address (Index = (First Address of Block) / 64K-byte). In SMHAPRn (n=1 to 4): from 0000h to 1111h , for indexes 0 - 15, respectively Refer to Table 3-4 on page 8 for the details.
3	W	0b	**Index Write (IW)** This bit represents an index write transaction. When read always back to 0. 0: Indicate a write transaction is to update all fields of this register. Use bit 4-7 for this writing to bit 0-2. 1: Indicate a write transaction is to update bit 4-7 only Bits 0-2 will not be updated by this writing. Writing 1 to this bit is only required for further reading bit 0-2 in this register.
2	R/W	0b	**Host Lock Protection (HLP)** When this bit is set, it will prevent changing the value in the Host Read/Write/Lock Protection bits(0-2) for this block. 0: Changes to protection bits (0-2) are enabled. 1: Protection bits (0-2) are locked, and so are the bits' values.
1	R/W	1b	**Host Write Protection (HWP)** 0: Program and erase are allowed for this block. 1: Program and erase are inhibited for this block.
0	R/W	0b	**Host Read Protection (HRP)** 0: Host Reads are allowed for this block 1: Host Reads are inhibited for this block.

6.3.5.7 Shared Memory Host Semaphore Register (SMHSR)

This register provides eight semaphore bits between the EC and the host. Bits 3-0 may be set by the host and Bits 7-4 may be set by the EC. The register reset on host domain hardware reset.
This is the register the same as the one in section 6.3.4.9 on page 81 but they are in different views.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-4	R	0h	**EC Semaphore (CSEM3-0)** Four bits that may be updated by the EC and read by both the host and the EC.
3-0	R/W	0b	**Host Semaphore (HSEM3-0)** Four bits that may be updated by the host and read by both the host and the EC.

6.4 System Wake-Up Control (SWUC)

6.4.1 Overview

SWUC detects wakeup events and generate SCI#, SMI# and PWUREQ# signals to the host side, or alert EC by interrupts to WUC.

6.4.2 Features

- Supports programmable wake-up events source from the host controlled modules.
- Generates SMI# or PWUREQ# interrupt to host to wake-up system.

6.4.3 Functional Description

The wakeup event and gathering scheme is shown in

Figure 6-8 on page 86.

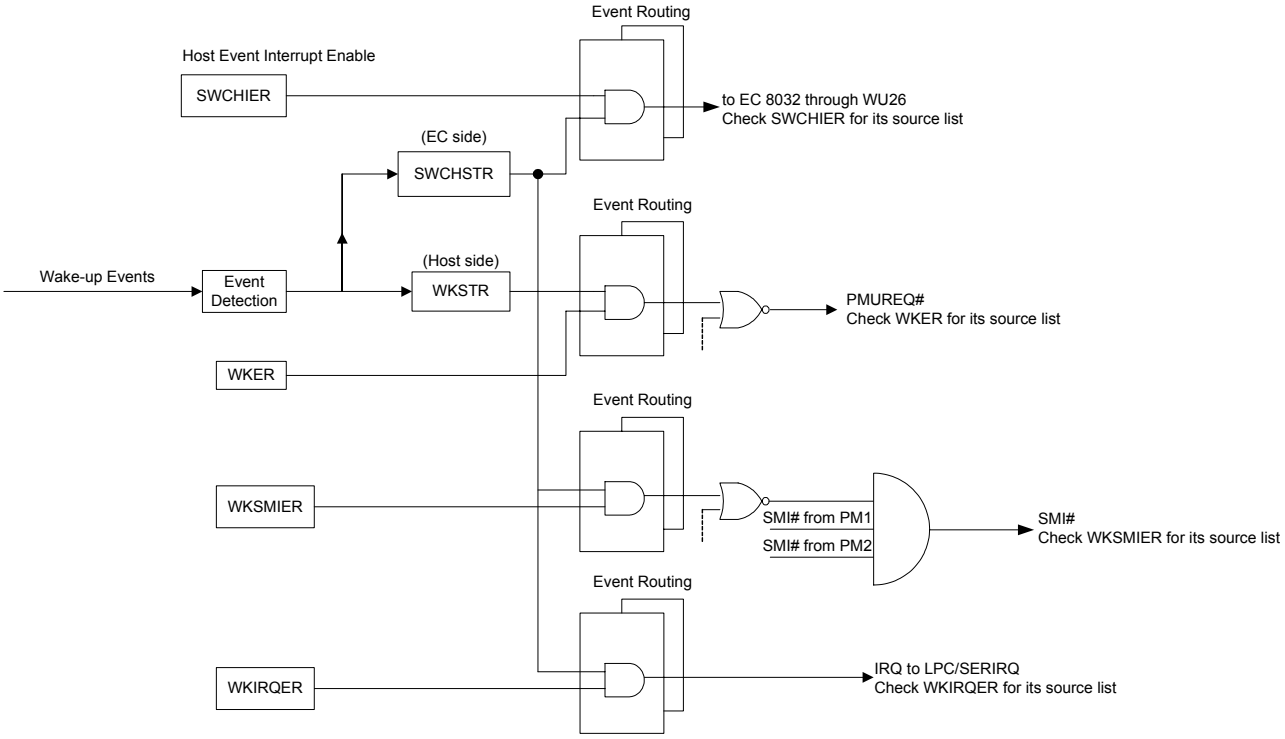


Figure 6-8. Wakeup Event and Gathering Scheme

6.4.3.1 Wake-Up Status

When the wake up event is detected, the relative status bit is set to 1 in both host and EC status registers, no matter whether any event enable bits are set or not. A status bit is cleared by writing 1 to it. Writing 0 to a status bit does not change its value. Clearing the event enable bit does not affect the status bit, but prevents it from issuing an event to output. The host uses a mask register (WKSMIER) to decide what the status bits will respond to.

6.4.3.2 Wake-Up Events

When a wake up event is detected, it is recorded on a status bit in WKSTR (host view) register and SWCHSTR register (EC view), regardless of the enabled bit. Each event behavior is determined by a wake up control logic controlled by a set of dedicated registers.

Input events are detected by the SWUC shown as follows:
- Module IRQ Wake up Event
- Modem Ring (RI1 and RI2)
- Telephone Ring (RING input)
- RTC Alarm
- Software event
- Legacy off event
- ACPI state change Event

Module IRQ Wake-Up Event
A module IRQ wake-up event from each logical device is asserted when the leading edge of the module IRQ is detected.
The relative enable bit (WKIRQEN) must be set to 1 to enable and trigger a wake-up event. Refer to the IRQNUM and WKIRQEN fields in IRQNUMX register. When the event is detected, MIRQ bit in WKSTR register is set to 1. If MIRQE in WKER register is also set to 1, the PWUREQ# output is still asserted and until the status bit is cleared.

Modem Ring
If transitions form high to low on RI1# (or RI2#) is detected on the Serial Port 1 (or Serial Port 2) connected to a modem, and then when the signal goes high on RI1#(or RI2#), it will cause a ring wake-up event asserted if the RI1#(or RI2#) event enable bit is set 1 in the WKER register (bit0 for RI1#, and bit1 for RI2#).

Telephone Ring
If transitions form high to low on the Ring input pin, and then when the signal goes high on Ring input pin. It will cause a ring wake-up event asserted when the ring event enable bit is set 1 in the WKER register (BIT3).

RTC Alarm
An alarm signal can be generated by RTC module and used as wake up event. After an alarm event is detected in the RTC, the RTC alarm status bit is set and RTCAL bit in SWCTL3 register is set to response it To enable RTC alarm as a wake-up event to EC, the software need to follow the sequence listed below:
1.Set the Alarm conditions in the RTC module.
2.Set EIRTCA bit in SWCIER register to enable Alarm status interrupt masking.
3.Make sure that the RTCA bit in SWCTL3 register is cleared.
4.Enable the Wake-Up on SWUC event in the WUC and INTC modules.

Software Event
This bit may trigger a wake event by software control. When the SIRQS (Software IRQ Event Status bit) in WKSTR register is set, a software event to the host is active. When the SIRQS bit in SWCHSTR register is set, a software event to the EC is active. The software event may be activated by the EC via access to the Host Controlled Module bridge regardless of the VCC status.
The SIRQS bit in SWCHSTR may be set when the respective bit toggles in WKSTR from 0 to 1 and when HSECM=0 is in SWCTL1 register. When HSECM =1 t, the SIRQS bit in SWCHSTR is set on a write of a 1 to the respective bit in WKSTR. The SIRQS bit in SWCHSTR is cleared by writing 1 to it.

Legacy Off Events
The host supports either legacy or ACPI mode. The operation mode is assigned on PWRBTN bit in the Super I/O Power Mode Register (SIOPWR). When EISCRDPBM bit in SWCIER register is set, any change in this bit will generate an interrupt to the EC. The EC may read this bit, using SCRDPBM bit in SWCTL2 register, to determine the other power state. In the legacy mode, the PWRSLY bit in SIOPWR register represents a turn

power off request. When this bit is set and SCRDPSO bit in SWCTL2 register is set, an interrupt is generated to EC if EISCRDPSO bit in SWCIER register is also set .

ACPI State Change Events
The bits (S1-S5) in WKACPIR register are used to provide a set of 'system power state change request' . The host uses these bits to issue an ACPI state change request. A write of 1 to any of these bits represents a state change request to the EC, the request may be also read out in SWCTL2 register even S0 is represented when all bits in WKACPI is cleared to 0. When any of S0-S5 bits in SWCTL2 is set and the respective mask bit in SWCIER register is set, an interrupt is generated to EC. All interrupt outputs may be cleared either writing 1 to the status bit or clear the masking interrupt enable register.

6.4.3.3 Wake-Up Output Events

The SWUC output four types of wake up events:

IRQ	Interrupt through SERIRQ to host side, which is activated by SWUC logical device of PNPCFG.
PWUREQ#	Routing as an SCI event.
SMI#	Routing as an SMI event.
WU26	An interrupt to the WUC module in the EC domain which is handled by EC firmware.

Output events are generated to host when their status bit is set (1 in WKSTR). Output event to the EC through the WUC is generated when their EC status bit is set (1 in SWCHSTR). The host can program three Event Routing Control registers (WKSTR, WKSMIER and WKIRQER) to handle each of the host events to be asserted. This allows selective routing of these events output to PWUREQ#, SMI# and/or SWUC interrupt request (IRQ). After an output event is asserted, it can be cleared either by clearing its status bit or being masked. The current status of the event may be read out at the Wake-Up Event Status Register(WKSTR), and Wake-Up Signals Monitor Register (WKSMR). The SWUC also handles the wake up event coming from the PMC 1 and 2 for SMI# event. In the EC domain, Wake-Up Event Interrupt Enable register (SWCHIER) holds an enable bit to allow selective routing of the event to output the EC wake-up interrupt (WU26) to the WUC.

6.4.3.4 Other SWUC Controlled Options

Additionally, the SWUC handles the following system control signals:
Host Keyboard Reset (KBRST#)
GA20 Signal
Host Configuration Address Option

- **Host Keyboard Reset (KBRST#)**

The Host Keyboard Reset output (KBRST#) can be asserted either by software or hardware:
Software: KBRST# will be asserted when the EC firmware issues a reset command by writing 1 to HRST in SWCTL1 register. Clear this bit to de-assert the KBRST#.
Hardware: KBRST# will be asserted during VSTBY Power-Up reset if HRAPU bit in SWCTL3 register is set and an LPC transaction is started.

The KBRST# signal will be active in the following conditions:
(1) HRSTA bit in the SWUC is enabled and LPC cycle is active when the VSTBY is power-on.
(2) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(3) HRST bit in the SWUC is enabled.
(4) Bit 0 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The KBRST# output scheme is shown in Figure 6-9 on page 89.
Note it is another way to use GPIO output function to send KBRST# signal.

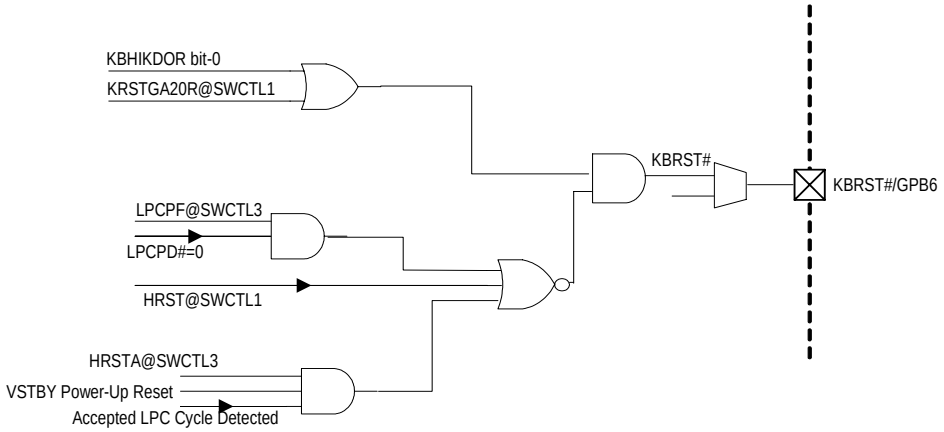


Figure 6-9. KBRST# Output Scheme

- **GA20 Signal**

In the chip, the GA20 is connected to a GPIO signal that is configured as output. Port GPB5 is recommended to be used as GA20 since its initialize state is output driving high. EC can assert the GA20 signal state either by modifying GPB5 in GPIO register or writing 1 to LPCPF in SWCTL3 register duration of the LPCPD# signal is active.

The GA20 signal will be active in the following conditions:
(1) LPCPF bit in the SWUC is enabled and LPCPD# signal is active.
(2) Bit-1 of KBHIKDOR in the KBC is enabled if KRSTGA20R is set.

The GA20 output scheme is shown in Figure 6-10 on page 89.
Note it is another way to use GPIO output function to send GA20 signal.

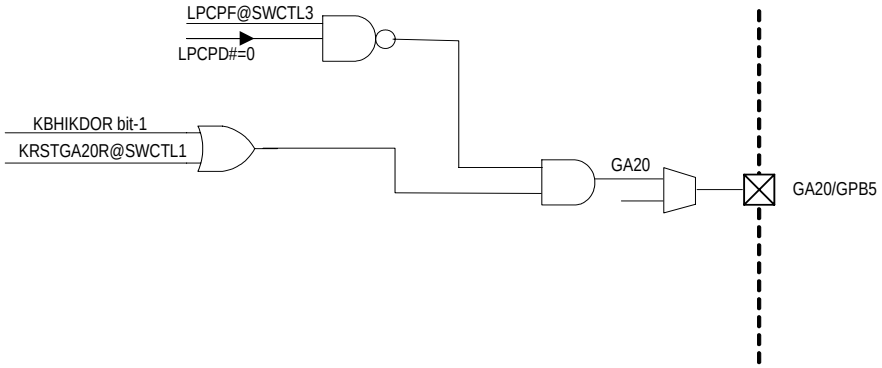


Figure 6-10. GA20 Output Scheme

- **Host Configuration Address Option**

The contents of SWCBAHR and SWCBALR change only during VSTBY Power -Up reset. To update the base address of the PNPCFG registers, refer to the followings:
1. Clear HCAV bit in SWCTL1 register by writing 1 to it.
2. Write the lower byte of the address to SWCBALR (LSB must be cleared).
3. Write the higher byte of the address to SWCBAHR.
4. Set HCAL bit to prevent the unintended change in the SWCBALR and SWCBAHR register.

6.4.4 Host Interface Registers

The registers of SWUC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. SWUC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The SWUC logical device number is 04h (LDN=04h).
SWUC host interface registers are battery-backed. These registers are listed below.

Table 6-18. Host View Register Map, SWUC

7	0	Offset
Wake-Up Event Status Register (WKSTR)		00h
Wake-Up Enable Register (WKER)		02h
Wake-Up Signals Monitor Register (WKSMR)		06h
Wake-Up ACPI Status Register (WKACPIR)		07h
Wake-Up SMI Enable Register (WKSMIER)		13h
Wake-Up Interrupt Enable Register (WKIRQER)		15h

6.4.4.1 Wake-Up Event Status Register (WKSTR)

The register is used to monitor the status of wake-up events. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/WC	0	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming the HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0 and writing 1 to this bit, the value of this bit will be inverted. When HSECM=1 and writing 1 to this bit, the bit is set to 1. The bit will be cleared when the SIRQS bit in SWUC Host Event Status Register (SWCHSTR) is written to 1. 0: Event is not active. 1: Event is active.
5-4	R	00	**Reserved.**
3	R/WC	0	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	00	**Reserved**
1	R/WC	0	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.4.4.2 Wake-Up Event Enable Register (WKER)

The register is used to enable the individual wake-up events to generate PWUREQ# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/W	0	**Module IRQ Event Enable (MIRQE)** 0: Disable. 1: Enable.
6	R/W	0	**Software IRQ Event Enable (SIRQE)** 0: Disable. 1: Enable.
5-4	R	00	**Reserved**
3	R/W	0	**RING# Event Enable (RINGE)** 0: Disable. 1: Enable.
2	R	00	**Reserved**
1	R/W	0	**RI2# Event Enable (RI2E)** 0: Disable. 1: Enable.
0	R/W	0	**RI1# Event Enable (RI1E)** 0: Disable. 1: Enable.

6.4.4.3 Wake-Up Signals Monitor Register (WKSMR)

The register is used to monitor the value of the SMI# and PWUREQ# signals and identify the generated source. This register is a read-only register.

Address Offset: 06h

Bit	R/W	Default	Description
7-6	R	00	**Reserved**
5	R	0	**PWUREQ# Output from SWUC (PWUREQOS)** 0: PWUREQ# output from SWUC is low. 1: PWUREQ# output from SWUC is high.
4	R	0	**PWUREQ# Signal Status (PWUREQS)** 0: PWUREQ# signal is low. 1: PWUREQ# signal is high.
3	R	0	**SMI# Output from PM2 (PM2SMI)** 0: SMI# output from PM channel 2 is low. 1: SMI# output from PM channel 2 is high.
2	R	0	**SMI# Output from PM1 (PM1SMI)** 0: SMI# output from PM channel 1 is low. 1: SMI# output from PM channel 1 is high.
1	R	0	**SMI# Output from SWUC (SWCSMI)** 0: SMI# output from SWUC is low. 1: SMI# output from SWUC is high.
0	R	0	**SMI# Signal Status (SMIS)** 0: SMI# signal is low. 1: SMI# signal is high.

6.4.4.4 Wake-Up ACPI Status Register (WKACPIR)

The register is used to monitor the status of ACPI. When this register is read, its value always returns 00h.

Address Offset: 07h

Bit	R/W	Default	Description
7-6	R	00	**Reserved**
5	R/W	0	**Change to S5 State (S5)** The host uses this bit to request the EC to change the ACPI S5 state. 0: Not request to change S5 state. 1: Request to change S5 state.
4	R/W	0	**Change to S4 State (S4)** The host uses this bit to request the EC to change the ACPI S4 state. 0: Not request to change S4 state. 1: Request to change S4 state.
3	R/W	0	**Change to S3 State (S3)** The host uses this bit to request the EC to change the ACPI S3 state. 0: Not request to change S3 state. 1: Request to change S3 state.
2	R/W	0	**Change to S2 State (S2)** The host uses this bit to request the EC to change the ACPI S2 state. 0: Not request to change S2 state. 1: Request to change S2 state.
1	R/W	0	**Change to S1 State (S1)** The host uses this bit to request the EC to change the ACPI S1 state. 0: Not request to change S1 state. 1: Request to change S1 state.
0	R	0	**Reserved**

6.4.4.5 Wake-Up SMI Enable Register (WKSMIER)

The register is used to enable the individual wake-up events to generate SMI# interrupt. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 13h

Bit	R/W	Default	Description
7	R/W	0	**Reserved**
6	R/W	0	**Software IRQ Event to SMI Enable (SSMIE)** 0: Disable. 1: Enable.
5-4	R	00	**Reserved**
3	R/W	0	**RING# Event to SMI Enable (RINGSMIE)** 0: Disable. 1: Enable.
2	R	00	**Reserved**
1	R/W	0	**RI2# Event to SMI Enable (RI2SMIE)** 0: Disable. 1: Enable.
0	R/W	0	**RI1# Event to SMI Enable (RI1SMIE)** 0: Disable. 1: Enable.

6.4.4.6 Wake-Up IRQ Enable Register (WKIRQER)

The register is used to enable the individual wake-up events to generate the interrupt signal that is assigned by SWUC. The register will be cleared when the VSTBY power is power-up, or the host domain software reset occurs.

Address Offset: 15h

Bit	R/W	Default	Description
7	R/W	0	**Reserved**
6	R/W	0	**Software IRQ Event to IRQ Enable (SIRQE)** 0: Disable. 1: Enable.
5-4	R	00	**Reserved**
3	R/W	0	**RING# Event to IRQ Enable (RINGIRQE)** 0: Disable. 1: Enable.
2	R	00	**Reserved**
1	R/W	0	**RI2# Event to IRQ Enable (RI2IRQE)** 0: Disable. 1: Enable.
0	R/W	0	**RI1# Event to IRQ Enable (RI1IRQE)** 0: Disable. 1: Enable.

6.4.5 EC Interface Registers

The registers of SWUC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for SWUC is 1400h.
These registers are listed below.

Table 6-19. EC View Register Map, SWUC

7 ... 0	Offset
SWUC Control Status 1 Register (SWCTL1)	00h
SWUC Control Status 2 Register (SWCTL2)	02h
SWUC Control Status 3 Register (SWCTL3)	04h
SWUC Host Configuration Base Address Low Byte Register (SWCBALR)	08h
SWUC Host Configuration Base Address High Byte Register (SWCBAHR)	0Ah
SWUC Interrupt Enable Register (SWCIER)	0Ch
SWUC Host Event Status Register (SWCHSTR)	0Eh
SWUC Host Event Interrupt Enable Register (SWCHIER)	10h

6.4.5.1 SWUC Control Status 1 Register (SWCTL1)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up. Bit 0 is only cleared when the warm reset occurs.

Address Offset: 00h

Bit	R/W	Default	Description
7	R/W	1	**KB Reset/GA20 Routing (KRSTGA20R)** 0: Enable routing bit-0 of KBHIKDOR as KBRST# source Enable routing bit-1 of KBHIKDOR as GA20 source 1: Disable above

Bit	R/W	Default	Description
6	R/W	0	**Reserved**
5	R/W	0	**Host Software Event Clear Mode (HSECM)** This bit is used to control the clear mode of SIRQS bit at the Wake-Up Event Status Register (WKSTR).
4	R/W	0	**Host Configuration Address Lock (HCAL)** When the bit is written to 1, the Host Configuration Address and the bit will be locked. The bit is only cleared at the following condition: VSTBY power-up or watchdog reset.
3	R/WC	0	**Host Configuration Address Valid (HCAV)** This bit is set after SWCBAHR register is written. 1: Indicate Host Configuration Base Address stored in SWCBALR and SWCBAHR registers are valid. 0: SWCBALR and SWCBAHR registers are not valid. The bit can be cleared by writing to 1.
2	R	0	**LPC Reset Active (LPCRST)** 0: LPCRST# is inactive. 1: LPCRST# is active.
1	R	-	**VCC Power On (VCCPO)** 0: VCC is power-off. 1: VCC is power-on.
0	R/W	-	**Host Reset Active (HRST)** When this bit is 1, the KBRST# is active to generate one host software reset.

6.4.5.2 SWUC Control Status 2 Register (SWCTL2)

The register is used to control the individual wake-up action on SWUC. The register will be cleared when the VSTBY power is power-up and LPCRST# is active.

Address Offset: 02h

Bit	R/W	Default	Description
7	R/WC	0	**Super I/O Configuration SIOPWR Power Supply Off (SCRDPSO)** The bit is used to monitor the Power Supply Off (PWRSLY) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the bit and the interrupt signal caused by a change in this bit value . A write of 0 to this bit is ignored.
6	R/WC	0	**Super I/O Configuration SIOPWR Power Button Mode (SCRDPBM)** The bit is used to monitor the Power Button Mode (PWRBTN) bit in SIOPWR register of PNPCFG. When the bit is written to 1, clear the interrupt signal caused by a change in this bit value. A write of 0 to this bit is ignored.
5-1	R/WC	0000	**ACPI request S5-1 (ACPIRS5-1)** These bits are used to monitor the S5-1 bit at the Wake-Up ACPI Status Register (WKACPIR). When the bit is written to 1, clear the bit and the interrupt signal caused by ACPI . A write of 0 to this bit is ignored.
0	R/WC	0000	**ACPI request S0 (ACPIRS0)** If all S5-1 bits at the WKACPIR are written to 0, the bit will be set to 1. The bit will be cleared if the bit is written to 1.

6.4.5.3 SWUC Control Status 3 Register (SWCTL3)

The register is used to control the individual wake-up action on SWUC. The register will only be cleared when the VBS power is power-up.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	R	00h	**Reserved**
2	R/WC	0	**RTC Alarm Active (RTCAL)** When the RTC alarm is active, the bit will be set to 1. The bit can be cleared by writing to 1.
1	R/W	0	**LPC Power Fail Turn Off KBRST# and GA20 (LPCPF)** If the bit is set to 1, the KBRST# and GA20 will be forced to low when the LPCPD# signal is active.
0	R/W	1	**Host Reset Active During VSTBY Power-Up (HRSTA)** If the bit is set to 1, the KBRST# signal will be active when the LPC cycle is active until VSTBY Power-Up Reset is finished. Writing to this bit is ignored if HCAL bit is set.

6.4.5.4 SWUC Host Configuration Base Address Low Byte Register (SWCBALR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-2 on page 44 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address Low Byte (BALB)**

6.4.5.5 SWUC Host Configuration Base Address High Byte Register (SWCBAHR)

The register is used to program the base address of the SWUC Host Interface registers.
See also Table 6-2 on page 44 and HCAL/HCAV bit in SWCTL1 register.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Base Address High Byte (BAHB)**

6.4.5.6 SWUC Interrupt Enable Register (SWCIER)

The register is used to enable the individual interrupt source on SWUC. The interrupt can be cleared by clearing the status bit or masking the source. On the other hand, the register will be cleared when the warm reset is active.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/W	0	**Enable Interrupt from Super I/O Configuration SIOPWR Power Supply Off (EISCRDPSO)** 1:Generate on high-level interrupt when the SCRDPSO bit in SWUC Control Status 2 Register (SWCTL2) is changing. 0:Disable the interrupt source.

Bit	R/W	Default	Description
6	R/W	0	**Enable Interrupt from Super I/O Configuration SIOPWR Power Button Mode (EISCRDPBM)** 1:Generate on high-level interrupt when the SCRDPBM bit in SWUC Control Status 2 Register (SWCTL2) is changing. 0:Disable the interrupt source.
5-1	R/W	0000	**Enable Interrupt from ACPI request S5-1 (EIACPIRS5-1)** 1:Generate on high-level interrupt when the ACPIRS5-1 bit in SWUC Control Status 2 Register (SWCTL2) is changing. 0: Disable the interrupt source.
0	R/W	0	**Enable Interrupt from RTC Alarm Active (EIRTCA)** 1:Generate on high-level interrupt when the RTCAL bit in SWUC Control Status 3 Register (SWCTL3) is setting to 1. 0:Disable the interrupt source.

6.4.5.7 SWUC Host Event Status Register (SWCHSTR)

The information of this register is mirror as the Wake-Up Event Status Register (WKSTR). The status bits can be cleared by writing to the corresponding bit in the two registers. The register will be cleared when the VSTBY power is power-up, or the host software reset occurs.

Address Offset: 0Eh

Bit	R/W	Default	Description
7	R/WC	0	**Module IRQ Event Status (MIRQS)** 0: Event is not active. 1: Event is active.
6	R/WC	0	**Software IRQ Event Status (SIRQS)** The function of this bit can be changed by programming HSECM bit in SWUC Control Status Register (SWCTL1). When HSECM=0, this bit is set to 1 when SIRQS toggles to 1 in WKSTR register. When HSECM=1 and this bit is set to 1 when writing 1 to SIRQS in WKSTR register. This bit will be cleared by writing 1 to it 0: Event is not active. 1: Event is active.
5-4	R	00	**Reserved**
3	R/WC	0	**RING# Event Status (RINGS)** If the RING detection mode is disabled, the bit is always 0. 0: Event is not active. 1: Event is active.
2	R	00	**Reserved**
1	R/WC	0	**RI2# Event Status (RI2S)** 0: Event is not active. 1: Event is active.
0	R/WC	0	**RI1# Event Status (RI1S)** 0: Event is not active. 1: Event is active.

6.4.5.8 SWUC Host Event Interrupt Enable Register (SWCHIER)

The register is used to enable the individual wake-up events to generate one interrupt to the EC 8032 via WU26 of WUC. The register will be cleared when the warm reset occurs.

Address Offset: 10h

Bit	R/W	Default	Description
7	R/W	0	**Module IRQ Event Enable (MIRQEE)** 0: Disable. 1: Enable.
6	R/W	0	**Software IRQ Event Enable (SIRQEE)** 0: Disable. 1: Enable.
5-4	R	00	**Reserved**
3	R/W	0	**RING# Event Enable (RINGEE)** 0: Disable. 1: Enable.
2	R	00	**Reserved**
1	R/W	0	**RI2# Event Enable (RI2EE)** 0: Disable. 1: Enable.
0	R/W	0	**RI1# Event Enable (RI1EE)** 0: Disable. 1: Enable.

6.5 Keyboard Controller (KBC)

6.5.1 Overview

This Keyboard Controller supports a standard keyboard and mouse controller interface.

6.5.2 Features

- Compatible with the legacy 8042 interface keyboard controller.
- Supports two standard registers for programming: Command/Data Register and Status Register.
- Automatically generates interrupts to the host side and EC side when the status is changed at the KBC.

6.5.3 Functional Description

This Keyboard Controller is compatible with the legacy 8042 interface keyboard controller.

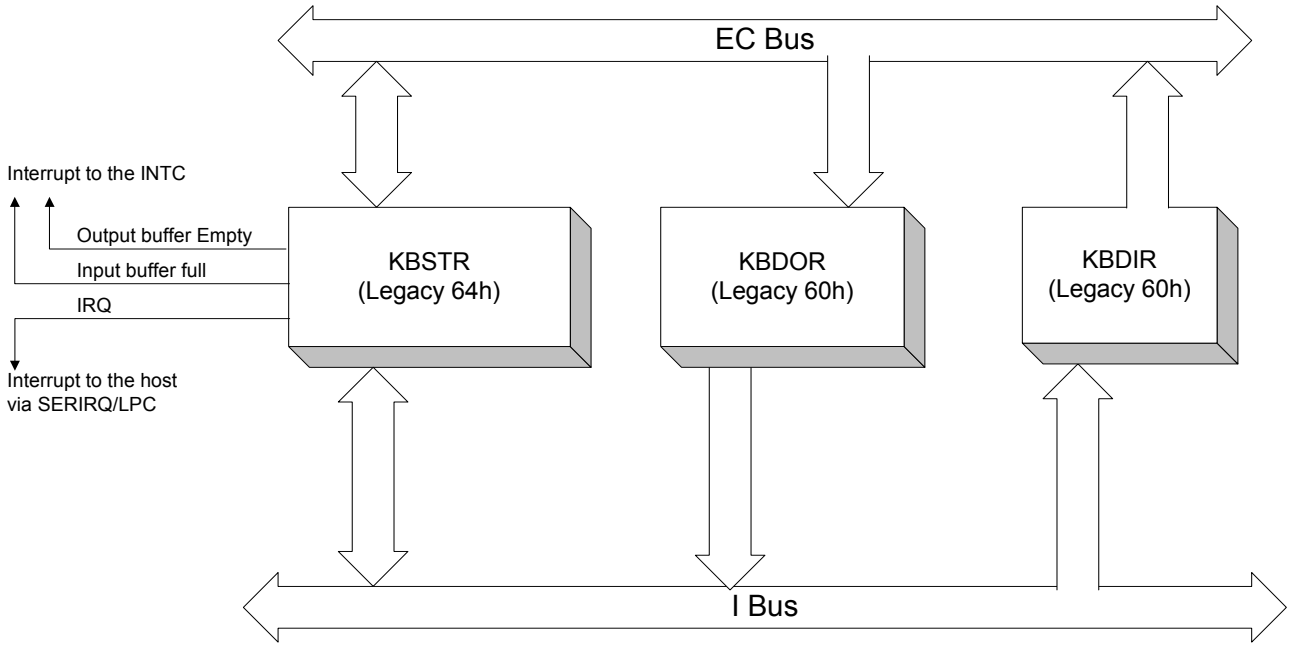


Figure 6-11. KBC Host Interface Block Diagram

Status
The host processor can read the status of KBC from the KBC Status Register. The internal 8032 can read the status of KBC from the KBC Host Interface Keyboard/Mouse Status Register.

Host Write Data to KBC Interface
When writing to address 60h or 64h (programmable), the IBF bit in the KBC Status Register is set and A2 bit in the KBC Status Register indicates to 8032 whose address was written. When writing to address 60h, A2 bit is 0. When writing to address 64h, A2 bit is 1.
EC 8032 can identify that the input buffer is full by either polling IBF bit in the Status register or detecting an interrupt (INT24) if the interrupt is enabled. EC 8032 can read the data from the KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR), and the IBF bit in the Status Register is cleared.

EC 8032 Write Data to KBC Interface
EC 8032 can write data to the KBC when it needs to send data to the host. When EC 8032 writes data to the KBC Host Interface Keyboard Data Output Register (KBHIKDOR), the OBF bit in the Status Register is set. If the IRQ1 interrupt is enabled, the IRQ1 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When EC 8032 writes data to the KBC Host Interface Mouse

Data Output Register (KBHIMDOR), the OBF bit in the Status Register is set. If the IRQ12 interrupt is enabled, the IRQ12 will be sent to the host. The host can read the Data Output Register when it detects the Output Buffer Full condition. When the Output Buffer Empty interrupt to INTC (INT2) is enabled, the interrupt signal is set high if the output buffer is empty.

Interrupts
There are two interrupts (Input Buffer Full Interrupt and Output Buffer Empty) connected to the INTC.
There are two interrupts (IRQ1 and IRQ12) connected to the host side (SERIRQ).
The IRQ numbers of KBC are programmable and use IRQ1 and IRQ12 as abbreviations in this section.

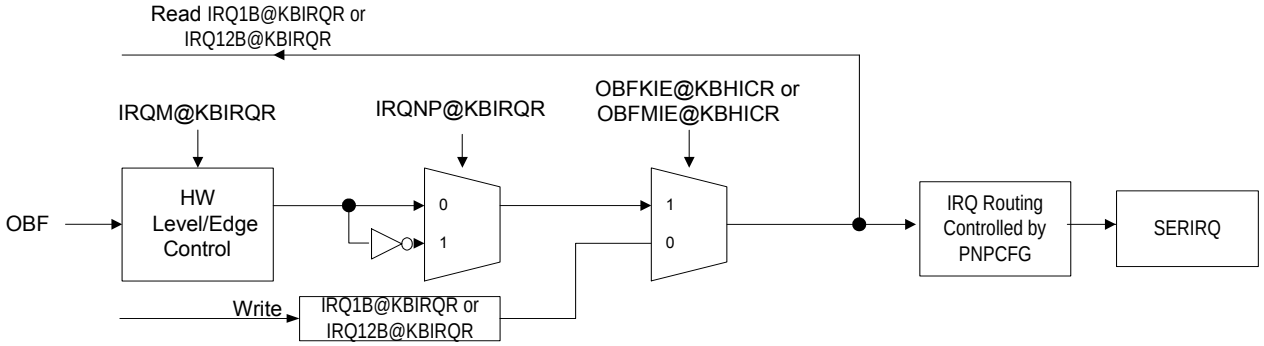


Figure 6-12. IRQ Control in KBC Module

GA20 and KBRST#
Refer to section 6.4.3.4 on page 88.

6.5.4 Host Interface Registers

The registers of KBC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor.
The KBC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The KBC/Keyboard logical device number is 06h (LDN=06h) and the KBC/Mouse logical device number is 05h (LDN=05h). For compatibility issue, the two I/O Port Base Addresses of KBC/Keyboard are suggested to configure at 60h and 64h.

These registers are listed below.

Table 6-20. Host View Register Map, KBC

7 ... 0	Offset
KBC Data Input Register (KBDIR)	Legacy 60h
KBC Data Output Register (KBDOR)	Legacy 60h
KBC Command Register (KBCMDR)	Legacy 64h
KBC Status Register (KBSTR)	Legacy 64h

Legacy 60h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 64h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-3 on page 45.

6.5.4.1 KBC Data Input Register (KBDIR)

When the host processor is writing this register, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be cleared. If the IBFCIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the write action will cause one interrupt to 8032 processor via INT24 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	W	-	**KBC Data Input (KBDI)** The data is used to output for Keyboard/Mouse.

6.5.4.2 KBC Data Output Register (KBDOR)

When the host processor is reading this register, The OBF bit in KBC Status Register (KBSTR) will be cleared. The reading access will also clear the interrupt for host processor when the IRQM bits of KBC Interrupt Control Register (KBIRQR) are programmed to be at level mode. If the OBECIE bit in KBC Host Interface Control Register (KBHICR) is enabled, the read action will cause one interrupt to 8032 processor via INT2 of INTC.

Address Offset: 00h for I/O Port Base Address 0, Legacy 60h

Bit	R/W	Default	Description
7-0	R	-	**KBC Data Output (KBDO)** The data comes from the Keyboard/Mouse source.

6.5.4.3 KBC Command Register (KBCMDR)

When the register is written, the IBF bit in KBC Status Register (KBSTR) will be set and the A2 bit will be set.

Address Offset: 00h for I/O Port Base Address 1, Legacy 64h

Bit	R/W	Default	Description
7-0	W	-	**KBC Command (KBCMD)** The command data is used to output for Keyboard/Mouse.

6.5.4.4 KBC Status Register (KBSTR)

The host processor uses the register to monitor the status of KBC. The same information will minor to the KBC Host Interface Keyboard/Mouse Status Register (KBHISR). It is used by the internal 8032.

Address Offset: 01h for I/O Port Base Address 0, Legacy 64h

Bit	R/W	Default	Description
7-4	R	0h	**Programming Data 3-0 (PD3-0)** The data is used by the 8032 firmware to be the general-purpose setting.
3	R	0	**A2 Address (A2)** The bit is used to keep the A2 address information of the last write operation that the host processor accessed the KBC.
2	R	0	**Programming Data II (PDII)** The function is the same as the PD3-0.
1	R	0	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is setting. On the other hand, the bit will be cleared when the KBDIR or KBCMDR is read by the 8032 firmware.

Bit	R/W	Default	Description
0	R	0	**Output Buffer Full (OBF)** When the EC 8032 is writing data to KBDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the host processor.

6.5.5 EC Interface Registers

The registers of KBC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for KBC is 1300h.

These registers are listed below

Table 6-21. EC View Register Map, KBC

7	0	Offset
KBC Host Interface Control Register (KBHICR)		00h
KBC Interrupt Control Register (KBIRQR)		02h
KBC Host Interface Keyboard/Mouse Status Register (KBHISR)		04h
KBC Host Interface Keyboard Data Output Register (KBHIKDOR)		06h
KBC Host Interface Mouse Data Output Register (KBHIMDOR)		08h
KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)		0Ah

.

6.5.5.1 KBC Host Interface Control Register (KBHICR)

Address Offset: 00h

Bit	R/W	Default	Description
7	R	0	**Reserved**
6	R/W	0	**PM Channel 1 Input Buffer Full 8032 Interrupt Enable (PM1ICIE)** The bit is used to enable the interrupt to 8032 for PM channel 1 when the input buffer is full via INT25 of INTC.
5	R/W	0	**PM Channel 1 Output Buffer Empty 8032 Interrupt Enable (PM1OCIE)** The bit is used to enable the interrupt to 8032 for PM channel 1 when the output buffer is empty via INT3 of INTC.
4	R/W	0	**PM Channel 1 Host Interface Interrupt Enable (PM1HIE)** 0: The IRQ11 is controlled by the IRQ11B bit in KBC Interrupt Control Register (KBIRQR). 1: Enables the interrupt to the host side via SERIRQ for PM channel 1 when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.
3	R/W	0	**Input Buffer Full 8032 Interrupt Enable (IBFCIE)** The bit is used to enable the interrupt to 8032 for Keyboard/Mouse when the input buffer is full via INT24 of INTC.
2	R/W	0	**Output Buffer Empty 8032 Interrupt Enable (OBECIE)** The bit is used to enable the interrupt to 8032 for Keyboard/Mouse when the output buffer is empty via INT2 of INTC.
1	R/W	0	**Output Buffer Full Mouse Interrupt Enable (OBFMIE)** 0: The IRQ12 is controlled by the IRQ12B bit in KBIRQR. 1: Enables the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.

Bit	R/W	Default	Description
0	R/W	0	**Output Buffer Full Keyboard Interrupt Enable (OBFKIE)** 0: The IRQ1 is controlled by the IRQ1B bit in KBIRQR. 1: Enables the interrupt to mouse driver in the host processor via SERIRQ when the output buffer is full. The interrupt type is controlled by the IRQM and IRQNP bit in KBIRQR.

6.5.5.2 KBC Interrupt Control Register (KBIRQR)

Address Offset: 02h

Bit	R/W	Default	Description
7	R	0	**Reserved**
6	R/W	0	**Interrupt Negative Polarity (IRQNP)** The bit is enabled, and then the interrupt level is inverted.
5-3	R/W	0	**Interrupt Mode (IRQM)** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is high and a negative pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from SCIPM field in PMCTL register and SMIPM field in PMIC register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	1	**IRQ11 Control Bit (IRQ11B)** When the PMHIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ11 signal. The bit can be used to monitor the status of IRQ11 signal.
1	R/W	1	**IRQ12 Control Bit (IRQ12B)** When the OBFMIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ12 signal. The bit can be used to monitor the status of IRQ12 signal.
0	R/W	1	**IRQ1 Control Bit (IRQ1B)** When the OBFKIE bit in KBC Host Interface Control Register (KBHICR) is 0, the bit directly controls the IRQ1 signal. The bit can be used to monitor the status of IRQ1 signal.

6.5.5.3 KBC Host Interface Keyboard/Mouse Status Register (KBHISR)

The 8032 firmware uses the register to monitor the status of KBC. It can use bit 7-4 and bit 2 to send the information to the host processor. The data of this register is the same as the data of KBC Status Register (KBSTR).

Address Offset: 04h

Bit	R/W	Default	Description
7-4	R/W	0h	**Programming Data 3-0 (PD3-0)** The data is used by the 8032 firmware to be the general-purpose setting.
3	R	0	**A2 Address (A2)** The bit is used to keep the A2 address information of the last write operation that the host processor accessed the KBC.
2	R/W	0	**Programming Data II (PDII)** The function is the same as the PD3-0.
1	R	0	**Input Buffer Full (IBF)** When the host processor is writing data to KBDIR or KBCMDR, the bit is set. On the other hand, the bit will be cleared when the KBDIR or KBCMDR is read by the 8032 firmware.
0	R	0	**Output Buffer Full (OBF)** When the host processor is writing data to KBDOR, the bit is set. On the other hand, the bit will be cleared when the KBDOR is read by the 8032 firmware.

6.5.5.4 KBC Host Interface Keyboard Data Output Register (KBHIKDOR)

The 8032 firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	W	-	**KBC Keyboard Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.5.5.5 KBC Host Interface Mouse Data Output Register (KBHIMDOR)

The 8032 firmware can write the register to send the data of the KBC Data Output Register (KBDOR). Besides, the action will set the OBF bit in the KBC Status Register (KBSTR). If the OBECIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	W	-	**KBC Mouse Data Output (KBKDO)** The data output to the KBC Data Output Register (KBDOR).

6.5.5.6 KBC Host Interface Keyboard/Mouse Data Input Register (KBHIDIR)

The 8032 firmware can read the register to get the data of the KBC Data Input Register (KBDIR). Besides, the action will clear the IBF bit in the KBC Status Register (KBSTR). If the IBFCIE bit in the KBC Interrupt Control Register (KBIRQR) is enabled, the action will clear the interrupt.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**KBC Keyboard/Mouse Data Input (KBKMDI)** The data is the same as the data of KBC Data Input Register (KBDIR).

6.6 Power Management Channel (PMC)

6.6.1 Overview

The power management channel is defined in ACPI specification and used as a communication channel between the host processor and embedded controller.

6.6.2 Features

- Supports two PM channels
- Supports compatible mode and enhanced mode (both channels)
- Supports shared and private interface
- Supports Command/Status and Data ports
- Supports IRQ/SMI/SCI generation

6.6.3 Functional Description

To generate the SCI and SMI interrupts to the host

6.6.3.1 General Description

The PM channel supports two operation modes: one is called Compatible mode that is available for channel 1 only. The other is called Enhanced mode. PMC is available for both channels. The PM channel provides four registers: PMDIR, PMDOR, PMCMDR and PMSTR for communication between the EC and host side. The PMDIR register can be written to by the host and read by the EC. The PMDOR register can be written to by the EC and read by the host. The PMCMDR/PMSTR register can be read by both the EC and Host side.

The PMC host interface block diagram is shown below.

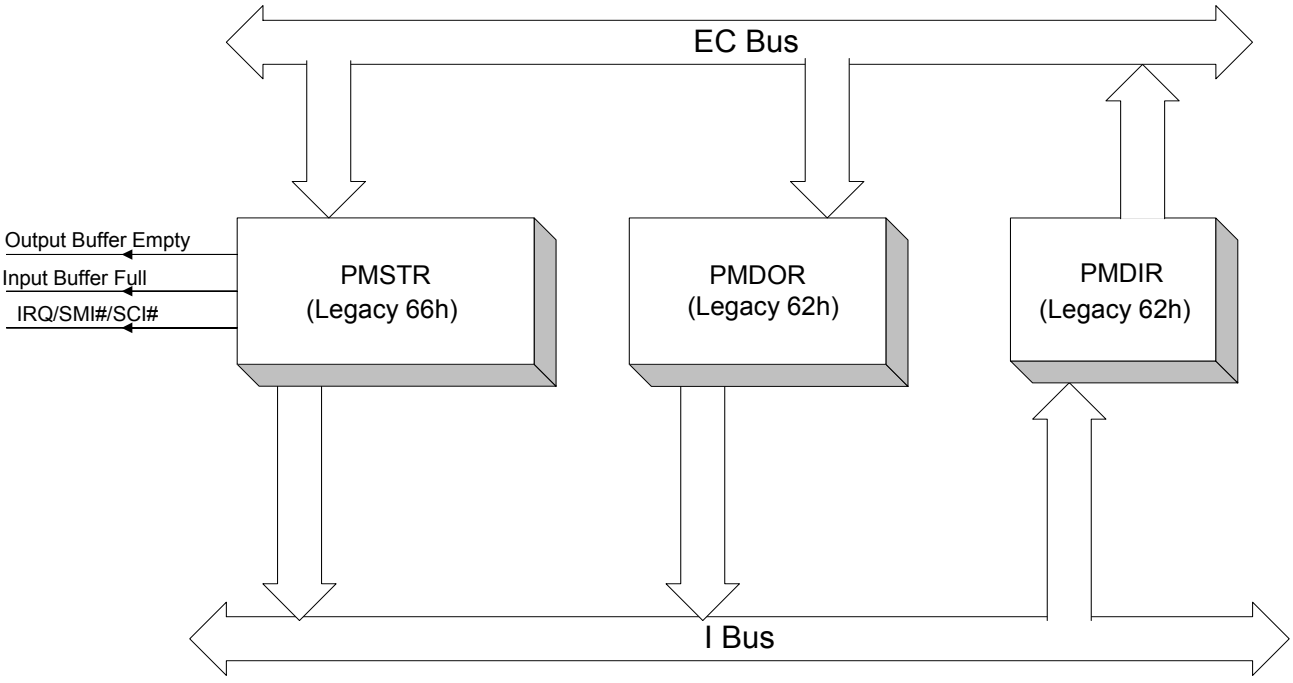


Figure 6-13. PMC Host Interface Block Diagram

EC Interrupts

Two interrupts (IBF and OBF) are connected to INTC. These interrupts are enabled by OBEIE and IBFIE in PMCTLn register, respectively.

The diagram of PMC interrupt to EC 8032 via INT3/INT25 of INTC is shown below.

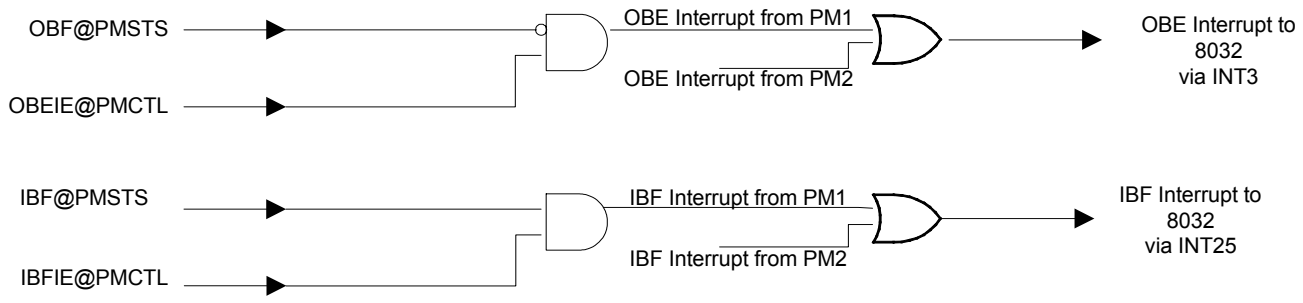


Figure 6-14. EC Interrupt Request for PMC

Host Interrupt
The EC can select to access to different address space to generate IRQ, SMI or SCI interrupt when either IBF or OBF is set.

The IRQ numbers of PMC are programmable and use IRQ11 as abbreviation in the following section, and n in an abbreviation represents channel 1 and/or channel 2 of this register.

6.6.3.2 Compatible Mode

When IRQ numbers in host configuration register are assigned by host software, and the interrupt can be generated either by hardware via PM1HIE in KBHICR register or by programming KBIRQR register. In Normal Polarity mode (IRQNP in KBIRQR register is cleared), IT8510 supports legacy level for PM compatible mode interrupt. When a level interrupt is selected (IRQM in KBIRQR register is cleared), the interrupt signal is asserted when the OBF flag has been set, which is still asserted until the output buffer is read (i.e.,OBF flag is cleared). The EC can control the interrupts generated by the PM channel to the one as follows:
IRQ signal to LPC/SERIRQ, when IRQEN bit in PMIEn register is set
SMI# output to SWUC, when SMIEN bit in PMIEn register is set
SCI# signal, using the SCIEC output, when SCIEN bit in PMIEn register is set.

The IRQ/SCI#/SMI# control diagram in PMC compatible mode is shown below.

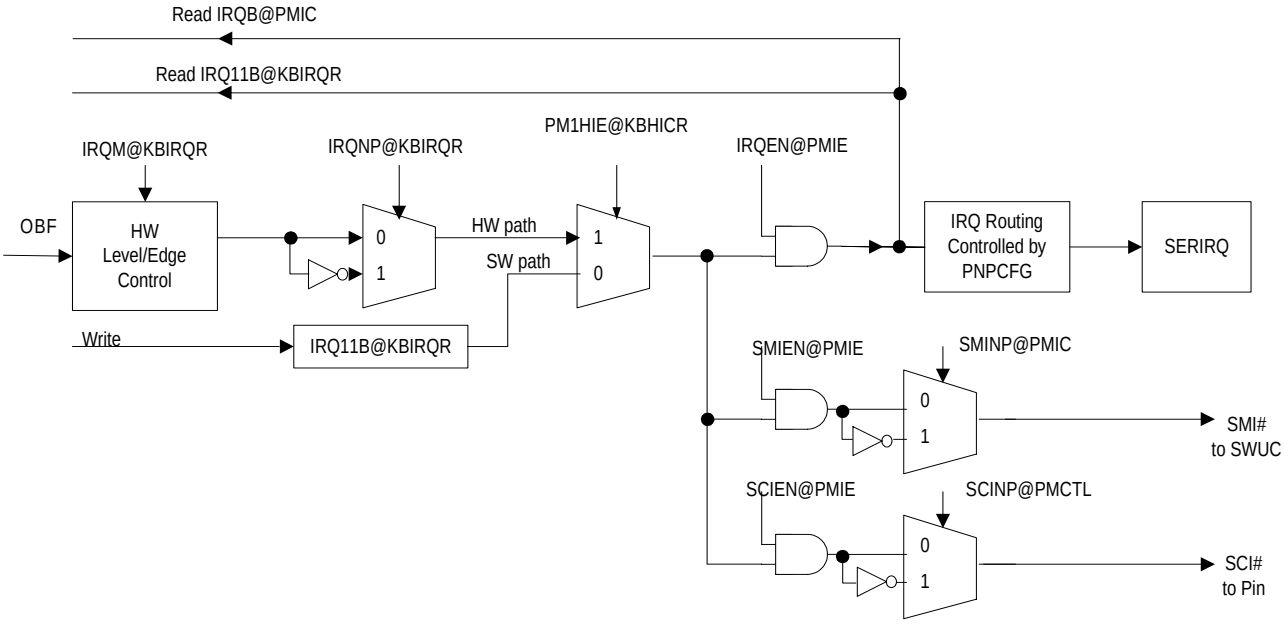


Figure 6-15. IRQ/SCI#/SMI# Control in PMC Compatible Mode

6.6.3.3 Enhanced PM mode

Enhanced PM mode is activated when APM is set to 1 in PMCTLn register. IRQ, SMI or SCI interrupts generated can be selected to output via software control or hardware. Which channel will be output an IRQ is decided by programming IRQEN bit in PMIEn register. SCI and SMI are generated when EC writes to the Data output buffer. SCI is generated when EC reads the Data Input buffer. Different data register generate different interrupt. The OBF flag in PMSTSn register is set and both SMI and SCI interrupts are deasserted when PMDOn register is written into data. The OBF_SMI interrupt is generated when PMDOSMIn register is written into data. The OBF_SMI flag is cleared when OBF flag is cleared. The OBF_SCI interrupt is generated When PMDOSCIn register is written into data.OBF_SCI which is cleared when OBF is cleared.
The IBF flag is cleared and SCI interrupt is generated when PMDISCIn register is read out data. The IBF flag is cleared and SCI interrupt is not asserted when PMDIn register is read out data.

The IRQ/SCI/SMI control diagram in PMC enhanced mode is shown below.

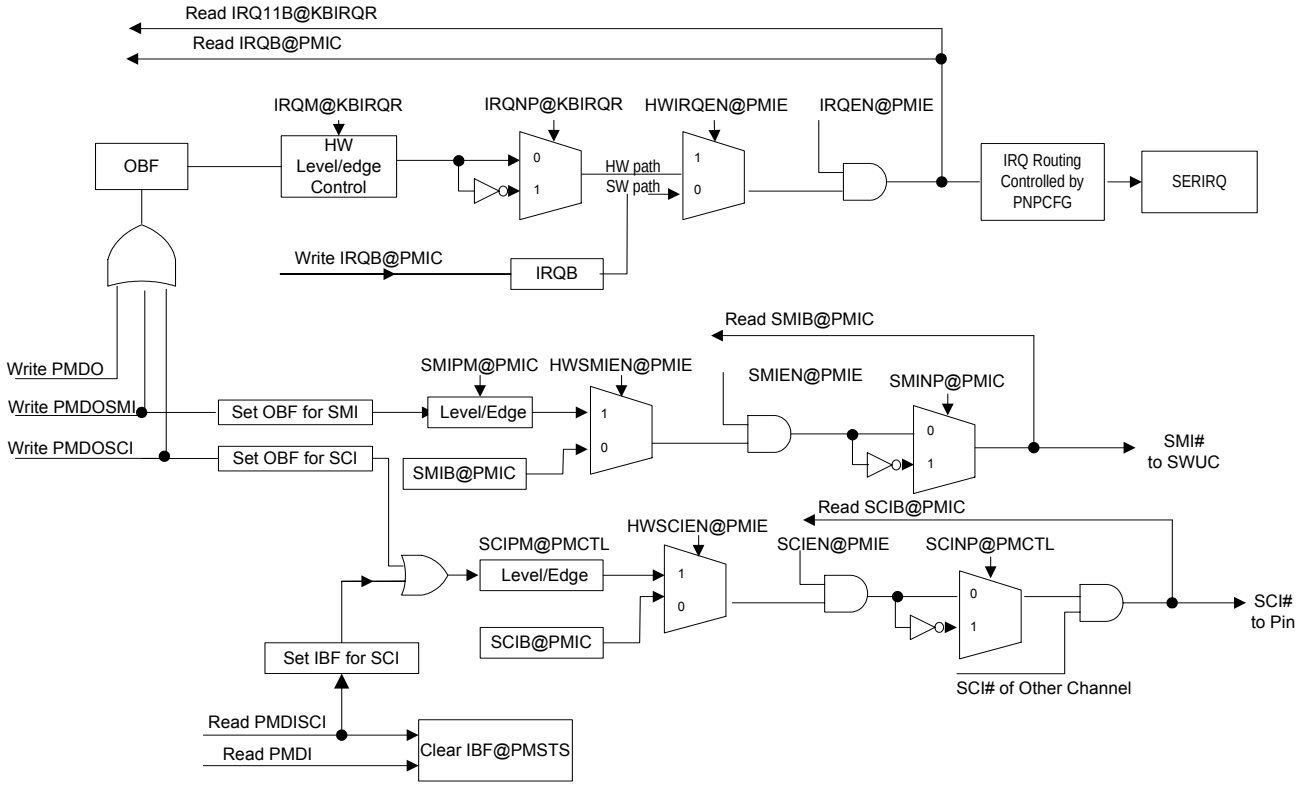


Figure 6-16. IRQ/SCI#/SMI# Control in PMC Enhanced Mode

6.6.4 Host Interface Registers

The registers of PMC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the host interface. The host interface registers can only be accessed by the host processor. The PMC Channel 1 and 2 reside at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The channel 1 logical device number is 11h (LDN=11h) and the channel 2 logical device number is 12h (LDN=12h). For compatibility issue, the two I/O Port Base Addresses of channel 1 are suggested to configure at 62h and 66h.

These registers are listed below.

Table 6-22. Host View Register Map, PMC

7	0	Offset
PMC Data Input Register (PMDIR)		Legacy 62h
PMC Data Output Register (PMDOR)		Legacy 62h
PMC Command Register (PMCMDR)		Legacy 66h
PMC Status Register (PMSTR)		Legacy 66h

Legacy 62h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 66h represents (I/O Port Base Address 1) + (Offset 0h)
See also Table 6-3 on page 45.

6.6.4.1 PMC Data Input Register (PMDIR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	W	0h	**Data Input Register Bit [7:0] (DIRB)** This is the data input register for power management channel data communication between the host and EC side. When the host writes this port, data is written to PMDIR register and EC 8032 can read it. Notice that when the Command/Status register is written, the data is also stored into PMDIR register. Users must read A2 to decide whether the PMDIR data is data or command.

6.6.4.2 PMC Data Output Register (PMDOR)

Address Offset: 00h for I/O Port Base Address 0, Legacy 62h for Channel 1

Bit	R/W	Default	Description
7-0	R	0h	**Data Output Register Bit [7:0] (DORB)** This is the data output register for power management channel data communication between the host and EC. When the host reads this port, data is read from PMDOR register and EC 8032 can write it.

6.6.4.3 PMC Command Register (PMCMDR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-0	W	0h	**Command Register Bit [7:0] (CRB)** The port is written by the host when A2 = 1 in PMSTR register.

6.6.4.4 Status Register (PMSTR)

Address Offset: 00h for I/O Port Base Address 1, Legacy 66h for Channel 1

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** This is a general purpose flag used for signaling between host and EC side. When used as ACPI PM channel, the predefined meaning is burst, SCI event and SMI event.
3	R	0h	**A2 (A2)** This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written by the host is data. If this bit is 1, it represents that the data written by the host is command.
2	R/W	0h	**General Purpose flag (GPF)** This bit is used as a general-purpose flag.
1	R	0h	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when the host writes data input register or command register and is cleared when the EC 8032 reads the data input register. Notice that the write to data input register or command register by the host all trigger this flag and EC must use A2 to distinguish whether the write is a command or data.
0	R	0h	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes the data output port and is cleared when the host reads the data out buffer.

6.6.5 EC Interface Registers

The registers of PMC can be divided into two parts: Host Interface Registers and EC Interface Registers and this section lists the EC interface. The EC interface can only be accessed by the internal 8032 processor. The base address for PM channel 1 and PM channel 2 are 1500h and 1510h respectively.

These registers are listed below.

Table 6-23. EC View Register Map, PMC

7 — 0	Offset
Host Interface PM Status (PMSTS)	00h
Host Interface PM Data Out Port (PMDO)	01h
Host Interface PM Data Out Port with SCI (PMDOSCI)	02h
Host Interface PM Data Out Port with SMI (PMDOSMI)	03h
Host Interface PM Data In Port (PMDI)	04h
Host Interface PM Data In Port with SCI (PMDISCI)	05h
Host Interface PM Control (PMCTL)	06h
Host Interface PM Interrupt Control (PMIC)	07h
Host Interface PM Interrupt Enable (PMIE)	08h

6.6.5.1 PM Status Register (PMSTS)

This register is the same as the Status register in host side but reside at EC side.

Address Offset: 00h

Bit	R/W	Default	Description
7-4	R/W	0h	**Status Register (STS)** This is a general-purpose flag used for signaling between the host and EC. When used as ACPI PM channel, the predefined meaning is burst, SCI event and SMI event.
3	R	0h	**A2 (A2)** This bit is used to indicate the last write (by host) address bit A2. If the bit is 0, it represents that the data written to the data port is data. If this bit is 1, it represents that the data written to the data port is command.
2	R/W	0h	**General Purpose flag (GPF)** This bit is used as a general-purpose flag.
1	R	0h	**Input Buffer Full (IBF)** This bit is used to indicate that the PMDIR of the PM channel has been written by the host. This bit is set when host write data port or command port and is cleared when the EC read the data in the buffer.
0	R	0h	**Output Buffer Full (OBF)** This bit is used to indicate that the PMDOR of the PM channel has been written by the EC. This bit is set when EC writes data port and is cleared when the host reads the data output buffer.

6.6.5.2 PM Data Out Port (PMDO)

This register is the PMDOR buffer. The data written to this register is stored in PMDOR.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	W	0h	**PM Data Out (PMDO[7:0])** This is the data output buffer.

6.6.5.3 PM Data Out Port with SCI (PMDOSCI)

This register is the PMDOR buffer with SCI. The data written to this register is stored in PMDOR. SCI is generated upon write.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	W	0h	**PM Data Out with SCI (PMDOSCI[7:0])** This is the data output buffer with SCI. Writing to this port will generate hardware SCI if enabled.

6.6.5.4 PM Data Out Port with SMI (PMDOSMI)

This register is the PMDOR buffer with SMI. The data written to this register is stored in PMDOR. SMI is generated upon write.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	W	0h	**PM Data Out with SMI (PMDOSMI[7:0])** This is the data output buffer with SMI. Writing to this port will generate hardware SMI if enabled.

6.6.5.5 PM Data In Port (PMDI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	0h	**PM Data In (PMDI[7:0])** This is the data input buffer.

6.6.5.6 PM Data In Port with SCI (PMDISCI)

This register is the PMDIR buffer. Host written data or command is stored in this buffer. Reading this register (EC) generates SCI.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R	0h	**PM Data In with SCI (PMDISCI[7:0])** This is the data input buffer with SCI. Reading this port will generate SCI when enabled.

6.6.5.7 PM Control (PMCTL)

Address Offset: 06h

Bit	R/W	Default	Description
7	R/W	0h	**Enhance PM Mode (APM)** Setting this bit to '1' enables the enhance PM mode. The interrupts (IRQ, SCI or SMI) are automatically generated by hardware operations if enabled.
6	R/W	1h	**SCI Negative Polarity (SCINP)** Setting this bit to '1' causes the SCI polarity inversed (low active).
5-3	R/W	0h	**SCI Pulse Mode (SCIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.

Bit	R/W	Default	Description
2	-	0h	**Reserved**
1	R/W	0h	**Output Buffer Empty Interrupt Enable (OBEIE)** Setting this bit to '1' enables the EC interrupt generation when the output buffer full flag is cleared (by host reading the data port).
0	R/W	0h	**Input Buffer Full Interrupt Enable (IBFIE)** Setting this bit to '1' enables the EC interrupt generation when the input buffer full flag is set (by host writing the data port or command port).

6.6.5.8 PM Interrupt Control (PMIC)

Address Offset: 07h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	1b	**SMI Negative Polarity (SMINP)** Setting this bit to '1' causes the SMI polarity inversed.
5-3	R/W	0h	**SMI Pulse Mode (SMIPM[2:0])** These bits are used to control the interrupt type to be level-triggered or edge-triggered (pulse) mode. In level-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and will be set to high when the interrupt condition occurs. In edge-triggered mode, the default value of IRQ1/11/12 to SERIRQ via routing logic is low and a positive pulse will be generated when the interrupt condition occurs. Note that the polarity definition in edge-triggered is different from IRQM field in KBIRQR register. 000: Level-triggered mode. 001: Edge-triggered mode with 1-cycle pulse width. 010: Edge-triggered mode with 2-cycle pulse width. 011: Edge-triggered mode with 4-cycle pulse width. 100: Edge-triggered mode with 8-cycle pulse width. 101: Edge-triggered mode with 16-cycle pulse width. Other: reserved.
2	R/W	0b	**Host SCI Control Bit (SCIB)** This bit is the SCI generation bit when hardware SCI is disabled. Read always returns the current value of SCI.
1	R/W	0b	**Host SMI Control Bit (SMIB)** This bit is the SMI generation bit when hardware SMI is disabled. Read always returns the current value of SMI.
0	R/W	1b	**Host IRQ Control Bit (IRQB)** This bit is the IRQ generation bit when hardware IRQ is disabled. Read always returns the current value of IRQ.

6.6.5.9 PM Interrupt Enable (PMIE)

Address Offset: 08h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5	R/W	0h	**Hardware SMI Enable (HWSMIEN)** Setting this bit to '1' enables the SMI generated by hardware control. Writing to the SMIB bit generates the SMI if this bit is set to '0'.

Bit	R/W	Default	Description
4	R/W	0h	**Hardware SCI Enable (HWSCIEN)** Setting this bit to '1' enables the SCI generated by hardware control. Writing to the SCIB bit generates the SCI if this bit is set to '0'.
3	R/W	0h	**Hardware IRQ Enable (HWIRQEN)** Setting this bit to '1' enables the IRQ generated by hardware control. Writing to the IRQB bit generates the IRQ if this bit is set to '0'.
2	R/W	0h	**SMI Enable (SMIEN)** Setting this bit to '1' enables the SMI generated by this module.
1	R/W	0h	**SCI Enable (SCIEN)** Setting this bit to '1' enables the SCI generated by this module.
0	R/W	0h	**IRQ Enable (IRQEN)** Setting this bit to '1' enables the IRQ generated by this module.

6.7 Real-Time Clock (RTC)

6.7.1 Overview

The RTC module provides timekeeping and calendar management capabilities. The alarm function is available ranging from once a second to once a month.

6.7.2 Feature

- Timekeeping and calendar management.
- Supports two-bank SRAM.
- Time of day alarm ranging from once a second to once a month.
- Four interrupt features are available: periodic interrupt, alarm 1 interrupt, alarm 2 interrupt, and update ended interrupt.
- Valid timekeeping during power-down.
- Supports BCD or Binary format to represent the time.
- Supports Daylight Saving Compensation function.
- Supports automatic leap year compensation function.

6.7.3 Functional Description

Timekeeping
The RTC includes two bank SRAM with 128 bytes for each bank, and provides the function of timekeeping and calendar. It uses a 32.768KHz clock signal for timekeeping. The 32.768 KHz clock can be supplied by the internal RTC oscillator circuit.
The RTC update cycle occurs once a second if the SET MODE bit in the RTC Control Register B is programmed to 0 and the Divider Chain Control field in the RTC Control Register A is programmed to 010. Time is kept in BCD or binary format, as determined by Data Mode field in the RTC Control Register B, and in either 12 or 24-hour format, as determined by Hour Mode field in the RTC Control Register B. The Daylight Saving Time function is enabled by settling the Daylight Savings (DS) bit in the RTC Control Register B.

Update Cycles
Because the time and calendar registers are updated serially, unpredictable results may occur if they are accessed during the update. Therefore, we need to ensure that reading or writing to the time registers does not coincide with a system update of these locations. There are two methods to avoid this contention. The first method is using the update-ended interrupt to avoid the update cycle period. When the update-ended interrupt is enabled, the interrupt will be generated immediately following the end of the update cycle. When the interrupt is received, this implies that an update has just been completed, and 999 ms remain until the next update. The second method uses the “Update In Progress” (UIP) bit in the RTC Control Register A to determine whether the update cycle is in progress or not. If the UIP bit is 0, it is committed that the update cycle will not start for at least 244 μs.

Interrupts
The RTC has three interrupt lines, one (IRQ) is connected to SERIRQ and handles the three interrupt conditions: Periodic Interrupt, Alarm 1 Interrupt, and Update End Interrupt The others are alarm1 interrupt and alarm2 interrupt which are connected to SWUC and INTC (INT29) respectively. The interrupts are generated if the respective enable bits in RTC Control Register B are set prior to an interrupt event occurrence. The Periodic Interrupt Rate Select (PIRSEL) field in RTC Control Register A controls the rate of the periodic interrupt. The Alarm 1 Interrupt and Alarm 2 Interrupt will be generated when the current time reaches a stored alarm time. Any alarm registers may be set to “Unconditional Match” by setting bits 7 and 6 in the alarm register. The Update Ended Interrupt is generated in the end of the update cycle.

6.7.4 Host Interface Registers

The RTC resides at LPC I/O space and the base address can be configured through LPC PNPCFG registers. The RTC logical device number is 10h (LDN=10h). For compatibility issue, the two I/O Port Base Addresses of channel are suggested to configure at 70h and 72h and it make two Index/Data pairs mapped into 70h-73h.

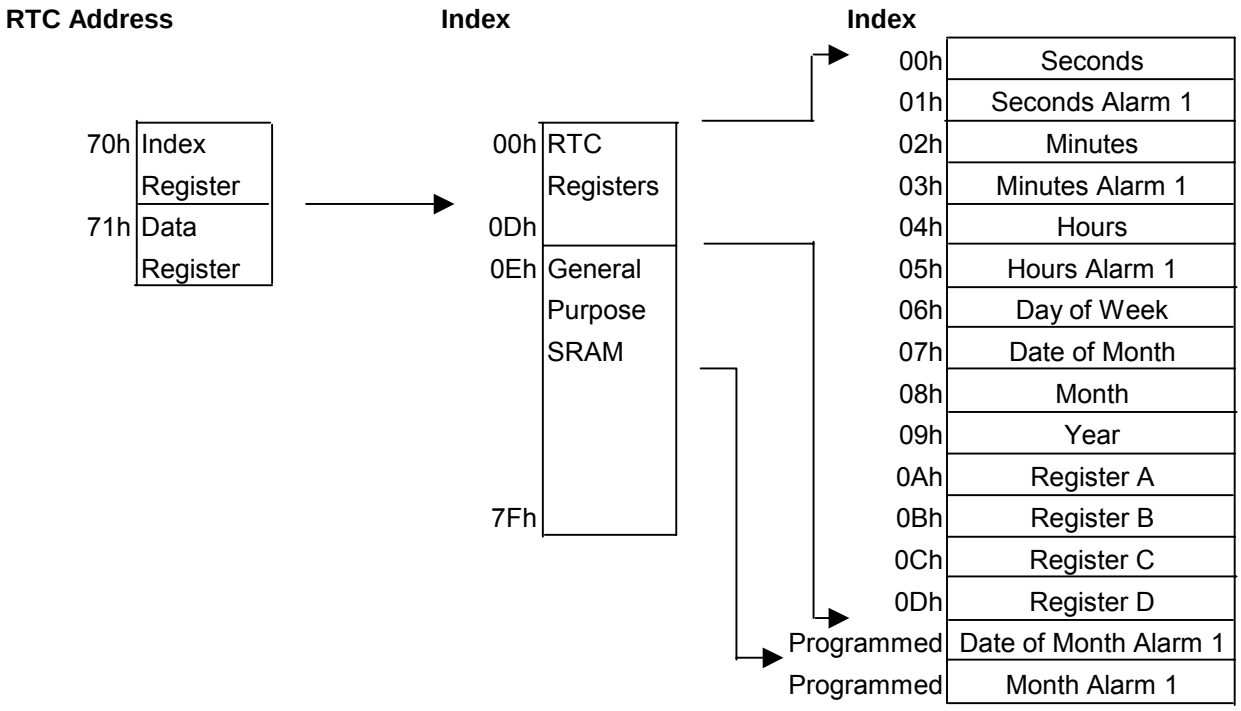
These registers are listed below.

Table 6-24. Host View Register Map, RTC

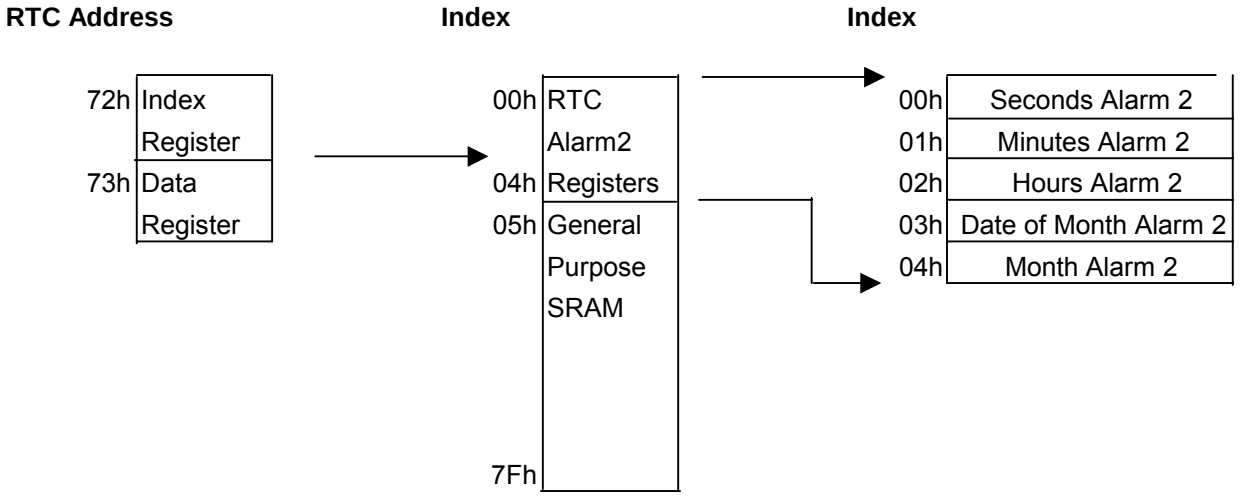
7	0	Offset
RTC Index Register of Bank 0 (RIRB0)		Legacy 70h
RTC Data Register of Bank 0 (RDRB0)		Legacy 71h
RTC Index Register of Bank 1 (RIRB1)		Legacy 72h
RTC Data Register of Bank 1 (RDRB1)		Legacy 73h

Legacy 70h represents (I/O Port Base Address 0) + (Offset 0h)
Legacy 71h represents (I/O Port Base Address 0) + (Offset 1h)
Legacy 72h represents (I/O Port Base Address 1) + (Offset 0h)
Legacy 73h represents (I/O Port Base Address 1) + (Offset 1h)
See also Table 6-3 on page 45.

The RTC has two banks of SRAM, which are Bank 0 SRAM and Bank 1 SRAM.
All RTC time, alarm data, and control registers are accessed by the RTC Index and Data Registers. Note RTC registers are not allowed to be accessed if LKRTC bit in LSIOHA register of EC2I module is set. The Index Register points to the register location being accessed, and the Data Register contains the data to be transferred to or from the location. The Bank 0 SRAM is accessed via the first pair of the Index and Data Registers (Legacy Index 70h, 71h). The Bank 1 SRAM is accessed via the second pair of the Index and Data Registers (Legacy Index 72h, 73h). The first 14 bytes and two programmable bytes of the Bank 0 SRAM are RTC time, alarm 1 data and control registers. The first 5 bytes of the Bank 1 SRAM are RTC alarm 2 data registers. Access to the RTC SRAM may be locked.



Bank 0 Register



Bank 1 Register

Figure 6-17. Register Map of RTC

Table 6-25. Host View Register Map via Index-Data I/O Pair, RTC Bank 0

	Index
Seconds Register (SECREG)	00h
Seconds Alarm 1 Register (SECA1REG)	01h
Minutes Register (MINREG)	02h
Minutes Alarm 1 Register (MINA1REG)	03h
Hours Register (HRREG)	04h
Hours Alarm 1 Register (HRA1REG)	05h
Day Of Week Register (DOWREG)	06h
Date Of Month Register (DOMREG)	07h
Month Register (MONREG)	08h
Year Register (YRREG)	09h
RTC Control Register A (CTLREGA)	0Ah
RTC Control Register B (CTLREGB)	0Bh
RTC Control Register C (CTLREGC)	0Ch
RTC Control Register D (CTLREGD)	0Dh
Date of Month Alarm 1 Register (DOMA1REG)	Programmed
Month Alarm 1 Register (MONA1REG)	Programmed

Table 6-26. Host View Register Map via Index-Data I/O Pair, RTC Bank 1

	Index
Seconds Alarm 2 Register (SECA2REG)	00h
Minutes Alarm 2 Register (MINA2REG)	01h
Hours Alarm 2 Register (HRA2REG)	02h
Date of Month Alarm 2 Register (DOMA2REG)	03h
Month Alarm 2 Register (MONA2REG)	04h

6.7.4.1 RTC Bank 0 Register

6.7.4.1.1 Seconds Register (SECREG)

Index: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Data (SECDAT)** 00 to 59 in BCD format. 00 to 3B in binary format.

6.7.4.1.2 Seconds Alarm 1 Register (SECA1REG)

Index: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Alarm 1 Data (SECA1DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.1.3 Minutes Register (MINREG)

Index: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Data (MINDAT)** 00 to 59 in BCD format. 00 to 3B in binary format.

6.7.4.1.4 Minutes Alarm 1 Register (MINA1REG)

Index: 03h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Alarm 1 Data (MINA1DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.1.5 Hours Register (HRREG)

Index: 04h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Data (HRDAT)** In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format.

6.7.4.1.6 Hours Alarm 1 Register (HRA1REG)

Index: 05h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Alarm 1 Data (HRA1DAT)** **1**. In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. **2**. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.1.7 Day Of Week Register (DOWREG)

Index: 06h

Bit	R/W	Default	Description
7-0	R/W	00h	**Day Of Week Data (DOWDAT)** 01 to 07 in BCD format. 01 to 07 in binary format.

6.7.4.1.8 Date Of Month Register (DOMREG)

Index: 07h

Bit	R/W	Default	Description
7-0	R/W	00h	**Date Of Month Data (DOMDAT)** 01 to 31 in BCD format. 01 to 1F in binary format.

6.7.4.1.9 Month Register (MONREG)

Index: 08h

Bit	R/W	Default	Description
7-0	R/W	00h	**Month Data (MONDAT)** 01 to 12 in BCD format. 01 to 0C in binary format.

6.7.4.1.10 Year Register (YRREG)

Index: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**Year Data (YRDAT)** 00 to 99 in BCD format. 00 to 63 in binary format.

6.7.4.1.11 RTC Control Register A (CTLREGA)

Index: 0Ah

Bit	R/W	Default	Description
7	R	-	**Update in Progress (UIP)** It is 0 when bit 7 of CTLREGB register is 1. 0: Timing registers will not be updated within 244 μs 1: Timing registers will be updated within 244 μs
6-4	R/W	010b	**Divider Chain Control (DICCTL)** Control the divider chain for timing generation. The following is the table of the divider chain control and test selection: **CTLREGA[6:4] Configuration** 000 Oscillator Disabled 010 Normal Operation 11x Divider Chain Reset others Test Mode

Bit	R/W	Default	Description
3-0	R/W	0000b	**Periodic Interrupt Rate Select (PIRSEL)** Control the rate of the periodic interrupt. The following is the table of the periodic interrupt rate encoding: **Rate Select / Periodic Interrupt Rate (ms) / Divider Chain Output** 0000 / No interrupts / --- 0001 / 3.906250 / 7 0010 / 7.812500 / 8 0011 / 0.122070 / 2 0100 / 0.244141 / 3 0101 / 0.488281 / 4 0110 / 0.976562 / 5 0111 / 1.953125 / 6 1000 / 3.906250 / 7 1001 / 7.812500 / 8 1010 / 15.625000 / 9 1011 / 31.250000 / 10 1100 / 62.500000 / 11 1101 / 125.000000 / 12 1110 / 250.000000 / 13 1111 / 500.000000 / 14

6.7.4.1.12 RTC Control Register B (CTLREGB)

Index: 0Bh

Bit	R/W	Default	Description
7	R/W	00h	**Set Mode (SM)** 0: Timing updates occur normally. 1: Update cycles will not occur until this bit is 0.
6	R/W	00h	**Periodic Interrupt Enable (PIE)** Enable the periodic interrupt. The rate is determined by CTLREGA[3:0]. It is cleared to 0 on RTC reset or at the time when RTC is disabled. 0: Disabled 1: Enabled
5	R/W	00h	**Alarm 1 Interrupt Enable (A1IE)** This interrupt is generated when the alarm1 condition matches the current data time. It is cleared to 0 when bit7 of CTLREGD register is 0. 0: Disabled 1: Enabled
4	R/W	00h	**Update Ended Interrupt Enable (UEIE)** This interrupt is generated when an update occurs. It is cleared to 0 on RTC reset or at the time when the RTC is disabled. 0: Disabled 1: Enabled
3	R/W-	00h	**Alarm 2 Interrupt Enable (A2IE)** This interrupt is generated when the alarm 2 condition matches the current data time. It is cleared to 0 when bit7 of CTLREGD register is 0. 0: Disabled 1: Enabled
2	R/W	00h	**Data Mode (DAM)** 0: Enable BCD format 1: Enable binary format

Bit	R/W	Default	Description
1	R/W	00h	**Hour Mode (HRM)** 0: Enable 12-hour format 1: Enable 24-hour format
0	R/W	00h	**Daylight Savings (DS)** In spring, time advances from 1:59:59 AM to 3:00:00 AM on the first Sunday in April. In fall, time returns from 1:59:59 AM to 1:00:00 AM on the last Sunday in October. 0: Disabled 1: Enabled

6.7.4.1.13 RTC Control Register C (CTLREGC)

Index: 0Ch

Bit	R/W	Default	Description
7	R	00h	**IRQ Flag (IRQF)** This flag will be set and an interrupt will be generated when one of the following conditions occurs: PIF=1 and PIE=1 A1IF=1 and A1IE=1 UEIF=1 and UEIE=1 This bit is cleared to 0 on RTC reset or at the time when the RTC is disabled. This bit is also cleared to 0 when this register is read.
6	R	00h	**Periodic Interrupt Flag (PIF)** This bit is cleared to 0 on RTC reset or at the time when the RTC is disabled. This bit is also cleared to 0 when this register is read. When the CTLREGA [3:0] bits are not 0000b, the interrupt will be generated and this bit is set to 1 once the period is specified.
5	R	00h	**Alarm 1 Interrupt Flag (A1IF)** This bit is cleared to 0 when bit 7 of CTLREGD register is 0. This bit is also cleared to 0 when this register is read. 0: No alarm condition occurred 1: Alarm 1 condition occurred
4	R	00h	**Update Ended Interrupt Flag (UEIF)** This bit is cleared to 0 on RTC reset or at the time when the RTC is disabled. This bit is also cleared to 0 when this register is read. 0: No update occurred. 1: Updated cycle is ended
3	R	00h	**Alarm 2 Interrupt Flag (A2IF)** This bit is cleared to 0 when bit 7 of CTLREGD register is 0. This bit is also cleared to 0 when this register is read. 0: No alarm condition occurred 1: Alarm 2 condition occurred
2-0	-	00h	**Reserved**

6.7.4.1.14 RTC Control Register D (CTLREGD)

Index: 0Dh

Bit	R/W	Default	Description
7	R	00h	**Valid RAM and Time (VRAT)** This bit responses whether the voltage that feeds the RTC is too low or not. 0: RTC contents are not valid. 1: RTC contents are valid.
6-0	-	00h	**Reserved**

6.7.4.1.15 Date of Month Alarm 1 Register (DOMA1REG)

The index of this register is programmable. Please see the "RTC Logical Device" for details.

Index: Programmed

Bit	R/W	Default	Description
7-0	R/W	C0h	**Date of Month Alarm 1 Data (DOMA1DAT)** 01 to 31 in BCD format. 01 to 1F in binary format. Unconditional match is selected when bit 7 and 6 are "11".

6.7.4.1.16 Month Alarm 1 Register (MONA1REG)

The index of this register is programmable. Please see the "RTC Logical Device" for details.

Index: Programmed

Bit	R/W	Default	Description
7-0	R/W	C0h	**Month Alarm 1 Data (MONA1DAT)** 01 to 12 in BCD format. 01 to 0C in binary format. Unconditional match is selected when bit 7 and 6 are "11".

6.7.4.2 RTC Bank 1 Register

6.7.4.2.1 Seconds Alarm 2 Register (SECA2REG)

Index: 00h

Bit	R/W	Default	Description
7-0	R/W	00h	**Seconds Alarm 2 Data (SECA2DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. Unconditional match is selected when bit 7 and 6 are "11".

6.7.4.2.2 Minutes Alarm 2 Register (MINA2REG)

Index: 01h

Bit	R/W	Default	Description
7-0	R/W	00h	**Minutes Alarm 2 Data (MINA2DAT)** 00 to 59 in BCD format. 00 to 3B in binary format. Unconditional match is selected when bit 7 and 6 are "11".

6.7.4.2.3 Hours Alarm 2 Register (HRA2REG)

Index: 02h

Bit	R/W	Default	Description
7-0	R/W	00h	**Hours Alarm 2 Data (HRA2DAT)** 1. In 12-hour mode: 01 to 12 (AM) and 81 to 92 (PM) in BCD format. 01 to 0C (AM) and 81 to 8C (PM) in binary format. 2. In 24-hour mode: 00 to 23 in BCD format. 00 to 17 in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.2.4 Date of Month Alarm 2 Register (DOMA2REG)

Index: 03h

Bit	R/W	Default	Description
7-0	R/W	C0h	**Date of Month Alarm 2 Data (DOMA2DAT)** 01 to 31 in BCD format. 01 to 1F in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.2.5 Month Alarm 2 Register (MONA2REG)

Index: 04h

Bit	R/W	Default	Description
7-0	R/W	C0h	**Month Alarm 2 Data (MONA2DAT)** 01 to 12 in BCD format. 01 to 0C in binary format. Unconditional match is selected when bit 7 and 6 are “11”.

6.7.4.3 RTC I/O Register

6.7.4.3.1 RTC Index Register of Bank 0 (RIRB0)

Address offset: 70h

Bit	R/W	Default	Description
7-0	R/W	-	**RTC Index Register of Bank 0(RIRB0)** This register is used to locate the data on bank 0, and is a read/write access register. It must be paired with RTC Data Register of Bank 0 to program or read the indexed registers.

6.7.4.3.2 RTC Data Register of Bank 0 (RDRB0)

Address offset: 71h

Bit	R/W	Default	Description
7-0	R/W	-	**RTC Data Register of Bank 0 (RDRB0)** This register is used to preserve the data that are to program or to read from the bank 0, and is a read/write access register. It must be paired with RTC Index Register of Bank 0 to program or read the indexed registers.

6.7.4.3.3 RTC Index Register of Bank 1 (RIRB1)

Address offset: 72h

Bit	R/W	Default	Description
7-0	R/W	-	**RTC Index Register of Bank 1(RIRB1)** This register is used to locate the data on bank 1, and is a read/write access register. It must be paired with RTC Data Register of Bank 1 to program or read the indexed registers.

6.7.4.3.4 RTC Data Register of Bank 1 (RDRB1)

Address offset: 73h

Bit	R/W	Default	Description
7-0	R/W	-	**RTC Data Register of Bank 1 (RDRB1)** This register is used to preserve the data that are to program or to read from the bank 1, and is a read/write access register. It must be paired with RTC Index Register of Bank 1 to program or read the indexed registers.

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7. EC Domain Functions

7.1 8032 Embedded Controller (EC)

7.1.1 Overview

The embedded controller is an 8032 micro-controller which is an 8051-compatible micro-controller.

7.1.2 Features

- Supports Sleep (a.k.a. power-down) and Idle mode
- Supports two external interrupts and one power fail interrupt
- Supports 64K code/data space
- Supports 256 bytes internal(w.r.t. 8032) RAM, with 128 bytes special function register
- Supports 3x16-bit timer/counter from RTC clock, TMRI0 and TMRI1
- Supports 1xwatch dog timer
- Supports full duplex UART
- Memory mapped I/O configuration
- Supports 2K bytes external SRAM

7.1.3 General Description

The 8032TT is a high-performance 8051 family compatible micro-controller based on RISC architecture & Pipeline design. This IP Specification of interface timing, external Data Memory read / write timing and external Program Memory read timing are different from that of the standard 80C52. But instruction-set is fully compatible with standard 8051 family.

Table 7-1. 8032 Port Usage

Signal	Port	Note
8032 External Data Bus	P0[7:0], P2[7:0], P3[7:6]	EC Bus MOVX instruction
INT0#	P3[2]	Driven by INTC
INT1#	P3[3]	Driven by INTC
TXD	P3[1]	TXD signal on pin
RXD	P3[0]	RXD signal on pin
T0 Timer	P3[4]	Driven by RTC 32.768 KHz
T1 Timer	P3[5]	Driven by TMRI0 pin
T2 Timer	P1[0] Note: T2 and T2EX should be taken care of if 8032 banks are switched by P1. See also section 6.3.4.2	Driven by TMRI1 pin
T2EX Timer	P1[1]	Unused

7.1.4 Functional Description

Memory
The 8032 manipulates operands in four memory spaces. There are 64K-byte Program Memory space, 64K-byte External Data Memory space, 256-byte Internal Data Memory, and with a 16-bit Program Counter space. The Internal Data Memory address space is further divided into the 256-byte Internal Data RAM and 128-byte Special Function Register address space. The up 128-bytes RAM can be reached by indirect addressing. Four Register Banks, 128 addressable bits, and the stack reside in the Internal Data RAM.

I/O ports
The 8032 has 8-bit I/O ports. The four ports provide 32 I/O lines to interface to the external world. All four ports are both byte and bit addressable. Port 0 is used as an Address/Data bus and Port 2 is used as the upper 8-bits address when external memory/device is accessed. Port 3 contains special control signals such as the read

and write strobes. Port 1 is used for both I/O and external interrupts.

Interrupts
In the 8032 there are six hardware resources that generate an interrupt request. The starting addresses of the interrupt service program for each interrupt source are like standard 8052. The external interrupt request inputs (INT0# , INT1#) can be programmed for either negative edge or low level-activated operation.

Timers / Counters
The 8032 has three 16-bit timers/counters that are the same as the timers of the standard 8051 family. The 8032 has two additional watchdog timers for system failure monitor.

Serial I/O ports
The 8032 has 1 programmable, full-duplex serial I/O ports that the function is the same as that of 8051 family and dependent on requirement.

Power Management
The 8032 supports Idle and Doze/Sleep modes of operation. In the Idle mode, the EC 8032 is stopped operation while the peripherals continue operating. In the Doze/Sleep mode, all the clocks are stopped. The Doze/Sleep mode can be waked up by INT0# or INT1# external interrupt with level trigger.

Dual Data Pointer
The 8032 has 2 data pointers (DTPR, DTPR1). These two data pointers can help users enhance lots of block data memory moving. Using dual data pointers to move block data almost saves half of the time spent by original 8051 codes.

Watch Dog Timers Interrupt / Reset
The 8032 creates one programmable watchdog timers to monitor system failure. That is maximum 2^26.

Hardware Multiply
8032 includes a hardware multiplier to enhance calculating speed. 8032 can finish one multiply instruction at 1 machine cycle.

7.1.5 Memory Organization

In 8032, the memory is organized as three address spaces and the program counter.
The memory spaces are shown in EC Memory Map.
- 16-bit Program Counter
- 64k-byte Program Memory address space
- 64k-byte External Data Memory address space
- 256-byte Internal Data Memory address

The 16-bit Program Counter register provides 8032 with its 64k addressing capabilities. The program Counter allows users to execute calls and branches to any location within the Program Memory space. There are no instructions that permit program execution to move from the Program Memory space to any of the data memory spaces.

The 64k-byte Program Memory address space is located by dedicated address bus. The 64k-byte External Data Memory address space is automatically accessed when the MOVX instruction is executed. The Internal Data Memory space is subdivided into a 256-byte Internal Data RAM address Space and a 128-byte Special Function Register address space as shown in the SFRs Map. The Internal Data RAM address space is 0 to 255. Four 8-Register Banks occupy locations 0 through 31. The stack can be located anywhere in the Internal Data RAM address space. In addition, 128 bit location ns of the on-chip RAM are accessible through Direct Addressing.

7.1.6 On-Chip Peripherals

Table 7-2. System Interrupt Table

Interrupt Source	Request Flag		Priority Flag	Enable Flag	Vector Address	Priority-Within-Level	Flag Cleared by Hardware?
External Request	IE0/TCON.1		PX0/IP.0	EX0/IE.0	0003h	1	Edge-Yes Level-No
Internal Timer0/Counter0	TF0/TCON.5		PT0/IP.1	ET0/IE.1	000Bh	2	Yes
External Request	IE1/TCON.3		PX1/IP.2	EX1/IE.2	0013h	3	Edge-Yes Level-No
Internal Timer1/Counter1	TF1/TCON.7		PT1/IP.3	ET1/IE.3	001Bh	4	Yes
Internal Serial Port	Xmit	TI/SCON.1	PS/IP.4	ES/IE.4	0023h	5	No
	Rcvr	RI/SCON.0					
Internal Timer2/Counter2	TF2/T2CON.7		PT2/IP.5	ET2/IE.5	002Bh	6	No
	EXF2/TSCON.6						

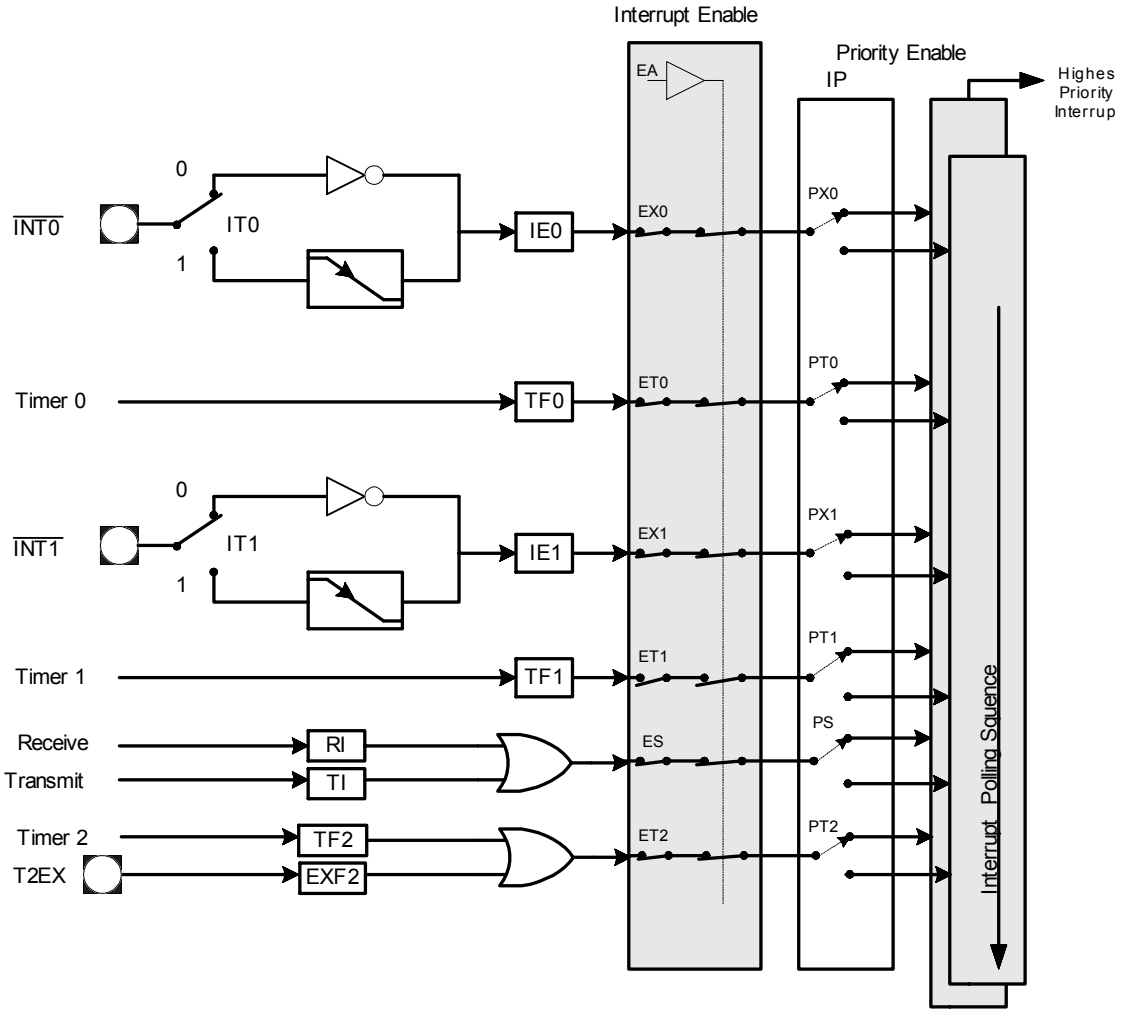

Figure 7-1. Interrupt Control System Configuration

Note: T2EX is tied to logic high and is not available in IT8510.

External Interrupt

External Interrupt INT0# and INT1# input signal may each be programmed to be level-triggered or edge triggered depending upon bits IT0 and IT1 in the TCON register. If IT0 or IT1 = 0, INT0# or INT1# is triggered by

detected low at the input signal. If IT0 or IT1 = 1, INT0# or INT1# is negative-edge triggered. External interrupts are enabled with bits EX0 and EX1in the IE register. Evens on the external interrupt input signals set the interrupt flags IE0 or IE1 in TCON. These request bits are cleared by hardware vectors to service routines only if the interrupt is negative-edge triggered. If the interrupt is level triggered, the interrupt service routine must clear the request bit. External hardware must release INT0# or INT1# before the service routine completes, or an additional interrupt is requested.

External interrupt input signals are sampled once every oscillator clock's rising edge. A level-triggered interrupt input signal held low or high for at least three clocks guarantees detection. Edge-triggered external interrupts only the request input signal for one clo/ck time. This ensures edge recognition and sets interrupt request bit EX0 or EX1. The 8032 clears EX0 or EX1 automatically during service routine fetch cycles for edge-triggered interrupts.

Timer Interrupts
Sources of timer 0, timer 1 and timer 2 are RTC clock (32.768KHz), TMRI0 and TMRI1 from pins. Three timer-interrupt request bits TF0, TF1 and TF2 are set by timer 0, timer 1 and timer 2 overflow. When timer 0 and timer 1 interrupts are generated, the bits TF0 and TF1 are cleared by an on-chip hardware vector to an interrupt service routine. Timer 2 is different from timer 0 or timer 1. Timer 2 has to clear TF2 bit by software writing when timer 2 interrupt is generated. Timer interrupts are enabled by bits ET0, ET1, and ET2 in the IE register.

Timer 2 interrupts are generated by a logical OR of bits TF2 and EXF2 in register T2CON. Neither flag is cleared by a hardware vector to a service routine. In fact, the interrupt service routine must determine if TF2 or EXEF2 generates the interrupt, and then clear the bit. Timer 2 interrupt is enabled by ET2 in register IE.

Serial Port Interrupt
Serial port interrupts are generated by the logical OR of bits RI and TI in the SCON register. Neither flag is cleared by a hardware vector to the service routine. The service routine resolves RI and TI interrupt generation and clears the serial port request flag. The serial port interrupt is enabled by bit ES in the IE register in the same way by using serial port 1.

Interrupt Priority
8032 has 2 level priorities. Setting / clearing a bit in the Interrupt Priority register (IP) or Extent Interrupt Priority register (EIP) establish its associated interrupt request as a high / low priority. If a low-priority level interrupt is being serviced, a high-priority level interrupt will interrupt it. However, an interrupt source cannot interrupt a service program of the same or higher level. The interrupt priority is shown on Interrupt Control System Configuration.

Interrupt Response Time
The Figure of Interrupt Response Time shows the response time is between the interrupt request being active and the interrupt service routing being executed. The minimum interrupt response time is eight clocks that when an interrupt request asserts after the ending instruction execution completes. The maximum interrupt response time is 24 clocks when an interrupt request asserts during the ending instruction, DJNZ direct, rel or other instruction sets whose operation period is 16 clocks and is decoded ok. However, a high priority interrupt asserts while a low priority interrupt service program is executing. The minimum and the maximum interrupt response time is 8 clocks and 24 clocks respectively.

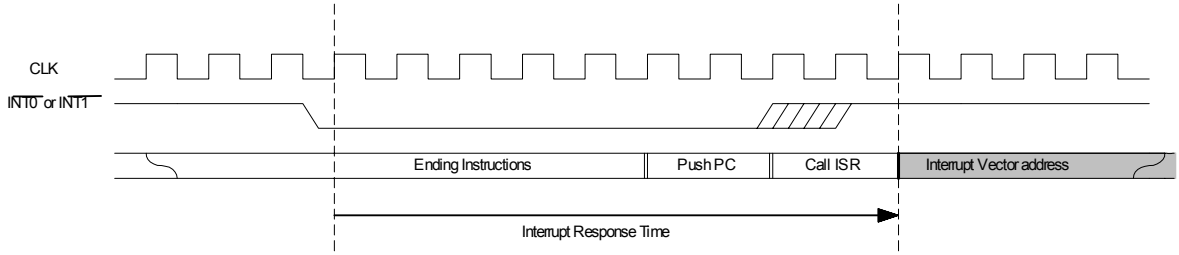

Figure 7-2. Interrupt Response Time

7.1.7 Timer / Counter

Timer 0
Timer 0 functions as either a timer or event counter in four modes of operation. Timer 0 is controlled by the four low-order bits of the TMOD register and bits 5, 4, 1 and 0 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/T), and mode of operation (M1, M0). The TCON register provides timer 0 control functions: overflag (TF0), run control (TR0), interrupt flag (IE0), and interrupt type control (IT0). For normal timer operation (GATE = 0), setting TR0 allows TL0 to be incremented by the selected input. Setting GATE and TR0 allows INT0# to control timer operation.

Timer0/Mode 0 (13-bit Timer)
Mode 0 configures timer 0 as a 13-bit timer which is set up as an 8-bit timer (TH0 register) with a module 32 prescaler implemented with the lower five bits of the TL0 register. The upper three bits of TL0 register are indeterminate and should be ignored. Prescaler overflow increments the TH0 register.

Timer 0/ Mode 1 (16-bit Timer)
Mode 1 configures timer 0 as a 16-bit timer with TH0 and TL0 connected in cascade. The selected input increments TL0.

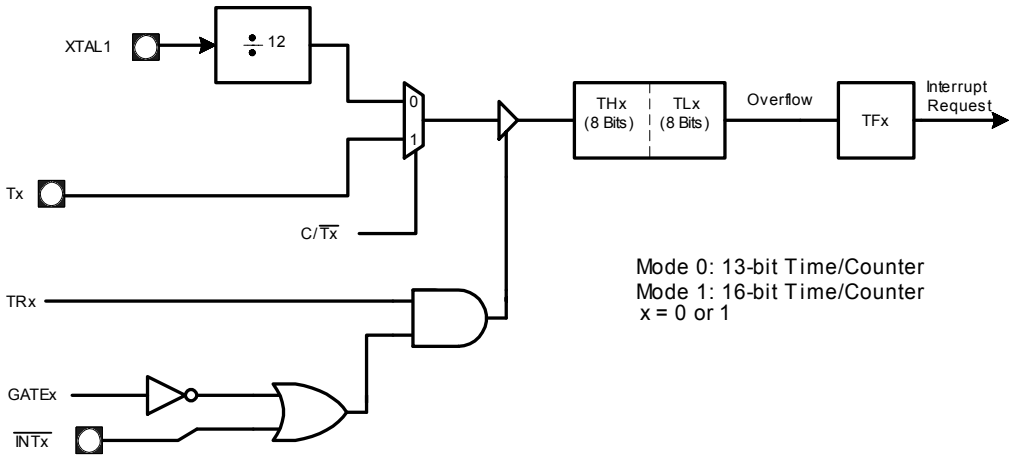

Figure 7-3. Timer 0/1 in Mode 0 and Mode 1

Timer 0/ Mode 2 (8-bit Timer With Auto-reload)
Mode 2 configures timer 0 as an 8-bit timer (TL0 register) that automatically reloads from the TH0 register. TL0 overflow sets the timer overflow flag (TF0) in the TCON register and reloads TL0 with the contents of TH0, which is preset by software. When the interrupt request is serviced, hardware clears TF0. The reload leaves TH0 unchanged.

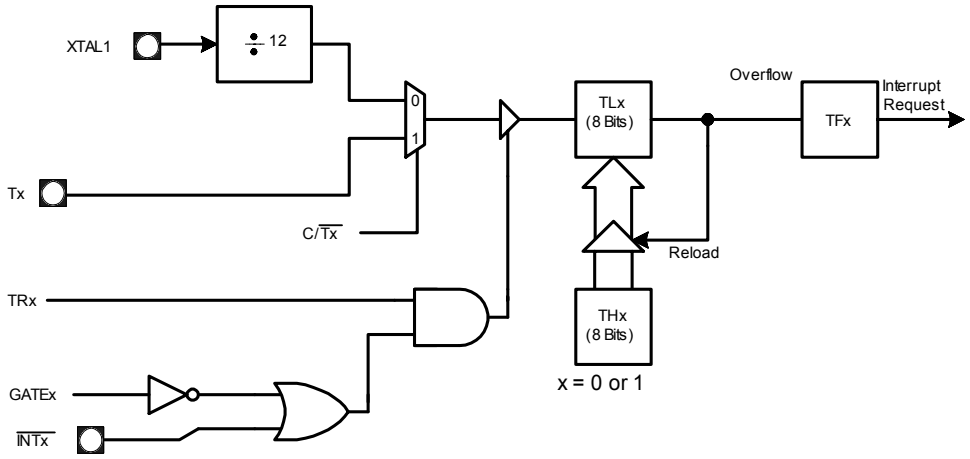

Figure 7-4. Timer 0/1 in Mode 2, Auto-Reload

Timer 0/ Mode 3(Two 8-bit Timers)

Mode 3 configures timer 0 such that registers TL0 and TH0 operate as separate 8-bit timers. This mode is provided for application requiring an additional 8-bit timer or counter. TL0 uses the timer 0 control bits C/T and GATE in TMOD, and TR0 in TCON in the normal manner. TH0 is locked into a timer function (counting 8032_Freq/12) and takes over use of the timer 1 interrupt (TF1) and run control (TR1) bits. Thus, operation of timer 1 is restricted when timer 0 is in mode 3.

Note:

8032_Freq is normally EC Clock 10 MHz and may be divided by CFSELR register.

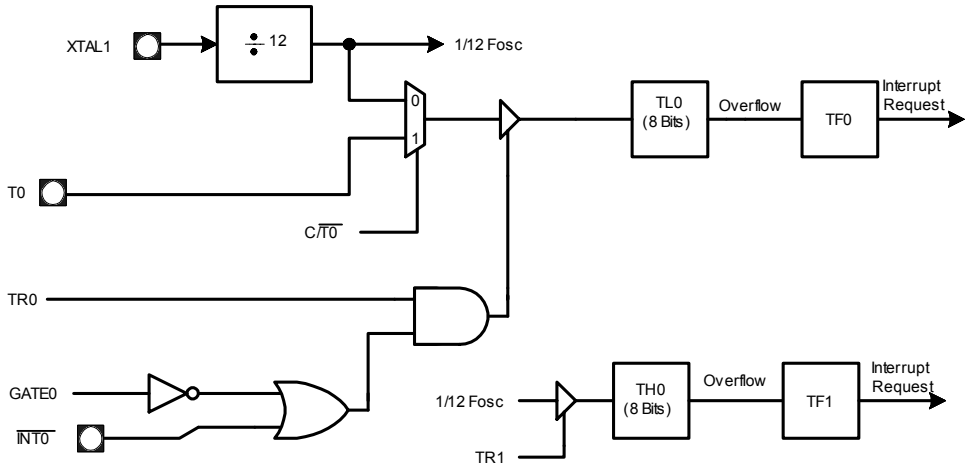

Figure 7-5. Timer 0 in Mode 3 Two 8-bit Timers

Timer 1

Timer 1 functions as either a timer or event counter in three modes of operation. The logical configuration for modes 0, 1 and 2 is the same as that of Timer 0. Mode 3 of timer 1 is a hold-count mode.

Timer 1 is controlled by the four high-order bits of the TMOD register and bits 7, 6, 3 and 2 of the TCON register. The TMOD register selects the method of timer gating (GATE), timer or counter operation (C/ T), and mode of operation (M1 and M0). The TCON register provides timer 1 control functions: overflow flag (TF1), run control (TR1), interrupt flag(IE1), and interrupt type control (IT1).

For normal timer operation (GATE = 0), setting TR1 allows timer register TL1 to be incremented by the selected

input. Setting GATE and TR1 allows external input signal INT1# to control timer operation. This setup can be used to make pulse width measurements.

Timer 1/ Mode 0 (13-bit Timer)
Mode 0 configures timer 0 as a 13-bit timer, which is set up as an 8-bit timer (TH1 register) with a modulo-32 prescaler implemented with the lower 5 bits of the TL1 register. The upper 3 bits of the TL1 register are ignored. Prescaler overflow increment the TH1 register.

Timer1/ Mode 1 (16-bit Timer)
Mode 1 configures timer 1 as a16-bit timer with TH1 and TL1 connected in cascade. The selected input increments TL1.

Timer 1/ Mode 2 (8-bit Timer)
Mode 2 configures timer 1 as an 8-bit timer (TL1 register) with automatic reload from the TH1 register on overflow. Overflow from TL1 sets overflow flag TF1 in the TCON register and reloads TL1 with the contents of TH1, which is preseted by software. The reload leaves TH1 unchanged.

Timer 1/ Mode3 (Halt)
Placing timer in mode 3 causes it to halt and its count. This can be used to halt timer 1 when the TR1 run control bit is not available, i.e., when timer 0 is in mode 3.

Timer 2
Timer 2 is a 16-bt timer/count maintained by two eight-bit timer registers, TH2 and TL2, which are connected in cascade. The timer/counter 2 mode control register T2MOD and the timer /counter control register T2CON control the operation of timer 2.

Timer 2 provides the following operating modes: capture mode, auto-reload mode, baud rate generator mode, and programmable clock-out mode. Select the operating mode with T2MOD and TCON register bits as shown in table of Timer 2 Modes of Operation. Auto-reload is the default mode. Setting RCLK and/or TCLK selects the baud rate generator mode.

Timer 2 operation is similar to timer 0 and timer 1. C/2 T selects 8032_Freq/12 (timer operation) or external input signal T2 (counter operation) as the timer register input. Setting TF2 to be incremented by the selected input.

Timer 2/ Capture Mode
In the capture mode, timer 2 function as a 16-bit timer or counter. An overflow condition sets bit TF2, which you can use to request an interrupt. Setting the external enable bit EXEN2 allows the RCAP2Hand RCAP2L registers to capture the current value in timer registers TH2 and TL2 in response to a l-to-0 transition at external input T2EX. The transition at T2EX also sets bit EXF2 on T2CON. The EXF2 bit, like TF2, can generate an interrupt. TR2 must be enabled when this mode is run.
Note: T2EX is tied to logic high and is not available in IT8510.

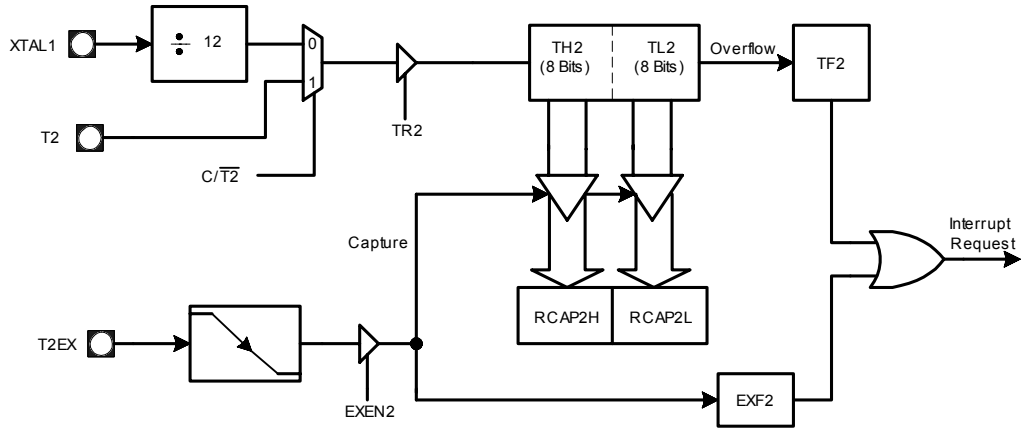

Figure 7-6. Timer 2: Capture Mode

Note: T2EX is tied to logic high and is not available in IT8510.

Timer 2/ Auto-reload Mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. The timer operates as an up counter or up/down counter, as determined by the down counter enable bit (DCEN). At device reset, DCEN is cleared, so in the auto-reload mode, timer 2 defaults to operation as an up counter. TR2 must be enabled when this mode is run.

Up Counter Operation

When DCEN = 0, timer 2 operates as an up counter. If EXEN = 0, timer 2 counts up to FFFFh and sets the TF2 overflow flag. The overflow condition loads the 16-bit value in the reload/capture registers (RCAP2H, RCAP2L) into the timer registers (TH2, TL2). The values in RCAP2H and RCAP2L are preset by software.

If EXEN2 = 1, the timer registers are reloaded by either a timer overflow or a high-to-low transition at external input T2EX. This transition also sets the EXF2 bit in the T2CON register. Either TF2 or EXF2 bit can generate a timer 2 interrupt request. TR2 must be enabled when his mode is run.

Up/Down Counter Operation

When DCEN = 1, timer 2 operates as an up/down counter. External input signal T2EX controls the direction of the count. When T2EX is high, timer 2 counts up. The timer overflow occurs at FFFFh, which sets the timer 2 overflow flag (TF2) and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers (TH2, TL2) equals the value stored in RCAP2H and RCAP2L. The underflow sets the TF2 bit and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows changing the direction of the count. When timer 2 operates as an up/down counter, EXF2 does not generate an interrupt. This bit can be used to provide 17-bit resolution. TR2 must be enabled when his mode is run.

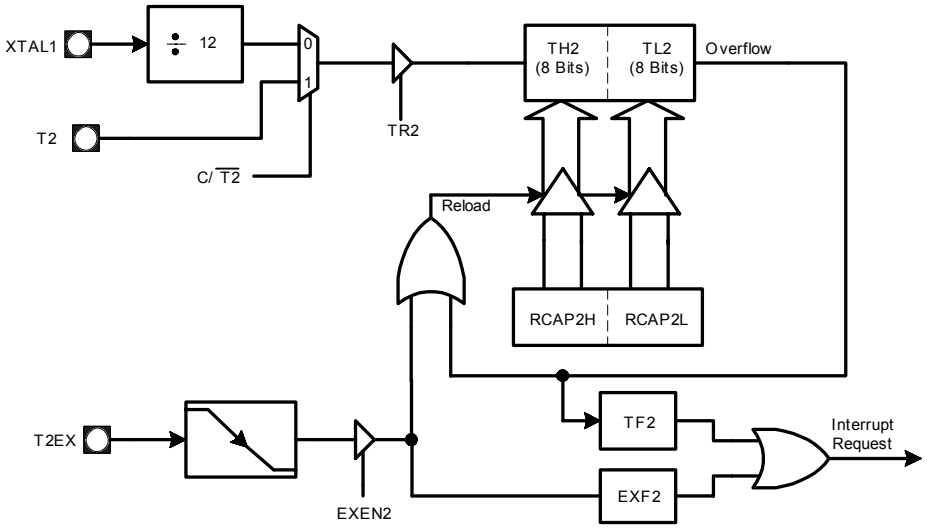

Figure 7-7. Timer 2: Auto Reload (DECN = 0)

Note: T2EX is tied to logic high and is not available in IT8510.

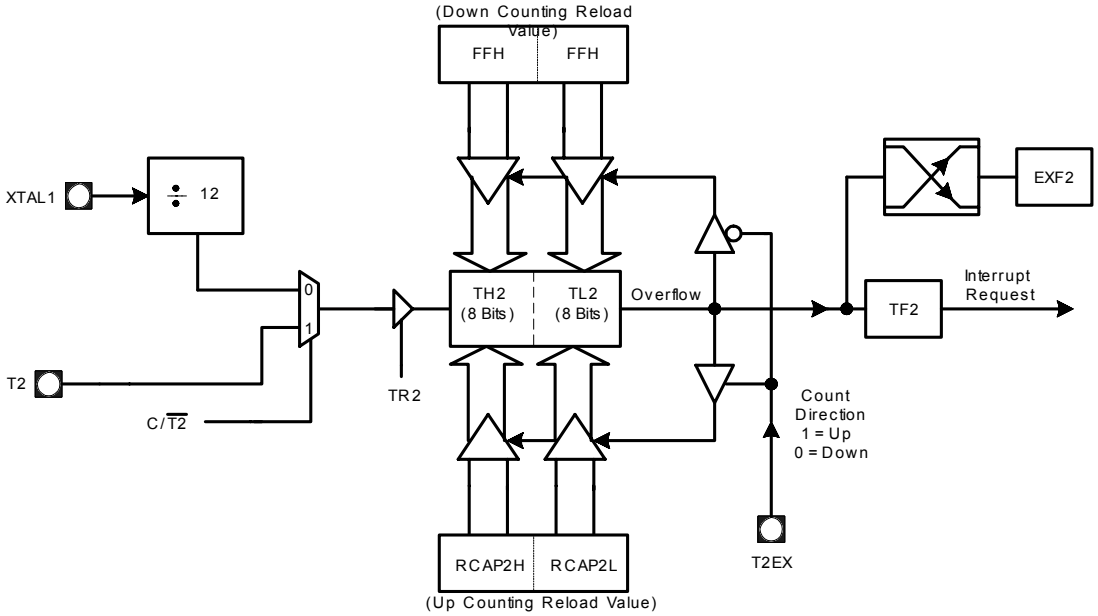

Figure 7-8. Timer 2: Auto Reload Mode (DECN = 1)

Note: T2EX is tied to logic high and is not available in IT8510.

Timer 2/ Baud Rate Generator Mode

This mode configures timer 2 as a baud rate generator for use with the serial port. Select this mode by setting the RCLK and/or TCLK bits in T2CON.

Timer 2/ Clock-out Mode

In the clock-out mode, timer 2 functions as a 50%-duty-cycle, variable-frequency clock. The input clock increments TL0 at frequency 8032_Freq/2. The timer repeatedly counts to overflow from a preloaded value. At overflow, the contents of the RCAP2H and RCAP2L registers are loaded into TH2/TL2. In this mode, timer 2 overflows do not generates interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers:

Clock-out Frequency = 8032_Freq / {4X(65536 - RCAP2H, RCAP2L)}

Note:
8032_Freq is normally EC Clock 10 MHz and may be divided by CFSELR register.

Table 7-3. Timer 2 Modes of Operation

Mode	RCLK OR TCLK (in T2COON)	CP/RL2# (in T2MOD)	T2OE (in T2MOD)
Auto-reload Mode	0	0	0
Capture Mode	0	1	0
Baud Rate Generator Mode	1	X	X
Programmable Clock-Out	X	0	1

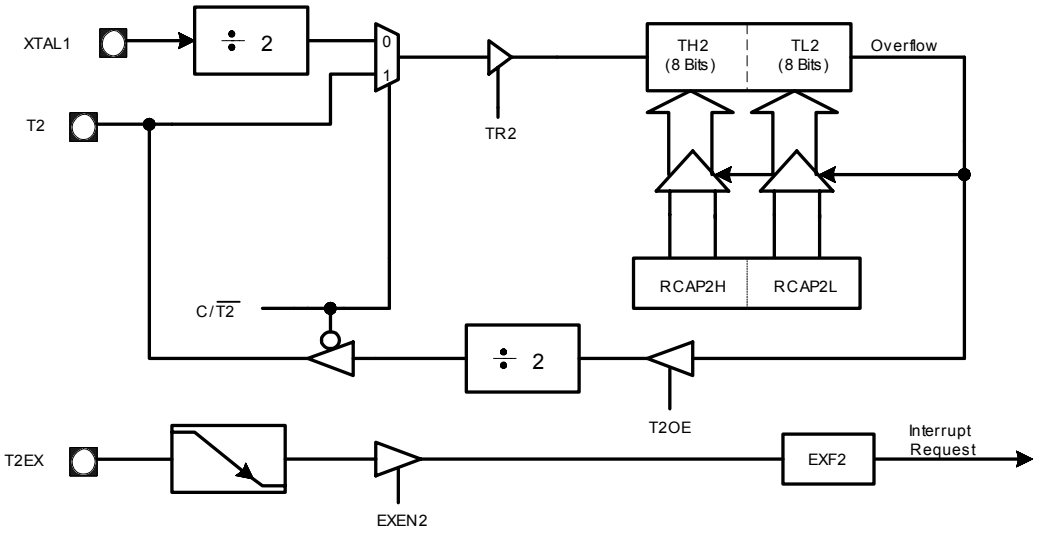

Figure 7-9. Timer 2: Clock Out Mode

Note: T2EX is tied to logic high and is not available in IT8510.

Watchdog Timer
The watchdog timer has system reset functions. Users can set WD1-1, WD1-0 (in register CKCON, 8Eh) to choose 2^17, 2^20, (56/63)*2^23 or 2^26 counter for Watchdog Timer. After the Watchdog Timer counts the specific counter and an overflow occurs, set WDTRST Flag (in register WDTCON, D8h) and finally reset the 8032. If 8032 has been reset by Watchdog Timer, WDTEN Flag remains one.

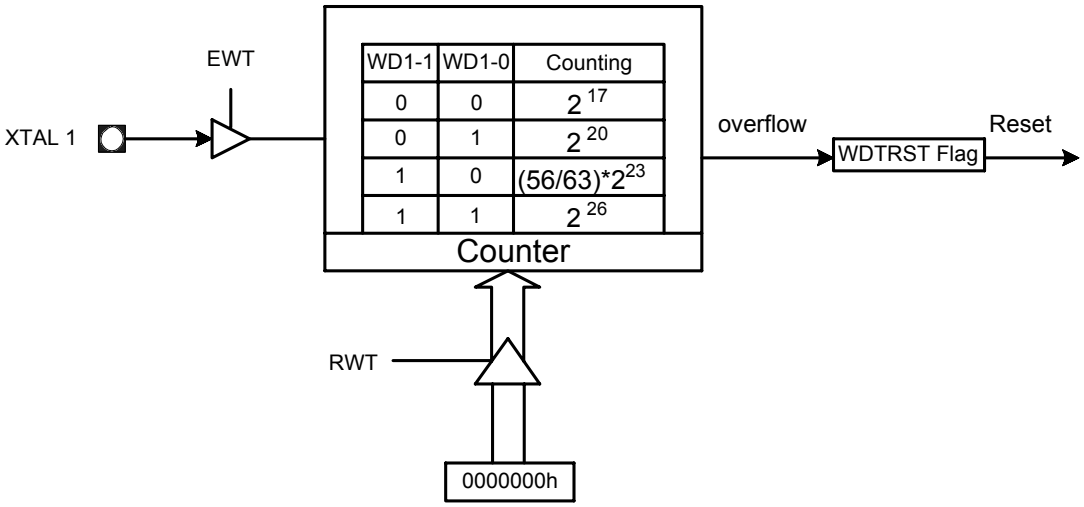

Figure 7-10. Watchdog Timer

SERIAL I/O PORT

The serial I/O port provides both synchronous and asynchronous communication modes. It operates as a universal asynchronous receiver and transmitter (UART) in three full-duplex modes (modes 1, 2, and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates. The serial port also operates in a single synchronous mode (mode 0).

The synchronous mode (mode 0) operates at a single baud rate. Mode 2 operates at a two-baud rate. Modes 1 and 3 operate over a wide range of baud rates, which are generated by timer 1 and timer 2.

The serial port signals are defined in Table of Serial Port Signals, and the serial port special function registers (SBUF, SCON) are described in the section of Special Function Registers.

For the three asynchronous modes, the UART transmits on the TXD pin and receives on the RXD pin. For the synchronous mode (mode 0), the UART outputs a clock signal on the TXD pin and sends and receives messages in the RXD pin. The SBUF register, which holds received bytes and bytes to be transmitted, actually consists of two physically different registers. To send, software writes a byte to SBUF; to receive, software reads SBUF. The receive shift register allows reception of a second byte before the byte has been read from SBUF. However, if software has not read the first byte by the time the second byte is received, the second byte will overwrite the first. The UART sets interrupt bits TI and RI on transmission and reception, respectively. These two bits share a single interrupt request and interrupt vector.

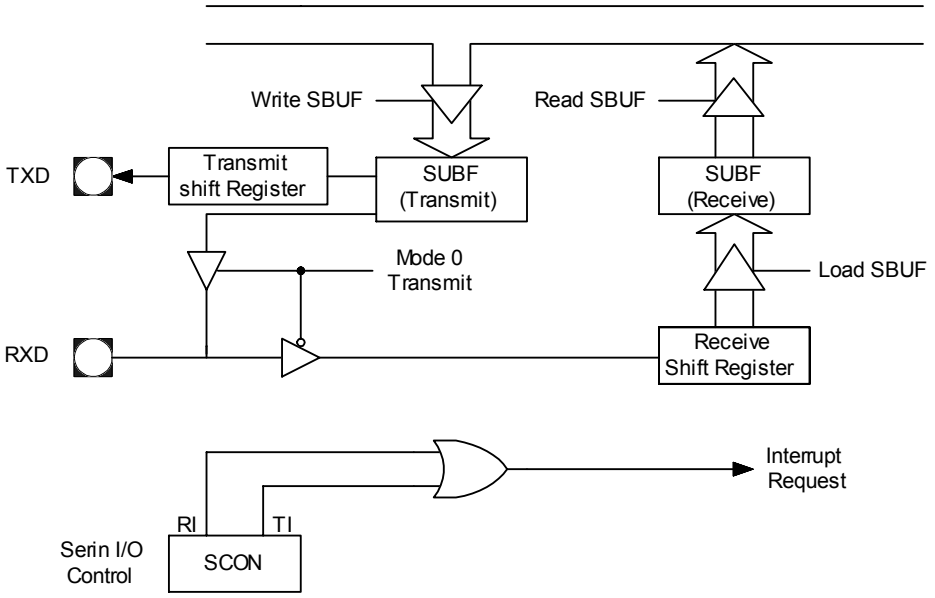

Figure 7-11. Serial Port Block Diagram

Table 7-4. Serial Port Signals

Function Name	Type	Description	Multiplexed With
TXD	O	Transmit Data. In mode 0, TXD transmits the clock signal. In modes 1, 2, and 3, TXD transmits serial data.	P3.1
RXD	I/O	Receive Data. In mode 0, RXD transmits and receives serial data. In mode 1, 2, and 3, RXD receives serial data.	P3.0

Synchronous Mode (Mode 0)

Mode 0 is a half-duplex, synchronous mode, which is commonly used to expand I/O capabilities of device with shift registers. The transmit data (TXD) pin outputs a set of eight clock pulses. The receive data (RXD) pin transmits or receives a byte of data. The eight data bits are transmitted and received least-significant bit (LSB) first. Shifts occur in the last phase (S6P2) of every peripheral cycle, which corresponds to a baud rate of 8032_Freq/12.

Transmission (Mode 0)

Follow the following steps to begin a transmission:

1. Write to the SCON register, and clear bits SM0, SM1, and REN.
2. Write the byte to be transmitted to the SBUF register. This write starts the transmission.

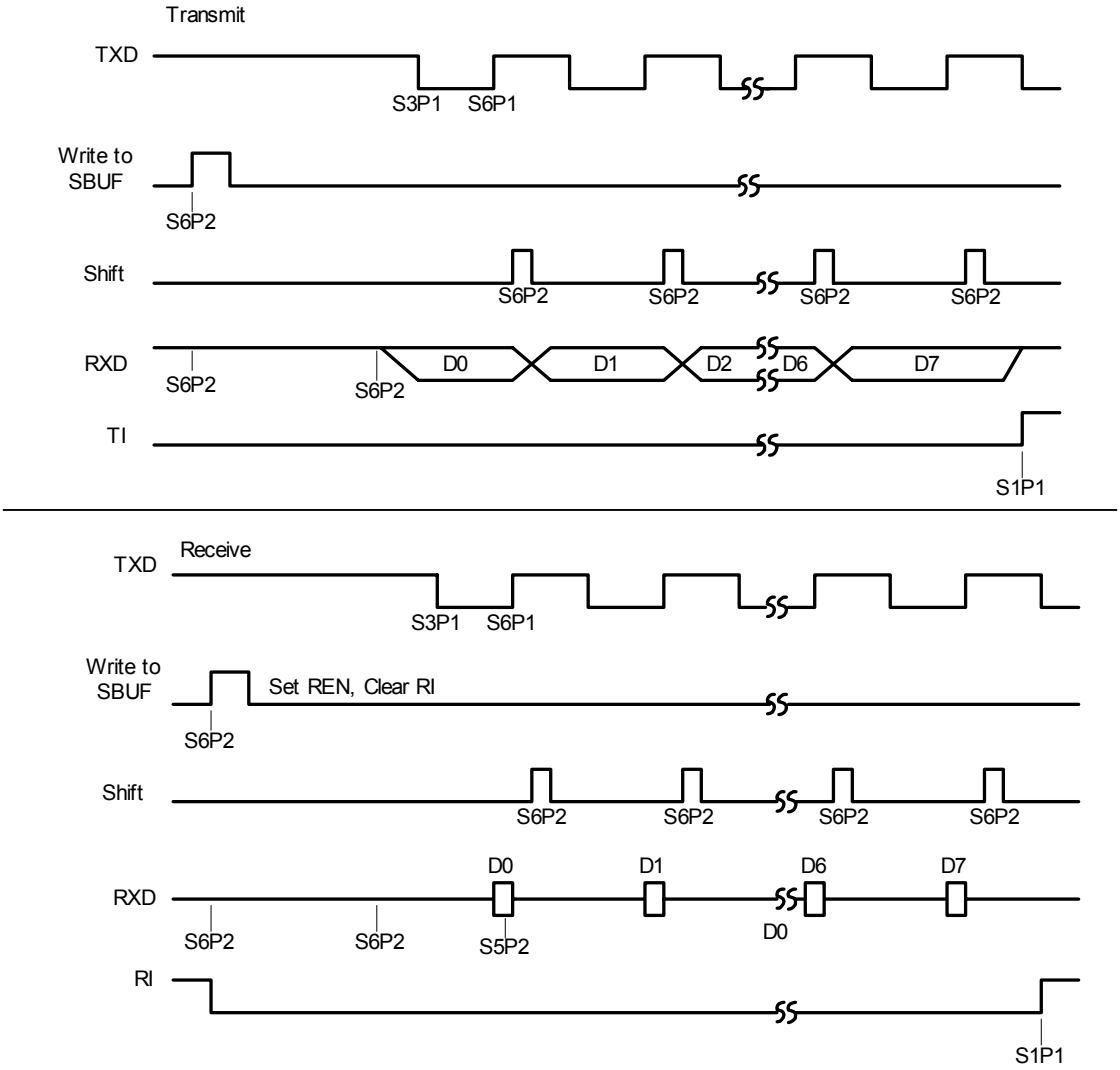

Figure 7-12. Mode 0 Timing

Hardware executes the write to SBUF in the last phase (S6P2) of a peripheral cycle. At S6P2 of the following cycle, hardware shifts the LSB (D0) onto the RXD pin. At S3P1 of the next cycle, the TXD pin goes low for the first clock-signal pulse. Shifts continue every peripheral cycle. In the ninth cycle after the write to SBUF, the MSB (D7) is on the RXD pin. At the beginning of the tenth cycle, hardware drives the RXD pin high and asserts TI (S1P1) to indicate the end of the transmission.

Reception (Mode 0)
To start a reception in mode 0, write to the SCON register. Clear bits SM0, SM1 and RI and set the REN bit.

Hardware executes the write to SCON in the last phase (S6P2) of a peripheral cycle. In the second peripheral cycle following the write to SCON, TXD goes low at S3P1 for the first clock-signal pulse, and the LSB (D0) is sampled on the RXD pin at S5P2. The D0 bit is then shifted into the shift register. After eight shifts at S6P2 of every peripheral cycle, the LSB (D7) is shifted into the shift register, and hardware asserts RI (S1P1) to indicate a completed reception. Software can then read the received byte from SBUF.

Asynchronous Modes (Modes 1, 2, and 3)
The serial port has three asynchronous modes of operation.

Mode 1
Mode 1 is a full-duplex, asynchronous mode. The data frame consists of 10 bits: one start bit, eight data bits, and one stop bit. Serial data is transmitted on the TXD pin and received on the RXD pin. When a message is received, the stop bit is read in the RB8 bit in the SCON register. The baud rate is generated by overflow of timer 1 or timer 2.

Mode 2 and 3
Mode 2 and 3 are full-duplex and asynchronous modes. The data frame consists of 11 bits: one start bit, eight data bits (transmitted and received LSB first), one programmable ninth data bit, and one stop bit which is read from the RB8 bit in the SCON register. On transmit, the ninth data bit is written to the TB8 bit in the SCON register. Alternatively, you can use the ninth bit as a command/data flag.
- In mode 2, the baud rate is programmable to 1/32 or 1/64 of the oscillator frequency.
- In mode 3, the baud rate is generated by overflow of timer 1 or timer 2.

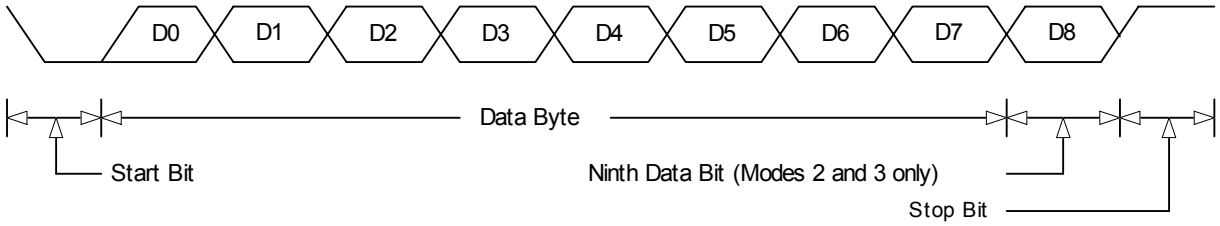

Figure 7-13. Data Frame (Mode 1, 2 and 3)

Transmission (Mode 1, 2, 3)
Follow these steps below to initiate a transmission:
1. Write to the SCON register. Select the mode with the SM0 and SM1 bits, and clear the REN bit.
For mode 2 and 3, write the ninth bit to the TB8 bit.
2. Write the byte to be transmitted to the SBUF register. This write starts the transmission.

Reception (Mode 1, 2, 3)
To prepare for a reception, set the REN bit in the SCON register. The actual reception is then initiated by a detected high-to-low transition on the RXD pin.

Baud Rates

Baud Rate for Mode 0
The baud rate for mode 0 is fixed at 8032_Freq/12.

Baud Rates for Mode 2
Mode 2 has a two-baud rate, which is selected by the SMOD bit in the PCON register. The following expression defines the baud rate:
Serial I/O Mode 2 Baud Rate = (2 ^ SMOD) x (8032_Freq / 64)
Note: 8032_Freq is normally EC Clock 10 MHz and may be divided by CFSELR register.

Baud Rates for Mode 1 and 3
In mode 1 and 3, the baud rate is generated by overflow of timer (default) and/or timer 2. You may select either or both timers to generate the baud rate(s) for the transmitter and/or the receiver.

Timer 1 Generated Baud Rates (Mode 1 and 3)
Timer 1 is the default baud rate generator for the transmitter and the receiver in mode 1 and 3. The baud rate is determined by the timer 1 overflow rate and the value of SMOD, as shown in the following formula:
Serial I/O Mode 1 and 3 Baud Rate = (2 ^ SMOD) x (Timer 1 Overflow Rate) / 32
Selecting Timer 1 as the Baud Rate Generator
To select timer 1 as the baud rate generator:
• Disable the timer interrupt by clearing the IE0 register.

• Configure timer 1 as a timer or an event counter (set or clear the C/T bit in the TMOD register).
Serial I/O Mode 1 and 3 Baud Rate = (2 ^ SMOD) x 8032_Freq / (32 x 12 x (256 – TH1))
Note:
8032_Freq is normally EC Clock 10 MHz and may be divided by CFSELR register.

• Select timer mode 0-3 by programming the M1 and M0 bits in the TMOD register.
In most applications, timer 1 is configured as a timer in auto-reload mode (high nibble of TMOD = 0010B). The resulting baud rate is defined by the following expression:
Timer 1 can generate very low baud rates by the following setups:
• Enable the timer 1 interrupt by setting the ET1 bit in the IE register.
• Configure timer 1 to run as a 16-bit timer (high nibble of TMOD = 0001B).
• Use the timer 1 interrupt to initiate a 16-bit software reload.

Timer 2 Generated Baud Rates (Modes 1 and 3)
Timer 2 may be selected as the baud rate generator for the transmitter and/or receiver. The baud rate generator mode of timer 2 is similar to the auto-reload mode. A rollover in the TH2 register reloads registers TH2 and TL2 with the 16-bit value on registers RCAP2H and RCAP2L, which are presented by software.
The baud rate of timer 2 is expressed by the following formula:
Serial I/O Mode 1 and 3 Baud Rate = (Timer 2 Overflow Rate) / 16

Selecting Timer 2 as the Baud Rate Generator
To select timer 2 as the baud rate generator for the transmitter and/or receiver, program the RCLCK and TCLCK bits in the T2CON register. Setting RCLK and/or TCLK puts timer 2 into its baud rate generator mode. In this mode, a rollover in the TH2 register does not set the TF2 bit in the T2CON register. Besides, a high-to-low transition at the T2EX input signal sets the EXF2 bit in the T2CON register but does not cause a reload from (RCAP2H, RCAP2L) to (TH2, TL2). You can use the T2EX input signal as an additional external interrupt by setting the EXEN2 bit in T2CON.

Note: T2EX is tied to logic high and is not available in IT8510.
Note:
Turn off the timer (clear the TR2 bit in the T2CON register) before accessing registers TH2, TL2, CAP2H and RCAP2L. You may configure timer 2 as a timer or a counter. In most applications, it is configured for timer operation (i.e., the C/T2 bit is cleared in the T2CON register).

Table 7-5. Selecting the Baud Rate Generator(s)

RCLK Bit	TCLCK Bit	Receiver Baud Rate Generator	Transmit ter Baud Rate generator
00		Timer 1	Timer 1
01		Timer 1	Timer 2
10		Timer 2	Timer 1
11		Timer 2	Timer 2

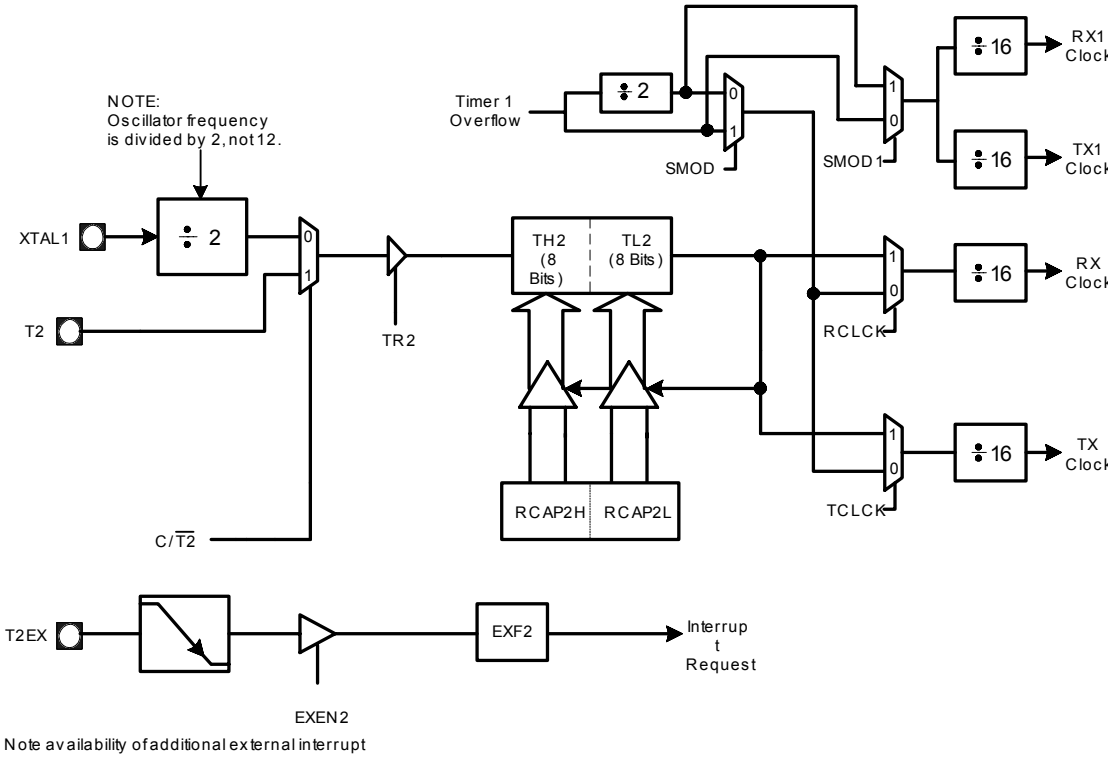

Figure 7-14. Timer 2 in Baud Rate Generator Mode

Note: T2EX is tied to logic high and is not available in IT8510.

Note that timer 2 increments every state time (2Tosc) when it is in the baud rate generator mode. In the baud rate formula that follows, “RCAP2H, RCAP2L” denoting the contents of RCAP2H and RCAP2L is taken as a 16-bit unsigned integer:
Serial I/O Mode 1 and 3 Baud Rate = 8032_Freq x (32 X [65536 - (RCAP2H,RACAP2L)])

Note:
8032_Freq is normally EC Clock 10 MHz and may be divided by CFSELR register.

When timer 2 is configured as a timer and is in baud rate generator mode, do not read or write the TH2 or TL2 registers. The timer is being incremented every state time, and the result of a read or write may not be accurate. In addition, you may read but not write to the RCAP2 registers; a write may overlap a reload and cause write and/or reload errors.

7.1.8 Idle and Doze/Sleep Mode

Idle Mode
When set IDL bit in PCON(87h), the 8032 will enter an Idle mode. In the Idle mode, the 8032 is idle while all the on-chip peripherals remain active. The internal RAM and SFRs registers remain unchanged during this mode. The Idle mode can be terminated by any enabled internal/external interrupt or by a hardware reset.
Doze/Sleep Mode
When set PD bit in PCON(87h), the 8032 will enter a Doze/Sleep mode. In the Doze/Sleep mode, the 8032 clock is stopped, and the 10 MHz PLL may be alive or stopped depending on PLLCTRL . The Doze/Sleep mode can be waked up by the hardware reset or by the external enabled interrupt with level trigger activation (ITx in register TCON is set to 0). The Program Counter, internal RAM and SFRs registers retain their values and will not be changed after the exiting Doze/Sleep mode by external interrupt. The reset will restart the 8032, while the SFRs with initial values and the internal RAM retain their values.

7.1.9 EC Internal Register Description

The embedded 8032 internal memory space and special function registers (F0h-80h) are listed below.

Table 7-6. Internal RAM Map

7							0	Index
Bank 0								7h-0h
Bank 1								Fh-8h
Bank 2								17h-10h
Bank 3								1Fh-18h
Addressable Bits								2Fh-20h
General Purpose RAM								7Fh-2Fh
Indirect Addressing Register								FFh-80h

7							0	SFR Index
PCON	DPS	DPH1	DPL1	DPH	DPL	SP	P0	80h
	CKCON	TH1	TH0	TL1	TL0	TMOD	TCON	88h
							P1	90h
						SBUF	SCON	98h
							P2	A0h
							IE	A8h
							P3	B0h
							IP	B8h
		STATUS						C0h
		TH2	TL2	RCAP2H	RCAP2L	T2MOD	T2CON	C8h
							PSW	D0h
							WDTCON	D8h
						PDCON	ACC	E0h
								E8h
							B	F0h
								F8h

7.1.9.1 Port 0 Register (P0R)

Address: 80h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P0 Register Bit [7:0] (P0)** This is the 8-bit 8032 port 0.

7.1.9.2 Stack Pointer Register (SPR)

Address: 81h

Bit	R/W	Default	Description
7-0	R/W	07h	**Stack Pointer Bit [7:0] (SP)** This is the 8-bit stack pointer.

7.1.9.3 Data Pointer Low Register (DPLR)

Address: 82h

Bit	R/W	Default	Description
7-0	R/W	0h	**Data Pointer Low Bit [7:0] (DPL)** This is the 8-bit data pointer low byte.

7.1.9.4 Data Pointer High Register (DPHR)

Address: 83h

Bit	R/W	Default	Description
7-0	R/W	0h	**Data Pointer High Bit [7:0] (DPH)** This is the 8-bit data pointer high byte.

7.1.9.5 Data Pointer 1 Low Register (DP1LR)

Address: 84h

Bit	R/W	Default	Description
7-0	R/W	0h	**Data Pointer 1 Low Bit [7:0] (DPL1)** This is the 8-bit data pointer 1 low byte.

7.1.9.6 Data Pointer 1 High Register (DP1HR)

Address: 85h

Bit	R/W	Default	Description
7-0	R/W	0h	**Data Pointer 1 High Bit [7:0] (DPH1)** This is the 8-bit data pointer 1 high byte.

7.1.9.7 Data Pointer Select Register (DPSR)

Address: 86h

Bit	R/W	Default	Description
7-1	-	0h	**Reserved**
0	R/W	0h	**Data Pointer Select (DPS)** Setting '1' selects the data pointer 1 (DPL1, DPH1) while setting '0' selects the data pointer (DPL, DPH).

7.1.9.8 Power Control Register (PCON)

Address: 87h

Bit	R/W	Default	Description
7	R/W	0h	**Serial Port Double Baud Rate (SMOD1)** Setting '1' doubles the baud rate when timer 1 is used and mode 1, 2, or 3 is selected in SCON register.
6	-	0h	**Reserved**
5-2	-	0h	**Reserved**
1	R/W	0h	**Power Down Mode (PD)** Set "1" to enter a Sleep (a.k.a power-down) or Doze mode immediately. The Sleep or Doze mode is controlled by PPDC bit. Exit Sleep or Doze mode and clear this bit by external interrupt or hardware reset.
0	R/W	0h	**Idle Mode (IDL)** Set "1" to enter idle mode immediately. Exit idle mode and clear this bit by internal interrupt and external interrupt or hardware reset.

7.1.9.9 Timer Control Register (TCON)

Address: 88h

Bit	R/W	Default	Description
7	R/W	0h	**Timer 1 Overflow (TF1)** This bit is set by hardware when timer 1 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
6	R/W	0h	**Timer 1 Run Control (TR1)** Setting '1' enables timer 1 operation and setting '0' disables timer 1.
5	R/W	0h	**Timer 0 Overflow (TF0)** This bit is set by hardware when timer 0 register overflows. This bit is cleared by hardware when the processor vectors to the interrupt service routine.
4	R/W	0h	**Timer 0 Run Control (TR0)** Setting '1' enables timer 0 operation and setting '0' disables the timer 0.
3	R/W	0h	**Interrupt 1 Edge Detect (IE1)** This bit is set by hardware when an edge or a level is detected on external INT1 (depends on the setting of **IT1**). This bit is cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.
2	R/W	0h	**Interrupt 1 Type Select (IT1)** Setting '1' selects the edge-triggered for INT1. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and need IT0 and IT1 to be set as level-low triggered.
1	R/W	0h	**Interrupt 0 Edge Detect (IE0)** Set by hardware when an edge or a level is detected on external INT0 (depends on the setting of **IT0**). Cleared by hardware when the interrupt service routine is processed if an edge trigger is selected.
0	R/W	0h	**Interrupt 0 Type Select (IT0)** Setting '1' selects the edge-triggered for INT0. Setting '0' selects a level-triggered. Don't write 1 to this bit because interrupt triggered type is considered in INTC module and need IT0 and IT1 to be set as level-low triggered.

7.1.9.10 Timer Mode Register (TMOD)

Address: 89h

Bit	R/W	Default	Description
7	R/W	0h	**Timer 1 Gate (GATE1)** 0: Timer 1 will clock when **TR1=**1, regardless of the state of INT1. 1: Timer 1 will clock only when **TR1=**1 and INT1 is deasserted.
6	R/W	0h	**Timer 1 Source (SRC1)** 0: timer 1 counts the divided-down EC clock. 1: timer 1 counts negative transitions on T1 input of 8032 from TMRI0 pin.
5-4	R/W	0h	**Timer 1 Mode (MODE1)** 0h: 8-bit timer/counter (TH1) with 5-bit prescaler (TL1) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL1). Reload from TH1 at overflow. 3h: timer 1 halted. Retains count.
3	R/W	0h	**Timer 0 Gate (GATE0)** 0: Timer 0 will clock when TR0=1, regardless of the state of INT0. 1: Timer 0 will clock only when TR0=1 and INT0 is deasserted.

Bit	R/W	Default	Description
2	R/W	0h	**Timer 0 Source (SRC0)** 0: timer 0 counts the divided-down EC clock. 1: timer 0 counts negative transitions on T0 input of 8032 from RTC 32.768 KHz.
1-0	R/W	0h	**Timer 0 Mode (MODE0)** 0h: 8-bit timer/counter (TH0) with 5-bit prescaler (TL0) 1h: 16-bit timer/counter 2h: 8-bit auto-reload timer/counter (TL0). Reload from TH0 at overflow. 3h: timer 0 halted. Retains count.

7.1.9.11 Timer 0 Low Byte Register (TL0R)

Address: 8Ah

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 0 Low Byte Bit [7:0] (TL0)** Timer 0 low byte register.

7.1.9.12 Timer 1 Low Byte Register (TL1R)

Address: 8Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 1 Low Byte Bit [7:0] (TL1)** Timer 1 low byte register.

7.1.9.13 Timer 0 High Byte Register (TH0R)

Address: 8Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 0 High Byte Bit [7:0] (TH0)** Timer 0 high byte register.

7.1.9.14 Timer 1 Low Byte Register (TH1R)

Address: 8Dh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 1 High Byte Bit [7:0] (TH1)** Timer 1 high byte register.

7.1.9.15 Clock Control Register (CKCON)

Address: 8Eh

Bit	R/W	Default	Description
7-6	R/W	0h	**Watch Dog Time Out Counter Select (WD[1:0])** 0h: 17-bit counter 1h: 20-bit counter 2h: (56/63)*2^{23} counter 3h: 26-bit counter
5	R/W	0h	**Timer 2 Clock (T2M)** 0: timer 2 clock is EC clock / 12. 1: timer 2 clock is EC clock / 4.

Bit	R/W	Default	Description
4	R/W	0h	**Timer 1 Clock (T1M)** 0: timer 1 clock is EC clock / 12. 1: timer 1 clock is EC clock / 4.
3	R/W	0h	**Timer 0 clock (T0M)** 0: timer 0 clock is EC clock / 12. 1: timer 0 clock is EC clock / 4.
2-0	R/W	0h	**Wait State for MOVX (MD[2:0])** 0h : no wait state 1h : Original+4T 2h : Original+8T 3h : Original+12T 4h : Original+16T 5h : Original+20T 6h : Original+24T 7h : Original+28T

7.1.9.16 Port 1 Register (P1R)

Address: 90h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P1 Register Bit [7:0] (P1)** This is the 8-bit 8032 port 1.

7.1.9.17 Serial Port Control Register (SCON)

Address: 98h

Bit	R/W	Default	Description
7	R/W	0h	**Serial Port Mode 0 (SM0_0)** Serial port mode control is set/cleared by software.
6	R/W	0h	**Serial Port Mode 1 (SM1_0)** Serial port mode control is set/cleared by software.
5	-	0h	**Reserved**
4	R/W	0h	**Receive Enable (REN)** Receiver enable bit. Setting '1' enables the serial data reception. Setting '0' disables the serial data reception.
3	R/W	0h	**Transmit Bit 8 (TB8)** Transmit bit 8, set/cleared by hardware to determine the state of the ninth data bit transmitted in 9-bit UART mode.
2	R/W	0h	**Receive Bit 8 (RB8)** Receive bit 8, set/cleared by hardware to determine the state of the ninth data bit received in 9-bit UART mode.
1	R/W	0h	**Transmit Interrupt (TI)** Transmit interrupt, set by hardware when the byte is transmitted and cleared by software after serving.
0	R/W	0h	**Receive Interrupt (RI)** Receive interrupt, set by hardware when the byte is received and cleared by software when data is processed.

7.1.9.18 Serial Port Buffer Register (SBUFR)

Address: 99h

Bit	R/W	Default	Description
7-0	R/W	0h	**Serial Port Buffer Bit [7:0] (SBUF)** This is the 8-bit 8032 serial port data buffer. Writing to **SBUF** loads the transmit buffer to the serial I/O port. Reading **SBUF** reads the receive buffer of the serial port.

7.1.9.19 Port 2 Register (P2R)

Address: A0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P2 Register Bit [7:0] (P2)** This is the 8-bit 8032 port 2.

7.1.9.20 Interrupt Enable Register (IE)

Address: A8h

Bit	R/W	Default	Description
7	R/W	0h	**Global Interrupt Enable (EA)** Setting this bit enables all interrupts that are individually enabled by bit 0-6. Clearing this bit disables all interrupts.
6	R/W	0h	**Serial Port 1 Interrupt Enable (ES1)** Setting this bit enables the serial port 1 interrupt.
5	R/W	0h	**Timer 2 Overflow Interrupt Enable (ET2)** Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0h	**Serial Port 0 Interrupt Enable (ES0)** Setting this bit enables the serial port 0 interrupt.
3	R/W	0h	**Timer 1 Overflow Interrupt Enable (ET1)** Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0h	**External Interrupt 1 Enable (EX1)** Setting this bit enables the external interrupt 1.
1	R/W	0h	**Timer01 Overflow Interrupt Enable (ET0)** Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0h	**External Interrupt 0 Enable (EX0)** Setting this bit enables the external interrupt 0.

7.1.9.21 Port 3 Register (P3R)

Address: B0h

Bit	R/W	Default	Description
7-0	R/W	FFh	**P3 Register Bit [7:0] (P3)** This is the 8-bit 8032 port 3.

7.1.9.22 Interrupt Priority Register (IP)

Address: B8h

Bit	R/W	Default	Description
7	-	0h	**Reserved**
6	R/W	0h	**Serial Port 1 Interrupt Priority (PS1)** Setting this bit enables the serial port 1 interrupt.
5	R/W	0h	**Timer 2 Overflow Interrupt Priority (PT2)** Setting this bit enables the timer 2 overflow interrupt.
4	R/W	0h	**Serial Port 0 Interrupt Priority (PS0)** Setting this bit enables the serial port 0 interrupt.
3	R/W	0h	**Timer 1 Overflow Interrupt Priority (PT1)** Setting this bit enables the timer 1 overflow interrupt.
2	R/W	0h	**External Interrupt 1 Priority (PX1)** Setting this bit enables the external interrupt 1.
1	R/W	0h	**Timer01 Overflow Interrupt Priority (PT0)** Setting this bit enables the timer 0 overflow interrupt.
0	R/W	0h	**External Interrupt 0 Priority (PX0)** Setting this bit enables the external interrupt 0.

7.1.9.23 Status Register (STATUS)

Address: C5h

Bit	R/W	Default	Description
7	-	0b	**Reserved**
6	R/W	0b	**High priority interrupt status (HIP)**
5	R/W	0b	**Low priority interrupt status (LIP)**
4-2	-	0h	**Reserved**
1	R/W	0b	**Serial Port 0 Transmit Activity Monitor (SPTA0)**
0	R/W	0b	**Serial Port 0 Receive Activity Monitor (SPRA0)**

7.1.9.24 Timer 2 Control Register (T2CON)

Address: C8h

Bit	R/W	Default	Description
7	R/W	0h	**Timer 2 Overflow (TF2)** Set by hardware when the timer 2 overflows. It must be cleared by software. TF2 is not set if RCLK=1orTCLK=1.
6	R/W	0h	**Timer 2 External Flag (EXF2)** If EXEN2=1, a capture or reload is caused by a negative transition on T2EX sets EFX2. EFX2 dose not cause an interrupt in up/down counter mode (DCEN=1).
5	R/W	0h	**Receive Clock (RCLK)** Selects timer 2 overflow pulses (RCLK=1) or timer 1 overflow pulses (RCLK=0) as the baud rate generator for port mode 1 and 3.
4	R/W	0h	**Receive Clock (RCLK)** Selects timer 2 overflow pulses (TCLK=1) or timer 1 overflow pulses (TCLK=0) as the baud rate generator for port mode 1 and 3.

Bit	R/W	Default	Description
3	R/W	0h	**Timer 2 External Enable (EXEN2)** Setting EXEN2 causes a capture or reload to occur as a result of a negative transition on T2EX unless timer 2 is being used as the baud rate generator for the serial port. Clearing EXEN2 causes timer 2 to ignore events at T2EX.
2	R/W	0h	**Timer 2 Run Control (TR2)** Setting this bit starts the timer.
1	R/W	0h	**Timer/Counter 2 Select (CT2)** 0: timer 2 counts the divided-down EC clock. 1: timer 2 counts negative transitions on T2 input of 8032 from TMRI1 pin.
0	R/W	0h	**Capture/Reload (CPRL2)** When this bit is set, captures occur on negative transitions at T2EX if EXEN2=1. When reloads occur o if EXEN2=1, the CP/ 2 RL bit is ignored and timer 2 is forced to auto-reload on timer 2 overflow if RCLK =1 or TCLK = 1.

7.1.9.25 Timer Mode Register (T2MOD)

Address: C9h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0h	**Timer 2 Output Enable (T2OE)** In the timer 2 clock-out mode, this bit connects the programmable clock output to External signal T2.
0	R/W	0h	**Down Count Enable (DCEN)** This bit configures timer 2 as an up/down counter.

7.1.9.26 Timer 2 Capture Low Byte Register (RCAP2LR)

Address: CAh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 2 Capture Low Byte Bit [7:0] (RCAP2L)** Low byte of the timer2 reload/recapture register. This register stores 8-bit values to be loaded into or captured from the timer register TL2 in timer 2**.**

7.1.9.27 Timer 2 Capture High Byte Register (RCAP2HR)

Address: CBh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 2 Capture High Byte Bit [7:0] (RCAP2H)** High byte of the timer2 reload/recapture register. This register stores 8-bit values to be loaded into or captured from the timer register TH2 in timer 2**.**

7.1.9.28 Timer 2 Low Byte Register (TL2R)

Address: CCh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 2 Low Byte Bit [7:0] (TL2)** Timer 2 low byte register.

7.1.9.29 Timer 2 High Byte Register (TH2R)

Address: CDh

Bit	R/W	Default	Description
7-0	R/W	0h	**Timer 2 High Byte Bit [7:0] (TH2)** Timer 2 high byte register.

7.1.9.30 Program Status Word Register (PSW)

Address: D0h

Bit	R/W	Default	Description
7	R/W	0h	**Carry Flag (CF)** CY is set if the operation result in a carry out of (during addition) or a borrow into (during subtraction) the high-order bit of the result; otherwise CY is cleared.
6	R/W	0h	**Auxilary Carry Flag (AC)** AC is set if the operation result in a carry out of the low-order 4 bits of the result (during addition) or a borrow form the high-order bits into the low-order 4 bits (during subtraction); otherwise AC is cleared.
5	R/W	0h	**User Flag 0 (F0)** General-purpose flag.
4-3	R/W	0h	**Register Bank Select Bit [1:0](RS1:0)** 0h: bank 0, 00h-07h 1h: bank 1, 08h-0Fh 2h: bank 2, 10h-17h 3h: bank 3, 18h-1Fh
2	R/W	0h	**Overflow Flag (OV)** This bit is set if an addition or signed variables result in an overflow error (i.e., if the magnitude of the sum or difference is too great for the seven LSBs in 2's – complement representation). The overflow flag is also set if the multiplication product overflows one byte or if a division by zero is attempted.
1	R/W	0h	**User Defined Flag (UD)** General-purpose flag.
0	R/W	0h	**Parity Flag (P)** This bit indicates the parity of the accumulator. It is set if an odd number of bits in the accumulator is set. Otherwise, it is cleared. Not all instructions update the parity bit. The parity bit is set or cleared by instructions that change the contents to the accumulator.

7.1.9.31 Watch Dog Timer Control Register (WDTCON)

Address: D8h

Bit	R/W	Default	Description
7	-	0h	**Reserved**
6-2	-	0h	**Reserved**
1	R/W	0h	**Watch Dog Timer Enable (WDTEN)** Setting '1' enables the watchdog timer.
0	R/W	0h	**Watch Dog Timer Reset (WDTRST)** Setting '1' resets the watchdog timer.

7.1.9.32 Accumulator Register (ACC)

Address: E0h

Bit	R/W	Default	Description
7-0	R/W	0h	**Accumulator Bit [7:0] (ACC[7:0])** The instruction uses the accumulator as both source and destination for calculations and moves.

7.1.9.33 Power Down Control Register (PDCON)

Address: E1h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2	R/W	0h	**Reserved**
1	R/W	0h	**Just Wake Up (JWP)** 0: Execute interrupt after wake-up even interrupt had been de-asserted. 1: Don't execute interrupt after wake-up if interrupt had been de-asserted.
0	R/W	1h	**Power Down Control (PDC)** Reserved, always write 1 to it.

7.1.9.34 B Register (BR)

Address: F0h

Bit	R/W	Default	Description
7-0	-	0h	**B Register (B[7:0])** The B Register is used as both a source and destination in multiply and divide operations.

7.1.10 Programming Guide

Code snipper of entering Idle/Doze/Sleep mode

```
; Power-down ADC/DAC analog circuit
; Disable unnecessary channel of INTC/WUC

mov     dptr, #1e03h        ; PLLCTRL register
mov     a, #01h             ; 00h for Doze mode
                            ; 01h for Sleep mode
movx    @dptr, a

nop                         ; Reserved
orl     pcon, #01h          ; #01h for Idle mode
                            ; #02h for Doze/Sleep mode

; Repeat "nop" eight times immediately
; for internal bus turn-around
nop                         ; 1st
nop                         ; 2nd
nop                         ; 3rd
nop                         ; 4th
nop                         ; 5th
nop                         ; 6th
nop                         ; 7th
nop                         ; 8th
```

Code snipper of Scratch ROM

```
; First copy data from code space to Scratch RAM in data space,
; then switch the location of Scratch SRAM from data to code space.

; copy 256 bytes from code space to scratch RAM
;   code space: ff00h ~ ffffh (byte)
;   data space: 0700h ~ 07ffh (byte)

        mov     r6, #00h
copy_loop:
        mov     dptr, #0ff00h       ; read from code space from ff00h (byte)
        mov     a, r6
        movc    a,  @a+dptr
        mov     dph, #07h           ; write to  data space from 0700h (byte)
        mov     dpl, r6
        movx    @dptr, a

        inc     r6
        cjne    r6, #00h, copy_loop ; copy 256 bytes

        ; switch scratch SRAM from scratch RAM to scratch ROM
        mov     dptr, #1000h        ; FBCFG register
        movx    a, @dptr
        orl     a, #82h             ; Scratch ROM
        movx    @dptr, a
```

7.2 Interrupt Controller (INTC)

7.2.1 Overview

INTC mainly collects several interrupts from modules. Using interrupt driven design has a better performance than polling-driven.

It traps PWRFAIL# and samples 31 interrupt channels, then outputs to the INT0# and INT1# of 8032.

Both interrupts INT0# and INT1# to 8032 are generated by INTC, and don't write 1 to IT0 and IT1 bit in TCON because interrupt triggered type is considered in INTC and need IT0 and IT1 to be set as level-low triggered.

Note INT0# and INT1# are external interrupts of 8032 and they are controlled by EA, EX0 and EX1 in IE register.

External interrupts can wakeup 8032 from Idle/Doze/Sleep mode, but internal interrupts can wakeup 8032 from Idle mode only.

7.2.2 Features

- Configurable level-triggered and edge-triggered mode
- Configurable interrupt polarity of triggered mode
- Clear registers for edge-triggered interrupts
- Each interrupt source can be enabled/masked individually
- Special handler for power-fail (INT0# of 8032)

7.2.3 Functional Description

7.2.3.1 Power Fail Interrupt

The INTC collects interrupts sources from internal and external (through WUC) and provides two interrupt requests INT0# and INT1# to 8032. 8032 treats INT0# as a higher priority interrupt request than INT1#. INTC uses INT0# as a power-fail interrupt and INT1# as a maskable interrupt. The firmware should enable the IE0 and IE1 bit in TCON before all.

To implement a power-fail application, connect GPB7 to external circuit. Firmware puts the GPB7 in alternative function, enables the Smitter Trigger of GPB7 to receive an asynchronous external input, and provides relative INT0# interrupt routine.

There are two methods to trap a power-fail event: “Trap Enabled” and “Trap Enabled and Locked”. Users select “Trap Enabled” by setting TREN bit in PFAILR and select “Trap Enabled and Locked” by setting TRENL bit in PFAILR. If both bits are selected, TREN bit is ignored. If “Trap Enabled” is used, power-fail event is detected by falling edge transition of PWRFAIL#, and INT0# to 8032 is asserted. After INT0# is set, TREN bit is cleared. “Trap Enabled and Locked” method is similar to “Trap Enabled” method but TRENL will not be cleared after INT0# is set.

7.2.3.2 Programmable Interrupts

INTC also collects 31 maskable interrupt sources and make a request on INT1 # of 8032 if triggered. Each channel can be individually enabled or masked by IERx. If an interrupt channel is masked and one interrupt request is triggered, the request is masked (inhibited, not canceled), and will be asserted the request on INT1# if it is enabled.

The ISRx indicates the status of interrupt regardless of IERx. In the level-triggered mode, ISRx is affected by corresponding interrupt sources, and firmware should clear the interrupt status on interrupt sources after its request is handled. In edge-triggered mode, ISRx is set by selected edge transition (determined by IELMRx) of corresponding interrupts sources, and firmware should write 1 to clear to ISRx after this request is handled.

Firmware may use the IVECT to determine which channel is to be serviced first or have its priority rule by reading ISRx and IERx. IVECT treats INT1 as the lowest priority interrupt and INT31 as the highest priority interrupt.

The 8032 always wakes up from Idle/Doze/Sleep mode when it detects an enabled external interrupt and it wakes up from Idle mode by internal interrupt, too. Firmware should disable unwanted interrupt sources to prevent from waking up unexpectedly.

Note that interrupts from WUC are not always level-triggered interrupts since they may be just throughout WUC if the corresponding channels at WUC are disabled (bypassed). If an edge-triggered passes through WUC and INTC with WUC corresponding channel is disabled and INTC corresponding channel is level-trig mode, it may cause 8032 interrupt routine called but finds no interrupt source to service, or it may cause 8032 to wake up from Idle/Doze/Sleep mode and enters interrupt routine but finds no interrupt source to service. Unless firmware set PDC bit in PDCON before entering the Idle/Doze/Sleep mode to ignore this kind of edge-triggered interrupt.

7.2.4 EC Interface Registers

The EC interface registers are listed below. The base address for INTC is 1100h.

Table 7-7. EC View Register Map, INTC

7	0	Offset
Interrupt Status Register 0 (ISR0)		00h
Interrupt Status Register 1 (ISR1)		01h
Interrupt Status Register 2 (ISR2)		02h
Interrupt Status Register 3 (ISR3)		03h
Interrupt Enable Register 0 (IER0)		04h
Interrupt Enable Register 1 (IER1)		05h
Interrupt Enable Register 2 (IER2)		06h
Interrupt Enable Register 3 (IER3)		07h
Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)		08h
Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)		09h
Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)		0Ah
Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)		0Bh
Interrupt Polarity Register 0 (IPOLR0)		0Ch
Interrupt Polarity Register 1 (IPOLR1)		0Dh
Interrupt Polarity Register 2 (IPOLR2)		0Eh
Interrupt Polarity Register 3 (IPOLR3)		0Fh
Interrupt Vector Register (IVECT)		10h
INT0# status (INT0ST)		11h
Power Fail Register (PFAILR)		12h

7.2.4.1 Interrupt Status Register 0 (ISR0)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 00h

Bit	R/W	Default	Description
7-1	R/WC Or R	-	**Interrupt Status (IS7-1)** It indicates the interrupt input status of INTx. INTST7 to INTST1 correspond to INT7 to INT1 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.
0	R	0b	**Reserved**

7.2.4.2 Interrupt Status Register 1 (ISR1)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS15-8)** It indicates the interrupt input status of INTx. INTST15 to INTST8 correspond to INT15 to INT8, respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending Read 1: Interrupt input to INTC is pending For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.

7.2.4.3 Interrupt Status Register 2 (ISR2)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS23-16)** It indicates the interrupt input status of INTx. INTST23 to INTST16 correspond to INT23 to INT16 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending Read 1: Interrupt input to INTC is pending For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.

7.2.4.4 Interrupt Status Register 3 (ISR3)

This register indicates which maskable interrupts are pending regardless of the state of the corresponding IERx bits.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/WC Or R	-	**Interrupt Status (IS31-24)** It indicates the interrupt input status of INTx. INTST31 to INTST24 correspond to INT31 to INT24 respectively. Each bit is R/WC if the corresponding bit in IELMRx register indicates edge-triggered mode, and is R if it indicates level-triggered mode. For each bit: Read 0: Interrupt input to INTC is not pending. Read 1: Interrupt input to INTC is pending. For each bit: Write 0: No action Write 1: Clear this bit when it is in the edge-triggered mode, and writing 1 is ignored when it is in the level-triggered mode.

7.2.4.5 Interrupt Enable Register 0 (IER0)

Address Offset: 04

Bit	R/W	Default	Description
7-1	R/W	0h	**Interrupt Enable (IE7-0)** Each bit determines the corresponding interrupt channel (INT7-0) is masked or enabled. Note that it has no effect on INT0 0: Masked 1: Enabled
0	-	0b	**Reserved**

7.2.4.6 Interrupt Enable Register 1 (IER1)

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE15-8)** Each bit determines the corresponding interrupt channel (INT15-8) is masked or enabled 0: Masked 1: Enabled.

7.2.4.7 Interrupt Enable Register 2 (IER2)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE23-16)** Each bit determines the corresponding interrupt channel (INT23-16) is masked or enabled. 0: Masked 1: Enabled

7.2.4.8 Interrupt Enable Register 3 (IER3)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Enable (IE31-24)** Each bit determines the corresponding interrupt channel (INT31-24) is masked or enabled. 0: Masked 1: Enabled

7.2.4.9 Interrupt Edge/Level-Triggered Mode Register 0 (IELMR0)

It determines the corresponding interrupt channel is level triggered or edge-triggered.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Edge/Level-Triggered Mode (IELM7-0)** Each bit determines the triggered mode of the corresponding interrupt channel (INT7-0). 0: Level-triggered 1: Edge-triggered

7.2.4.10 Interrupt Edge/Level-Triggered Mode Register 1 (IELMR1)

It determines the corresponding interrupt channel is level triggered or edge-triggered.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Edge/Level-Triggered Mode (IELM15-8)** Each bit determines the triggered mode of the corresponding interrupt channel (INT15-8). 0: Level-triggered 1: Edge-triggered

7.2.4.11 Interrupt Edge/Level-Triggered Mode Register 2 (IELMR2)

It determines the corresponding interrupt channel is level triggered or edge-triggered.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00011101b	**Interrupt Edge/Level-Triggered Mode (IELM23-16)** Each bit determines the triggered mode of the corresponding interrupt channel (INT23-16). 0: level-triggered 1: edge-triggered

7.2.4.12 Interrupt Edge/Level-Triggered Mode Register 3 (IELMR3)

It determines the corresponding interrupt channel is level triggered or edge-triggered.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	01001100b	**Interrupt Edge/Level-Triggered Mode (IELM31-24)** Each bit determines the triggered mode of the corresponding interrupt channel (INT31-24). 0: level-triggered 1: edge-triggered

7.2.4.13 Interrupt Polarity Register 0 (IPOLR0)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL7-0)** Each bit determines the active high/low of the corresponding interrupt channel (INT7-0). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered

7.2.4.14 Interrupt Polarity Register 1 (IPOLR1)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL15-8)** Each bit determines the active high/low of the corresponding interrupt channel (INT15-8). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered

7.2.4.15 Interrupt Polarity Register 2 (IPOLR2)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL23-16)** Each bit determines the active high/low of the corresponding interrupt channel (INT23-16 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered

7.2.4.16 Interrupt Polarity Register 3 (IPOLR3)

For level-triggered interrupt, it determines this interrupt is level-high-triggered or level-low-triggered.
For edge-triggered interrupt, it determines this interrupt is rising-edge-triggered or falling-edge-triggered.

Address Offset: 0Fh

Bit	R/W	Default	Description
7-0	R/W	0h	**Interrupt Polarity (IPOL31-24)** Each bit determines the active high/low of the corresponding interrupt channel (INT31-24). 0: level-high-triggered or rising-edge-triggered 1: level-low-triggered or falling-edge-triggered

7.2.4.17 Interrupt Vector Register (IVCT)

Address Offset: 10h

Bit	R/W	Default	Description
7-6	R	00b	**Reserved**
5-0	R	10000b	**Interrupt Vector (IVECT)** It contains the interrupt number, which is the highest priority, enabled and pending interrupt. The valid values range from 10h to 2Fh. Note that INT1 has the lowest priority and INT31 has the highest priority. If no enabled interrupt is pending, it returns 10h.

7.2.4.18 8032 INT0# Status (INT0ST)

It represents the INT0# input of 8032, which is set when falling edge transition of PWRFAIL# with TREN or TRENL bit in PFAILR is set, and it is clear when reset or reading its content.

Address Offset: 11h

Bit	R/W	Default	Description
7-1	-	00h	**Reserved**
0	R	-	**INT0# Status (INT0)** 0: INT0# of 8032 is high (deasserted) 1: INT0# of 8032 is low (asserted)

7.2.4.19 Power Fail Register (PFAILR)

It provides two methods to trap the PWRFAIL# event.
This register can't be reset by WDT Reset.

Address Offset: 12h

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	0b	**PWRFAIL# Trap Enabled and Locked (TRENL)** Firmware sets this bit to enable PWRFAIL# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of PWRFAIL# is detected. This bit can't be clear by writing 0 to it until reset. 0: no PWRFAIL# Trap 1: PWRFAIL# Trap
1	R	-	**PWRFAIL# Status (PFAILST)** 0: PWRFAIL# is low (asserted) 1: PWRFAIL# is high (deasserted)
0	R/W	0b	**PWRFAIL# Trap Enabled (TREN)** Firmware sets this bit to enable PWRFAIL# trap. When trap is enabled, INT0 bit in INT0ST will be set if the falling edge transition of PWRFAIL# is detected, and TREN will be clear. This bit is ignored when TRENL bit is set. 0: no PWRFAIL# Trap 1: PWRFAIL# Trap

7.2.5 INTC Interrupt Assignments

Table 7-8. INTC Interrupt Assignments

Interrupt	Source	Default Type(Adjustable)	Description	Reference
INT0	Reserved	-	-	-
INT1	External/WUC	High-Level Trig	WKO[20]	Figure 7-17, p172
INT2	Internal	High-Level Trig	KBC Output Buffer Empty Interrupt	Section 6.5.3, p98
INT3	Internal	High-Level Trig	PMC Output Buffer Empty Interrupt	Section 6.6.3.1, p105
INT4	Reserved	-	-	-
INT5	External/WUC	High-Level Trig	WKINTAD (WKINTA or WKINTD)	Figure 7-17, p172
INT6	External/WUC	High-Level Trig	WKO[23]	Figure 7-17, p172
INT7	Internal	High-Level Trig	PWM Interrupt	Section 7.11.4.27, p231
INT8	Internal	High-Level Trig	ADC Interrupt	Section 7.10.3.1, p205
INT9	Internal	High-Level Trig	SMBUS0 Interrupt	Section 7.7.3.2, p185
INT10	Internal	High-Level Trig	SMBUS1 Interrupt	Section 7.7.3.2, p185
INT11	Internal	High-Level Trig	KB Matrix Scan Interrupt	Section 7.4.2, p173
INT12	External/WUC	High-Level Trig	WKO[26]	Figure 7-17, p172
INT13	External/WUC	High-Level Trig	WKINTC	Figure 7-17, p172
INT14	External/WUC	High-Level Trig	WKO[25]	Figure 7-17, p172
INT15	Reserved	-	-	-
INT16	Internal	Rising-Edge Trig	PS/2 Interrupt 3	Section 7.8.2, p198
INT17	External/WUC	High-Level Trig	WKO[24]	Figure 7-17, p172
INT18	Internal	Rising-Edge Trig	PS/2 Interrupt 2	Section 7.8.2, p198
INT19	Internal	Rising-Edge Trig	PS/2 Interrupt 1	Section 7.8.2, p198
INT20	Internal	Rising-Edge Trig	PS/2 Interrupt 0	Section 7.8.2, p198
INT21	External/WUC	High-Level Trig	WKO[22]	Figure 7-17, p172
INT22	Internal	High-Level Trig	SMFI Semaphore Interrupt	Section 6.3.4.8, p80
INT23	Internal	High-Level Trig	SMFI Lock Error Interrupt	Section 6.3.3.7, p71
INT24	Internal	High-Level Trig	KBC Input Buffer Full Interrupt	Section 6.5.3, p98
INT25	Internal	High-Level Trig	PMC Input Buffer Full Interrupt	Section 6.6.3.1, p105
INT26	Internal	Rising-Edge Trig	-	-
INT27	Internal	Rising-Edge Trig	-	-
INT28	External	High-Level Trig	GINT from function 1 of GPD5	Table 5-10, p20
INT29	Internal	High-Level Trig	RTC Alarm 2	Section 6.7.3, p115
INT30	Internal	Rising-Edge Trig	External Timer Interrupt	Section 7.14.3, p243
INT31	External/WUC	High-Level Trig	WKO[21]	Figure 7-17, p172

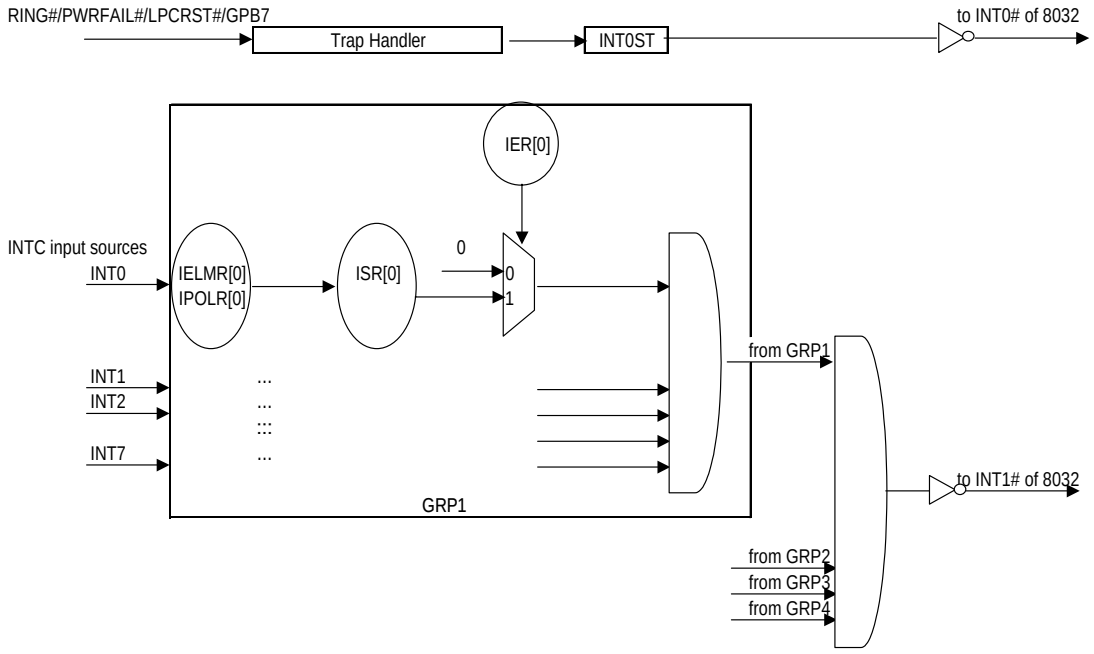

Figure 7-15. INTC Simplified Digram

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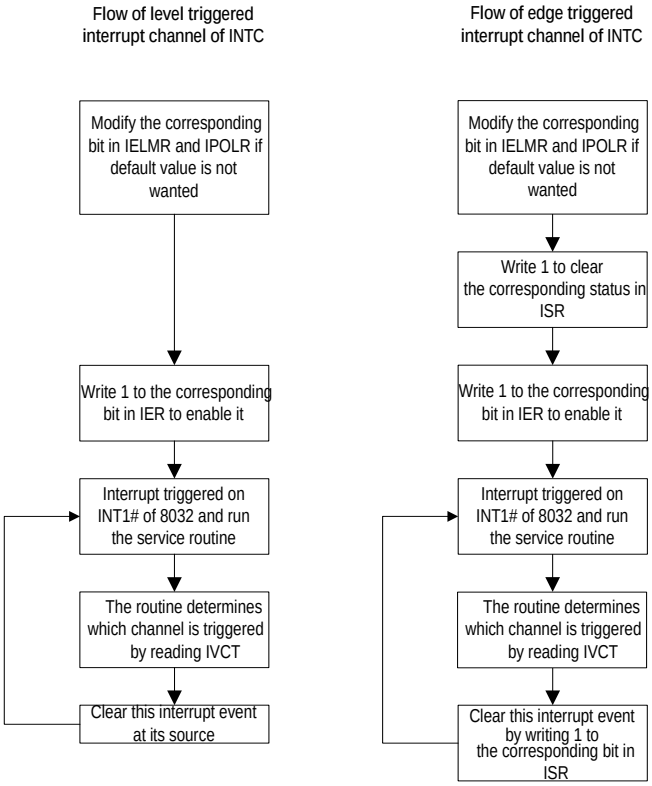

Figure 7-16. Program Flow Chart for INTC

Note: The routine may has its own interrupt priority by reading ISR register.
Note: If this channel source comes from WUC, the corresponding bit of WUESR needed to be cleared, too

7.3 Wake-Up Control (WUC)

7.3.1 Overview

WUC groups internal and external inputs, and asserts wake-up signals to INTC that allows 8032 to exit an Idle/Doze/Sleep mode.

7.3.2 Features

- Supports up to 32 wake-up, internal and external interrupt inputs.
- Supports both the rising-edge and falling-edge triggered mode.
- Input can be connected to INTC directly.

7.3.3 Functional Description

Input sources of WUC are external inputs such as pins about PS/2, GPIO and KB Matrix Scan, or inputs from internal module such as SWUC, LPC and SMBUS that handled external inputs.

Each channel can be selected to be rising or falling edge triggered mode. If one channel is disabled, the input bypasses WUC pending logic and is connected directly to INTC.

7.3.4 EC Interface Registers

The EC interface registers are listed below. The base address for WUC is 1B00h.

Table 7-9. EC View Register Map, WUC

7	0	Offset
Wake-Up Edge Mode Register (WUEMR1)		00h
Wake-Up Edge Mode Register (WUEMR2)		01h
Wake-Up Edge Mode Register (WUEMR3)		02h
Wake-Up Edge Mode Register (WUEMR4)		03h
Wake-Up Edge Sense Register (WUESR1)		04h
Wake-Up Edge Sense Register (WUESR2)		05h
Wake-Up Edge Sense Register (WUESR3)		06h
Wake-Up Edge Sense Register (WUESR4)		07h
Wake-Up Enable Register (WUENR1)		08h
Wake-Up Enable Register (WUENR2)		09h
Wake-Up Enable Register (WUENR3)		0Ah
Wake-Up Enable Register (WUENR4)		0Bh

7.3.4.1 Wake-Up Edge Mode Register (WUEMR1)

This register configures the trigger mode of input signals WU10 to WU17.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM17-10)** 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected.

7.3.4.2 Wake-Up Edge Mode Register (WUEMR2)

This register configures the trigger mode of input signals WU20 to WU27.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM27-20)** 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected.

7.3.4.3 Wake-Up Edge Mode Register (WUEMR3)

This register configures the trigger mode of input signals WU30 to WU37.

Address Offset: 02h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM37-30)** 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected.

7.3.4.4 Wake-Up Edge Mode Register (WUEMR4)

This register configures the trigger mode of input signals WU40 to WU47.

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Edge Mode (WUEM47-40)** 0: Rising-edge triggered is selected. 1: Falling-edge triggered is selected.

7.3.4.5 Wake-Up Edge Sense Register (WUESR1)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU10 to WU17.

Note:
Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES17-10)** For each bit: Read 1: It indicates a trigger condition occurred on the corresponding input. Read 0: otherwise For each bit: Write 1: Clear this bit Write 0: No action

7.3.4.6 Wake-Up Edge Sense Register (WUESR2)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU20 to WU27.

Note:
Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 05h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES27-20)** For each bit: Read 1: It indicates a trigger condition occurred on the corresponding input. Read 0: otherwise For each bit: Write 1: Clear this bit Write 0: No action

7.3.4.7 Wake-Up Edge Sense Register (WUESR3)

This register indicates the occurrence of a selected trigger condition and is associated with input signals WU30 to WU37.

Note:
Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES37-30)** For each bit: Read 1: It indicates a trigger condition occurred on the corresponding input. Read 0: otherwise For each bit: Write 1: Clear this bit Write 0: No action

7.3.4.8 Wake-Up Edge Sense Register (WUESR4)

This register indicates the occurrence of a selected trigger condition occurred and is associated with input signals WU40 to WU47.
Note: Each bit cannot be set by software. Writing a 1 can clear these bits and writing a 0 has no effect.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R/WC	-	**Wake-Up Sense (WUES47-40)** For each bit: Read 1: It indicates a trigger condition occurred on the corresponding input. Read 0: otherwise For each bit: Write 1: Clear this bit Write 0: No action

7.3.4.9 Wake-Up Enable Register (WUENR1)

This register enables a wake-up function of the corresponding input signal WU10 to WU17.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN17-10)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending.

7.3.4.10 Wake-Up Enable Register (WUENR2)

This register enables a wake-up function of the corresponding input signal WU20 to WU27.

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN27-20)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC, and the WUO27-20 from WUI27-20 is processed by WUEMR2 and WUESR2. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal and the WUO27-20 is connected to the INTC directly.

7.3.4.11 Wake-Up Enable Register (WUENR3)

This register enables a wake-up function of the corresponding input signal WU30 to WU37.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN37-30)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled, not pending.

7.3.4.12 Wake-Up Enable Register (WUENR4)

This register enables a wake-up function of the corresponding input signal WU40 to WU47.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-0	R/W	0h	**Wake-Up Enable (WUEN47-40)** 1: A trigger condition on the corresponding input generates a wake-up signal to the power management control of EC. 0: A trigger condition on the corresponding input doesn't assert the wake-up signal; it is canceled but not pending.

7.3.5 WUC Input Assignments

Table 7-10. WUC Input Assignments

WUC Input	Source	Description	Output to INTC	Default Type (Adjustable)
WU10	PS2CLK0	External Source from Pin	WKINTA, to INT5	Rising Edge Trig
WU11	PS2DAT0	External Source from Pin		Rising Edge Trig
WU12	PS2CLK1	External Source from Pin		Rising Edge Trig
WU13	PS2DAT1	External Source from Pin		Rising Edge Trig
WU14	PS2CLK2	External Source from Pin		Rising Edge Trig
WU15	PS2DAT2	External Source from Pin		Rising Edge Trig
WU16	PS2CLK3	External Source from Pin		Rising Edge Trig
WU17	PS2DAT3	External Source from Pin		Rising Edge Trig
WU20	WUI0	External Source from Pin	WKO[20], to INT1	Rising Edge Trig
WU21	WUI1	External Source from Pin	WKO[21], to INT31	Rising Edge Trig
WU22	WUI2	External Source from Pin	WKO[22], to INT21	Rising Edge Trig
WU23	WUI3	External Source from Pin	WKO[23], to INT6	Rising Edge Trig
WU24	WUI4	External Source from Pin	WKO[24], to INT17	Rising Edge Trig
WU25	PWRSW	External Source from Pin	WKO[25], to INT14	Rising Edge Trig
WU26	SWUC Wake Up	From SWUC Module	WKO[26], to INT12	Rising Edge Trig
WU27	Reserved			
WU30	KSI[0]	External Source from Pin	WKINTC, to INT13	Rising Edge Trig
WU31	KSI[1]	External Source from Pin		Rising Edge Trig
WU32	KSI[2]	External Source from Pin		Rising Edge Trig
WU33	KSI[3]	External Source from Pin		Rising Edge Trig
WU34	KSI[4]	External Source from Pin		Rising Edge Trig
WU35	KSI[5]	External Source from Pin		Rising Edge Trig
WU36	KSI[6]	External Source from Pin		Rising Edge Trig
WU37	KSI[7]	External Source from Pin		Rising Edge Trig
WU40	WUI5	External Source from Pin	WKINTD, to INT5	Rising Edge Trig
WU41	Reserved			
WU42	LPC Access	LPC Cycle with Address Recognized See also Section 6.1.6, p41		Rising Edge Trig
WU43	SMBUS Wake Up 0	From SMBUS Module See also Section 7.7.3.1 and 7.7.3.2, p184		Rising Edge Trig
WU44	SMBUS Wake Up 1	From SMBUS Module See also Section 7.7.3.1 and 7.7.3.2, p184		Rising Edge Trig
WU45	WUI6	External Source from Pin		Rising Edge Trig
WU46	WUI7	External Source from Pin		Rising Edge Trig
WU47	Reserved			

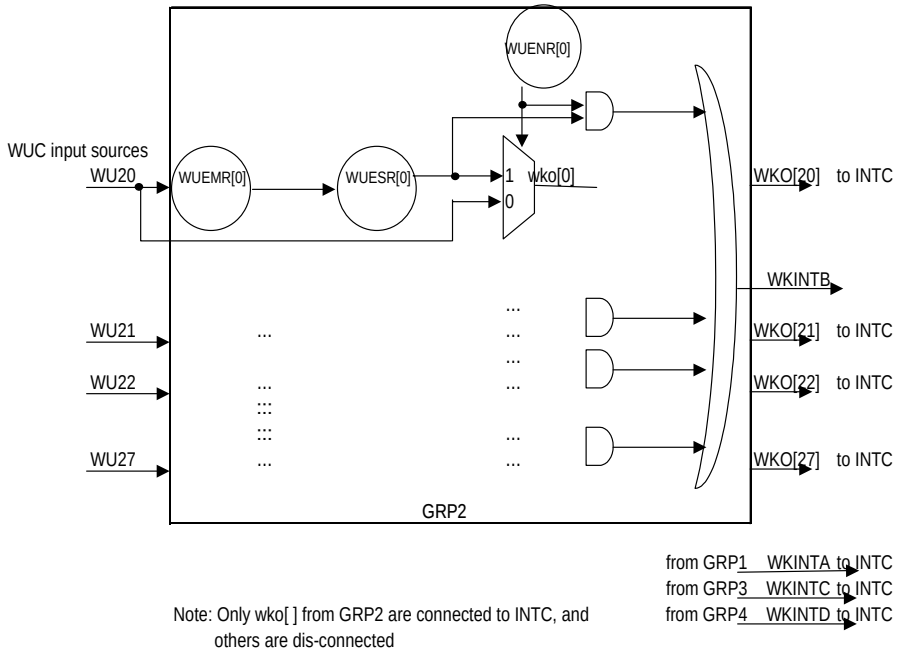

Figure 7-17. WUC Simplified Digram

7.3.6 Programming Guide

If the WUC source is from GPIO port, the firmware should not enable the corresponding channel when this GPIO is not in alternate function.

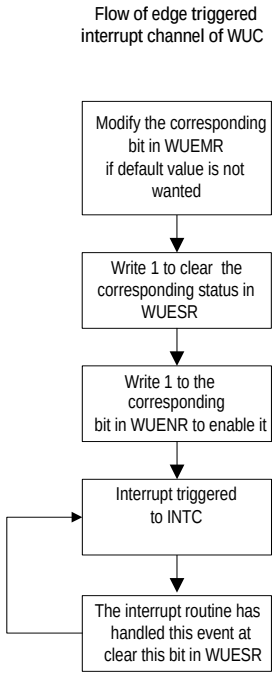

Figure 7-18. Program Flow Chart for WUC

7.4 Keyboard Matrix Scan Controller

7.4.1 Overview

The module provides control for keyboard matrix scan.

7.4.2 Features

- Supports 16 x scan output
- Supports 8 x scan input
- Supports Schmitt trigger input pin
- Supports programmable pull-up on all output/input pins
- Supports one interrupt (connected to INT11 of INTC) for any KSI inputs goes low to wake up the system

7.4.3 EC Interface Registers

The keyboard matrix scan registers are listed below. The base address is 1D00h.

Table 7-11. EC View Register Map, KB Scan

7	0	Offset
Keyboard Scan Out [7:0] (KSOL)		00h
Keyboard Scan Out [15:8] (KSOH)		01h
Keyboard Scan Out Control (KSOCTRL)		02h
Reserved		03h
Keyboard Scan In [7:0] (KSI)		04h
Keyboard Scan In Control (KSICTRL)		05h

7.4.3.1 Keyboard Scan Out Low Byte Data Register (KSOLR)

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	0h	**Keyboard Scan Out Low Data [7:0] (KSOL)** This is the 8-bit keyboard scan output register which controls the KSO[7:0] pins.

7.4.3.2 Keyboard Scan Out High Byte Data Register (KSOHR)

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	0h	**Keyboard Scan Out High Data [7:0] (KSOH)** This is the 8-bit keyboard scan output register which controls the KSO[15:8] pins.

7.4.3.3 Keyboard Scan Out Control Register (KSOCTRLR)

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-3	-	-	**Reserved**
2	R/W	0h	**KSO Pull Up (KSOPU)** Setting 1 enables the internal pull up of the KSO[15:0] pins.
1	-	-	**Reserved**

Bit	R/W	Default	Description
0	R/W	0h	**KSO Open Drain (KSOOD)** Setting 1 enables the open-drain mode of the KSO[15:0] pins. Setting 0 selects the push-pull mode.

7.4.3.4 Keyboard Scan In Data Register (KSIR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R	0h	**Keyboard Scan In High Data [7:0] (KSI)** This is the 8-bit keyboard scan input register which shows the value of the KSI[7:0] pins.

7.4.3.5 Keyboard Scan In Control Register (KSICTRLR)

Address Offset: 05h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	R/W	0h	**Override Hardware Strap PPEN (OVRPPEN)** Override hardware strap SHBM and always treat its result as 0.
2	R/W	0h	**KSI Pull Up (KSIPU)** Setting 1 enables the internal pull up of the KSI[7:0] pins.
1	-	-	**Reserved**
0	-	-	**Reserved**

7.5 General Purpose I/O Port (GPIO)

7.5.1 Overview

The General Purpose I/O Port is composed of 71 independent I/O pins controlled by registers.

7.5.2 Features

- I/O pins individually configured as input, output or alternate function
- Configurable internal pull-up resistors
- Configurable internal pull-down resistors
- Supports Schmitt-Trigger input on all ports

7.5.3 EC Interface Registers

The EC interface registers are listed below. The base address for GPIO is 1600h.

Table 7-12. EC View Register Map, GPIO

7 … 0	Offset
General Control Register (GCR)	00h
Port Data Register (GPDRA)	01h
Port Data Register (GPDRB)	02h
…	…
Port Data Register (GPDRI)	09h
Port Control n Registers (GPCRA0)	10h
Port Control n Registers (GPCRA1)	11h
…	…
Port Control n Registers (GPCRI6)	56h
Output Type Register (GPOTA)	71h
Output Type Register (GPOTB)	72h
…	…
Output Type Register (GPOTF)	79h

7.5.3.1 General Control Register (GCR)

This register individually controls the bus state of each port. The input gating and output floating control signals can be used to reduce power consumption in various system conditions.

Address Offset: 00h

Bit	R/W	Default	Description
7	W	0h	**GPB5 Follow LPCRST# Enable (GFLE)** 1: GPDRB bit 5 will be set immediately if there is a high-to-low transition on WUI4. 0: Otherwise Note that GA20 is function 1 of GPB5, LPCRST# is function 1 of GPD2 and WUI4 is function 2 of GPD2.
6	R/W	0b	**WUI7 Enabled (WUI7EN)** When set, WUI7 is on input from GPE7. It is valid only when GPMD is input or output mode.
5	R/W	0b	**WUI6 Enabled (WUI6EN)** When set, WUI6 is on input from GPE6. It is valid only when GPMD is input or output mode.
4-3	-	00b	**Reserved**
2-1	R/W	10b	**LPC Reset Enabled (LPCRSTEN)** 00: Reserved 01: LPC Reset is enabled on GPB7. 10: LPC Reset is enabled on GPD2. 11: LPC Reset is disabled.
0	R/W	0b	**Input Gating Control (INGC)** 0: Input remains unaffected. 1: Input to port is gated to a fixed value '0'.

7.5.3.2 Port Data Registers A-I (GPDRA-GPDRI)

The Port Data register (GPDR) is an 8-bit register. The pin function is controlled by Port Control Register (GPCRn). When the pin function is set to be a general output pin, the value of the GPDRx bit is directly output to its corresponding pin. When the pin function is set to be a general input pin, the pin level status can be detected by reading the corresponding register bit. Each register contains one group which has eight ports.

Address Offset: 01h-09h

Bit	R/W	Default	Description
7-0	R/W	GPDRB: 20h Otherwise: 00h	**Port Data Register (GPDRn[7:0])** When the pin function is set to be a general output pin, the value of this bit is directly output to its corresponding pin. Reading this register always returns the pin level status.

7.5.3.3 Port Control n Registers (GPCRn, n = A0-I7)

These registers are used to control the functions of each I/O port pin. Each register is responsible for the settings of one pin in the port. Total 71 registers for 71 ports are listed.
If Operation Mode is "Alternate Function", Function 1 and/or Function 2 will be enabled. Refer to Table 7-13. GPIO Alternate Function on page 179 for details. Note that GPEO-GPE4 don't have output mode and the corresponding GPMD cannot be assigned as 01.
Note GPCRI5 can't be reset by Warm Reset.

Address Offset: 10h-17h for GPCRA0-GPCRA7, respectively (Group A)
Address Offset: 18h-1Fh for GPCRB0-GPCRB7, respectively (Group B)
Address Offset: 20h-27h for GPCRC0-GPCRC7, respectively (Group C)
Address Offset: 28h-2Fh for GPCRD0-GPCRD7, respectively (Group D)
Address Offset: 30h-37h for GPCRE0-GPCRE7, respectively (Group E)
Address Offset: 38h-3Fh for GPCRF0-GPCRF7, respectively (Group F)
Address Offset: 40h-47h for GPCRG0-GPCRG7, respectively (Group G)
Address Offset: 48h-4Fh for GPCRH0-GPCRH7, respectively (Group H)
Address Offset: 50h-56h for GPCRI0- GPCRI6, respectively (Group I)

<table>
<tr><th>Bit</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7-6</td><td>R/W</td><td>GPCRB5: 01b
GPCRB6: 00b
Otherwise: 10b</td><td>Port Pin Mode (GPMD[1:0])
These bits are used to select the GPIO operation Mode.
<table>
<tr><th>GPMD[1:0]</th><th>Pin Status</th><th>READ GPDRn</th><th>WRITE GPDRn</th></tr>
<tr><td>00b</td><td>Alternate Function</td><td>Pin Status</td><td>GPDR is writable but it has no effects on the pin status.</td></tr>
<tr><td>01b</td><td>Output</td><td>Pin Status</td><td>The value written to GPDR is output to pin.</td></tr>
<tr><td>10b</td><td>Input</td><td>Pin Status</td><td>GPDR is writable but it has no effects on the pin status.</td></tr>
<tr><td>11b</td><td>Reserved</td><td>-</td><td>-</td></tr>
</table></td></tr>
<tr><td>5-3</td><td>R/W</td><td>-</td><td>Reserved</td></tr>
<tr><td>2</td><td>R/W</td><td>Refer to Table 7-13 on page 179</td><td>Port Pin Pull (GPPU)
This bit is used to pull the port. This bit is always valid regardless of GPMD, input or output. Enable this bit will increase power consumption. Note that if one port is operated in output mode, it should not enable this bit unless its output type is open-drain. For example, clear this bit when FA16/GPG0 is switched to alternative function.

for GPG0-G7:
0: Disable the pull down function.
1: Enable the pull down function.
for others:
0: Disable the pull up function.
1: Enable the pull up function.</td></tr>
<tr><td>1</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>R/W</td><td>0</td><td>Reserved</td></tr>
</table>

7.5.3.4 Output Type Registers A-I (GPOTA-GPOTI)

The Output Type register (GPOT) is an 8-bit register. These registers control the output type of GPIO. Each register contains one group which has eight ports. Note that these bits are valid only when corresponding

GPMD equals to 01 (Output mode).

Address Offset: 71h-79h

Bit	R/W	Default	Description
7-0	R/W	00h	**Output Type Register (GPOTn[7:0])** For each bit: 0: Push-pull output 1: Open-drain output

7.5.4 Alternate Function Selection

The following lists function 1 and function 2 of each GPIO port. Notice that the GA20 function can be implemented by GPO or function 1 which is implemented at KBC module. Function 1 of GPB6 is KBRST# from KBC module through SWUC mode. LPCRST# is recommended to input from GPD2 port.

Table 7-13. GPIO Alternate Function

Group		Function 1	Condition	Function 2	Condition	Output Driving (mA)	Schmitt Trigger	Default Pull	Default Mode
GPIOA	0	PWM0	GPCRA0[7:6]=00			8	Y	Up	GPI
	1	PWM1	GPCRA1[7:6]=00			8	Y	Up	GPI
	2	PWM2	GPCRA2[7:6]=00			8	Y	Up	GPI
	3	PWM3	GPCRA3[7:6]=00			8	Y	Up	GPI
	4	PWM4	GPCRA4[7:6]=00			8	Y	Up	GPI
	5	PWM5	GPCRA5[7:6]=00			8	Y	Up	GPI
	6	PWM6	GPCRA6[7:6]=00			8	Y	Up	GPI
	7	PWM7	GPCRA7[7:6]=00			8	Y	Up	GPI
GPIOB	0	RXD	GPCRB0[7:6]=00			2	Y	Up	GPI
	1	TXD	GPCRB1[7:6]=00			2	Y	Up	GPI
	2					2	Y		GPI
	3	SMCLK0	GPCRB3[7:6]=00			2	Y		GPI
	4	SMDAT0	GPCRB4[7:6]=00			2	Y		GPI
	5	GA20	GPCRB5[7:6]=00			2	Y		GPO
	6	KBRST#	GPCRB6[7:6]=00			2	Y	Up	Func1
	7	RING#	GPCRB7[7:6]=00	PWRFAIL#/ LPCRST#	GPCRB7[7:6]=00 /LPCRSTEN=01	2	Y		GPI
GPIOC	0	CLKOUT	GPCRC0[7:6]=00			2	Y		GPI
	1	SMCLK1	GPCRC1[7:6]=00			2	Y		GPI
	2	SMDAT1	GPCRC2[7:6]=00			2	Y		GPI
	3					2	Y		GPI
	4	TMRI0	GPCRC4[7:6]=00	WUI2	GPCRC4[7:6]=00	2	Y		GPI
	5					2	Y		GPI
	6	TMRI1	GPCRC6[7:6]=00	WUI3	GPCRC6[7:6]=00	2	Y		GPI
	7	CK32KOUT	GPCRC7[7:6]=00			4	Y	Up	GPI
GPIOD	0	RI1#	GPCRD0[7:6]=00	WUI0	GPCRD0[7:6]=00	4	Y	Up	GPI
	1	RI2#	GPCRD1[7:6]=00	WUI1	GPCRD1[7:6]=00	4	Y	Up	GPI
	2	LPCRST#	LPCRSTEN=10	WUI4	GPCRD2[7:6]=00	8	Y	Up	Func1
	3	ECSCI#	GPCRD3[7:6]=00			8	Y	Up	GPI
	4					8	Y	Up	GPI
	5	GINT	GPCRD5[7:6]=00			8	Y	Up	GPI
	6	TACH0	GPCRD6[7:6]=00			2	Y		GPI
	7	TACH1	GPCRD7[7:6]=00			2	Y		GPI

Group		Function 1	Condition	Function 2	Condition	Output Driving (mA)	Schmitt Trigger	Default Pull	Default Mode
GPIOE	0	ADC4	GPCRE0[7:6]=00			N/A			GPI
	1	ADC5	GPCRE1[7:6]=00			N/A			GPI
	2	ADC6	GPCRE2[7:6]=00			N/A			GPI
	3	ADC7	GPCRE3[7:6]=00			N/A			GPI
	4	PWRSW	GPCRE4[7:6]=00			2	Y	Up	GPI
	5			WUI5	GPCRE5[7:6]=00	2	Y		GPI
	6	LPCPD#	GPCRE6[7:6]=00	WUI6	WUI6EN bit GCR register	2	Y		GPI
	7	CLKRUN#	GPCRE7[7:6]=00	WUI7	WUI7EN bit GCR register	6	Y	Up	GPI
GPIOF	0	PS2CLK0	GPCRF0[7:6]=00			8	Y	Up	GPI
	1	PS2DAT0	GPCRF1[7:6]=00			8	Y	Up	GPI
	2	PS2CLK1	GPCRF2[7:6]=00			8	Y	Up	GPI
	3	PS2DAT1	GPCRF3[7:6]=00			8	Y	Up	GPI
	4	PS2CLK2	GPCRF4[7:6]=00			8	Y	Up	GPI
	5	PS2DAT2	GPCRF5[7:6]=00			8	Y	Up	GPI
	6	PS2CLK3	GPCRF6[7:6]=00			8	Y	Up	GPI
	7	PS2DAT3	GPCRF7[7:6]=00			8	Y	Up	GPI
GPIOG	0	FA16	GPCRG0[7:6]=00			4	Y	Down	GPI
	1	FA17	GPCRG1[7:6]=00			4	Y	Down	GPI
	2	FA18	GPCRG2[7:6]=00			4	Y	Down	GPI
	3	FA19	GPCRG3[7:6]=00			4	Y	Down	GPI
	4	FA20	GPCRG4[7:6]=00			4	Y	Down	GPI
	5	FA21	GPCRG5[7:6]=00			4	Y	Down	GPI
	6	LPC80HL	GPCRG6[7:6]=00			4	Y		GPI
	7	LPC80LL	GPCRG7[7:6]=00			4	Y		GPI
GPIOH	0					2	Y		GPI
	1					8	Y	Up	GPI
	2					8	Y	Up	GPI
	3					8	Y		GPI
	4					8	Y		GPI
	5					2	Y		GPI
	6					2	Y		GPI
	7					4	Y		GPI
GPIOI	0					2/12	Y		GPI
	1					2/12	Y		GPI
	2					2/12	Y		GPI
	3					2/12	Y		GPI
	4					2/12	Y		GPI
	5					2/12	Y		GPI
	6					2/12	Y		GPI

Note: Since all GPIO belong to VSTBY power plane, and there are some special considerations below:
(1) If it is output to external VCC derived power plane circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power plane circuit, this external circuit must consider not to float the GPIO input.

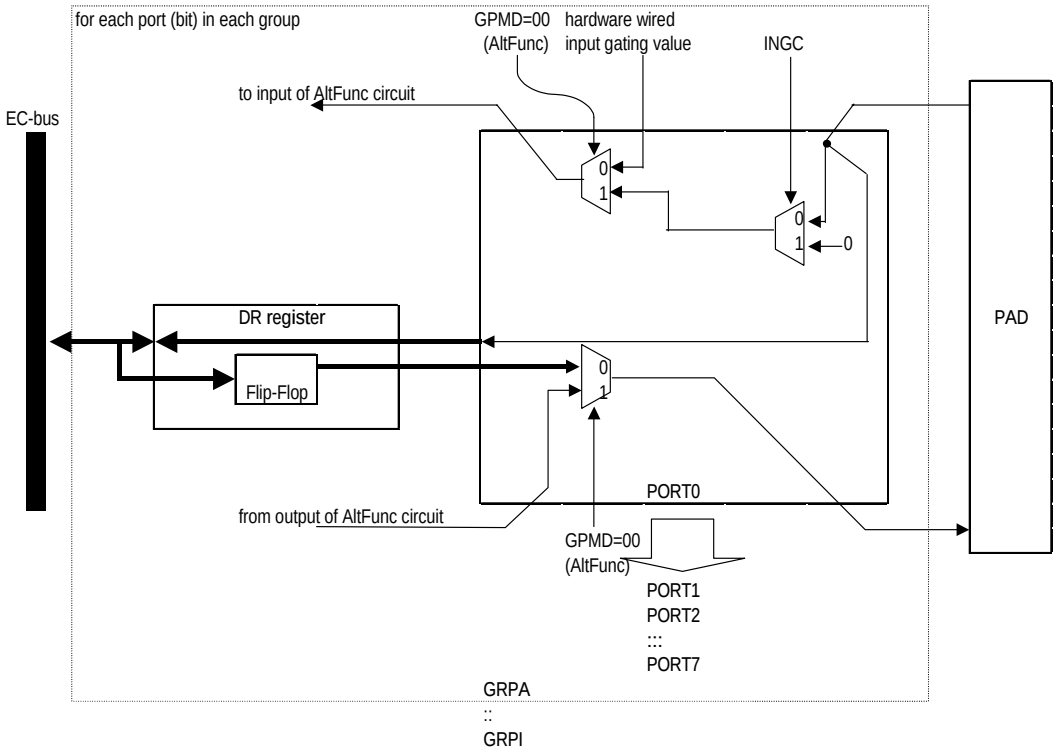

Figure 7-19. GPIO Simplified Diagram

7.5.5 Programming Guide

The firmware should modify LPCRSTEN and enable FA16-FA21 alternative function when it boots up if necessary.

7.6 EC Clock and Power Management Controller (ECPM)

7.6.1 Overview

The EC Clock and Power Management module provide the EC clock control and power management. Default EC Clock is divided into 5 MHz, and should be programmed to 10 MHz.

7.6.2 Features

- Supports programmable EC clock frequency
- Supported by module power-down mode control
- Supports PLL power-down when 8032 enters a Sleep mode

7.6.3 EC Interface Registers

The clock generation and power management registers are listed below. The base address is 1E00h.

Table 7-14. EC View Register Map, ECPM

7	0	Offset
Clock Frequency Select (CFSELR)		00h
Clock Gating Control 1 (CGCTRL1R)		01h
Clock Gating Control 2 (CGCTRL2R)		02h
PLL Control (PLLCTRL)		03h

7.6.3.1 Clock Frequency Select Register (CFSELR)

Address Offset: 00h

Bit	R/W	Default	Description
7-5	-	-	**Reserved**
4	R/W	0b	**Clock Frequency Select (CFSEL)** 0: Clock is divided and it depends on CDNUM (bit 3-0). 1: No clock divided.
3-0	R/W	0h	**Clock Div Number (CDNUM)** Clock frequency is divided by (CDNUM + 1) * 2 and that is 2~32.

7.6.3.2 Clock Gating Control 1 Register (CGCTRL1R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 01h

Bit	R/W	Default	Description
7	R/W	0h	**GPIO Clock Gating (GPIOCG)** 0: Operation 1: Clock to this module is gated
6	R/W	0h	**ETWD Clock Gating (ETWDCG)** 0: Operation 1: Clock to this module is gated
5	R/W	0h	**SMB Clock Gating (SMBCG)** 0: Operation 1: Clock to this module is gated
4	R/W	0h	**Keyboard Scan Clock Gating (KBSCG)** 0: Operation 1: Clock to this module is gated

Bit	R/W	Default	Description
3	R/W	0h	**PS/2 Clock Gating (PS2CG)** 0: Operation 1: Clock to this module is gated
2	R/W	0h	**PWM Clock Gating (PWMCG)** 0: Operation 1: Clock to this module is gated
1	R/W	0h	**DAC Clock Gating (DACCG)** 0: Operation 1: Clock to this module is gated
0	R/W	0h	**ADC Clock Gating (ADCCG)** 0: Operation 1: Clock to this module is gated

7.6.3.3 Clock Gating Control 2 Register (CGCTRL2R)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 02h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	0h	**SWUC Clock Gating (SWUCCG)** 0: Operation 1: Clock to this module is gated
3	R/W	0h	**PMC Clock Gating (PMCCG)** 0: Operation 1: Clock to this module is gated
2	R/W	0h	**KBC Clock Gating (KBCCG)** 0: Operation 1: Clock to this module is gated
1	R/W	0h	**EC2I Clock Gating (EC2ICG)** 0: Operation 1: Clock to this module is gated
0	R/W	0h	**SMFI Clock Gating (SMFICG)** 0: Operation 1: Clock to this module is gated

7.6.3.4 PLL Control (PLLCTRL)

This register is reset by VSTBY Power-Up reset only.

Address Offset: 03h

Bit	R/W	Default	Description
7-1	-	-	**Reserved**
0	R/W	1b	**PLL Power Down Control (PPDC)** 0: PLL will not be power-down by software until VSTBY is not supplied. Setting PD bit in PCON will enter an EC Doze mode. 1: PLL will be power down after setting PD bit in PCON and enter an EC power-down mode.

7.7 SM Bus Interface (SMB)

7.7.1 Overview

The SMBUS interface includes two SMBUS channels. The module can maintain bi-directional communication with the external device through SMCLK0/SMDAT0 (Channel A) and SMCLK1/SMDAT1 (Channel B) pins. It is compatible with ACCESS BUS and I2C BUS.

7.7.2 Features

- Supports SMBUS 2.0.
- Supports two SMBUS channels.
- Performs SMBUS messages with packet error checking (PEC) either enabled or disabled.

7.7.3 Functional Description

This SMBUS Interface provides an SMBUS master and an SMBUS slave for each channel. The master supports eight command protocols of the SMBUS (see System Management Bus Specification): Quick Command, Send Byte, Receive Byte, Write Byte/Word, Read Byte/Word, Process Call, Block Read/Write, and Host Notify. The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.

7.7.3.1 SMBUS Master Interface

When an interrupt to INTC (INT9 and INT10 for channel A and B, respectively) is detected, Software can read the Host Status Register to know the interrupt source. There are 5 interrupt conditions: Byte Done, Failed, Bus Error, Device Error, and Finish.

Quick Command:
In the Quick Command, the Transmit Slave Address Register is sent. Software should force the PEC_EN bit in Host Control Register and I2C_EN bit in Host Control 2 Register to 0 when this command is run.

Send Byte/ Receive Byte:
In the Send Byte command, the Transmit Slave Address and Host Command Registers are sent.
In the Receive Byte command, the Transmit Slave Address Register is sent. The received data is stored in the Host DATA 0 register. Software must force the I2C_EN bit in Host control 2 Register to 0 when this command is run.

Write Byte/ Write Word
In the Write Byte command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Registers are sent.
In the Write Word command, the Transmit Slave Address Register, Host Command Register, Host Data 0, and Host Data 1 Registers are sent.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Read Byte/ Read Word
In the Read Byte command, the Transmit Slave Address Register and Host Command Register are sent. Data is received into the Host Data 0 Register.
In the Read Word command, the Transmit Slave Address Register and Host Command Register are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register.
In these commands, software must force the I2C_EN bit in Host Control 2 Register to 0.

Process Call
In the Process Call command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data1 registers are sent. The returned 2 bytes of data are received into the Host Data 0 Register and Host Data 1 Register. When the I2C_EN bit in Host Control 2 Register is set to 1, the Host Command Register will not be sent.

Note: The Process Call command with I2C_EN bit set and the PEC_EN bit set produce undefined results.

Block Write/ Block Read
In the Block Write command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 (byte count) register are sent. Data is then sent from the Host Block Data Byte register.
In the Block Read commands, the Transmit Slave Address Register, and Host Command Register are sent. The first byte (byte count) received is stored in the Host Data 0 register, and the remaining bytes are stored in the Host Block Data Byte register.
The Byte Done Status bit in the Host Status Register will be set 1 when the master has received a byte (for Block Read commands) or if it has completed transmission of a byte (for Block Write commands).
Note: On the block read command, software shall write 1 to LAST BYTE bit in Host Control Register when the next byte will be the last byte to be received.

I2C Block Read
This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent. Bit 0 of the Transmit Slave Address Register must be 0. The received data is stored in the Host Block Data Byte register.

7.7.3.2 SMBUS Slave Interface

The slave supports the following three types of messages: Byte Write, Byte Read, and Host Notify.
When an interrupt to INTC (INT9 and INT10 for channel A and B respectively) is detected, Software can read the Slave Status Register to know the interrupt source. There are 3 interrupt conditions: Slave Timeout Status, Slave Data Status, and Host Notify Status. The SMBUS interface also supports an interrupt (connected to WU43 and WU44 of WUC for channel A and B respectively) to wake-up the 8032 when the SMBUS detects a start condition in slave interface.

Byte Write
In the byte write command, the first received byte (Slave Address) must match value in Receive Slave Address register. If the first byte is matched, the second byte (Command Data) is received and stored in the Slave Data Register and waiting for the software to read the data. The SMBUS CLOCK line will be held low until the data is read. After the data is read, the third byte (Data) is received and stored in the Slave Data Register. The SMBUS CLOCK line will be held low until the data is read.

Byte Read
In the byte read command, the first received byte (Slave Address) must match value in Receive Slave Address register. If the first byte is matched, the second byte (Command Data) is received and stored in the Slave Data Register and waiting for the software to read the data. The SMBUS CLOCK line will be held low until the data is read. After the Repeated Start and Slave Address cycle, the software shall write the data to the Slave Data Register and this register will be sent during the Data Byte Cycle.

Host Notify Command
In the host notify command, the fist received byte must be 0001000b. The second received byte is stored in the Notify Device Address Register. The next two bytes are stored in the Notify Data Low Byte Register and Notify Data High Byte Register.

7.7.3.3 SMBUS Porting Guide

(1).SMBus Master Interface:

The SMBus controller requires that the various data and command registers be setup for the message to be sent. When the START bit in the Host Control Register is set, the SMBus controller will perform the requested transaction. Any register values needed for computation purposes should be saved prior to issuing of a new command.

The "Timing Registers"(22h~28h) should be programmed before the transaction starts. Besides the 25ms Register, all of the other count numbers are based on 10M clock. For example, write the 28h (40*10M clock=4.0us) into the 4.0us register.

The IT8510 SMBus Interface can perform SMBus messages with either packet error checking (PEC) enabled or disabled (PEC_EN bit =1 or 0 in Host Control Register). The actual PEC calculation and checking is performed in software.
Here is the steps the software shall follow to program the registers for various command.

1. Quick Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Quick Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register).
(3). Start the transaction (Write 41h to the Host Control Register, which will select the "Quick Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
Note: After reading the Status Register, the software must write 1 to clear it.

2. Send Byte Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Send Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to the Transmit Slave Address Register and Host Command Register). Bit 0 of the Transmit Slave Address Register must be 0.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

3. Receive Byte Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Receive Byte Command, the Transmit Slave Address Register is sent (Software shall write data to the Transmit Slave Address Register). Bit 0 of the Transmit Slave Address Register must be 1.
(3). Start the transaction (Write 45h to the Host Control Register, which will select the "Send Byte/Receive Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Receive Byte Command, the received data is stored in the Host Data 0 Register. Software can read this register to get the data.

4. Write Byte Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Write Byte Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 0.
If the Packet Error Checking(PEC) is enabled, software shall write the PEC value to the Packet Error Check Register. And this register will be sent, too.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

5. Write Word Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Write Word Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 0.
If the Packet Error Checking (PEC) is enabled, software shall write the PEC value to the Packet Error Check Register. And this register will be sent, too.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

6. Read Byte Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Read Byte Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 1.
(3). Start the transaction (Write 49h to the Host Control Register, which will select the "Write Byte/Read Byte Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Byte Command, the data received is stored in the Host Data 0 Register. Software can read this register to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

7. Read Word Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Read Word Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). The bit 0 of the Transmit Slave Address Register must be 1.
(3). Start the transaction (Write 4dh to the Host Control Register, which will select the "Write Word/Read Word Command", enable the interrupts, and start the transaction).
(4). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(5). In Read Word Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking(PEC) is enabled, software can read the PEC value from the Packet Error

Check Register.

8. Process Call Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Process Call Command will skip the command code.
(3). In Process Call Command, the Transmit Slave Address Register, Host Command Register (if I2C_EN = 0), Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 0.
(4). Start the transaction (Write 51h to the Host Control Register, which will select the "Process Call Command", enable the interrupts, and start the transaction).
(5). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.
(6). In Process Call Command, the received data is stored in the Host Data 0 Register and Host Data 1 Register. Software can read these registers to get the data.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

9. Block Write Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1).
(2). Set the I2C_EN bit (in Host Control Register 2) to 1 or force it to 0. When the I2C_EN bit is set, the SMBus logic will instead be set to communicate with I2C device. The Block Write Command will skip sending the byte count (Host Data 0 Register).
(3). In Block Write Command, the Transmit Slave Address Register, Host Command Register, and Host Data 0 Register (byte count, if I2C_EN = 0), are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 0. The data is then sent from the Host Block Data Byte Register (Software shall write data to this register).
(4). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(5). When the data in Host Block Data Byte Register was sent, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(6). Software writes the data to the Host Block Data Byte Register, then the data is sent from this register by SMBus logic.
(7). Repeat step (5) and (6) for the other data byte until all of the data were sent.
If the Packet Error Checking(PEC) is enabled, software shall write the PEC value to the Packet Error Check Register and this register will be sent, too.
(8). When the data transmission was completed, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt.

Note: The I2C_EN bit and PEC_EN bit can't be set high at the same time. It will produce the undefined results.

10. Block Read Command

(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In Block Read Command, the Transmit Slave Address Register and Host Command Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 1.
(3). Start the transaction (Write 55h to the Host Control Register, which will select the "Block Read/Block Write Command", enable the interrupts, and start the transaction).
(4). When the byte count and the first byte data were received, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software read the data from the Host Data 0 Register to get the byte count, and read the data from the

Host Block Data Byte Register to get the first data byte.
(6). When the next data was received, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(7). Software read the data from the Host Block Data Byte Register to get the data.
(8). Repeat step (6) and (7) until the last byte.
(9). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(10). Get an interrupt and receive the last byte.
If the Packet Error Checking (PEC) is enabled, software can read the PEC value from the Packet Error Check Register.

11. I2C Block Read Command

This command allows the SMBus logic to perform block reads to I2C devices in a 10-bit addressing mode.
(1). Enable the SMBus Host Controller (SMBUS Host Enable bit in Host Control Register 2 is set to 1). I2C_EN bit must be 0 in this command.
(2). In I2C Block Read Command, the Transmit Slave Address Register, Host Command Register, Host Data 0 Register, and Host Data 1 Register are sent (Software shall write data to these registers). Bit 0 of the Transmit Slave Address Register must be 0.
(3). Start the transaction (Write 59h to the Host Control Register, which will select the "I2C Block Read Command", enable the interrupts, and start the transaction).
(4). When the data was received, an interrupt was generated. Software can read the Host Status Register to know the source of the interrupt (Byte Done Status is 1).
(5). Software can read the data from the Host Block Data Byte Register to get the data.
(6). Repeat step (4) and (5) until the last byte.
(7). Set the LAST BYTE bit in the Host Control Register to indicate that the next byte will be the last byte to be received.
(8). Get an interrupt and receive the last byte.

(2). SMBus Slave Interface:

The slave supports three types of messages: Byte Write, Byte Read, and Host Notify.
Here are the steps the software shall follow to program the registers for various command.

1. Byte Write

(1). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(2). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to response the data transmission from the external SMBus device.
(3). When an interrupt was generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(4). Software can read the data from the Slave Data Register. (This data byte is the command code.)
(5). When the next interrupt was generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Write Command).
(6). Software can read the data from the Slave Data Register. (This data is the Data Byte in SMBUS Protocol)

2. Byte Read

(1). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(2). Write a slave address to Receive Slave Address Register. Now the SMBus logic is ready to response the data transmission from the external SMBus device.
(3). When an interrupt was generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 02h for Byte Read Command).
(4). Software can read the data from the Slave Data Register. (This data byte is the command code)
(5). When the next interrupt was generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 0Ah for Byte Read Command).

(6). Software shall write the data to the Slave Data Register. (This data will be sent to the external device)

3. Host Notify

(1). Enable the interrupts (Write 03h to Slave Interrupt Control Register).
(2). When an interrupt was generated, the software can read the Slave Status Register to know the source of the interrupt (It shall be 01h for Host Notify Command).
(3). Software can read the data from the Notify Device address Register, Notify Data Low Byte Register, and Notify Data High Byte Register.

7.7.4 EC Interface Registers

The SMBUS I/O registers are listed below. The base address for SMBUS is 1C00h.
A and B are for channel A and B respectively.

Table 7-15. EC View Register Map, SMBUS

7	0	Offset
Host Status (HOSTA)(A,B)		00h,11h
Host Control (HOCTL)(A,B)		01h,12h
Host Command (HOCMD)(A,B)		02h,13h
Transmit Slave Address (TRASLA)(A,B)		03h,14h
Host Data 0 (D0REG)(A,B)		04h,15h
Host Data 1 (D1REG)(A,B)		05h,16h
Host Block Data Byte (HOBDB)(A,B)		06h,17h
Packet Error Check (PECERC)(A,B)		07h,18h
Receive Slave Address (RESLADR)(A,B)		08h,19h
Slave Data (SLDA)(A,B)		09h,1Ah
SMBUS Pin Control (SMBPCTL)(A,B)		0Ah,1Bh
Slave Status (SLSTA)(A,B)		0Bh,1Ch
Slave Interrupt Control (SICR)(A,B)		0Ch,1Dh
Notify Device Address (NDADR)(A,B)		0Dh,1Eh
Notify Data Low Byte (NDLB)(A,B)		0Eh,1Fh
Notify Data High Byte (NDHB)(A,B)		0Fh,20h
Host Control2 (HOCTL2)(A,B)		10h,21h
4.7 μs Register (4P7USREG)		22h
4.0 μs Register (4P0USREG)		23h
300 ns Register (300NSREG)		24h
250 ns Register (250NSREG)		25h
25 ms Register (25MSREG)		26h
45.3 μs Low Register (45P3USLREG)		27h
45.3 μs High Register (45P3USHREG)		28h

7.7.4.1 Host Status Register (HOSTA)

All status bits are set by hardware and cleared by writing a one to the particular bit position by the software. Software can read this register to know the source of the interrupt (Master Interface).

Address Offset: Channel A: 00h
Channel B: 11h

Bit	R/W	Default	Description
7	R/WC	00h	**Byte Done Status (BDS)** This bit will be set 1 when the host controller has received a byte (for Block Read commands) or if it has completed the transmission of a byte (for Block Write commands).
6-5	-	00h	**Reserved**
4	R/WC	00h	**Failed (FAIL)** 0: This bit is cleared by writing a 1 to the bit position. 1:This bit is set when the KILL is set to.
3	R/WC	00h	**Bus Error (BSER)** 0: This bit is cleared by writing a 1 to the bit position. 1: The source of the interrupt is that the SMBUS has lost arbitration.
2	R/WC	00h	**Device Error (DVER)** 0: This bit is cleared by writing a 1 to this bit position. 1: This bit is set in one of the following conditions: (1)Illegal Command Field. (2)25ms Time-out Error. (3)Not response ACK.
1	R/WC	00h	**Finish Interrupt (FINTR)** This bit will be set by termination of a command. 0: This bit is cleared by writing 1 to this position. 1: The source of the interrupt was the stop condition detected.
0	R	00h	**Host Busy (HOBY)** 0: This bit is cleared when the current transaction is completed. 1: This bit is set while the command is in operation.

7.7.4.2 Host Control Register (HOCTL)

Address Offset: Channel A: 01h
Channel B: 12h

Bit	R/W	Default	Description
7	R/W	00h	**PEC Enable (PEC_EN)** 0: The transaction without the PEC (Packet Error Checking) phase appended 1: The transaction with the PEC phase appended.
6	W	00h	**Start (SRT)** 0: This bit will always return 0 on reads. 1: When this bit is set, the SMBUS host controller will perform the requested transaction.
5	W	00h	**Last Byte (LABY)** This bit is used for Block Read command. 0: This bit will always return 0 on reads. 1: Software shall write 1 to this bit when the next byte will be the last byte to be received for the block read command.

Bit	R/W	Default	Description
4-2	R/W	00h	**SMBUS Command (SMCD)** These bits indicate which command will be performed. Bit 0 of the Transmit Slave Address Register determines if this is a read or write command. 000:Quick Command 001:Send Byte/ Receive Byte 010:Write Byte/ Read Byte 011:Write Word/ Read Word 100:Process Call 101:Block Read/ Block Write 110:I2C Block Read 111:Reserved
1	R/W	00h	**Kill (KILL)** 0: Normal SMBUS Host controller functionality. 1: When this bit is set, kill the current host transaction. This bit, once set, must be cleared by software to allow the SMBUS Host controller to function normally.
0	R/W	00h	**Host Interrupt Enable (INTREN)** 0: Disable. 1: Enable the generation of an interrupt for the master interface

7.7.4.3 Host Command Register (HOCMD)

Address Offset: Channel A: 02h
Channel B: 13h

Bit	R/W	Default	Description
7-0	R/W	00h	**Host Command Register (HCREG)** These bits are transmitted in the command field of the SMBUS protocol.

7.7.4.4 Transmit Slave Address Register (TRASLA)

Address Offset: Channel A: 03h
Channel B: 14h

Bit	R/W	Default	Description
7-1	R/W	00h	**Address (ADR)** Address of the targeted slave.
0	R/W	00h	**Direction (DIR)** Direction of the host transfer. 0: Write 1: Read

7.7.4.5 Data 0 Register (D0REG)

Address Offset: Channel A: 04h
Channel B: 15h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data 0 (D0)** These bits contain the data sent in the DATA0 field of the SMBUS protocol. For block write commands, this register reflects the number (from 1 to 32) of bytes to transfer.

7.7.4.6 Data 1 Register (D1REG)

Address Offset: Channel A: 05h
Channel B: 16h

Bit	R/W	Default	Description
7-0	R/W	00h	**Data 1 (D1)** These bits contain the data sent in the DATA1 field of the SMBUS protocol.

7.7.4.7 Host Block Data Byte Register (HOBDB)

Address Offset: Channel A: 06h
Channel B: 17h

Bit	R/W	Default	Description
7-0	R/W	00h	**Block Data (BLDT)** For a block write command, data is sent from this register. On block read command, the received data is stored in this register.

7.7.4.8 Packet Error Check Register (PECERC)

Address Offset: Channel A: 07h
Channel B: 18h

Bit	R/W	Default	Description
7-0	R/W	00h	**PEC Data (PECD)** These bits are written with the 8-bit CRC value that is used as the SMBUS PEC data prior to a write transaction. For read transactions, the PEC data is loaded from the SMBUS into this register and is then read by software.

7.7.4.9 Receive Slave Address Register (RESLADR)

Address Offset: Channel A: 08h
Channel B: 19h

Bit	R/W	Default	Description
7	-	00h	**Reserved**
6-0	R/W	00h	**Slave Address (SADR)** These bits are the slave address decoded for read and write cycles.

7.7.4.10 Slave Data Register (SLDA)

Address Offset: Channel A: 09h
Channel B: 1Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Slave Data Byte0 (SDB0)** This register stored the data received from the external master.

7.7.4.11 SMBUS Pin Control Register (SMBPCTL)

Address Offset: Channel A: 0Ah
Channel B: 1Bh

Bit	R/W	Default	Description
7-3	-	00h	**Reserved**
2	R/W	1b	**SMCLK Control (SMBC)** 0: SMCLK0/1 pin will be driven low, independent of what the other SMB logic will be. 1: The SMCLK0/1 pin will not be driven low. The other SMBUS logic controls this pin.
1	R	-	**SMDAT Current State (SMBDCS)** This bit returns the value of the SMDAT0/1 pin. 0: Low 1: High
0	R	-	**SMCLK Current State (SMBCS)** This bit returns the value of the SMCLK0/1 pin. 0: Low 1: High

7.7.4.12 Slave Status Register (SLSTA)

Software can read this register to know the source of the interrupt (Slave Interface).

Address Offset: Channel A: 0Bh
Channel B: 1Ch

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
3	R	00h	**Read Cycle Status (RCS)** Direction of the slave transfer. 0: Write. 1: Read.
2	R/WC	00h	**Slave Timeout Status (STS)** 0: Cleared by writing a 1 to this bit. 1: Timeout status occurs.
1	R/WC	00h	**Slave Data Status (SDS)** 0: Cleared by writing a 1 to this bit. 1: Slave Data Register is waiting for read or write. When this bit is set and the Read Cycle Status (RCS) bit is low, the software shall read the data from the Slave Data Register. When this bit is set and the Read Cycle Status (RCS) bit is high, the software shall write the data to the Slave Data Register.
0	R/WC	00h	**Host Notify Status (HONOST)** This bit will be set to a 1 when a Host Notify Command has been completely received. Software can read this bit to determine that the source of the interrupt was the reception of the Host Notify Command.

7.7.4.13 Slave Interrupt Control Register (SICR)

Address Offset: Channel A: 0Ch
Channel B: 1Dh

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	00h	**Slave Interrupt Enable (SITEN)** 0: Disable. 1: Enable the generation of an interrupt for the slave interface.
0	R/W	00h	**Host Notify Interrupt Enable (HONOIN)** 0: Disable. 1: Enable the generation of interrupt when Host Notify Status is set and it does not affect the setting of the Host Notify Status bit.

7.7.4.14 Notify Device Address Register (NDADR)

Address Offset: Channel A: 0Dh
Channel B: 1Eh

Bit	R/W	Default	Description
7-1	R	00h	**Device Address (DVADR)** These bits contain the 7-bit device address received during the Host Notify protocol of the SMBUS 2.0 Specification.
0	-	00h	**Reserved**

7.7.4.15 Notify Data Low Byte Register (NDLB)

Address Offset: Channel A: 0Eh
Channel B: 1Fh

Bit	R/W	Default	Description
7-0	R	00h	**Data Low Byte (DALB)** These bits contain the first (low) byte of data received during the Host Notify protocol of the SMBUS 2.0 Specification.

7.7.4.16 Notify Data High Byte Register (NDHB)

Address Offset: Channel A: 0Fh
Channel B: 20h

Bit	R/W	Default	Description
7-0	R	00h	**Data High Byte (DAHB)** These bits contain the second (high) byte of data received during the Host Notify protocol of the SMBUS 2.0 Specification.

7.7.4.17 Host Control Register 2 (HOCTL2)

Address Offset: Channel A: 10h
Channel B: 21h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**
1	R/W	00h	**I2C Enable (I2C_EN)** 0: SM BUS behavior. 1: Enable to communicate with I2C device. When this bit is set, the SMBUS logic will instead be set to communicate with I2C devices. This forces the following changes: (1) The Process Call command will skip the Command code. (2) The Block Write command will skip sending the Byte Count.
0	R/W	00h	**SMBUS Host Enable (SMHEN)** 0: Disable the SMBUS Host Controller. (Operate as slave interface) 1: The SMB Host interface is enabled to execute commands.

7.7.4.18 4.7 μs Register (4P7USREG)

The following registers (22h-28h) define the SMCLK0/1 and SMDAT0/1 timing.

Address Offset: 22h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.7 μs Register (4P7US)** This field defines the SMCLK0/1 low period. This byte is the count number of the counter for 4.7 μs. The 4.7 μs is T_CLK $_{10M}$* count number.

7.7.4.19 4.0 μs Register (4P0USREG)

Address Offset: 23h

Bit	R/W	Default	Description
7-0	R/W	00h	**4.0 μs Register (4P0US)** This field defines the SMCLK0/1 high period (minimal). This byte is the count number of the counter for 4.0 μs. The 4.0 μs is T_CLK $_{10M}$* count number.

7.7.4.20 300 ns Register (300NSREG)

Address Offset: 24h

Bit	R/W	Default	Description
7-0	R/W	00h	**300ns Register (300NS)** This field defines the SMDAT0/1 hold time. This byte is the count number of the counter for 300 ns. The 300 ns is T_CLK $_{10M}$* count number

7.7.4.21 250 ns Register (250NSREG)

Address Offset: 25h

Bit	R/W	Default	Description
7-0	R/W	00h	**250ns Register (250NS)** This field defines the SMDAT0/1 setup time. This byte is the count number of the counter for 250 ns. The 250 ns is T_CLK $_{10M}$* count number.

7.7.4.22 25 ms Register (25MSREG)

Address Offset: 26h

Bit	R/W	Default	Description
7-0	R/W	00h	**25 ms Register (25MS)** This field defines the SMCLK0/1 clock low timeout. This byte is the count number of the counter for 25 ms. The 25 ms is T_CLK $_{1k}$* count number.

7.7.4.23 45.3 μs Low Register (45P3USLREG)

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs Low Register (45P3USLOW)** This 45.3 μs Low Register, 45.3 μs High Register and 4.7us Register define the SMCLK0/1 high periodic (maximal). (45.3μs + 4.7μs=50μs) This byte is the count number bits [7:0] of the counter for 45.3 μs. The 45.3 μs is T_CLK $_{10M}$* count number [15:0].

7.7.4.24 45.3 μs High Register (45P3USHREG)

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00h	**45.3 μs High Register (45P3USHGH)** This 45.3 μs Low Register, 45.3 μs High Register and 4.7us Register define the SMCLK0/1 high periodic (maximal). (45.3 μs + 4.7μs=50μs). This byte is the count number bits [15:8] of the counter for 45.3 μs. The 45.3 μs is T_CLK $_{10M}$* count number [15:0].

7.8 PS/2 Interface

7.8.1 Overview

The PS/2 device uses a two-wire bidirectional interface for data transmission. The device consists of four identical channels. Each of the four channels provides two signals (CLK and DATA line) to communicate with the auxiliary device. The PS/2 interface also connects the CLK line and DATA line to the WUC (WU10-WU17) to wake-up the 8032 when these lines are toggled.

CLK line and DATA line are the same as PS2CLKn and PS2DATn (n=0,1,2 or 3) pins. Refer to Table 5-5 on page 18 for the details.

7.8.2 Features

- Supports four PS/2 channels.
- Supports hardware/software mode selection.
- Three interrupt features are available: Start Interrupt, Transaction Done Interrupt, and Software Mode Interrupt (INT16, INT18, INT19 and INT20).

7.8.3 Functional Description

The PS/2 Interface has two operation methods: Hardware mode and software mode. When the hardware mode is enabled, the PS/2 interface can perform automatic reception or transmission depending on the TRMS bit in the PSCTL register. When the hardware mode is disabled (software mode is enabled), the PS/2 CLK line and DATA line are controlled by the firmware via the CCLK bit and CDAT bit in the PSCTL register. The following sections will describe how to use the PS/2 interface.

7.8.3.1 Hardware Mode Selected

Receive Mode:
Here are the steps the host shall follow to receive data from a PS/2 device.

1. Enable the hardware mode, select the receive mode, and release the CLK line and DATA line (Write 07h to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register must be set to 1 because when the data transmission was completed, the data in PS/2 Data Register needs to be read.)

After these steps, the PS/2 interface is ready to receive data. When the data transmission was completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register and the received data can be read from the PS/2 Data Register. The PS/2 CLK line will be held low until the PS/2 Data Register is read.

Transmit Mode:
Here are the steps the host shall follow to send data to a PS/2 device.
1. Enable the hardware mode, select the transmit mode, and pull the CLK line low and DATA line high (Write 0Dh to the PS/2 Control Register).
2. Enable the interrupts. (TDIE bit in PS/2 Interrupt Control Register must be set to 1 because when the data transmission was completed, the data in PS/2 Status Register needs to be read.)
3. Write the data to be transmitted to the PS/2 Data Register.
4. Pull the DATA line low (Write 0Ch to the PS/2 Control Register).
5. Pull the CLK line high (Write 0Eh to the PS/2 Control Register).

After these steps, the PS/2 interface is ready to transmit data. When the data transmission was completed, an interrupt signal is set high (Transaction Done interrupt). The status (Transaction Done Status) can be read from PS/2 Status Register. The CLK line will be held low until the PS/2 Status Register is read.

Input Signal Debounce
This PS/2 Interface performs a debounce operation on the CLK input signal before determining its logical value. When this operation is enabled (DCEN bit in the PS/2 Control Register is set to 1), the CLK input signal must be stable for at least 4 clock cycles.

7.8.3.2 Software Mode Selected

Software Control PS/2 CLK line and DATA line
When the Software Mode is selected (PSHE=0 in PS/2 Control Register), the software can control the PS/2 CLK line and DATA line. The CCLK bit and CDAT bit in the PS/2 Control Register control the CLK line and DATA line. When one of these bits is cleared, the relevant pin is held low. When one of these bits is set, the relevant pin is pulled high.

Software Control the Interrupt
When the PS/2 Hardware Enable bit is cleared (PSHE=0 in PS/2 Control Register) and the Software Mode Interrupt Enable bit is set (SMIE=1 in PS/2 Interrupt Control Register), the software can control the PS/2 interrupt. The interrupt is set high when the CCLK bit in PS/2 Control Register is set high. If such an interrupt is not desired, clear the Software Mode Interrupt Enable bit (SMIE=0 in PS/2 Interrupt Control Register).

7.8.4 EC Interface Registers

The PS/2 interface registers are listed below. The base address for PS/2 is 1700h.

Table 7-16. EC View Register Map, PS/2

7	0	Offset
PS/2 Control Register 1 (PSCTL1)		00h
PS/2 Control Register 2 (PSCTL2)		01h
PS/2 Control Register 3 (PSCTL3)		02h
PS/2 Control Register 4 (PSCTL4)		03h
PS/2 Interrupt Control Register 1 (PSINT1)		04h
PS/2 Interrupt Control Register 2 (PSINT2)		05h
PS/2 Interrupt Control Register 3 (PSINT3)		06h
PS/2 Interrupt Control Register 4 (PSINT4)		07h
PS/2 Status Register 1 (PSSTS1)		08h
PS/2 Status Register 2 (PSSTS2)		09h
PS/2 Status Register 3 (PSSTS3)		0Ah
PS/2 Status Register 4 (PSSTS4)		0Bh
PS/2 Data Register 1 (PSDAT1)		0Ch
PS/2 Data Register 2 (PSDAT2)		0Dh
PS/2 Data Register 3 (PSDAT3)		0Eh
PS/2 Data Register 4 (PSDAT4)		0Fh

7.8.4.1 PS/2 Control Register 1-4 (PSCTL1-4)

This register controls the operation of the PS/2 interface. PS/2 Control Register 1-4 are for channel 1-4 respectively.

Address Offset: 00h~03h

Bit	R/W	Default	Description
7-5	-	000b	**Reserved**
4	R/W	0b	**Debounce Circuit Enable (DCEN)** 0: The debounce circuit is disabled. 1: The debounce circuit is enabled.
3	R/W	0b	**Transmit / Receive Mode Selection (TRMS)** 0: Receive mode is selected. 1: Transmit mode is selected.
2	R/W	0b	**PS/2 Hardware Enable (PSHE)** When this bit is set to 1, the PS/2 channel can perform automatic reception or transmission. When this bit is 0, the channel's CLK and DATA lines are controlled by the CCLK and CDAT bits in this register. 0: PS/2 hardware mode is disabled (Software mode is enabled). 1: PS/2 hardware mode is enabled.
1	R/W	0b	**Control CLK Line (CCLK)** This bit can control the CLK line. 0: The CLK line is held low. 1: The CLK line is pulled high.
0	R/W	1b	**Control DATA Line (CDAT)** This bit can control the DATA line. 0: The DATA line is held low. 1: The DATA line is pulled high.

7.8.4.2 PS/2 Interrupt Control Register 1-4 (PSINT1-4)

This register enables or disables various interrupts sources. PS/2 Interrupt Control Register 1-4 are for channel 1-4 respectively.

Address Offset: 04h~07h

Bit	R/W	Default	Description
7-3	-	00000b	**Reserved**
2	R/W	0b	**Transaction Done Interrupt Enable (TDIE)** Enable or disable the interrupt generation when the Transaction Done status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
1	R/W	0b	**Start Interrupt Enable (SIE)** Enable or disable the interrupt generation when the Start status occurs. 0: Disable the interrupt. 1: Enable the interrupt.
0	R/W	0b	**Software Mode Interrupt Enable (SMIE)** Enable or disable the interrupt generation when the PS/2 hardware is disabled. The CCLK bit in PSCTL register can control the interrupt output when this bit is set to 1 and PS/2 hardware is disabled. 0: Disable the interrupt. 1: Enable the interrupt.

7.8.4.3 PS/2 Status Register 1-4 (PSSTS1-4)

This register contains the status information on the data transfer on the PS/2. Status Register 1-4 are for channel 1-4 respectively.

Address Offset: 08h~0Bh

Bit	R/W	Default	Description
7-6	-	00b	**Reserved**
5	R	0b	**Frame Error (FER)** This bit is 1 when the stop bit in a received frame was detected low.
4	R	0b	**Parity Error (PER)** This bit is 1 when a parity error condition occurs.
3	R	0b	**Transaction Done Status (TDS)** This bit is 1 when a PS/2 data transfer was done.
2	R	0b	**Start Status (SS)** This bit is 1 when a start bit was detected.
1	R	-	**CLK Line Status (CLS)** Reading this bit returns the current status of the PS/2 CLK line.
0	R	-	**DATA Line Status (DLS)** Reading this bit returns the current status of the PS/2 DATA line.

7.8.4.4 PS/2 Data Register 1-4 (PSDAT1-4)

In receive mode, this register holds the data received from the PS/2 device. In transmit mode, the data in this register is transmitted to the PS/2 device. Data Register 1-4 are for channel 1-4 respectively.

Address Offset: 0Ch~0Fh

Bit	R/W	Default	Description
7-0	R/W	00h	**Data (DAT)** Holds the data received from the PS/2 device in the receive mode or the data which will be transmitted in the transmit mode.

7.9 Digital To Analog Converter (DAC)

7.9.1 Overview

The DAC interface is used as a communication interface between the embedded controller and DAC.

7.9.2 Feature

- Supports 4-channel D/A converter
- 8-bit resolution
- Independent enable signals for each channel
- Power-down function

7.9.3 Functional Description

The DAC interface has four channels. Each channel generates an output in the range of 0V to AVCC with eight-bit resolution. When a DAC channel is enabled, its output is defined by the value written to its DACDAT register. DACDAT 0-3 control channel 0-3 respectively. The 0V output is obtained for a value of 00h in the DACDAT register. The AVCC output is obtained for a value of FFh in the DACDAT register. In power-down mode (POWDN=1 in DACCTRL Register), the DAC output is 0V.

DAC analog circuit has less power consumption if it is power-down. POWDN bit in DACCTRL register controls this and it's cleared when EC Domain Reset.
The firmware should clear POWDN bit before entering Idle/Doze/Sleep mode.

7.9.4 EC Interface Registers

The DAC interface registers are listed below. The base address for DAC is 1A00h.

Table 7-17. EC View Register Map, DAC

7	0	Offset
DAC Control (DACCTRL)		00h
DAC Data Channel 0 (DACDAT0)		01h
DAC Data Channel 1 (DACDAT1)		02h
DAC Data Channel 2 (DACDAT2)		03h
DAC Data Channel 3 (DACDAT3)		04h

7.9.4.1 DAC Control Register (DACCTRL)

This register controls the operation of the DAC module.

Address Offset: 0h

Bit	R/W	Default	Description
7-5	-	0h	**Reserved**
4	R/W	1b	**Power Down (POWDN)** 0: The DAC is not power-down. 1: The DAC is power-down.
3	R/W	0h	**DAC Channel 3 Enable (DACEN3)** This bit is used to enable the DAC channel 3. 0: Disable 1: Enable
2	R/W	0h	**DAC Channel 2 Enable (DACEN2)** This bit is used to enable the DAC channel 2. 0: Disable 1: Enable

Bit	R/W	Default	Description
1	R/W	0h	**DAC Channel 1 Enable (DACEN1)** This bit is used to enable the DAC channel 1. 0: Disable 1: Enable
0	R/W	0h	**DAC Channel 0 Enable (DACEN0)** This bit is used to enable the DAC channel 0. 0: Disable 1: Enable

7.9.4.2 DAC Data Channel 0~3 Register (DACDAT0~3)

The data in these registers will be loaded into channel 0~3.

Address Offset: Channel 0: 01h
Channel 1: 02h
Channel 2: 03h
Channel 3: 04h

Bit	R/W	Default	Description
7-0	R/W	-	**DAC Data Register (DACDAT)** 8 bit data will be loaded to the DAC for D/A operation.

7.10 Analog to Digital Converter (ADC)

7.10.1 Overview

The ADC(analog to digital converter) provides an accurate method for measuring slow changing voltages. The module can measure the channel up to fourteen-voltage with 10-bit resolution.

7.10.2 Features

- Supports 10-bit resolution after software calibration and 0 to 3V input voltage range
- Supports an digital low pass filter for spike smoothing
- Supports three voltage buffers
- Supports fast AD conversion of 16 channels within 100 ms
- Supports programmable conversion-start delay to guarantee input setting time
- Polling or interrupt-driven interface

7.10.3 Functional Description

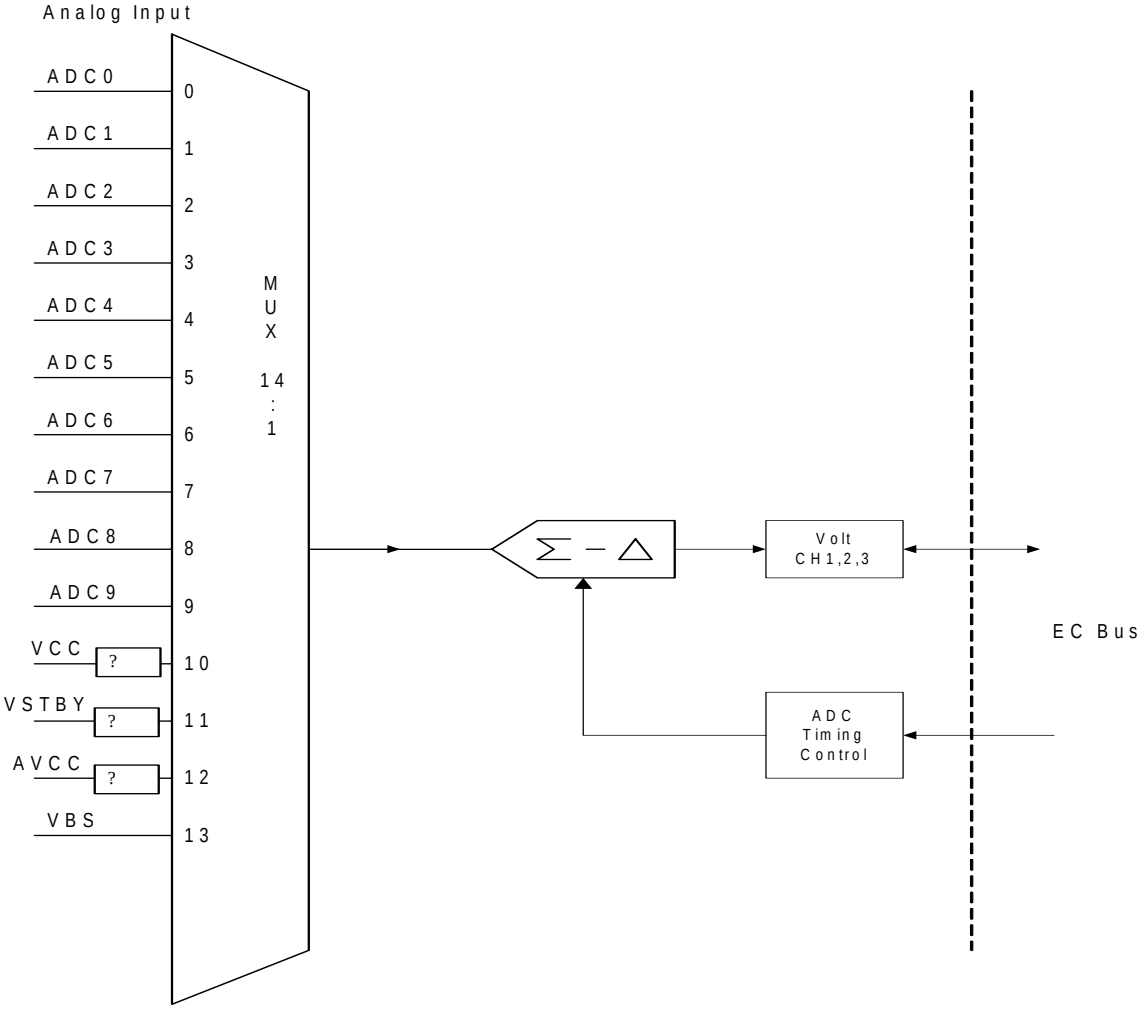

Figure 7-20. ADC Channels Control Diagram

7.10.3.1 ADC General Description

Inputs
The ADC has 14 inputs (ADC0-9, ADC10~13) divided into two groups described as the following:
• External Voltage (ADC0-9):
These are for DC voltage sources.

• Internal Voltage (ADC10-13):
These are connected to the internal supply voltages of the device (VCC, VSTBY AVCC and VBAT). The input voltages of ADC10, ADC11 and ADC12 are divided by 2 before being input to analog multiplexer.

A/D Converter
The sigma-delta high-resolution A/D converter receives the selected input with a 16 to 1 analog multiplier and converts it. The result of the conversion is 14-bit signed integer (2's complement) and it is a 10-bit, unsigned integer for voltage inputs after software calibration process.

The software calibration flow refers to section 7.10.5 ADC Programming Guide.

ADC Cycle
The ADC has three output buffers: These are for the voltage channel. The buffer for voltage measurement channels holds the current data until the next identical volt channel measurement is completed after one ADC cycle is finished. An ADC cycle includes measurements of all three channels. The first measurement is voltage channel 1 and followed by voltage channel 2, 3. After an A/D conversion is completed for a certain channel, its relative bit of the Data Valid (DATVAL bit in VCH1CTL, VCH2CTL and VCH3CTL register) flag is set that represents the channel of data is available and EC can read out.

Channel Conversion Time
If channel delay uses a default value, which means VOLDLY is delay 256 clock units, SCLKDIV factor in ADCCTL register is also set by default, and DFILEN is set to 1, the one channel conversion time is about 3.6msec. If DFILEN is set to 0, the one channel conversion time is about 780usec.

Interrupt to INTC
ADC interrupt (INT8) is active if end-of-cycle, voltage channel 1 data valid, voltage channel 2 data valid or voltage channel 3 data valid is true. See also INTECEN, INTDVEN1, INTDVEN2 and INTDVEN.

7.10.3.2 Voltage Measurement

The ADC converts the un-calibrated input voltage signal into a 14-bit singed integer (2's complement) in data buffer. The input signal should be applied relative to the AGND pin and should range from 0V to 3V.
The following should explain the input voltage based on the reading from the Voltage Channel Data result (VCHiDATL field in VCHiDATM register for voltage).

Example (Refer to the bottom of Figure 7-21 on page 216 for the details:
The un-calibrated input data is 14-bit singed integer (2's complement) in data buffer VCHiDATx.
An input signal equal to 3.0V is about 0FFFh
An input signal equal to 1.5V is about 0000h
An input signal equal to 0.0V is about 3000h
After software calibration flow, it is a 10-bit unsigned integer:
3.0V (about 0FFFh) is calibrated as 3FFh
1.5V (about 0000h) is calibrated as 200h
0.0V (about 3000h) is calibrated as 000h

Changing the input selection for a new measurement channel, the software needs to set a delay time to prevent the result of an unintended ADC operation. The ADC waits for a programmable delay time(in ADCDCTL register) between the selection of the input to be measured and the beginning of the A/D conversion.

7.10.3.3 ADC Operation

Reset
The ADC is disabled, and all interrupt is masked and all event status bits reset. The Selected Input for all three-voltage channels is disabled (Bit4-0 of the VCHiCTL register is set to Fh).

ADC Clock
The ADC clock is generated by dividing the EC clock by a factor defined in SCLKDIV in ACLKCTL register. The ADC clock must be at a frequency of 0.5 MHz. SCLKDIV must be programmed before enabling the ADC.

Initializing the ADC
The ADC must be initialized before ADC is enabled (ADCEN in the ADCCFG register is set to 1). The followings need to be done before the ADC is enabled.

1. Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on)
2. ADCEN bit in ADCCNF register is cleared.
3. programming (SCLKDIV factor in ADCCTL register).
4. Voltage Channel Delay (VOLDLY in ADCDCTL register).
5. Channel Select in VCHiCTL register
6. VOLT calibration information needs to be done by setting calibration active via KDCTL register.

Enabling the ADC
After the ADC is enabled, the voltage channel is measured as long as the ADCEN is set 1, and when Voltage channel is selected. The measurement operations may be enabled or disabled individually.

Disabling the ADC
ADC analog circuit has less power consumption if it is disabled. ADCEN bit in ADCCFG register controls this and it's cleared at EC Domain Reset.
The firmware should clear ADCEN bit before entering Idle/Doze/Sleep mode.

7.10.4 EC Interface Registers

The ADC control/status and data out registers set interfaces with the EC through the EC Dedicated bus. These registers are mapped in the address space of the EC. The registers are listed below and the base address is 1900h.

Table 7-18. EC View Register Map, ADC

7	0	Offset
ADC Status (ADCSTS)		00h
ADC Configuration (ADCCFG)		01h
ADC Clock Control (ADCCTL)		02h
ADC Delay Control (ADCDCTL)		03h
Calibration Data Control Register (KDCTL)		05h
Voltage Channel 1 Control (VCH1CTL)		06h
Voltage Channel 1 Data Buffer LSB (VCH1DATL)		07h
Voltage Channel 1 Data Buffer MSB (VCH1DATM)		08h
Voltage Channel 2 Control (VCH2CTL)		09h
Voltage Channel 2 Data Buffer LSB (VCH2DATL)		0ah
Voltage Channel 2 Data Buffer MSB (VCH2DATM)		0bh
Voltage Channel 3 Control (VCH3CTL)		0ch
Voltage Channel 3 Data Buffer LSB (VCH3DATL)		0dh
Voltage Channel 3 Data Buffer MSB (VCH3DATM)		0eh
Voltage High Scale Calibration Data Buffer LSB (VHSCDBL)		14h
Voltage High Scale Calibration Data Buffer MSB (VHSCDBM)		15h
Voltage High Scale Gain-error Calibration Data Buffer LSB (VHSGCDBL)		1Ch
Voltage High Scale Gain-error Calibration Data Buffer MSB (VHSGCDBM)		1Dh

For a summary of the abbreviations used for register type, see “Register Abbreviations and Access Rules”

7.10.4.1 ADC Status Register (ADCSTS)

This register indicates the global status of the ADC module.

Address Offset: 00h

Bit	R/W	Default	Description
7	W	0b	**Clear Data Overflow Event (CDOVE)** This bit is used to clear DOVE bit by writing 1 to it after overflow data buffer has read; reading this bit returns 0.
6	-	0b	**Reserved**
5-4	R/W	00b	**Decimation Filter Ratio (DFR)** These bits determine the down-sampling rate to remove the quantization noise. **Bits 5 4** 0 0: 32 Other: Reserved
3	R/W	0b	**Analog Accuracy Initialization Bit (AINITB)** Write 1 to this bit and write 0 to this bit immediately once and only once during the firmware initialization and do not write 1 again after initialization since IT8510 takes much power consumption if this bit is set as 1. Writing steps about this bit should be done before ADCEN bit is set in ADCCFG register. 1: Start ADC accuracy initialization. 0: Stop ADC accuracy initialization.

Bit	R/W	Default	Description
2	R/W	0b	**ADC Power Statement (ADCPS)** This bit remains zero when ADC power in normal state. When ADC power shut down or failure occur, the software must program this bit to one. The program must be wait 200usec at least for ADC internal initialization after power on. 0: indicate the ADC power in a normal state 1: indicate the ADC power in a shut down or failure state
1	R	0b	**Data Overflow Event (DOVE)** Measurement data from the previous cycle was overwritten with data From the current cycle before being read. In the event of a data overflow, the DATVAL bit remains set and new data is placed in Channel Data Buffer register. 0: No overflow (default) 1: Overflow
0	R/WC	0b	**End-of-Cycle Event (EOCE)** End of ADC cycle; all enabled measurements (up to three) are Completed. For each of the enabled channels, the DATVAL bit is set to 1 and the data stored in Channel Data Buffer register respectively. 0: Cycle in progress (default) 1: End of ADC cycle

7.10.4.2 ADC Configuration Register (ADCCFG)

This register controls the operation and global configuration of the ADC module.

Address Offset: 01h

Bit	R/W	Default	Description
7-6		10b	**Reserved**
5	R/W	0b	**Digital Filter Enable (DFILEN)** Enables the digital filter operation for spike smoothing on ADC output signal. Setting this bit to 1 enables the digital low pass filter to prevent unwanted signal changes based on the ADC conversion and the smoothing data is read on the VCHxDAT register. When this digital filter is enable, the EC Clock Division Factor (SCLKDIV) must be set to a value which is larger than 15(decimal), then digital filter will work fine. 0: Disabled digital filter operation(default) 1: Enabled digital filter operation on ADC output signal when ADCEN set 1. If ADCEN is cleared, this bit can be ignored.
4-3	-	-	**Reserved**
2	R/W	0b	**Interrupt from End-of-Cycle Event Enable (INTECEN)** Enables an ADC interrupt generated by End-of ADC-cycle event (EOCEV in ADCSTS register). 0: Disabled (default) 1: Enabled interrupt by EOCEV event
1	R/W	0b	**Reserved**
0	R/W	0b	**ADC Module Enable (ADCEN)** Controls ADC operation or not 0: ADC disabled (default), power-down 1: ADC enabled

7.10.4.3 ADC Clock Control Register (ADCCTL)

This register controls the EC clock to ADC clock division.

Address Offset: 02h

Bit	R/W	Default	Description
7-6	-	0h	**Reserved**
5-0	R/W	13h	**EC Clock Division Factor (SCLKDIV)** Divide the EC clock into the ADC clock. The EC clock is different from the ADC clock. ADC Clock Frequency = (EC Clock Frequency) / (SCLKDIV + 1) Normally EC clock frequency is 10 MHz and may be divided by CFSELR register. The resulting ADC clock frequency should be equal to 0.5 MHz. Range: 4 to 63; if values 0 to 3 are set and may result in undetermined ADC behavior.

7.10.4.4 ADC Delay Control Register (ADCDCTL)

This register controls the delay between “input switching” and “conversion start” for the voltage.

Address Offset: 03h

Bit	R/W	Default	Description
7-3	R/W	0h	**Reserved**
2-0	R/W	6h	**Voltage Channel Delay (VOLDLY)** Provide settling time for ADC volt conversion start after channel switching. Voltage Channel Delay = Voltage_Channel_Delay_Count * (EC Clock Period) * (SCLKDIV + 1) VOLDLY Voltage_Channel_Delay_Count Bits 2 1 0 0 0 1: 8 0 1 0: 16 0 1 1: 32 1 0 0: 64 1 0 1: 128 1 1 0: 256(default) 1 1 1: 512 Other: Reserved

7.10.4.5 Calibration Data Control Register (KDCTL)

This register both controls the operation and indicates the status of the Calibration channel.

Address Offset: 05h

B it	R/W	Default	Description
7	R/WC	0b	**Reserved**
6	R/WC	0b	**Reserved**

B it	R/W	Default	Description
5	R/WC	0b	**High-Scaler Calibration Data Valid (HCDATVAL)** The data may be read when this bit is set 1. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. If gain error calibration is selected, the valid data is for Gain Error Calibration; otherwise, it is for Offset Calibration . 0: No new valid data in volt Calibration data register (default). 1: End of volt Calibration – new data is available in data buffer.
4	R/WC	0b	**Gain_Error Calibration Data Valid (GCDATVAL)** The data may be read when this bit is set 1. This bit is cleared when the ADC module is disabled (ADCEN in ADCCFG register is cleared) or by writing 1 to it. When this bit is set, the valid data is for Gain Error Calibration. 0: No new valid data in High-Scaler Calibration data register (default) 1: End of High-scaler Calibration – new data is available in data buffer.
3	R/W	0b	**Reserved**
2	R/W	0b	**Reserved**
1	R/W	0b	**Volt High Scale Calibration Enable (VHSCKE)** When GECKE is cleared to 0, set this bit to 1 to enable the Volt High Scale (3volts) Calibration operation for volt ADC channel. To initialize one ADC calibration operation, calibration data will be stored on Voltage High Scale Calibration Data Buffer when ADC calibration data has been done (DATVAL=1), and this bit will be cleared to zero automatically. 0: Disabled calibration operation(default) 1: Enabled calibration operation when GECKE is cleared to 0.
0	R/W	0b	**Gain_Error Calibration Enable (GECKE)** Enables the Gain_Error Calibration operation for volt ADC channel. Set this bit to 1 to initialize one ADC gain_error calibration operation, and calibration data will be stored on Voltage Gain_error Calibration Data Buffer when ADC calibration data has been done(GCDATVAL=1), and this bit will be cleared to zero automatically. 0: Disabled calibration operation(default) 1: Enabled gain error calibration operation

7.10.4.6 Voltage Channel 1 Control Register (VCH1CTL)

This register both controls the operation and indicates the status of Voltage Channel 1.

Address Offset: 06h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The data may be read immediately when this bit is set 1. This bit is cleared when the ADC module is disabled or by writing 1 to it. 0: No valid data in VCH1DATx register (default) 1: End of conversion – New data is available.
6	R/W	0b	**Reserved**
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** Enabled to the ADC Interrupt for Data valid event of Volt channel 1. 0: Disabled (default) 1: Enabled – ADC Interrupt from local DATVAL

Bit	R/W	Default	Description
4-0	R/W	11111b	**Selected Input (SELIN)** Indicates which Volt channel input was selected for measurement. Channel selected must be done before beginning to measure channel. **Bits** 4 3 2 1 0 Description 0 0 0 0 0: Channel 0 0 0 0 0 1: Channel 1 .... 0 1 0 0 0: Channel 8 0 1 0 0 1: Channel 9 0 1 0 1 0: Channel 10 .... 0 1 1 0 1: Channel 13 Other: Reserved 1 1 1 1 1: Channel Disabled (default)

7.10.4.7 Volt Channel 1 Data Buffer LSB (VCH1DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 1.

Address Offset: 07h

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 1. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.8 Volt Channel 1 Data Buffer MSB (VCH1DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 1.

Address Offset: 08h

Bit	R/W	Default	Description
7-6		-	**Reserved**
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 1. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.9 Voltage Channel 2 Control Register (VCH2CTL)

This register both controls the operation and indicates the status of Voltage Channel 2.

Address Offset: 09h

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.10.4.10 Volt Channel 2 Data Buffer LSB (VCH2DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 2.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0**) Volt channel data is measured by the volt channel 2 . The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.11 Volt Channel 2 Data Buffer MSB (VCH2DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 2.

Address Offset: 0Bh

Bit	R/W	Default	Description
7-6		-	**Reserved**

Bit	R/W	Default	Description
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 2. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.12 Voltage Channel 3 Control Register (VCHN3CTL)

This register both controls the operation and indicates the status of Voltage Channel 3.

Address Offset: 0Ch

Bit	R/W	Default	Description
7	R/WC	0b	**Data Valid (DATVAL)** The same as Volt channel 1.
6	R/W	0b	**Reserved** The same as Volt channel 1.
5	R/W	0b	**Interrupt from Data Valid Enable (INTDVEN)** The same as Volt channel 1.
4-0	R/W	11111b	**Selected Input (SELIN)** The same as Volt channel 1.

7.10.4.13 Volt Channel 3 Data Buffer LSB (VCH3DATL)

This register (buffer) holds the data(LSB 8bits) measured by the Volt Channel 3.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-0	R	-	**Volt Channel Data (VCHDAT7-0)** Volt channel data is measured by the volt channel 3. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.14 Volt Channel 3 Data Buffer MSB (VCH3DATM)

This register (buffer) holds the data(MSB 6bits) measured by the Volt Channel 3.

Address Offset: 0Eh

Bit	R/W	Default	Description
7-6		-	**Reserved**
5-0	R	-	**Volt Channel Data (VCHDAT13-8)** Volt channel data is measured by the volt channel 3 . The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.15 Volt High Scale Calibration Data Buffer LSB (VHSCDBL)

This register (buffer) holds the calibration data(LSB 8bits) measured by the internal voltage channel.

Address Offset: 14h

Bit	R/W	Default	Description
7-0	R	-	**Volt Calibration Data (VCKD7-0)** Volt calibration data is measured by the internal voltage channel . The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.16 Volt High Scale Calibration Data Buffer MSB (VHSCDBM)

This register (buffer) holds the calibration data(MSB 4bits) measured by the internal voltage channel.

Address Offset: 15h

Bit	R/W	Default	Description
7-6	-	00h	**Reserved**
5-0	R	-	**Volt Calibration Data (VCKD13-8)** Volt calibration data is measured by the internal voltage channel. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.17 Volt High Scale Gain-Error Calibration Data Buffer LSB (VHSGCDBL)

This register (buffer) holds the gain-error calibration data(LSB 8bits) measured by the internal voltage channel.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R	-	**Volt Gain-Error Data (VGED7-0)** Volt gain-error data is measured by the internal voltage channel. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.4.18 Volt High Scale Gain-Error Calibration Data Buffer MSB (VHSGCDBM)

This register (buffer) holds the gain-error calibration data(MSB 6bits) measured by the internal voltage channel.

Address Offset: 1Dh

Bit	R/W	Default	Description
7-4	-	00h	**Reserved**
5-0	R	-	**Volt Gain-Error Data (VGED13-8)** Volt gain-error data is measured by the internal voltage channel. The data may be read only at the end-of-cycle. DATVAL must be cleared after read data.

7.10.5 ADC Programming Guide

Table 7-19. Detail Step of ADC Channel Conversion

Action	Step	Description
Determine Offset and Gain_Error during initialization	1	Set AINITB@ADCSTS = 1 then clear it (only once after VSTBY power on)
	2	Enable digital filter by setting DFILEN@ADCCFG = 1
	3	Set high scale offset calibration bit by setting VHSCKE@KDCTL = 1
	4	Start ADC conversion by setting ADCEN@ADCCFG = 1
	5	Waiting for HCDATVAL@KDCTL = 1 If true, get Offset Data **O** by reading VHSCDBM and VHSCDBL **O**[13:0] = {VHSCDBM[5:0], VHSCDBL[7:0]}
	6	Start Gain_Error calibration by setting GECKE@KDCTL = 1
	7	Waiting for GCDATVAL@KDCTL = 1 If true, get Gain_Error Data **G** by reading VHSGCDBM and VHSGCDBL **G**[13:0] = {VHSGCDBM[5:0], VHSGCDBL[7:0]}
	8	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0
ADC channel conversion	9	Enable VCHnCTL for measuring desired channels; n = 1, 2, or 3
	10	For example; To measure ADC0 voltage on voltage buffer 1 Set SELIN@VCH1CTL = 0
	11	Start ADC channel conversion by setting ADCEN@ADCCFG =1
	12	Waiting for DATVAL@VCH1CTL = 1 If true, get ADC0 output data **R** by reading VCH1DATM and VCH1DATAL **R**[13:0] = {VCH1DTM[5:0], VCH1DATL[7:0]}
	13	Disable ADC to reduce power consumption by setting ADCEN@ADCCFG = 0
	14	Follow to make a software calibration then go to step 8 in next time

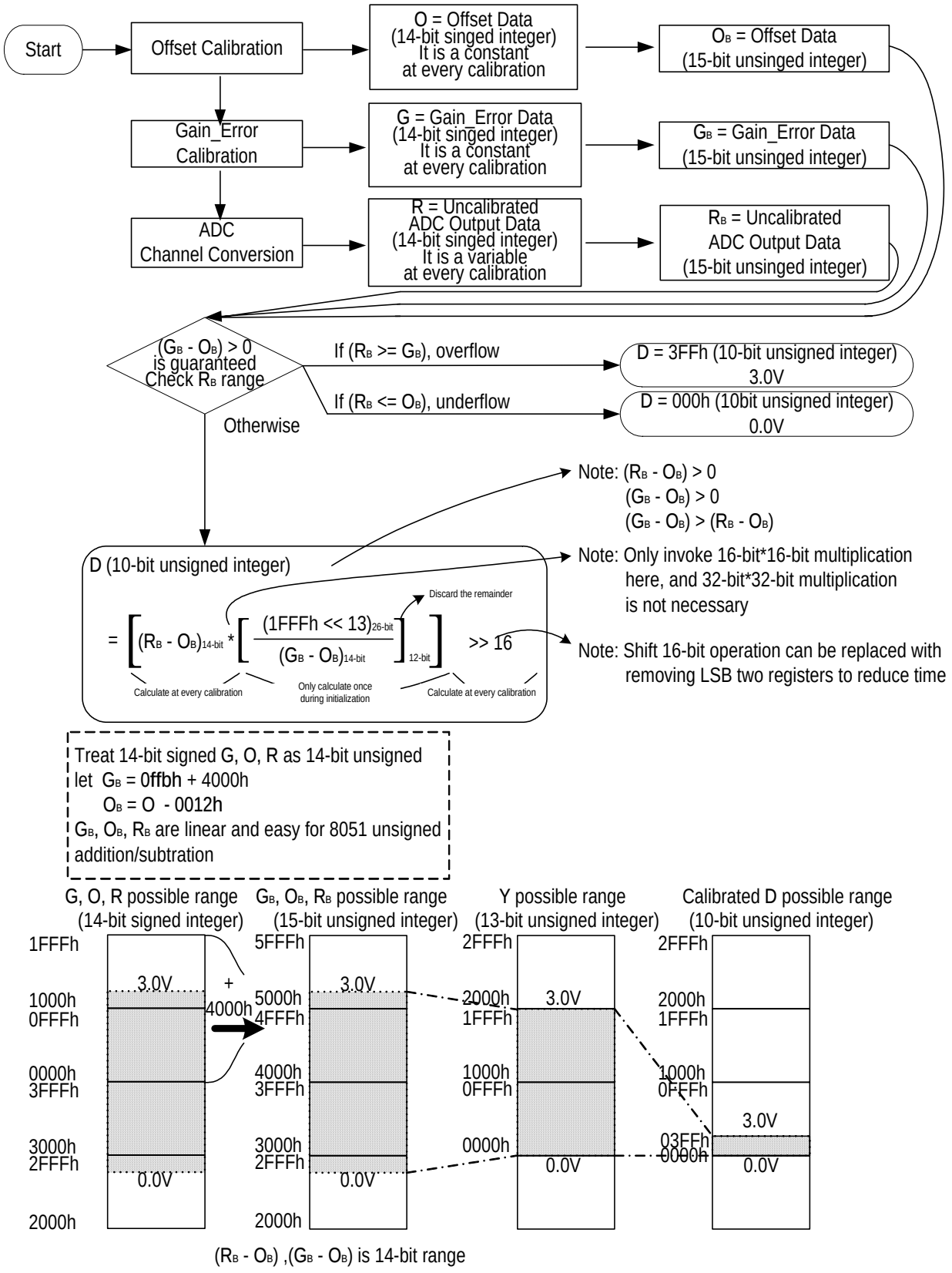

Figure 7-21. ADC Software Calibration Flow

Another quick way in a special case:

If D is used be compared with a threshold value, this threshold can be calculated first to be mapped into the data space of G_B, O_B, R_B during initialization, and the multiplication and division operation invoked to calibrate R_B can be omitted. There are only one multiplication and one division to calculate R_{BL} during initialization.

Threshold Low Boundary $$R_{BL}{}_{15\text{-bit}} = \left[\frac{(G_B - O_B)_{14\text{-bit}} * (D << 3)_{13\text{-bit}}}{1FFFh_{\ 13\text{-bit}}} \right]_{14\text{-bit}} + O_{B}{}_{15\text{-bit}}$$

Threshold High Boundary $$R_{BH}{}_{15\text{-bit}} = R_{BL} + (2 << 3) - 1 = R_{BL} + 7$$

Then uncalibrated R_B which satisies $R_{BL} <= R_B <= R_{BL}$ should be mapped into calibrated D
That is, normally there are 8 possible R_B values will be mapped into calibrated D

Example:

G_B = 5020h
O_B = 3010h
Threshold voltage = 2.0V, Target D = 3FFh * 2.0 / 3.0 = 2AAh
Then

$$R_{BL} = \left[\frac{(5020h - 3020h) * (2AAh << 3)}{1FFFh} \right] + 3010h = 456Bh$$

$$R_{BH} = R_{BL} + 7$$

Final

Calibrated ADC Output < 2.0V if R_B < 456Bh
Calibrated ADC Output <= 2.0V if R_B <= (456Bh + 7)
Calibrated ADC Output > 2.0V if R_B > (456Bh + 7)
Calibrated ADC Output >= 2.0V if R_B >= 456Bh

Figure 7-22. ADC Software Calibration Flow in a Special Case

7.11 PWM and SmartAuto Fan Control (PWM)

7.11.1 Overview

The PWM module generates eight 8-bit PWM outputs; each PWM output may have a different duty cycle. The fan speed may be controlled by software or automatically controlled by the SmartAuto fan control module. In SmartAuto fan mode, the SmartAuto fan control logic automatically adjusts the PWM output for driving the fan speed according to written data in F1TRR and F2TRR registers.

7.11.2 Features

- Supports eight PWM outputs
- Supports two fan tachometer inputs
- Supports programmable automatic SmartAuto fan control based on temperature
- Supports exchangeable PWM output for SmartAuto fan control
- Supports fan temperature limit configuration
- Supports Interrupt for Temperature Limit Exceeded

7.11.3 Functional Description

7.11.3.1 General Description

The PWM uses the 32.768K Hz or 10M Hz clock as a reference for its PWM output. The prescaler divider values in CiCRPS register which divides the PWM input clock into its working clock respectively. Each channel group can select their prescaler divider by {PCSSGH,PCSSGL} register. The prescaler divider C0CRPS register has 8 bits counter value; and the CiCRPS(i=4,6,7) has 16 bit counter value. The PWM provides eight 8-bit PWM outputs, which are PWM0 to PWM7. Each PWM output is controlled by its Duty Cycle registers (DCRi, i =0 to 7). All PWM output is controlled by an Cycle Time register (CTR).
When PWM working clock is enabled, the PWM cycle output is on Hight when the value in the DCRi register is larger than the value in CTR down-counter. When the value of DCRi register is not larger than the value in CTR down-counter, the PWMi cycle output is on LOW and PWMi cycle output polarity can be inversed by INVPi register.
When the value in CTR counter down-counter reaches 0, the value in CTR counter will be reloaded then start down-counter until the PWM working clock is disabled.

Cycle Time and Duty Cycle
The PWM module supports duty cycles ranging from 0% to 100%.
The PWMi output signal cycle time is:

$$(CiCPRS + 1) \times (CTR + 1) \times T_{32.768K}$$

Where:
• T 32.768K is the 32.768K HZ frequency of clock cycle time (i.e., the PWM input clock).
• The PWMi output signal duty cycle (in %, when INVPi is 0) is:

$$(DCRi) / (CTR + 1) \times 100.$$

In the following cases, the PWMi output is hold at a state(low or high):
•PWMi output is still low when the content of DCRi is larger than the CTR value.
•PWMi output is still high when the content of DCRi is equal to the CTR value.
•PWMi output is still low when the content of DCRi =0 & INVPi = 0 is in PWMPOL register.

PWM Inhibit Mode
The PWM is in an inhibit mode when PCCE in ZTIER Register is 0. In this mode, the PWM input clock is disabled (stopped). The PWMi signal is 0 when INVPi bit is 0; it is 1 when INVPi bit is 1. It is recommend the PRSC and CTR registers should be updated in a PWM inhibit mode.

7.11.3.2 SmartAuto Fan Control Mode

Fan PWM Channel Select

The EC chip provides 2 types of fan control operation mode using PMW output. A mode select can be set in FANCNF in the Fani configuration register (FANiCNF). When write FANCNF in FANiCNF register to 00, set Manual Fan Control Mode. When write FANCNF in FANiCNF register to 10, set SmartAuto Fan Control Mode. When in a SmartAuto fan mode, the fan will be assigned for a zone and its PWM duty cycle will be automatically adjusted according to the temperature of that zone.

When in a manual fan mode, its PWM duty cycle register can be read/written by software to control the PWM duty cycle output.

In a fan control mode, it is necessary to select which PWM channel outputs for driving Fan. The FPWMCS in FANiCNF register is set from 000b~111b to select CH0~7 PWM output as driving source for FANi respectively.

SmartAuto Fan Control Operation

When operating in SmartAuto Fan Control Mode, the hardware controls the fans based on writing temperature data into F1TRR and F2TRR registers. The following Initialization needs to be done:

1. Set the minimum temperature that will turn on/off the fans in FANi Temperature Limit register(FiTLIMITR).
2. Set the hysteresis value for the minimum temperature. The fan keeps at on state until the temperature below a certain amount which is set in FiTLIMITR register. The hysteresis value can be set in ZHYSR register.
3. The duty cycle for the minimum fan speed needs to be set in FiMPDCR register according to the actual temperature increase/decrease and to decide a linear function based on the fan speed range in AFiSRR register.
4. Set the Absolute temperature for the FANi in FiATLIMITR register. If the actual temperature is equal to or exceeds the absolute temperature value set in FiATLIMITR, the FANi will be set to Full on.
5. Set the mode to operate in a SmartAuto mode. After step 1 to 4 are set, FANi Configuration can be set to 10 (FANCNF=10) in FANiCNF register, then the fan is controlled by hardware automatically.

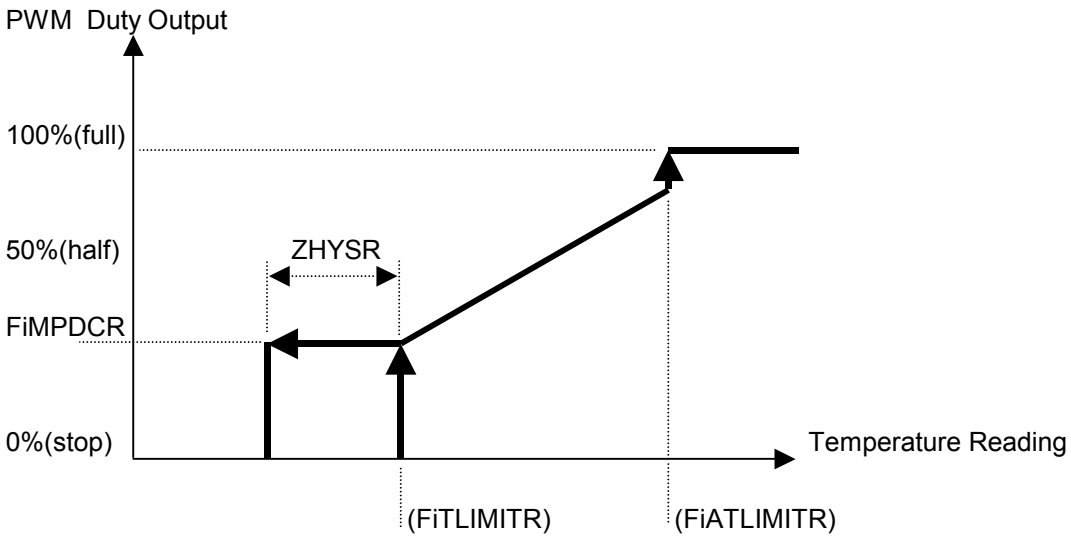

Figure 7-23. SmartAuto Fan PWM output vs Temperature Reading

7.11.3.3 Manual Fan Control Mode

In manual mode, the software may monitor either the fan Tachometer Reading Registers or Temperature Reading Register to control the fan speed by programming the duty cycle of the driving PWM (FiMPDCR) register.

The contents of the Tachometer Reading Register is still updated according to the sampling counter that samples the tachometer input. The sampling rate is 78.125 KHz.

Fan Speed (R.P.M.) = 60 / (12.8 μsec * {FnTMRR, FnTLRR} * P)
n denotes 1 or 2
P denotes the numbers of square pulses per revolution.
And {FnTMRR, FnTLRR} = 0000h denotes Fan Speed is zero.

7.11.4 EC Interface Registers

These registers are mapped in the address space of the EC. The registers are listed below and the base address is 1800h.

Table 7-20. EC View Register Map, PWM

7 — 0	Offset
Channel 0 Clock Prescaler Register (C0CPRS)	00h
Cycle Time (CTR)	01h
PWM Duty Cycle (DCR0-7)	02h-09h
PWM Polarity (PWMPOL)	0Ah
Prescaler Clock Frequency Select Register (PCFSR)	0Bh
Prescaler Clock Source Select Group Low (PCSSGL)	0Ch
Prescaler Clock Source Select Group High (PCSSGH)	0Dh
Fan 1 Configuration (FAN1CNF)	10h
Fan 2 Configuration (FAN2CNF)	11h
SmartAuto Fan 1 Speed Range (AF1SRR)	12h
SmartAuto Fan 2 Speed Range (AF2SRR)	13h
Min/Off PWM Limit (MOPL)	14h
Fan 1 Minimum PWM Duty (F1MPDCR)	15h
Fan 2 Minimum PWM Duty (F2MPDCR)	16h
Fan 1 Temperature Limit (F1TLIMITR)	17h
Fan 2 Temperature Limit (F2TLIMITR)	18h
Fan 1 Absolute Temperature Limit (F1ATLIMITR)	19h
Fan 2 Absolute Temperature Limit (F2ATLIMITR)	1Ah
Zone Hysteresis (ZHYSR)	1Bh
Fan 1 Temperature Record (F1TRR)	1Ch
Fan 2 Temperature Record (F2TRR)	1Dh
Fan 1 Tachometer LSB Reading (F1TLRR)	1Eh
Fan 1 Tachometer MSB Reading (F1TMRR)	1Fh
Fan 2 Tachometer LSB Reading (F2TLRR)	20h
Fan 2 Tachometer MSB Reading (F2TMRR)	21h
Zone Interrupt Status Control (ZINTSCR)	22h
Zone Temperature Interrupt Enable (ZTIER)	23h
Channel 4 Clock Prescaler Register (C4CPRS)	27h
Channel 4 Clock Prescaler MSB Register (C4MCPRS)	28h
Channel 6 Clock Prescaler Register (C6CPRS)	2Bh
Channel 6 Clock Prescaler MSB Register (C6MCPRS)	2Ch
Channel 7 Clock Prescaler Register (C7CPRS)	2Dh
Channel 7 Clock Prescaler MSB Register (C7MCPRS)	2Eh

For a summary of the abbreviations used for register types, see “Register Abbreviations and Access Rules”

7.11.4.1 Channel 0 Clock Prescaler Register (C0CPRS)

This register controls the cycle time and the minimal pulse width of channel 0~3.

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV)** PWM input clock is divided by the number of (C0CPRS+ 1). For example, the value of 01h results in a divide by 2. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode.

7.11.4.2 Cycle Time Register (CTR)

This register controls the cycle time and duty cycle steps.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	FFh	**Cycle Time Value (CTV)** The Prescaler output clock is divided by the number of (CTR + 1). For example, the value of 00h results in a divide by 1. The value of FFh results in a divide by 256. The contents of this register may be changed only when the PWM module is in the PWM inhibit mode. The clock source is 32.768KHz.

7.11.4.3 PWM Duty Cycle Register 0 to 7(DCRi)

This register (DCRi; I=0 to 7) controls the duty cycle of PWMi output signal.

Address Offset: 02h(ch0), 03h(ch1), 04h(ch2), 05h(ch3), 06h(ch4), 07h(ch5), 08h(ch6), 09h(ch7);

Bit	R/W	Default	Description
7-0	R/W	00h	**Duty Cycle Value (DCV)** DCRi register decides the number of clocks for which PWMi is high when INVPi bit is 0 in PWMPOL register. The PWMi Duty Cycle output = (DCRi)/(CTR+1) If the DCRi value > CTR value, PWMi signal is still low. If DCRi value = CTR value, PWMi signal is still high. When Inverse PWMi bit is 1, the value of PWMi is inversed.

7.11.4.4 PWM Polarity Register (PWMPOL)

This register controls the polarity of PWM0 to PWM7.

Address Offset: 0Ah

Bit	R/W	Default	Description
7-0	R/W	00h	**Inverse PWM Outputs (INVP7-0)** The bit 7 to 0 control the polarity of PWM7 to PWM0 respectively. 0: Non-inverting. 1: Inverting.

7.11.4.5 Prescaler Clock Frequency Select Register (PCFSR)

This register is used to select prescaler clock frequency for four channel groups 3-0. Each of them includes 2 channels. See the following table.

Channel Group	Prescaler Channels
0	C0CPRS
1	C4MCPRS,C4CPRS
2	C6MCPRS,C6CPRS
3	C7MCPRS,C7CPRS

Address Offset: 0Bh

Bit	R/W	Default	Description
7-4		0h	**Reserved**
3	R/W	0b	**Prescaler Clock Select (PCS)** Bit 3 select prescaler clock frequency for channel group 3. 0: select 32k Hz 1: select 10M Hz (EC Clock and maybe divided).
2	R/W	0b	**Prescaler Clock Select (PCS)** Bit 2 select prescaler clock frequency for channel group 2. 0: select 32k Hz 1: select 10M Hz (EC Clock and maybe divided).
1	R/W	0b	**Prescaler Clock Select (PCS)** Bit 1 select prescaler clock frequency for channel group 1. 0: select 32k Hz 1: select 10M Hz (EC Clock and maybe divided).
0	R/W	0b	**Prescaler Clock Select (PCS)** Bit 0 select prescaler clock frequency for channel group 0. 0: select 32k Hz 1: select 10M Hz (EC Clock and maybe divided).

7.11.4.6 Prescaler Clock Source Select Group Low(PCSSGL)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock source.

Address Offset: 0Ch

Bit	R/W	Default	Description
7-6	R/W	0h	**Prescaler Clock Select 3 (PCS3)** The bits select prescaler clock for channel 3. The bits 7-6 are the same as bit 1-0.
5-4	R/W	0h	**Prescaler Clock Select 2 (PCS2)** The bits select prescaler clock for channel 2. The bits 5-4 are the same as bit 1-0.
3-2	R/W	0h	**Prescaler Clock Select 1 (PCS1)** The bits select prescaler clock for channel 1. The bits 3-2 are the same as bit 1-0.
1-0	R/W	0h	**Prescaler Clock Select 0 (PCS0)** The bits select prescaler clock for channel 0. 00: select prescaler clock divided by C0CPRS 01: select prescaler clock divided by {C4MCPRS,C4CPRS} 10: select prescaler clock divided by {C6MCPRS,C6CPRS} 11: select prescaler clock divided by {C7MCPRS,C7CPRS}

7.11.4.7 Prescaler Clock Source Select Group High(PCSSGh)

This register is used to select prescaler clock source for four channels. Each channel uses 2 bits to select one from four prescaler clock source.

Address Offset: 0Dh

Bit	R/W	Default	Description
7-6	R/W	1h	**Prescaler Clock Select 7(PCS7)** The bits select prescaler clock for channel 7. The bits 7-6 are the same as bit 1-0.
5-4	R/W	1h	**Prescaler Clock Select 6(PCS6)** The bits select prescaler clock for channel 6. The bits 5-4 are the same as bit 1-0.
3-2	R/W	1h	**Prescaler Clock Select 5(PCS5)** The bits select prescaler clock for channel 5. The bits 3-2 are the same as bit 1-0.
1-0	R/W	1h	**Prescaler Clock Select 4 (PCS4)** The bits select prescaler clock for channel 4 00: select prescaler clock divided by C0CPRS 01: select prescaler clock divided by {C4MCPRS,C4CPRS} 10: select prescaler clock divided by {C6MCPRS,C6CPRS} 11: select prescaler clock divided by {C7MCPRS,C7CPRS}

7.11.4.8 Fan 1 Configuration Register (FAN1CNF)

This register controls the Fan 1 operation mode, which is associated with F1TRR register.

Address Offset: 10h

Bit	R/W	Default	Description
7-6	R/W	00b	**Fan Configuration (FANCNF)** When in a SmartAuto fan mode, the fan will be assigned to a zone and its PWM duty cycle will be automatically adjusted according to the temperature of that zone. When in a manual fan mode, its PWM duty cycle register can be read/written by software to control the PWM duty cycle output. **Bits Config.** 00 Fan on Zone SmartAuto 10 Fan manually controlled Others Reserved
5	-	0h	**Reserved**
4-2	R/W	0h	**Fan PWM Channel Select (FPWMCS)** Bit 4-2 Select PWM duty cycle output for driving Fan. In SmartAuto fan mode, the value of the PWM duty cycle register selected for fan will be update according the SmartAuto fan algorithm, so software may not write these PWM duty cycle register for fan. **Bits PWM CH for Fan** 000 PWM Channel 0 001 PWM Channel 1 010 PWM Channel 2 011 PWM Channel 3 100 PWM Channel 4 101 PWM Channel 5 110 PWM Channel 6 111 PWM Channel 7
1-0	R/W	0h	**Fan Spin Up Time (FANSUPT)** Bit 1-0 select the spin up time for the fan. When the fan spins up, after the fan stops for more than 31ms, the PWM output is held at 100% duty cycle during time specified. **Bits Times** 00 Zero sec 01 125m sec (+- 31ms) 10 250m sec (+- 31ms) 11 500m sec (+- 31ms)

7.11.4.9 Fan 2 Configuration Register (FAN2CNF)

This register controls the Fan 2 operation mode, which is associated with F2TRR register.

Address Offset: 11h

Bit	R/W	Default	Description
7-6	R/W	00b	**Fan Configuration (FANCNF)** The same as the FAN1CNF register
5	-	0h	**Reserved**
4-2	R/W	0h	**Fan PWM Channel Select (FPWMCS)** The same as the FAN1CNF register

Bit	R/W	Default	Description
1-0	R/W	0h	**Fan Spin Up Time (FANSUPT)** The same as the FAN1CNF register

7.11.4.10 SmartAuto Fan 1 Speed Range Register (AF1SRR)

This register controls the range of the Fan 1 speed activity in the SmartAuto fan mode.

Address Offset: 12h

Bit	R/W	Default	Description
7-4	R/W	0h	**Fan Speed Range (FSR)** In the SmartAuto fan mode, when the temperature drops on the range of the Temperature Limit(TLIMIT register) and the Absolute Temperature Limit(ATLIMIT register), the speed of the fan is increased linearly according to the temperature increment range. Bit 7-4 decide the temperature range. **Bits Temperature range (degree C)** 0001h 2 degree C 0010h 4 degree C 0011h 8 degree C 0100h 16 degree C 0101h 32 degree C 0110h 64 degree C others reserved
3-0		0h	**Reserved**

7.11.4.11 SmartAuto Fan 2 Speed Range Register (AF2SRR)

This register controls the range of the Fan 2 speed activity in the SmartAuto fan mode,

Address Offset: 13h

Bit	R/W	Default	Description
7-4	R/W	0h	**Fan Speed Range (FSR)** Same as the AF1SRR register
3-0		0h	**Reserved**

7.11.4.12 Min/Off PWM Limit Register (MOPL)

This register specifies whether duty cycle will be 0% or Minimun Fan Duty when the measured termperature is below the Temperature Limit register setting. Bit 7(OFF2) applies to Fan2 and Bit 6 (OFF1) applies to Fan1.

Address Offset: 14h

Bit	R/W	Default	Description
7	R/W	0b	**OFF2/Min Limit (O2MLIMIT)** 0: PWM activates at 0% duty when the temperature is below LIMIT, which means TLIMITV – ZHYSV + 1. 1: PWM activates at PWM Minimum duty when the temperature is below LIMIT, which means TLIMITV.
6	R/W	0b	**OFF1/Min Limit (O1MLIMIT)** 0: PWM activates at 0% duty when the temperature is below LIMIT, which means TLIMITV – ZHYSV + 1. 1: PWM activates at PWM Minimum duty when the temperature is below LIMIT which means TLIMITV.

Bit	R/W	Default	Description
5-0	-	0h	**Reserved**

7.11.4.13 Fan 1 Minimum PWM Duty Cycle Register (F1MPDCR)

This register specifies the Minimun Fan Duty that PWM will output when the measured termperature reaches the Temperature LIMIT register settting..

Address Offset: 15h

Bit	R/W	Default	Description
7-0	R/W	80h	**Minimum PWM Duty Cycle Value (MPWMDCV)** The value of this register is the same as the DCRi register, which defines the number of clocks for which PWMi is high (from the full cycle of the PWMi cycle), when INVPi bit is 0 in PWMPOL register.

7.11.4.14 Fan 2 Minimum PWM Duty Cycle Register (F2MPDCR)

This register specifies the Minimun Fan Duty that PWM will output when the measured termperature reaches the Temperature LIMIT register settting..

Address Offset: 16h

Bit	R/W	Default	Description
7-0	R/W	80h	**Minimum PWM Duty Cycle Value (MPWMDCV)** This register is the same as the F1MPDCR Register.

7.11.4.15 Fan 1 Temperature LIMIT Register (F1TLIMITR)

This register specifies the temperature LIMIT value for Fan 1 assigned to the Zone 1.

Address Offset: 17h

Bit	R/W	Default	Description
7-0	R/W	5Ah	**Temperature LIMIT Value (TLIMITV)** When the temperature exceeds this limit, the Fan will be turned on and speed increased according to the SmartAuto fan algorithm based on the setting in the SmartAuto fan x Speed Range register(AFxSRR). **BITS Minimum PWM Duty** 80h -128 degree C … … Ceh -50 degree C … … 00h 0 degree C … … 32h 50 degree C … … 7Fh 127 degree C

7.11.4.16 Fan 2 Temperature LIMIT Register (F2TLIMITR)

This register specifies the temperature LIMIT value for Fan 2 assigned to the Zone 2.

Address Offset: 18h

Bit	R/W	Default	Description
7-0	R/W	5Ah	**Temperature LIMIT Value (TLIMITV)** This register is the same as the F1TLIMITR register.

7.11.4.17 Fan 1 Absolute Temperature LIMIT Register (F1ATLIMITR)

This register specifeis the absolute temperature LIMIT value for Fan 1 assigned to the Zone 1.

Address Offset: 19h

Bit	R/W	Default	Description
7-0	R/W	64h	**Absolute Temperature LIMIT Value (ATLIMITV)** In a SmartAuto fan mode, when the current temperature exceeds this limit, the Fan will be running on PWM duty 100% except those are disable by FANxCNF register. **BITS Temperature** 80h -128 degree C … … Ceh -50 degree C … … 00h 0 degree C … … 32h 50 degree C … … 7Fh 127 degree C

7.11.4.18 Fan 2 Absolute Temperature LIMIT Register (F2ATLIMITR)

This register specifies the absolute temperature LIMIT value for Fan 2 assigned to the Zone 2.

Address Offset: 1Ah

Bit	R/W	Default	Description
7-0	R/W	64h	**Absolute Temperature LIMIT Value (ATLIMITV)** Same as the F1ATLIMITR register.

7.11.4.19 Zone Hysteresis Register (ZHYSR)

This register controls the amount that the Fan will turn off when the temperature is less than the Temperatur LIMIT value.

Address Offset: 1Bh

Bit	R/W	Default	Description
7-4	R/W	4h	**Zone Hysteresis Value (ZHYSV)** Used In SmartAuto fan mode. Bit 7-4 are assigned to Fan 2 and bit 3-0 are assigned to Fan 1. **Bits HYS value** 0h 0 degree C … … 5h 5 degree C … … Fh 15 degree C
3-0		4h	**Zone Hysteresis Value (ZHYSV)** Bit 3-0 are assigned to Fan 1 and others are the same as Bit7-0.

7.11.4.20 Fan 1 Temperature Record Register (F1TRR)

In a normal mode, the data written to this register represents the current temperature of Zone 1 when TBINM is cleared in ZTIER register.

Address Offset: 1Ch

Bit	R/W	Default	Description
7-0	R/W	5Ah	**Current Temperature Value (CTEMPV)** The value of the current temperature is represented as follows: **BITs 7-0 Current Temperature** 80h -128 degree C … … Ceh -50 degree C … … 00h 0 degree C … … 32h 50 degree C … … 7Fh 127 degree C

7.11.4.21 Fan 2 Temperature Record Register (F2TRR)

In a normal mode, the data written to this register represents the current temperature of the Zone 2. when TBINM is cleared in the ZTIER register.

Address Offset: 1Dh

Bit	R/W	Default	Description
7-0	R/W	5Ah	**Current Temperature Value (CTEMPV)** This register is the same as the F1TRR register.

7.11.4.22 Fan 1 Tachometer LSB Reading Register (F1TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 1 corresponds to TACH0.

Address Offset: 1Eh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bit 7-0 denote LSB Tachometer speed.

7.11.4.23 Fan 1 Tachometer MSB Reading Register (F1TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 1 corresponds to TACH0.

Address Offset: 1Fh

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bit 7-0 denote MSB Tachometer speed.

7.11.4.24 Fan 2 Tachometer LSB Reading Register (F2TLRR)

This register reflects the LSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 2 corresponds to TACH1.

Address Offset: 20h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer LSB Value (CTACHLV)** The value of bit 7-0 denote LSB Tachometer speed.

7.11.4.25 Fan 2 Tachometer MSB Reading Register (F2TMRR)

This register reflects the MSB value of the current tachometer of the Fan. The value is represented for each fan in a 16 bits. Fan 2 corresponds to TACH1.

Address Offset: 21h

Bit	R/W	Default	Description
7-0	R	-	**Current Tachometer MSB Value (CTACHMV)** The value of bit 7-0 denote MSB Tachometer speed.

7.11.4.26 Zone Interrupt Status Control Register (ZINTSCR)

The zone bits of the register indicate the temperature violation when the measured temperature violates the Limit in Temperature LIMIT register set for any of the two thermal zones.

Address Offset: 22h

Bit	R/W	Default	Description
7	R/WC	0b	**Zone 2 Limit Exceeded (Z2LE)** Set 1 when the temperature measured by Zone 2(remote) is larger than the limit set in Temperature Limit Register. Write 1 to this bit to cleared it and writing 0 is ignored.
6	R/WC	0b	**Zone 1 Limit Exceeded (Z1LE)** Set 1 when the temperature measured by Zone 1(internal) is larger than the limit set in Temperature Limit Register. Write 1 to this bit to cleared it and writing 0 is ignored.
5-0	-	0b	**Reserved**

7.11.4.27 Zone Temperature Interrupt Enable Register (ZTIER)

The register is used to enable the interrupt to the EC 8032 via INT7 when the zone temperature event occurs, either zone 1 limit exceeded or zone 2 limit exceeded.

Address Offset: 23h

Bit	R/W	Default	Description
7	R/W	0b	**Zone Temperature Event Enable (ZTEE)** This bit enables interrupt (INT7) to INTC if Z1LE and Z2LE bit in ZINTSCR register is set. 0: Disable 1: Enable

Bit	R/W	Default	Description
6	-	0b	**Temperature Bypass in Normal Mode (TBINM)** 1: Reserved 0: Temperature value is set from F1TRR or F2TRR written data. This bit is ignored in PWM test mode
5-2	-	0b	**Reserved**
1	R/W	0b	**PWM Clock Counter Enable (PCCE)** 1: Enable PWMs clock counter. Set this bit to 1 after all other registers have been set. 0: Disable PWMs clock counter
0	R/W	0b	**PWM Test Mode (PWMTM)** 1: PWM switches to a test mode 0: PWM works on a normal mode

7.11.4.28 Channel 4 Clock Prescaler Register (C4CPRS)

This register controls the cycle time and the minimal pulse width of channel 4-7.

Address Offset: 27h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV7-0)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and next register C4MCPRS defines the high byte.

7.11.4.29 Channel 4 Clock Prescaler MSB Register (C4MCPRS)

This register controls the cycle time and the minimal pulse width of channel 4-7.

Address Offset: 28h

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** Refer to previous register for detail.

7.11.4.30 Channel 6 Clock Prescaler MSB Register (C6MCPRS)

This register controls the cycle time and the minimal pulse width of channel 6.

Address Offset: 2Bh

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C6MCPRS defines the high byte.

7.11.4.31 Channel 6 Clock Prescaler Register (C6CPRS)

This register controls the cycle time and the minimal pulse width of channel 6.

Address Offset: 2Ch

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV7-0)** Refer to previous register for detail.

7.11.4.32 Channel 7 Clock Prescaler MSB Register (C7MCPRS)

This register controls the cycle time and the minimal pulse width of channel 7.

Address Offset: 2Dh

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV15-8)** PWM input clock is divided by the number of PSDV15-0 + 1 except 0 value. For example, the value of 0001h results in a divide by 2 and the value of FFFFh results in a divide by 65536 except 0 value. Set value 0 to disable clock prescaler divider. The contents of this register may be changed only when the PWM module is in a PWM inhibit mode. This register defines the low byte and the next register C7MCPRS defines the high byte.

7.11.4.33 Channel 7 Clock Prescaler Register (C7CPRS)

This register controls the cycle time and the minimal pulse width of channel 7.

Address Offset: 2Eh

Bit	R/W	Default	Description
7-0	R/W	00b	**Prescaler Divider Value (PSDV7-0)** Refer to the previous register for detail.

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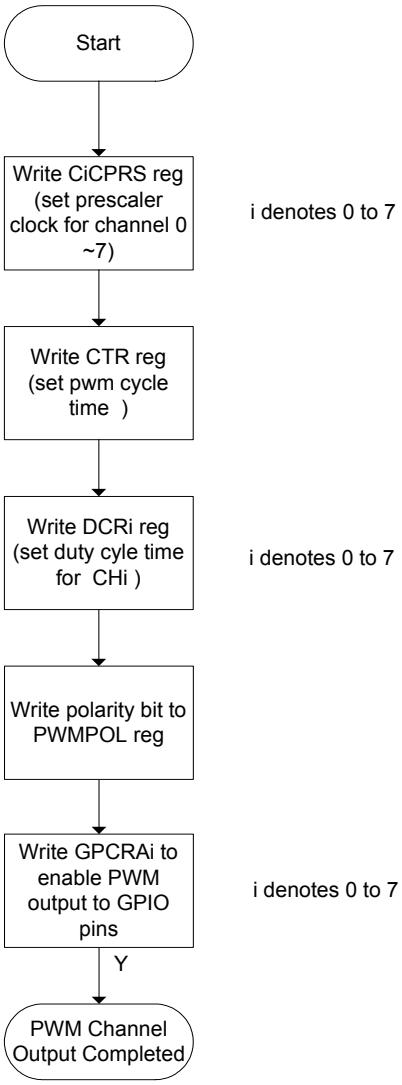

Figure 7-24. Program Flow Chart for PWM Channel Output

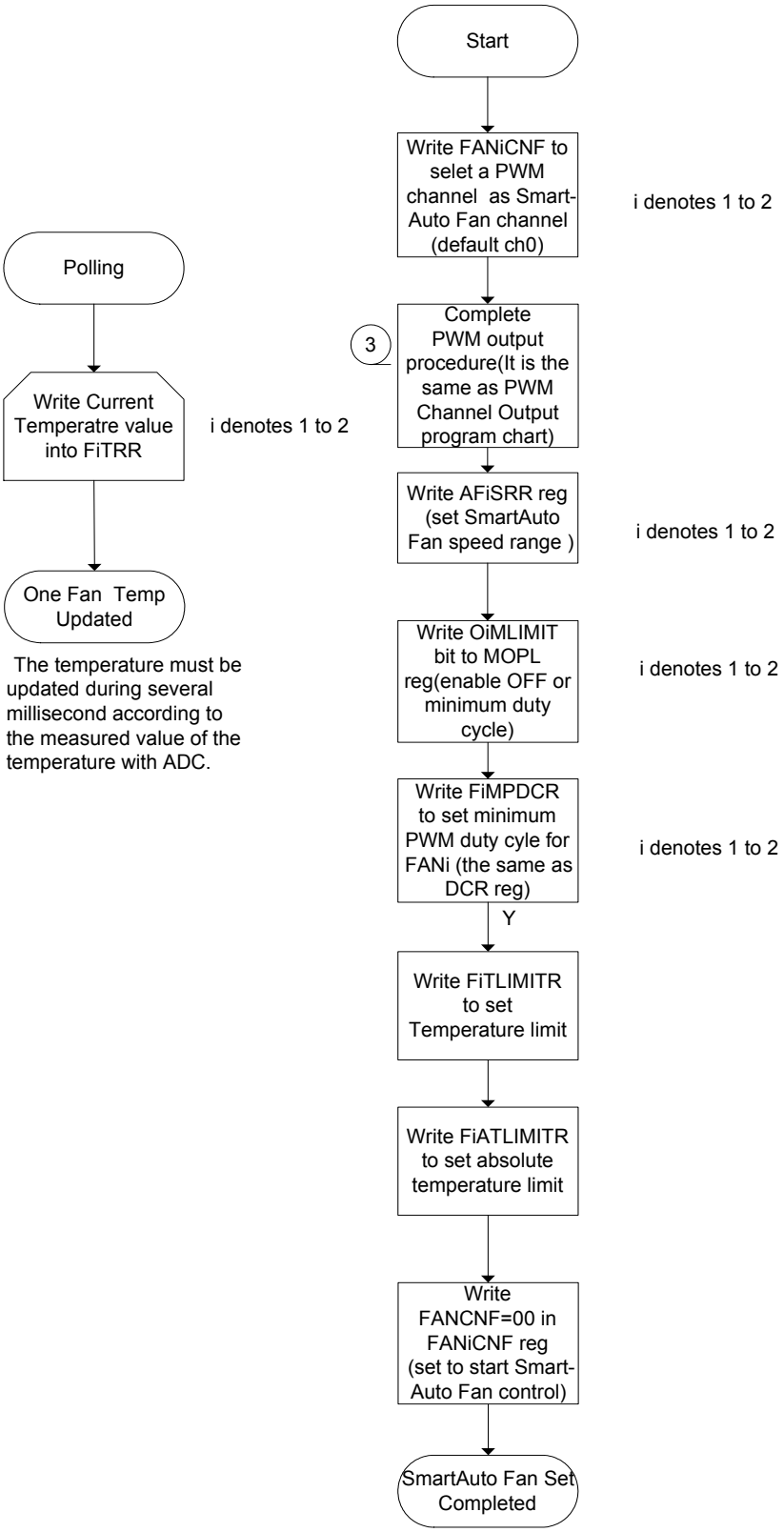

Figure 7-25. Program Flow Chart for SmartAuto Fan Channel Output

7.12 EC Access to Host Controlled Modules (EC2I Bridge)

7.12.1 Overview

The module enables EC access to PNPCFG, RTC and SWUC modules. It can access the host domain modules with host on alternate usage or take control of it and prevent any host from accessing that module.

7.12.2 Features

- Supports lock bit to prevent conflicts in host controlled module.
- Supports Super I/O I-Bus arbitration
- Supports Super I/O access lock violation indication

7.12.3 Functional Description

The EC2I bridge enables the EC to access the Host Controlled module registers (e.g., host configuration module(PNPCFG), RTC and SWUC), using the I-Bus which is arbitrated by I-Bus Arbiter to prevent fight from the host use the in Host Controlled module register. The bridge provides a lock bit to control the access of the Host Controlled modules. When the relative lock bit is cleared, the host is allowed to access to the Host Controlled modules registers. When the relative lock bit is set, the host is not allowed to access to the Host Controlled module registers (i.e., write operations are ignored and read operations return the unknown). Whenever if the host accesses to the locked register, a violation flag is set on the respective bit in the SIOLV register.
The EC should access the Host Controlled modules only after preventing host access to the module (using lock bits). The IB arbiter arbitrates IB usage between the host and EC. If an LPC transaction has started prior to the beginning of the EC transaction, EC waiting for the completion of the LPC transaction. If an EC transaction starts prior to an LPC transaction starts, the LPC translation needs waiting for the completion of the EC transaction.
The EC firmware may access the Host Controlled modules only when the VSTBY is on and the VCC is on and LPCCLK is active.

EC Read Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write 1 to CRIB bit in IBCTL register.
6. Read the CRIB bit in IBCTL until it returns 0.
7. Read the data from IHD register.

EC Write Operation from a Host Controlled module register, refer to the followings:
1. Set CSAE bit in IBCTL register.
2. Make sure that both CRIB and CWIB bits in IBCTL register are cleared.
3. Setting its enable bit in IBMAE register for access module, only one module can enable at a time.
4. Assign the offset of the register in the device in IHIOA register.
5. Write the data to IHD register, which begins a write transaction.
6. Read the CWIB bit in IBCTL until it returns 0, which represents that a write transaction has been finished.

For minimal conflict between host and EC in the use of Host Controlled modules, refer to the followings.

Notice for Read/Write Operation
1. The host is allowed to access the Host Controlled module only when the corresponding lock bit is cleared.
2. The firmware should not read any of the RTC read-volatile registers to prevent from host software access.

7.12.4 EC Interface Registers

The following set of registers is accessible only by the EC. The registers are maintained by VSTBY.

The registers are listed below and the base address is 1200h.

Table 7-21. EC View Register Map, EC2I

7	0	Offset
Indirect Host I/O Address.(IHIOA)		00h
Indirect Host Data (IHD)		01h
Lock Super I/O Host Access (LSIOHA)		02h
Super I/O Access Lock Violation (SIOLV)		03h
EC to I-Bus Modules Access Enable (IBMAE)		04h
I-Bus Control (IBCTL)		05h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.12.4.1 Indirect Host I/O Address Register (IHIOA)

This register defines the host I/O address for read or write transactions initializated by EC from/to the Host Controlled modules. The I/O address is an offset from the LSB bits of the address of the host controlled module. The accessed module is selected using the EC to IB Modules Access Enable Register (IBMAE).

Address Offset: 00h

Bit	R/W	Default	Description
7-0	R/W	00b	**Indirect Host I/O Offset (IHIOO)** These bits indicate the offsets within the device range are allowed.

7.12.4.2 Indirect Host Data Register (IHD)

This register holds host data for read or write transactions initializated by EC from/to the Host Controlled modules.

Address Offset: 01h

Bit	R/W	Default	Description
7-0	R/W	00b	**Indirect Host Data (IHDA)**

7.12.4.3 Lock Super I/O Host Access Register (LSIOHA)

This register controls locking of host access to the Host Controlled modules.

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/W	0b	**Lock Real-Time Clock (RTC) Host Access (LKRTCHA)** 0: Host access to the RTC registers is enabled 1: Host access to the RTC registers is disabled
0	R/W	0b	**Lock PNPCFG Registers Host Access (LKCFG)** 0: Host access to the PNPCFG Registers is enabled 1: Host access to the PNPCFG Registers is disabled

7.12.4.4 Super I/O Access Lock Violation Register (SIOLV)

This register provides an error indication when a host lock violation occurs on Host Controlled modules access.

Address Offset: 03h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1	R/WC	0b	**Real-Time Clock (RTC) Lock Violation (RTCLV)** 0: There is no lock violation when the host accesses RTC registers. 1: When the host accesses the RTC but LKRTCHA bit in LSIOHA register is set, this bit is set to indicate a violation and can be write-1-clear.
0	R/WC	0b	**PNPCFG Register Lock Violation (CFGLV)** 0: There is no lock violation when host access PNPCFG registers. 1: when the host access PNPCFG register but LKCFG bit in LSIOHA register is set, this bit is set to indicate a violation and can be write-1-clear.

7.12.4.5 EC to I-Bus Modules Access Enable Register (IBMAE)

This register enables EC access to the Host Controlled modules. Only one of the bits in this register may be set at a time.

Address Offset: 04h

Bit	R/W	Default	Description
7-3	-	0h	**Reserved**
2	R/W	0b	**Mobile System Wake-Up Control (SWUC) Access Enable (SWUCAE)** 0: EC access to the SWUC Registers is disabled. 1: EC access to the SWUC Registers is enabled.
1	R/W	0b	**Real-Time Clock (RTC) EC Access Enable (RTCAE)** The RTC has two selection signals defined in its configuration space. A1 of the offset is used to decode the two selection (when A1 is 0, the index 70h and 71h is selected; when A1 is 1, the index 72h and 73h is selected). 0: EC access to the RTC Registers is disabled. 1: EC access to the RTC Registers is enabled.
0	R/W	0b	**PNPCFG Register EC Access Enable (CFGAE)** 0: EC access to the PNPCFG Registers is disabled 1: EC access to the PNPCFG Registers is enabled.

7.12.4.6 I-Bus Control Register (IBCTL)

This register allows the EC to the I-Bus Bridge operation.

Address Offset: 05h

Bit	R/W	Default	Description
7-4	-	0h	**Reserved**
3	R/W	0b	**Real-Time Clock (RTC) Master Reset (RTCMR)** 0: Not reset the RTC module 1: Generates a reset pulse to the RTC module. This bit is cleared automatically after the reset pulse is completed. Writing 0 to this bit is ignored.

Bit	R/W	Default	Description
2	R	0b	**EC Write to IB (CWIB)** 0: No write operation is detected 1: when write data to the IHD register. It is cleared when the write to the IB is completed.
1	R/W	0b	**EC Read from IB (CRIB)** Set 1 to begin a read from the IB; the read operation is based on the setting in IBMAE register. A write of 0 to this bit is ignored. This bit is cleared when the read operation is completed and represents the data in IHD register is available.
0	R/W	0b	**EC to IB Access Enabled (CSAE)** 0: EC access to the IB bus is disabled (default) 1: EC access to the IB bus is enabled. The module to be accessed is selected in the IBMAE register.

7.12.5 EC2I Programming Guide

The read/write cycles PNPCFG, RTC and SWUC modules via EC2I are only valid when VCC is supplied. It means that such cycles may be executed after every VCC power-on.

Program flow chart for EC2I Read

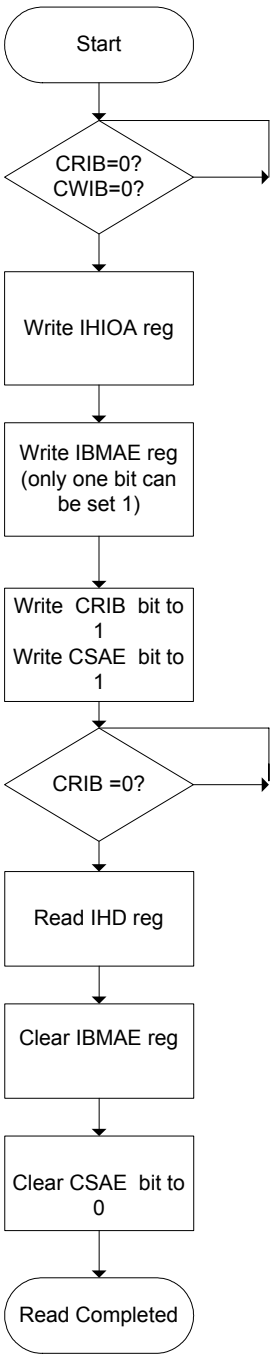

Figure 7-26. Program Flow Chart for EC2I Read

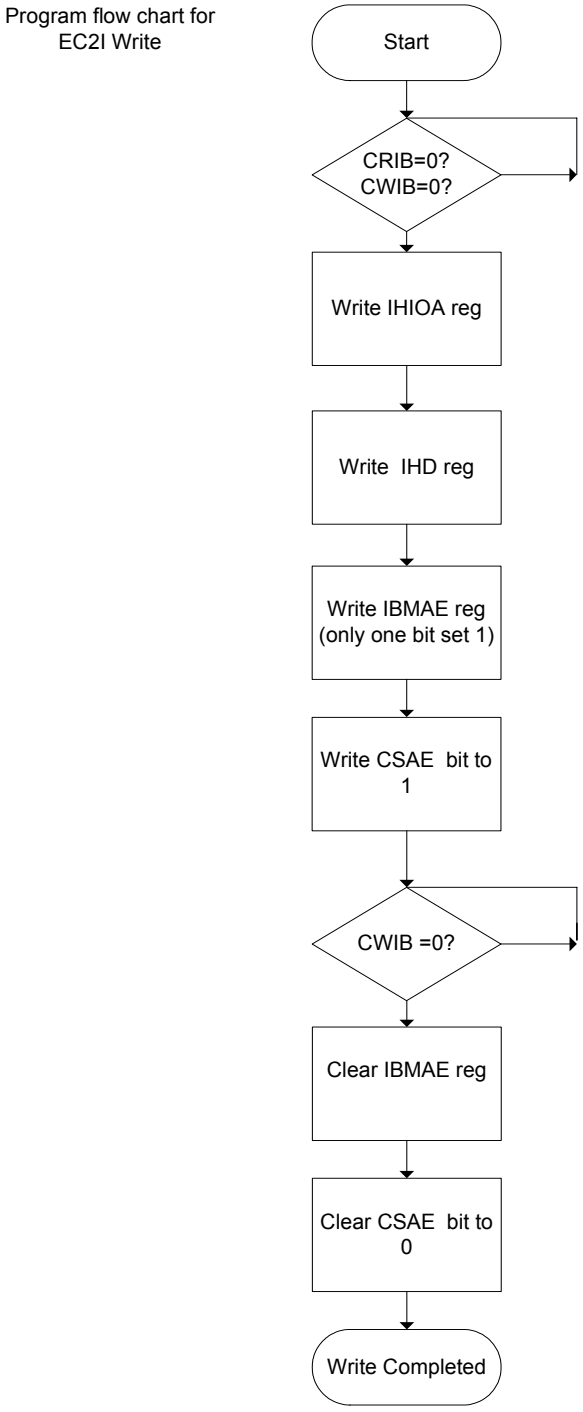

Figure 7-27. Program Flow Chart for EC2I Write

7.13 Hardware Strap (HWS)

7.13.1 Overview

The module simply provides read-only registers and contains hardware strap values sampled after VSTBY power up reset.

7.13.2 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 1F00h.

Table 7-22. EC View Register Map, HWS

7	0	Offset
Hardware Strap Register (HWSR)		00h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.13.2.1 Hardware Strap Register (HWSR)

Address Offset: 00h

Bit	R/W	Default	Description
7-3	-	-	**Reserved**
2-1	R	-	**I/O Base Address Value (BADDRV)** Sampled at VSTBY power up reset. 00: The register pair to access PNPCFG are 2Eh and 2Fh 01: The register pair to access PNPCFG are 4Eh and 4Fh 10: The register pair to access PNPCFG are determined by EC domain registers SWCBAHR and SWCBALR 11: Reserved
0	R	-	**Share Host BIOS Memory Value (SHBMV)** Sampled at VSTBY power up reset. 0: disable shared memory with host BIOS 1: enable shared memory with host BIOS

7.14 External Timer and External Watchdog (ETWD)

7.14.1 Overview

Besides the internal timer 0,1,2 and WDT inside the 8032, there are External Timer/WDT outside the 8032. External Timer/WDT is based on RTC 32.768 KHz clock and still works when EC is in Idle/Doze/Sleep mode. External timer is recommend to replace internal timer for periodical wakeup task.

External Timer/WDT have less power consumption than internal Timer/WDT due to the low frequency.

ETWD module cannot count external signal sources from pins. If the firmware wants to count external signal sources from pins, refer to TMRI0, TMRI1, TACH0 and TACH1. TMRI0/TMRI1 are used as Timer1/2 sources of 8032 and TACH0/1 are tachometer inputs of PWM.

7.14.2 Features

- 32.768 kHz, 1.024 kHz and 32 Hz prescaler for External Timer
- 16-bit count-down External Timer
- 16-bit count-down External WDT

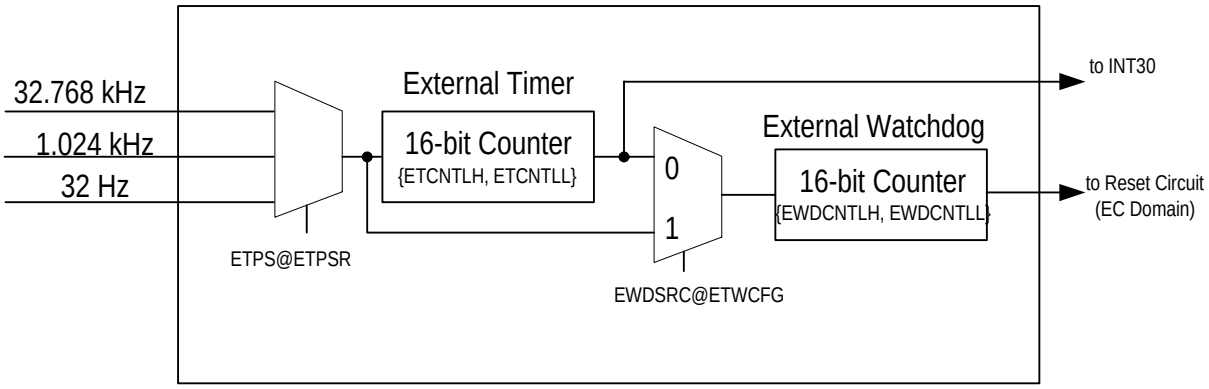

Figure 7-28. Simplified Diagram

7.14.3 Functional Description

7.14.3.1 External Timer Operation

The External Timer is a 16-bit counter down timer. Its clock source is based on RTC 32.768 KHz and can be selected by a prescaler defined at ETPS field in ETPSR register.

The count number is defined in ETCNTLHR and ETCNTLLR registers. External Timer is stopped after reset and started after writing data to ETCNTLLR register and never stops until reset. It asserts an interrupt to INTC when it counts to zero in every time.

The External Timer re-starts when
- it counts to zero periodically.
- writing data to ETCNTLL register.
- writing 1 to ETRST bit in ETWCTRL register.

External Timer asserts periodical interrupt to EC 8032 via INT30 of INTC.

7.14.3.2 External WDT Operation

External WDT is a 16-bit counter down timer. Its clock source is either External Timer output or the same clock source of External Timer, and it is controlled by EWDSRC bit in ETWCFG register. See also ETPSR register. The count number is defined in EWDCNTL register. External WDT is stopped after reset and started after writing data to EWDCNTL register and cannot be stopped until reset. It asserts an External Watchdog Reset to EC domain when it counts to zero. External WDT requires starting External Timer regardless of EWDSRC field in ETWCFG register. External WDT cannot be started until External Timer is started.

The External WDT re-starts when it is touched by the firmware.
There are two following ways to touch (re-start) External WDT:

- Writing data to EWDCNTL register (if LEWDCNTL bit in ETWCFG register is not set)
- Writing 5Ch to EWDKEYR register, called key-match

External WDT asserts an External Watchdog Reset to EC domain when

- it counts to zero.
- writing data except 5Ch to EWDKEYR register.

7.14.4 EC Interface Registers

The following set of the registers is accessible only by the EC. They are listed below and the base address is 1F00h.

Table 7-23. EC View Register Map, ETWD

7	0	Offset
External Timer/WDT Configuration Register (ETWCFG)		01h
External Timer Prescaler Register (ETPSR)		02h
External Timer Counter High Byte (ETCNTLHR)		03h
External Timer Counter Low Byte (ETCNTLLR)		04h
External Timer/WDT Control Register (ETWCTRL)		05h
External WDT Counter High Byte (EWDCNTLHR)		09h
External WDT Counter Low Byte (EWDCNTLLR)		06h
External WDT Key Register (EWDKEYR)		07h
Reset Scratch Register (RSTSCR)		08h
Chip Version (ECHIPVER)		10h

For a summary of the abbreviations used for the register type, see “Register Abbreviations and Access Rules”

7.14.4.1 External Timer/WDT Configuration Register (ETWCFG)

Address Offset: 01h

Bit	R/W	Default	Description
7	-	0h	**Reserved**
6	R/W	0b	**External WDT Stop Mode (EWDSM)** 1: Stop counting WDT when LPC memory/FWH cycles are processing. 0: Otherwise
5	R/W	0b	**External WDT Key Enabled (EWDKEYEN)** 1: Enabled the key match function to touch the WDT 0: Otherwise
4	R/W	0b	**External WDT Clock Source (EWDSRC)** 1: Select clock after prescaler of the external timer 0: Select clock from the output of the external timer

Bit	R/W	Default	Description
3	R/W	0b	**Lock EWDCNTL Register (LEWDCNTL)** 1: Writing to EWDCNTL is ignored, and this bit can't be cleared until reset. 0: Writing to EWDCNTL is allowed.
2	R/W	0b	**Lock ETCNTLx Registers (LETCNTL)** 1: Writing to ETCNTLH/ETCNTL is ignored, and this bit can't be cleared until reset. 0: Writing to ETCNTLH/ETCNTL is allowed.
1	R/W	0b	**Lock ETPS Register (LETPS)** 1: Writing to ETPS is ignored, and this bit can't be cleared until reset. 0: Writing to ETPS is allowed.
0	R/W	0b	**Lock ETWCFG Register (LETWCFG)** 1: Writing to ETWCFG itself is ignored, and this bit can't be cleared until reset. 0: Writing to ETWCFG itself is allowed.

7.14.4.2 External Timer Prescaler Register (ETPSR)

Address Offset: 02h

Bit	R/W	Default	Description
7-2	-	0h	**Reserved**
1-0	R/W	00b	**External Timer Prescaler Select (ETPS)** These bits control the clock input source to the external timer. 00b: 32.768 KHz 01b: 1.024 KHz 10b: 32 Hz 11b: Reserved Note the prescaler will not output clock until a data written to ETCNTLLR register.

7.14.4.3 External Timer Counter High Byte (ETCNTLHR)

Address Offset: 03h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer Counter High Byte (ETCNTLH)** Define the count number of high byte of the 16-bit count-down timer.

7.14.4.4 External Timer Counter Low Byte (ETCNTLLR)

Address Offset: 04h

Bit	R/W	Default	Description
7-0	R/W	FFh	**External Timer Counter Low Byte (ETCNTLL)** Define the count number of low byte of the 16-bit count-down timer. The external timer starts or re-starts after writing this register.

7.14.4.5 External Timer/WDT Control Register (ETWCTRL)

Address Offset: 05h

Bit	R/W	Default	Description
7-2	-	00h	**Reserved**

Bit	R/W	Default	Description
1	R	0b	**External Timer Terminal Count (ETTC)** 1: Indicates the external timer has counted down to zero, and it is cleared after reading it. 0: Otherwise Writing to this bit is ignored.
0	W	-	**External Timer Reset (ETRST)** Writing 1 forces the external timer re-start. Writing 0 is ignored. Read always returns zero.

7.14.4.6 External WDT Counter High Byte (EWDCNTLHR)

Address Offset: 09h

Bit	R/W	Default	Description
7-0	R/W	00h	**External WDT Counter High Byte (EWDCNTL)** Define the count number of high byte of the 16-bit count-down WDT.

7.14.4.7 External WDT Counter (EWDCNTLLR)

Address Offset: 06h

Bit	R/W	Default	Description
7-0	R/W	0Fh	**External WDT Counter Low Byte (EWDCNTLL)** Define the count number of low byte of the 16-bit count-down WDT.

7.14.4.8 External WDT Key Register (EWDKEYR)

Address Offset: 07h

Bit	R/W	Default	Description
7-0	W	-	**External WDT Key (EWDKEY)** External WDT is re-started (touched) is writing 5Ch to this register. Writing with other values causes an External Watchdog Reset. This function is enabled by EDWKEYEN bit. Read returns unpredictable value.

7.14.4.9 Reset Scratch Register (RSTSCR)

This register is used to detect the latest reset source.

Address Offset: 08h

Bit	R/W	Default	Description
7-3	R/W	0b	**Reserved**
2	R/W	0b	**External WDT Reset Scratch Bit (EWRSTSB)** This bit is reset by External Watchdog Reset and VSTBY Power-Up Reset only. Read this bit returns the last written value.
1	R/W	0b	**Internal WDT Reset Scratch Bit (IWRSTSB)** This bit is reset by Internal Watchdog Reset and VSTBY Power-Up Reset only. Read this bit returns the last written value.

Bit	R/W	Default	Description
0	R/W	0b	**Warm Reset Scratch Bit (WRSTSB)** This bit is reset by Warm Reset and VSTBY Power-Up Reset only. Read this bit returns the last written value.

7.14.4.10 Chip Version (ECHIPVER)

This register contains revision ID of this chip.
The content of this EC side register is the same as CHIPVER register in host side.

Address Offset: 08h

Bit	R/W	Default	Description
7-0	R	21h	**Chip Version (ECHIPVER)**

7.15 Print Port (PP)

7.15.1 Overview

IT8510 supports IEEE 1284 parallel port interface to allow in-system programming regardless of running firmware code.

7.15.2 Features

- ISP via parallel port interface on existed KBS connector
- Fast flash programming with software provided by ITE
- Programming software supports EPP/SPP mode

7.15.3 Functional Description

7.15.3.1 KBS Connection with Printer Port Connector

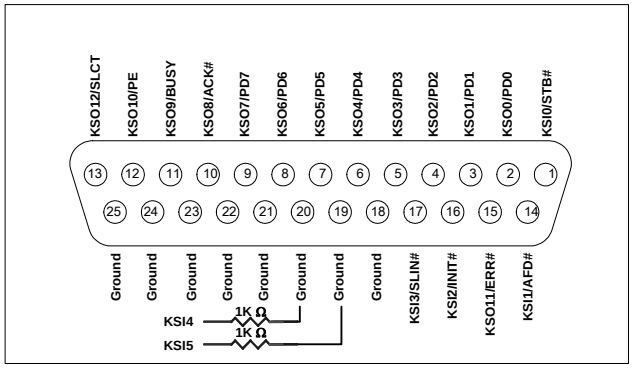

Figure 7-29. Parallel Port Female 25-Pin Connector

7.15.3.2 In-System Programming Operation

In-system programming takes place when VSTBY is supplied (other power is don't-care) and both IT8510 and the flash are soldered on PCB. Parallel port interface occupies the same interface pins with KBS to use the existing KBS connector.

IT8510 enters in-system programming mode if it detects parallel port signals when VSTBY power on or hardware strap pin PPEN is pulled high.

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8. DC Characteristics

(VSTBY, VCC =3.3V±0.3V, AVCC =3.3V±0.15V, VBAT = 2.3~3.3V, Ta=0°C to 70°C)

Absolute Maximum Ratings*

Applied Voltage of VSTBY, VCC, AVCC,

VBAT……..... 0.3V to +3.6V

Input Voltage of 3.3V Interface..... -0.3V to VCC +0.3V

Tcase..... 0°C to +70°C

Storage Temperature .....-40°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Ta=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
V_{IL}	Input Low Voltage	-0.3V	—	VCC x 0.3	VCC=3.0 - 3.6V
V_{IH}	Input High Voltage	VCC x 0.7	—	VCC+ 0.3V	VCC=3.0 - 3.6V
V_{IH}	Input High Voltage (5V tolerant pad)	VCC x 0.7	—	6.3V	VCC=3.0 - 3.6V
V_{OL}	Output Low Voltage	—	—	0.4	I_{OL}= -2, -4, -6, -8mA
V_{OH}	Output High Voltage	2.4	—	—	I_{OH}= 2, 4, 6, 8mA
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.9	1.2	—	
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—	2.1	2.5	
I_{IL}	Input leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	40KΩ	75KΩ	190KΩ	V_I= 0V
R_{pd}	Input Pull-Down Resistance	40KΩ	75KΩ	190KΩ	V_I= VCC
Cin	Input Capacitance	—	2.8pF	—	
Cout	Output Capacitance	2.7pF	—	4.9pF	
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	

Table 8-1. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
I_{SLEEP}	VSTBY supply current	—	50μA	—	Internal pull are disabled VIL = GND VIH = VSTBY No load
I_{BAT}	VBAT supply current	—	1.7μA	2.4μA	VSTBY and VCC are not supplied

9. AC Characteristics

Figure 9-1. Reset Timing

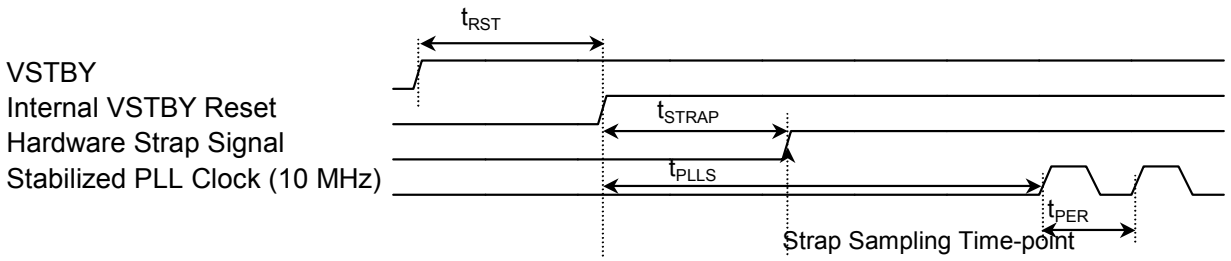


Table 9-1. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RST}	Reset time from VSTBY@2.5V to rising edge of internal reset	—	4.7	—	μs
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS}	PLL stabilization time NOTE	—	—	4.5	ms
t_{PER}	PLL clock period	—	100	—	ns

NOTE: The 32.768KHz crystal output has been stabilized.

Figure 9-2. Warm Reset Timing

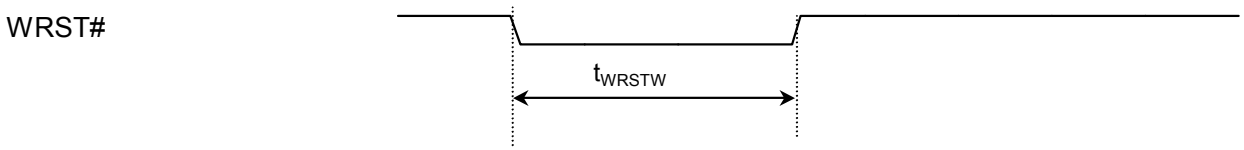


Table 9-2. Warm Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	μs

Figure 9-3. Wakeup from Doze Mode Timing

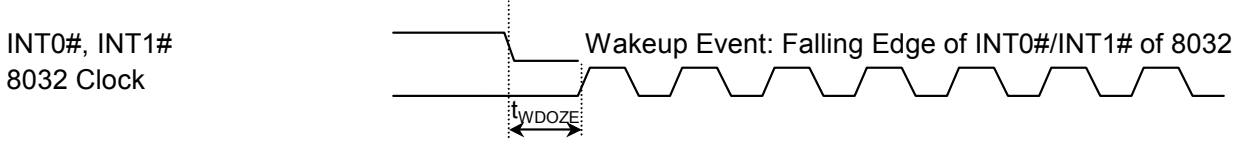


Table 9-3. Wakeup from Doze Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDOZE}	Doze wakeup time from falling edge of INT0#/INT1# to rising edge of first 8032 clock.	—	—	2 / (EC Clock Freq)	—

Note: (EC Clock Freq) is normally EC Clock 10 MHz and may be divided by CFSELR register.

Figure 9-4. Wake Up from Sleep Mode Timing

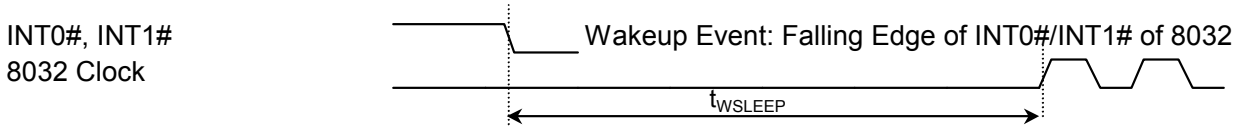


Table 9-4. Wake Up from Sleep Mode AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WSLEEP}	Sleep wakeup time from falling edge of INT0#/INT1# to rising edge of first 8032 clock.	—	—	4.2	ms

Figure 9-5. Asynchronous External Wakeup/Interrupt Source Edge Detected Timing

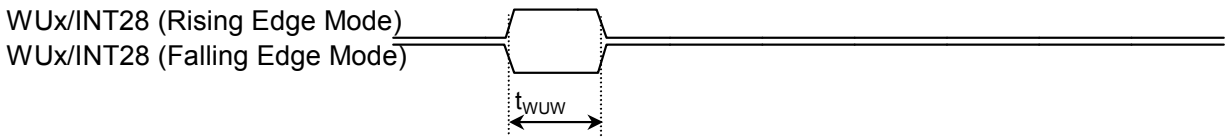


Table 9-5. Asynchronous External Wakeup/Interrupt Source Edge Detected AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{wuw}	Wakeup source pulse width	—	1	—	ns

Figure 9-6. LPC and SERIRQ Timing

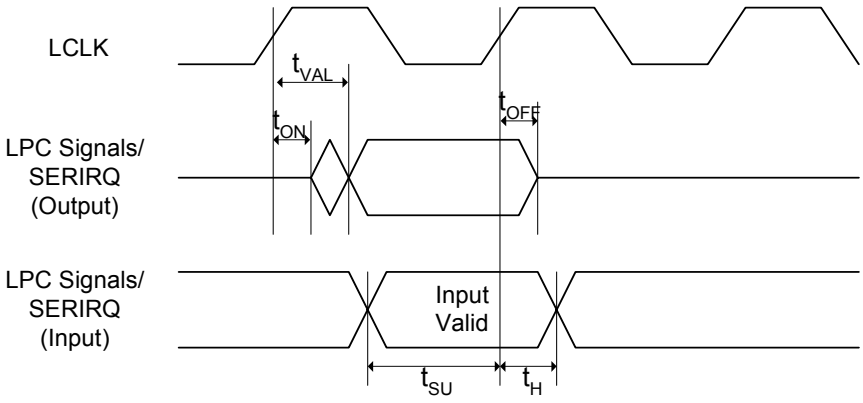


Table 9-6. LPC and SERIRQ AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{ON}	Float to Active Delay	3	—	—	ns
t_{VAL}	Output Valid Delay	—	—	12	ns
t_{OFF}	Active to Float Delay	—	—	20	ns
t_{SU}	Input Setup Time	7	—	—	ns
t_{H}	Input Hold Time	0	—	—	ns

Figure 9-7. SWUC Wake Up Timing

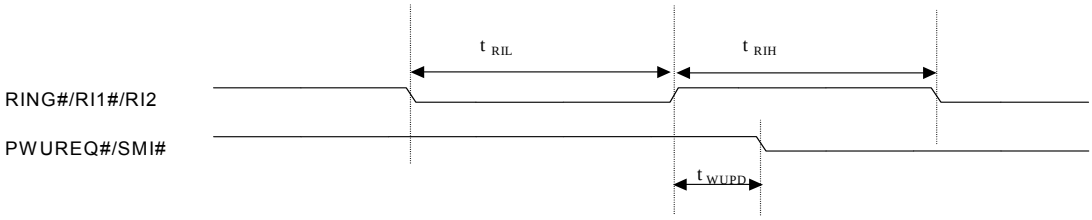


Table 9-7. SWUC Wake Up AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RIL}	RING#, RI1# , RI2# Low Time	10	—	—	ns
t_{RIh}	RING#, RI1# , RI2# High Time	10	—	—	ns
t_{WUPD}	Wake Up propagation delay time	—	20	—	ns

Figure 9-8. Flash Read Cycle Timing

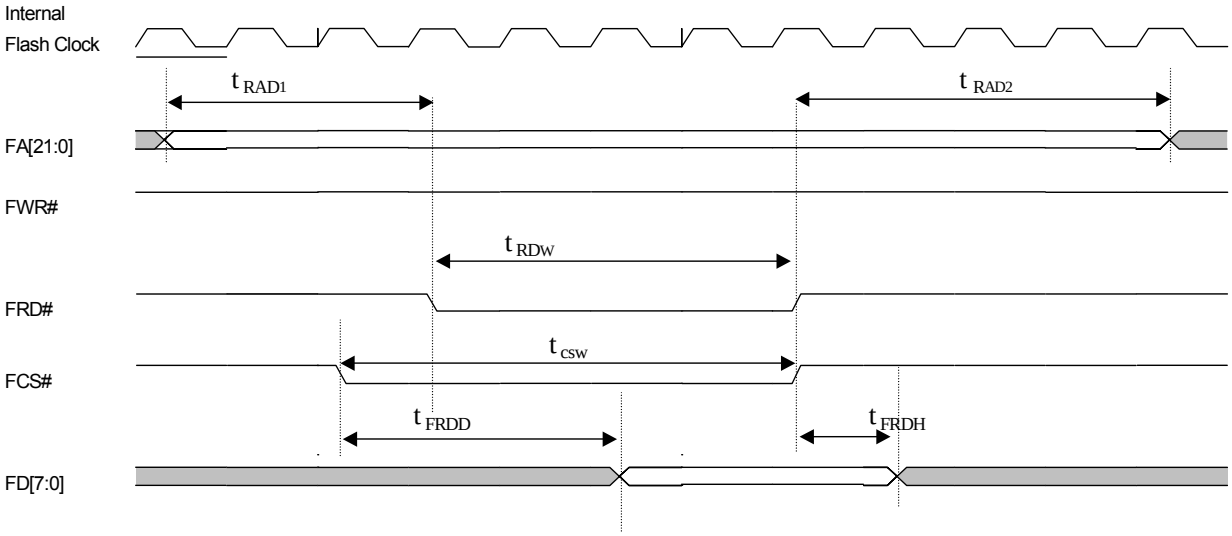


Table 9-8. Flash Read Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RAD1}	Read address delay time1	—	1	—	T NOTE2
t_{RAD2}	Read address delay time2	—	1	—	T NOTE2
t_{CSW}	Read chip select width time	2	—	—	T NOTE2
t_{RDW}	Read data output enable signal width	1	—	—	T NOTE2
t_{FRDD}	Read data output delay	—	—	80 NOTE1	ns
t_{FRDH}	FRD data hold time	0	—	—	ns

Note 1: "Read Cycle Time" and "Write Cycle Time" of the flash/EPROM have to be faster than or equal to t_{FRDD}.
2: T is the clock period and it is (FTDIV +1) / (EC Clock Frequency)
(EC Clock Frequency) is normally 10 MHz and may be divided by CFSELR register.

Figure 9-9. Flash Write Cycle Timing

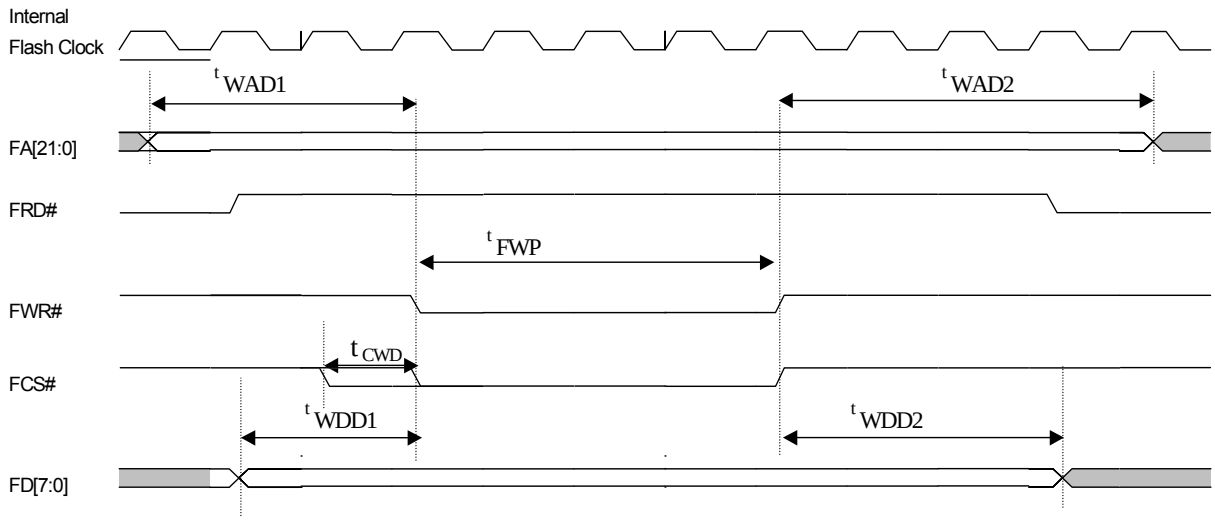


Table 9-9. Flash Write Cycle AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WAD1}	Write address delay time1	—	1	—	T NOTE2
t_{WAD2}	Write address delay time2	—	1	—	T NOTE2
t_{FWP}	Write width pulse time	1	—	—	T NOTE2
t_{CWD}	Chip Select to Write delay time	0	1 NOTE1	—	T NOTE2
t_{WDD1}	Write data delay time1	—	1	—	T NOTE2
t_{WDD2}	Write data delay time2	—	1	—	T NOTE2

Note1: t_{CWD} = 0 ns when EWR setting to 1 (Early write), t_{CWD} = 1 T when EWR setting to 0 (Late write)
2: T is the clock period and it is (FTDIV +1) / (EC Clock Frequency)
(EC Clock Frequency) is normally 10 MHz and may be divided by CFSELR register.

Figure 9-10. PWM Output Timing

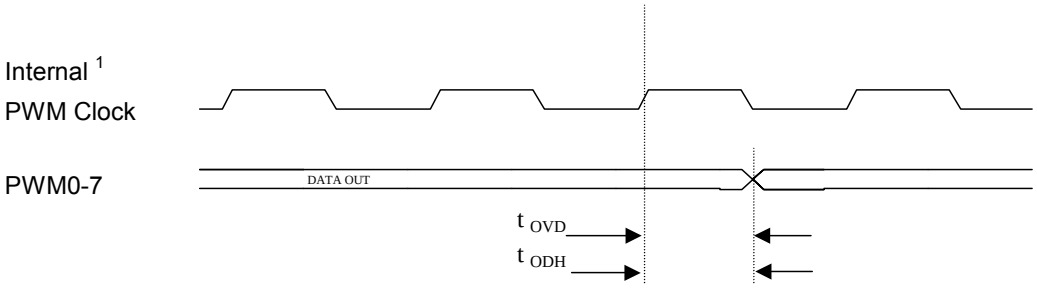


Table 9-10. PWM Output AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{OVD}	PWM output valid delay time	—	—	0.5	T^{NOTE1}
t_{ODH}	PWM output hold time	0	—	—	ns

Note 1: T is one time unit and its length is equal to the EC clock period X C0CPRS +1 (ns) for CH0~3, or X C4CPRS +1 (ns) for CH4~7.

Figure 9-11. PMC SMI#/SCI# Timing

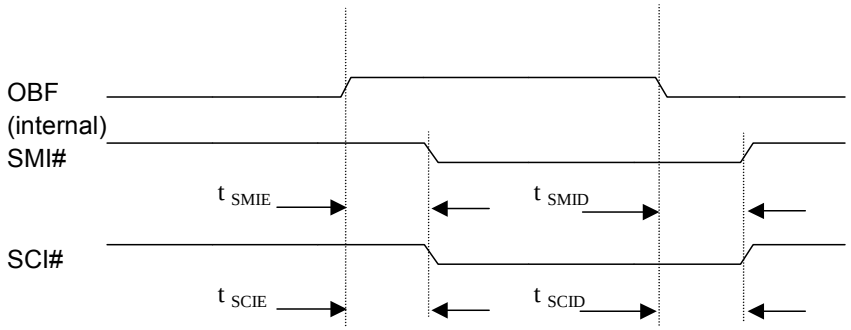


Table 9-11. PMC SMI#/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SMIE}	OBF asserted to SMI# asserted time	—	10	—	ns
t_{SMID}	OBF de-asserted to SMI# de-asserted time	—	5	—	ns
t_{SCIE}	OBF asserted to SCI# asserted time	—	10	—	ns
t_{SCID}	OBF de-asserted to SCI# de-asserted time	—	5	—	ns

Figure 9-12. PMC IBF/SCI# Timing

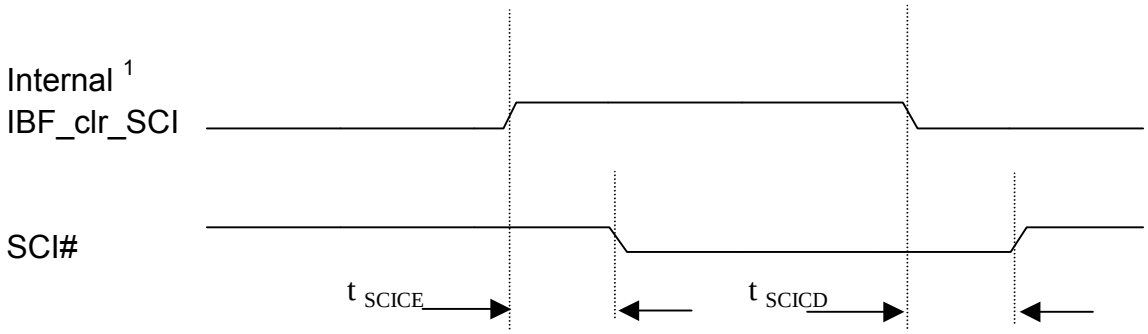


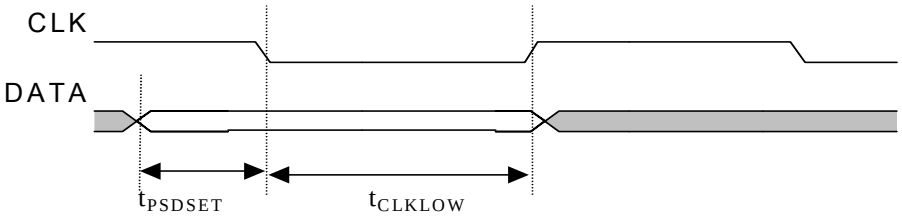
Table 9-12. PMC IBF/SCI# AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCICE}	IBF_clr_SCI asserted to SCI# asserted time	—	70	—	ns
t_{SCICD}	IBF_clr_SCI de-asserted to SCI# de-asserted time	—	40	—	ns

Note 1: IBF_clr_SCI means the invert signal of IBF, IBF_clr_SCI set to one when EC read PMDI or PMDISCI.

Figure 9-13. PS/2 Receive/Transmit Timing

Receive:



Transmit:

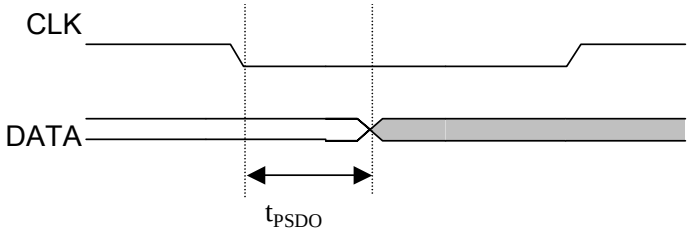


Table 9-13. PS/2 Receive/Transmit AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{PSDSET}	DATA line input set up time	1	—	—	ns
t_{CLKLOW}	CLK line low time	1	—	—	μs
t_{PSDO}	DATA line output data time	—	—	1	μs

Figure 9-14. SMBUS Timing

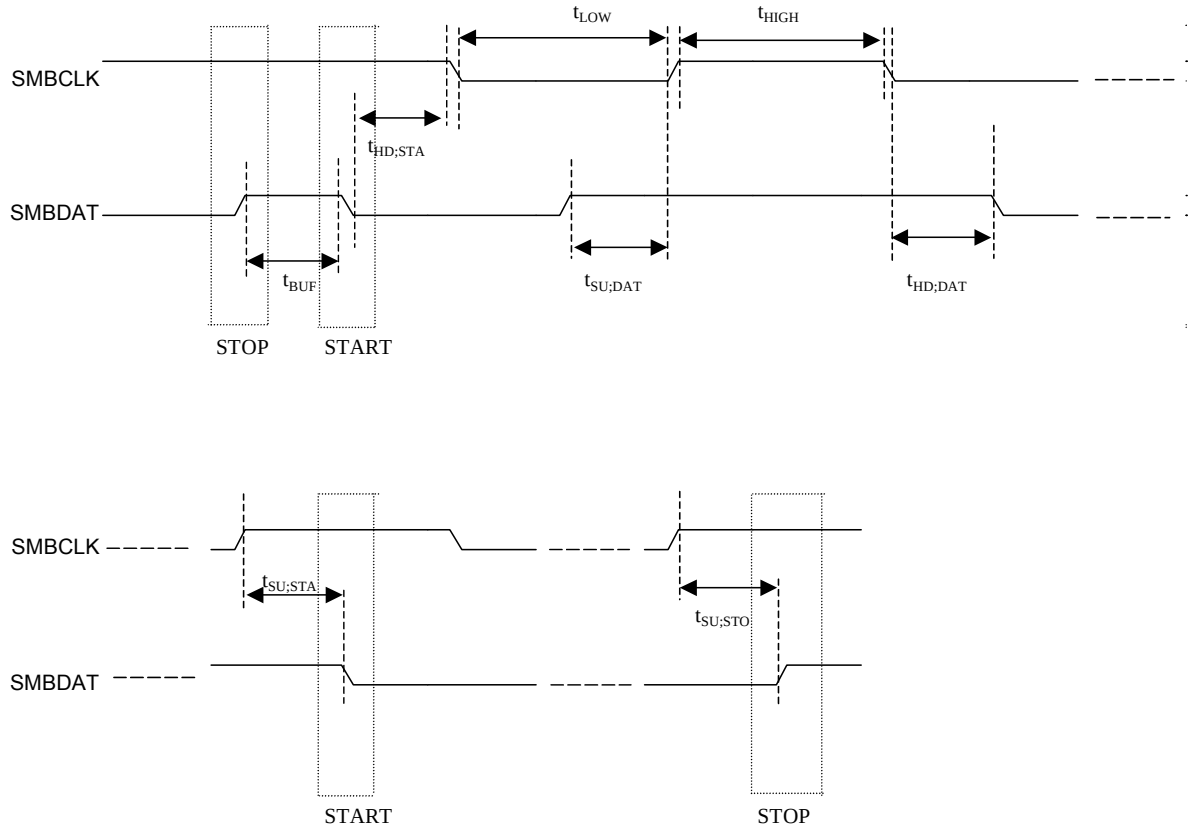


Table 9-14. SMBUS AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{BUF}	Bus free time between Stop and Start condition	4.7	—	—	μs
$t_{HD;STA}$	Hold time after (Repeated) Start condition. After this period, the first clock is generated.	4.0	—	—	μs
t_{LOW}	Clock low period	4.7	—	—	μs
t_{HIGH}	Clock high period	4.0	—	50	μs
$t_{SU;DAT}$	Data setup time	250	—	—	ns
$t_{HD;DAT}$	Data hold time	300	—	—	ns
$t_{SU;STA}$	Repeated Start condition setup time	4.7	—	—	μs
$t_{SU;STO}$	Stop condition setup time	4.0	—	—	μs

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10. Analog Device Characteristics

Table 10-1. ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Resolution	—	—	10		Bit
Integral Non-linearity Error (INL)	ADC0-9	—	—	±4	LSB
Differential Non-linearity Error (DNL)	ADC0-9	—	—	±4	LSB
Offset Error	ADC0-9	—	—	±4	LSB
Gain Error	ADC0-9	—	—	±4	LSB
External Input Accuracy	ADC0-9	—	—	±4	LSB
ADC Input Voltage Range	—	0	—	3	V
ADC Input Leakage Current	ADC0-9: 0 ≦ Vin ≦ AVCC	—	±1	—	μA
ADC Input Resistance	—	4	—	—	MΩ
ADC Input Capacitance	—	—	—	8	pF
ADC Clock Frequency	—	—	0.5	—	MHz
Voltage Conversion Delay	—	16	512	1000	μs
Voltage Conversion Time	—	—	3.6	—	ms

Table 10-2. DAC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Resolution	—	—	8	—	Bit
Integral Non-linearity Error (INL)	AVCC = 3.3V	—	—	±1	LSB
Differential Non-linearity Error (DNL)	AVCC = 3.3V	—	—	±0.5	LSB
Offset Error	AVCC = 3.3V	—	—	±1	LSB
Gain Error	AVCC = 3.3V	—	—	±1	LSB
DAC Output Voltage Range	—	0	—	AVCC	V
DAC settling time	C_{load} = 50pF	—	—	1	μs
DAC Output Resistance	0 ≦ Vout ≦ AVCC	3	—	800	Ω
DAC Output Capacitance	—	—	6.5	—	pF

Note: C_{load} = (DAC Output Capacitance) + (External Load Capacitance)

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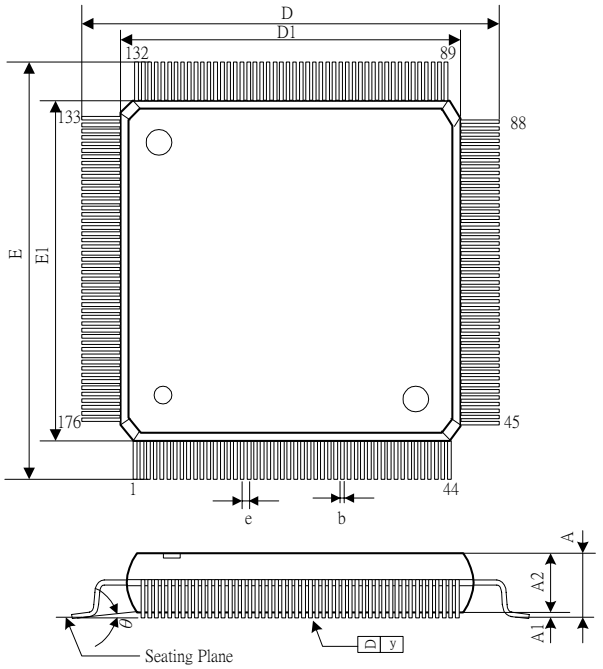
11. Package Information

LQFP 176L Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.005	—	0.008	0.12	—	0.20
D	1.018	1.024	1.030	25.85	26.00	26.15
D1	0.941	0.945	0.949	23.90	24.00	24.10
E	1.018	1.024	1.030	25.85	26.00	26.15
E1	0.941	0.945	0.949	23.90	24.00	24.10
e	0.020 BSC			0.50 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
y	—	—	0.004	—	—	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Note:

1. Dimensions D1 and E1 do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter.

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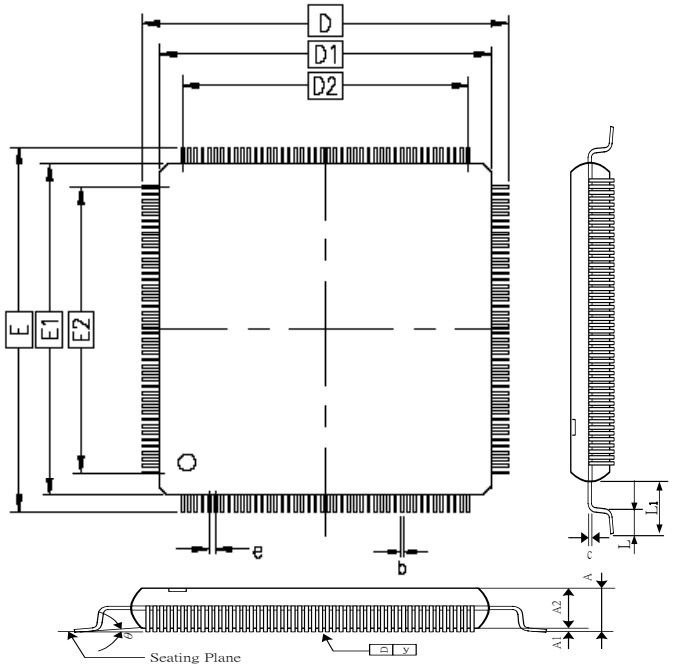
TQFP 176L Outline Dimensions unit: inches/mm

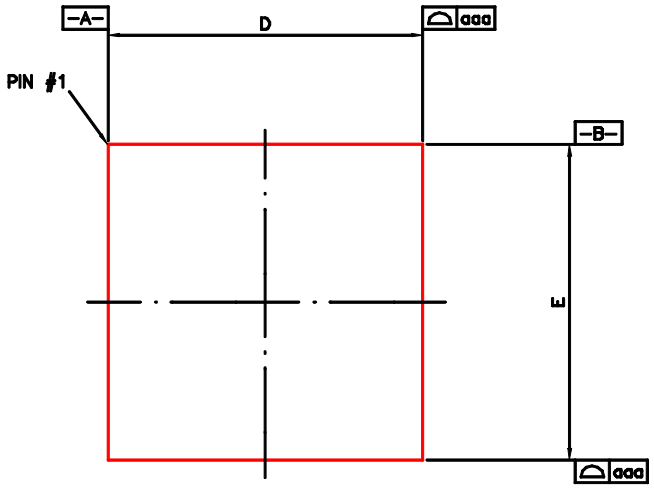


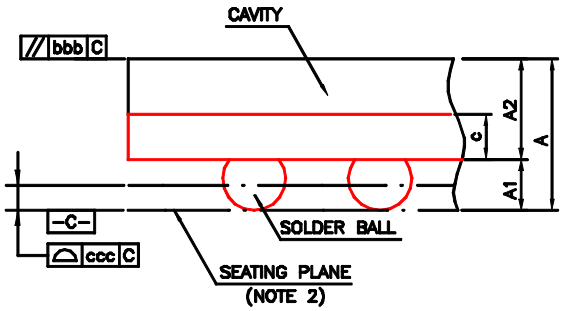
Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.039	0.043	0.047	1.00	1.10	1.20
A_1	0.002	0.004	0.006	0.05	0.1	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	—	0.006	—	—	0.16	—
c	0.004	—	0.008	0.09	—	0.20
D	0.866 BSC			22.00 BSC		
D1	0.787 BSC			20.00 BSC		
D2	0.677 BSC			17.20 BSC		
E	0.866 BSC			22.00 BSC		
E1	0.787 BSC			20.00 BSC		
E2	0.677BSC			17.20 BSC		
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF			1.00 REF		
y	—	—	0.004	—	—	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Note:
1. Dimensions D1 and E1 do not include mold protrusion.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension : millimeter

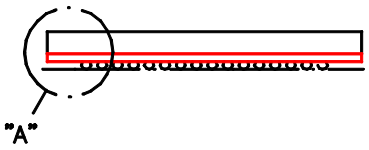
DI-TQFP176(20*20)v0

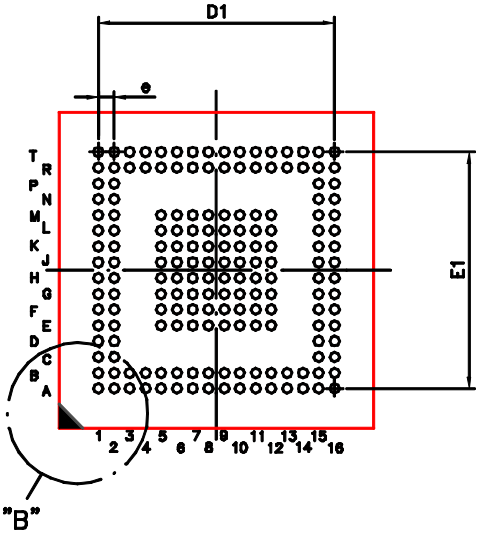
TFBGA 176 Outline Dimensions unit: inches/mm

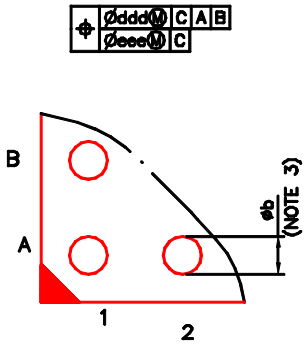




DETAIL : A







DETAIL : B

Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	--	--	1.20	--	--	0.047
A_1	0.16	0.21	0.26	0.006	0.008	0.010
A_2	0.84	0.89	0.94	0.033	0.035	0.037
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	--	7.50	--	--	0.295	--
E1	--	7.50	--	--	0.295	--
e	--	0.50	--	--	0.020	--
b	0.25	0.30	0.35	0.010	0.012	0.014
ccc	0.10			0.004		
ddd	0.15			0.006		
eee	0.10			0.004		
MD/ME	16/16			16/16		

Note:

1. Controlling dimension: millimeter
2. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-207
6. The pattern of pin 1 fiducial is for reference only.

DI-TFBGA176(10*10)v1

12. Ordering Information

Part No.	Package
IT8510E	LQFP 176L
IT8510TE	TQFP 176L
IT8510G	TFBGA 176

ITE provides lead-free component for the package of LQFP 176L. Please mark " -L " at the end of the Part No. when the parts ordered are lead-free. For the other two packages, please contact with ITE sales personnel if there is any lead-free component requirement.