IXDD404

4 Amp Dual Low-Side Ultrafast MOSFET Driver

Features

- Built using the advantages and compatibility of CMOS and IXYS HDMOS™ processes
- Latch-Up Protected up to 0.5A
- High Peak Output Current: 4A Peak
- Wide Operating Range: 4.5V to 35V
- Ability to Disable Output under Faults
- High Capacitive Load Drive Capability: 1800pF in <15ns
- Matched Rise And Fall Times
- Low Propagation Delay Time
- Low Output Impedance
- Low Supply Current
- Two identical drivers in single chip

Applications

- Driving MOSFETs and IGBTs
- Limiting di/dt under Short Circuit
- Motor Controls
- Line Drivers
- Pulse Generators
- Local Power ON/OFF Switch
- Switch Mode Power Supplies (SMPS)
- DC to DC Converters
- Pulse Transformer Driver
- Class D Switching Amplifiers

General Description

The IXDD404 is comprised of two 4 Amp CMOS high speed MOSFET drivers. Each output can source and sink 4 A of peak current while producing voltage rise and fall times of less than 15ns to drive the latest IXYS MOSFETS & IGBT's. The input of the driver is compatible with TTL or CMOS and is fully immune to latch up over the entire operating range. Designed with small internal delays, cross conduction/current shoot-through is virtually eliminated in the IXDD404. Improved speed and drive capabilities are further enhanced by very low, matched rise and fall times.

Additionally, each driver in the IXDD404 incorporates a unique ability to disable the output under fault conditions. When a logical low is forced into the Enable input of a driver, both of it's final output stage MOSFETs (NMOS and PMOS) are turned off. As a result, the respective output of the IXDD404 enters a tristate mode and achieves a Soft Turn-Off of the MOSFET/IGBT when a short circuit is detected. This helps prevent damage that could occur to the MOSFET/IGBT if it were to be switched off abruptly due to a dv/dt over-voltage transient.

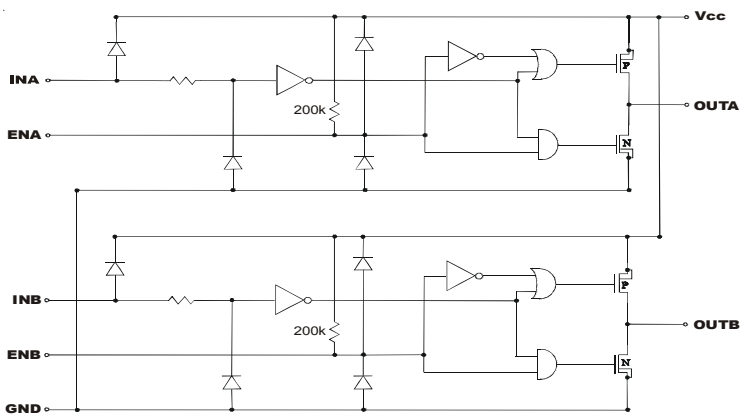
The IXDD404 is available in the standard 8 pin P-DIP (PI), SOIC-8 (SIA) and SOIC-16 (SIA-16) packages. For enhanced thermal performance, the SOIC-8 and SOIC-16 are also available with an exposed grounded metal back package as the SI and SI-16 respectively.

Ordering Information

Part Number	Package Type	Temp. Range	Configuration
IXDD404PI	8-Pin PDIP	-55◦C to +125◦C	Dual Non Inverting With Enable
IXDD404SI	8-Pin SOIC with Grounded Metal Back		
IXDD404SIA	8-Pin SOIC		
IXDD404SI-16	16-Pin SOIC with Grounded Metal Back		
IXDD404SIA-16	16-Pin SOIC		

NOTE: Mounting or solder tabs on all packages are connected to ground

Figure 1 - Functional Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value
Supply Voltage	40 V
All Other Pins	-0.3 V to V_{CC} + 0.3 V
Junction Temperature	150 °C
Storage Temperature	-65 °C to 150 °C
Lead Temperature (10 sec)	300 °C

Operating Ratings

Parameter	Value
Operating Temperature Range	-55 °C to 125 °C
Thermal Impedance (Junction to Ambient)	
8 Pin PDIP (PI) (θ_{JA})	120 °C/W
8 Pin SOIC (SIA) (θ_{JA})	110 °C/W
8 Pin SOIC (SI) (θ_{JA}) with heat sink** Heat sink area of 1cm^2	71 °C/W
16 Pin SOIC (SIA-16) (θ_{JA})	110 °C/W

**Heat sink area is 1 oz. copper on one side of .06" thick FR4 soldered to metal back plane.

Electrical Characteristics

Unless otherwise noted, T_A = 25 °C, 4.5V ≤ V_{CC} ≤ 35V .
All voltage measurements with respect to GND. IXDD404 configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage	4.5V ≤ V_{IN} ≤ 18V	2.5			V
V_{IL}	Low input voltage	4.5V ≤ V_{IN} ≤ 18V			0.8	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	V_{CC} = 18V		2	2.5	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V		1.5	2	Ω
I_{PEAK}	Peak output current	V_{CC} = 18V		4		A
I_{DC}	Continuous output current				1	A
V_{EN}	Enable voltage range		- 0.3		Vcc + 0.3	V
V_{ENH}	High En Input Voltage		2/3 Vcc			V
V_{ENL}	Low En Input Voltage				1/3 Vcc	V
t_R	Rise time	C_L=1800pF Vcc=18V		16	18	ns
t_F	Fall time	C_L=1800pF Vcc=18V		13	17	ns
t_{ONDLY}	On-time propagation delay	C_L=1800pF Vcc=18V		36	40	ns
t_{OFFDLY}	Off-time propagation delay	C_L=1800pF Vcc=18V		35	39	ns
t_{ENOH}	Enable to output high delay time				30	ns
t_{DOLD}	Disable to output low Disable delay time				30	ns
V_{CC}	Power supply voltage		4.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA
R_{EN}	Enable Pull-up Resistor			200		kΩ

Specifications to change without notice

Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Electrical Characteristics

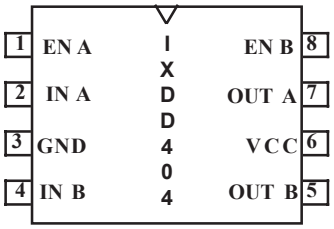
Unless otherwise noted, temperature over -55 °C to 150 °C, 4.5V ≤ V_{CC} ≤ 35V .
All voltage measurements with respect to GND. IXDD404 configured as described in *Test Conditions*. All specifications are for one channel.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	High input voltage		2			V
V_{IL}	Low input voltage				2.4	V
V_{IN}	Input voltage range		-5		V_{CC} + 0.3	V
I_{IN}	Input current	0V ≤ V_{IN} ≤ V_{CC}	-10		10	µA
V_{OH}	High output voltage		V_{CC} - 0.025			V
V_{OL}	Low output voltage				0.025	V
R_{OH}	Output resistance @ Output high	V_{CC} = 18V			3.4	Ω
R_{OL}	Output resistance @ Output Low	V_{CC} = 18V			2	Ω
I_{PEAK}	Peak output current	V_{CC} = 18V	3.2			A
I_{DC}	Continuous output current				1	A
t_R	Rise time	C_L=1000pF Vcc=18V			11	ns
t_F	Fall time	C_L=1000pF Vcc=18V			13	ns
t_{ONDLY}	On-time propagation delay	C_L=1000pF Vcc=18V			60	ns
t_{OFFDLY}	Off-time propagation delay	C_L=1000pF Vcc=18V			59	ns
V_{CC}	Power supply voltage		4.5	18	35	V
I_{CC}	Power supply current	V_{IN} = 3.5V V_{IN} = 0V V_{IN} = + V_{CC}		1 0	3 10 10	mA µA µA

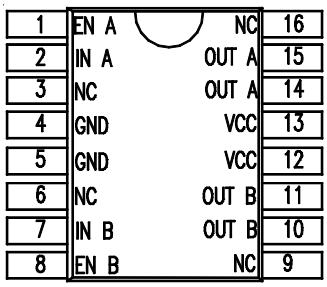
Specifications to change without notice

Pin Configurations

SO8 (SI)
8 PIN DIP (PI)



SO16 (SI-16)

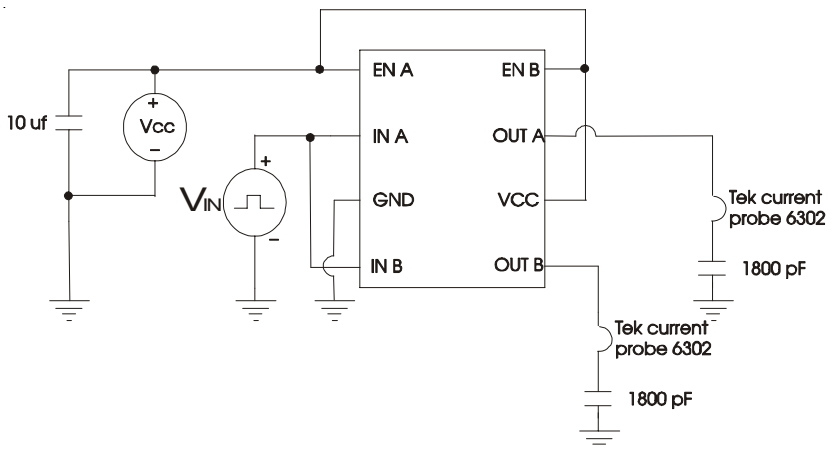


Pin Description

SYMBOL	FUNCTION	DESCRIPTION
EN A	A Channel Enable	The Channel A enable pin. This pin, when driven low, disables the A Channel, forcing a high impedance state to the A Channel Output.
IN A	A Channel Input	A Channel Input signal-TTL or CMOS compatible.
GND	Ground	The system ground pin. Internally connected to all circuitry, this pin provides ground reference for the entire chip. This pin should be connected to a low noise analog ground plane for optimum performance.
IN B	B Channel Input	B Channel Input signal-TTL or CMOS compatible.
OUT B	B Channel Output	B Channel Driver output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
VCC	Supply Voltage	Positive power-supply voltage input. This pin provides power to the entire chip. The range for this voltage is from 4.5V to 35V.
OUT A	A Channel Output	A Channel Driver output. For application purposes, this pin is connected, through a resistor, to Gate of a MOSFET/IGBT.
EN B	B Channel Enable	The Channel B enable pin. This pin, when driven low, disables the B Channel, forcing a high impedance state to the B Channel Output.

CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD procedures when handling and assembling this component.

Figure 2 - Characteristics Test Diagram



Typical Performance Characteristics

Fig. 3 Rise Times vs. Supply Voltage

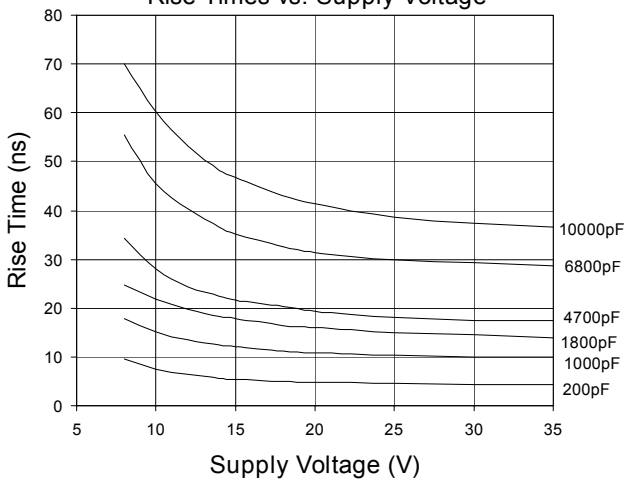


Fig. 4 Fall Times vs. Supply Voltage

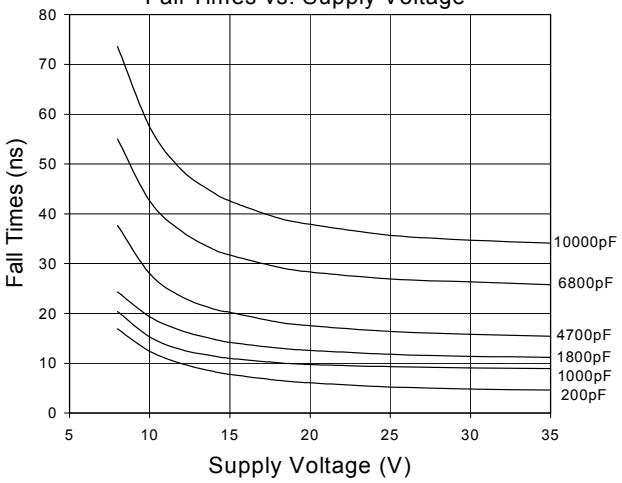


Fig. 5 Rise Times vs. Load Capacitance

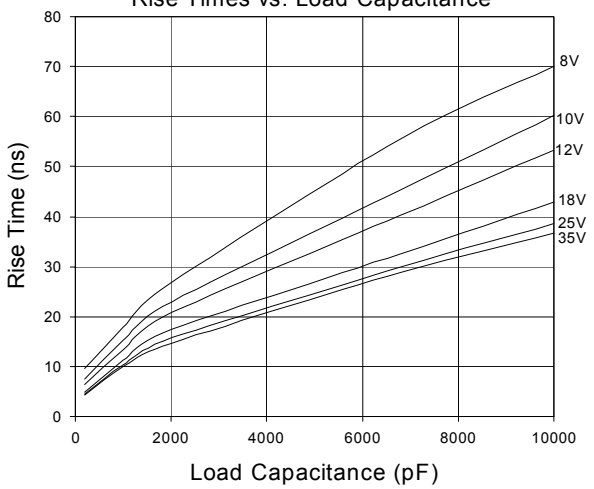


Fig. 6 Fall Times vs. Load Capacitance

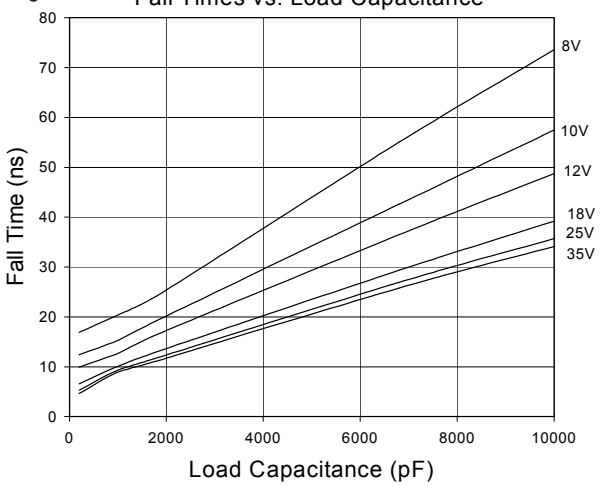


Fig. 7 Rise And Fall Times vs. Temperature
C_L = 1000pF, V_{cc} = 18V

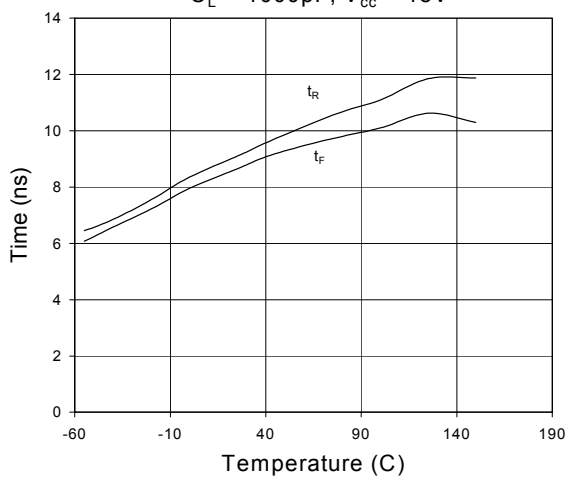


Fig. 8 Max / Min Input vs. Temperature
C_L = 1000pF, V_{cc} = 18V

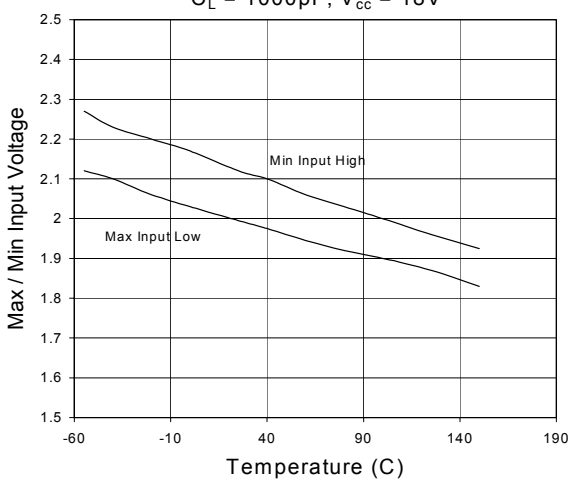


Fig. 9 Supply Current vs. Load Capacitance
Vcc = 8V

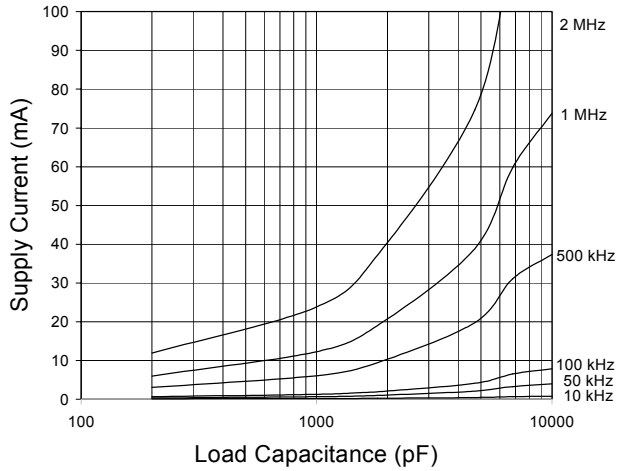


Fig. 10 Supply Current vs. Frequency
Vcc = 8V

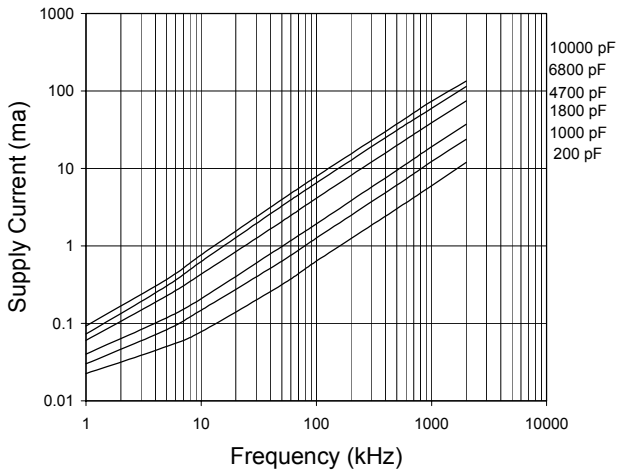


Fig. 11 Supply Current vs. Load Capacitance
Vcc = 12V

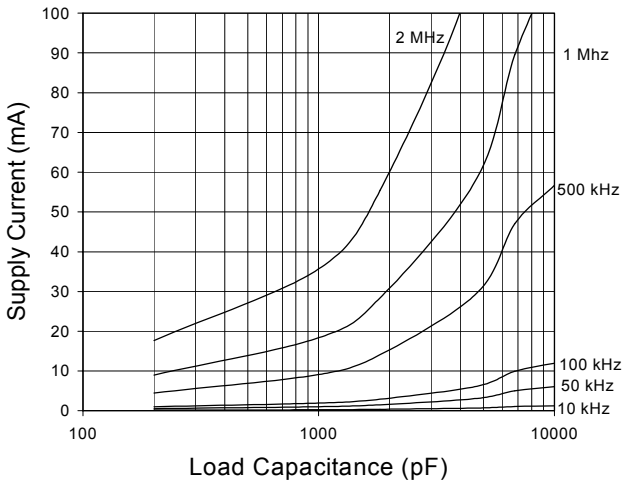


Fig. 12 Supply Current vs. Frequency
Vcc = 12V

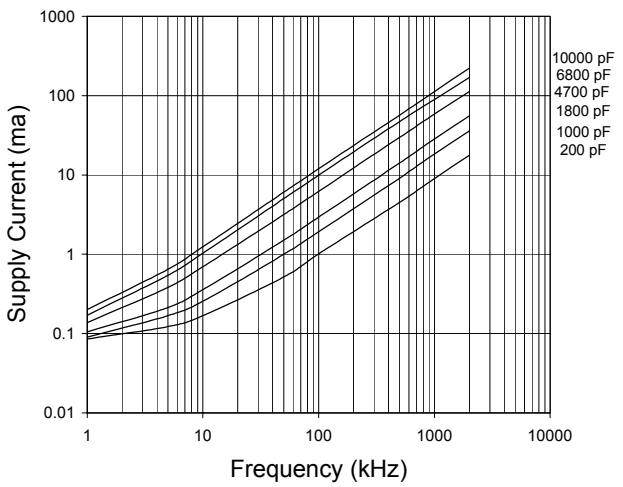


Fig. 13 Supply Current vs. Load Capacitance
Vcc = 18V

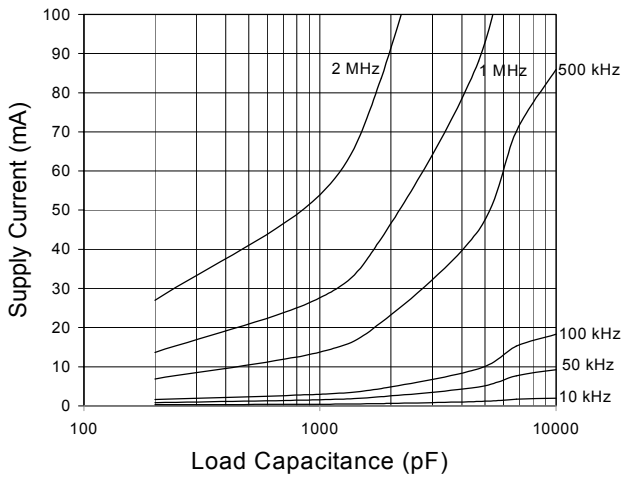


Fig. 14 Supply Current vs. Frequency
Vcc = 18V

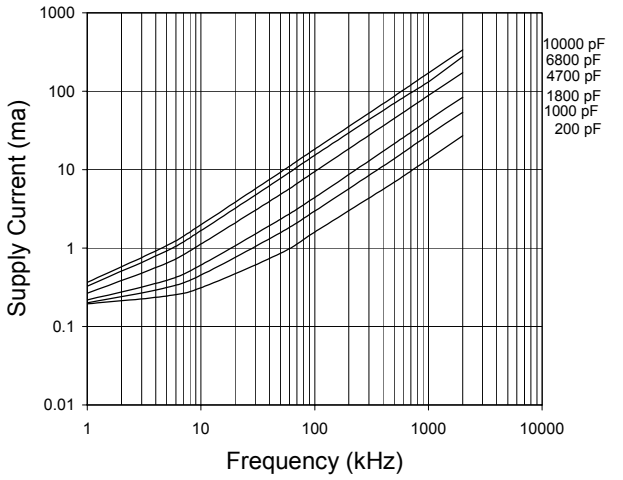


Fig. 15

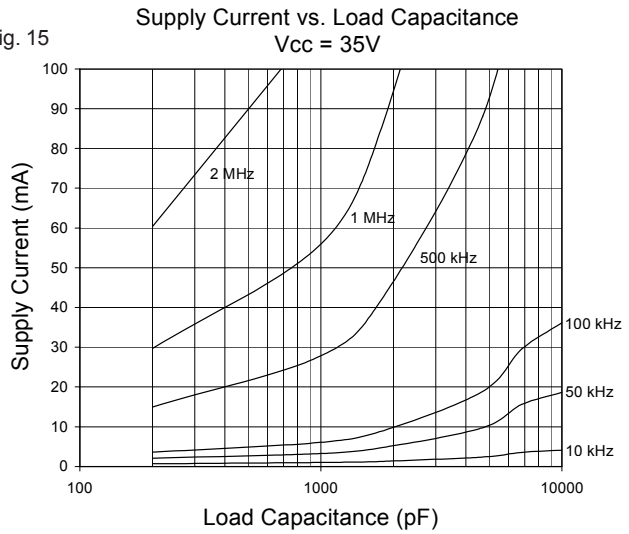


Fig. 16

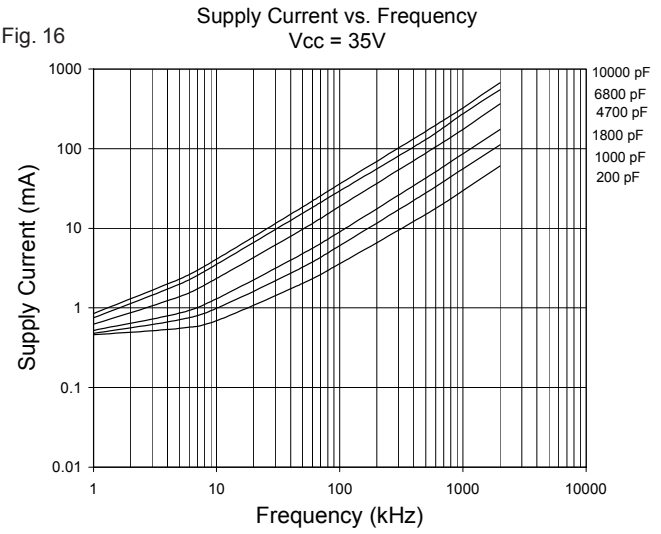
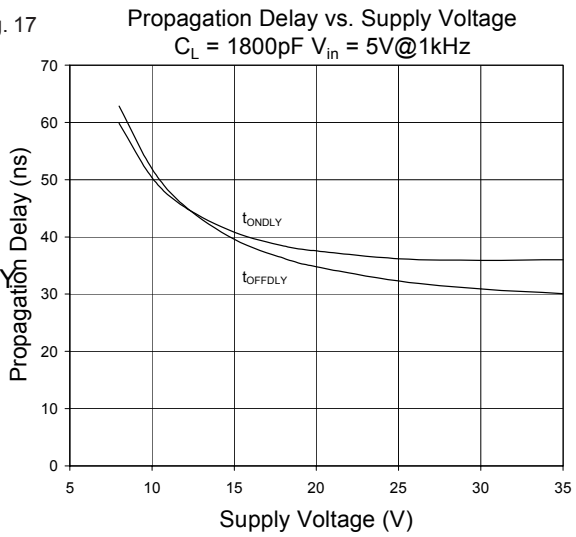


Fig. 17



tONDLY

Fig. 18

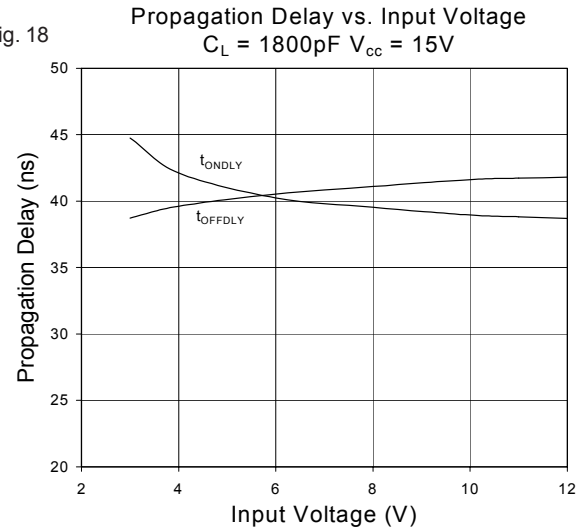


Fig. 19

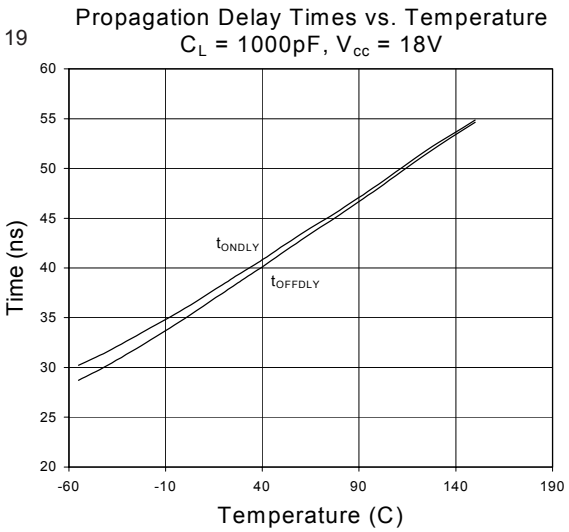


Fig. 20

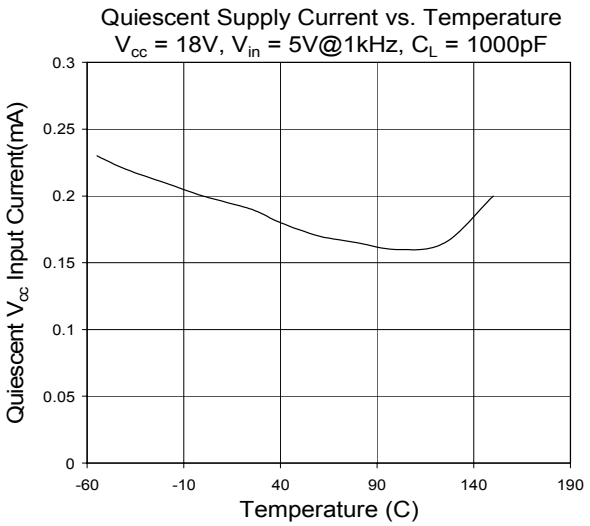


Fig. 21 High State Ouput Resistance vs. Supply Voltage

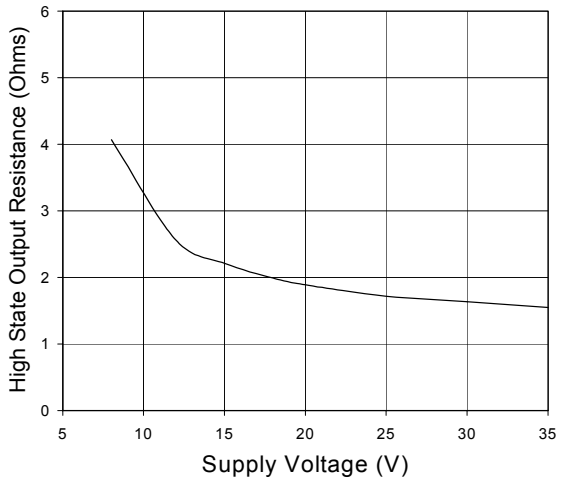


Fig. 22 Low State Output Resistance vs. Supply Voltage

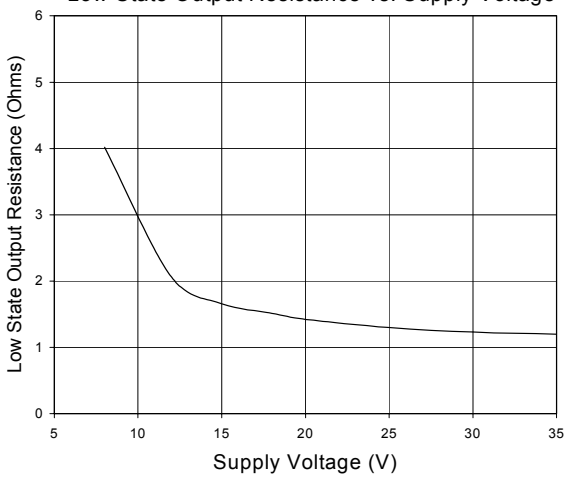


Fig. 23 Vcc vs. P Channel Output Current

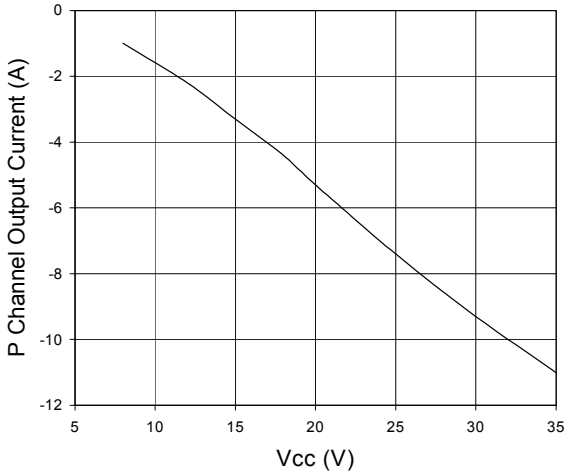


Fig. 24 Vcc vs. N Channel Ouput Current

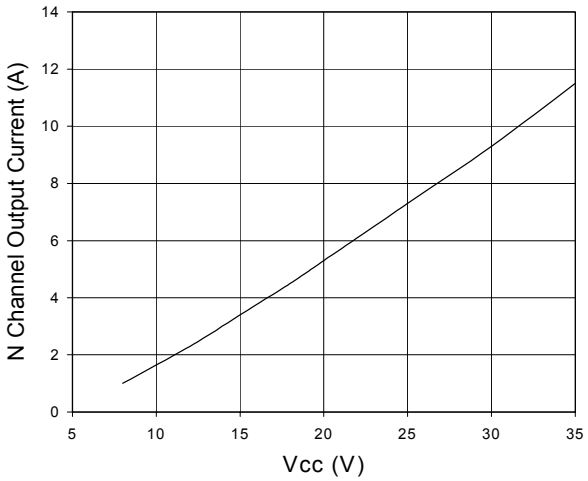


Fig. 25 P Channel Output Current vs. Temperature
V_{cc} = 18V, C_L = 1000pF

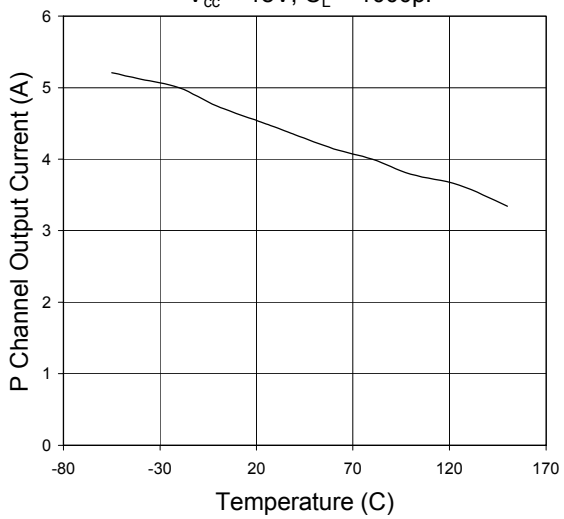


Fig. 26 N Channel Output Current vs. Temperature
V_{cc} = 18V C_L = 1000pF

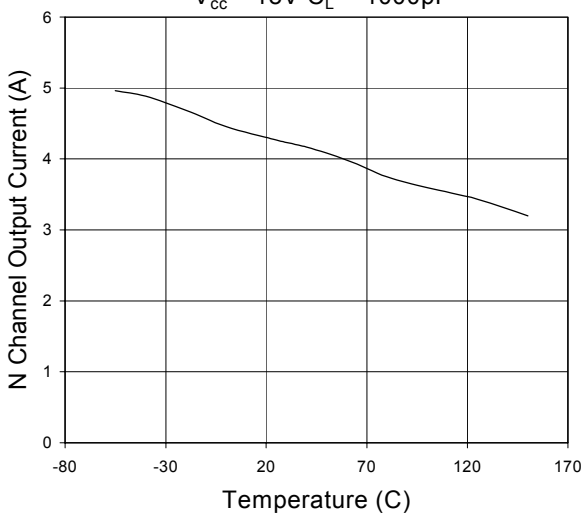


Fig. 27

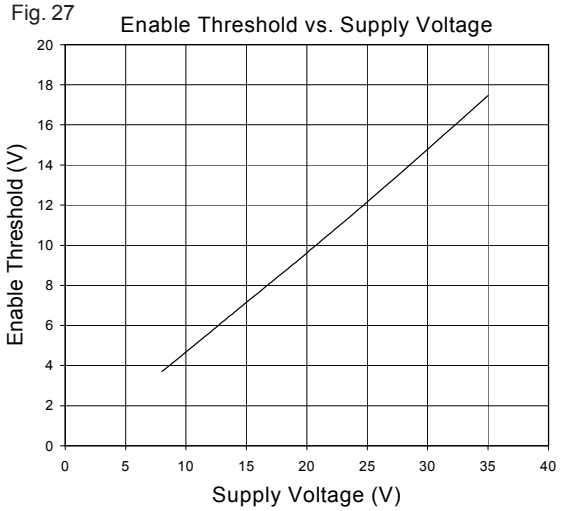
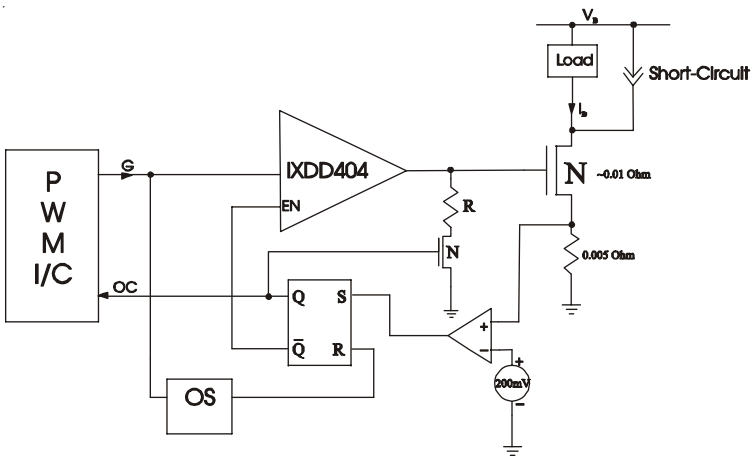


Figure 28 - Typical Application Short Circuit di/dt Limit



APPLICATIONS INFORMATION

Short Circuit di/dt Limit

A short circuit in a high-power MOSFET such as the IXFN100N20, (20A, 1000V), as shown in Figure 26, can cause the current through the module to flow in excess of 60A for 10µs or more prior to self-destruction due to thermal runaway. For this reason, some protection circuitry is needed to turn off the MOSFET module. However, if the module is switched off too fast, there is a danger of voltage transients occuring on the drain due to Ldi/dt, (where L represents total inductance in series with drain). If these voltage transients exceed the MOSFET's voltage rating, this can cause an avalanche breakdown.

The IXDD404 has the unique capability to softly switch off the high-power MOSFET module, significantly reducing these Ldi/dt transients.

Thus, the IXDD404 helps to prevent device destruction from *both* dangers; over-current, and avalanche breakdown due to di/dt induced over-voltage transients.

The IXDD404 is designed to not only provide ±4A per output under normal conditions, but also to allow it's outputs to go into a high impedance state. This permits the IXDD404 output to control a separate weak pull-down circuit during detected overcurrent shutdown conditions to limit and separately control d_{VGS}/dt gate turnoff. This circuit is shown in Figure 27.

Referring to Figure 27, the protection circuitry should include a comparator, whose positive input is connected to the source of the IXFD100N20. A low pass filter should be added to the input of the comparator to eliminate any glitches in voltage caused by the inductance of the wire connecting the source resistor to ground. (Those glitches might cause false triggering of the comparator).

The comparator's output should be connected to a SRFF(Set Reset Flip Flop). The flip-flop controls both the Enable signal, and the low power MOSFET gate. Please note that CMOS 4000-series devices operate with a V_{CC} range from 3 to 15 VDC, (with 18 VDC being the maximum allowable limit).

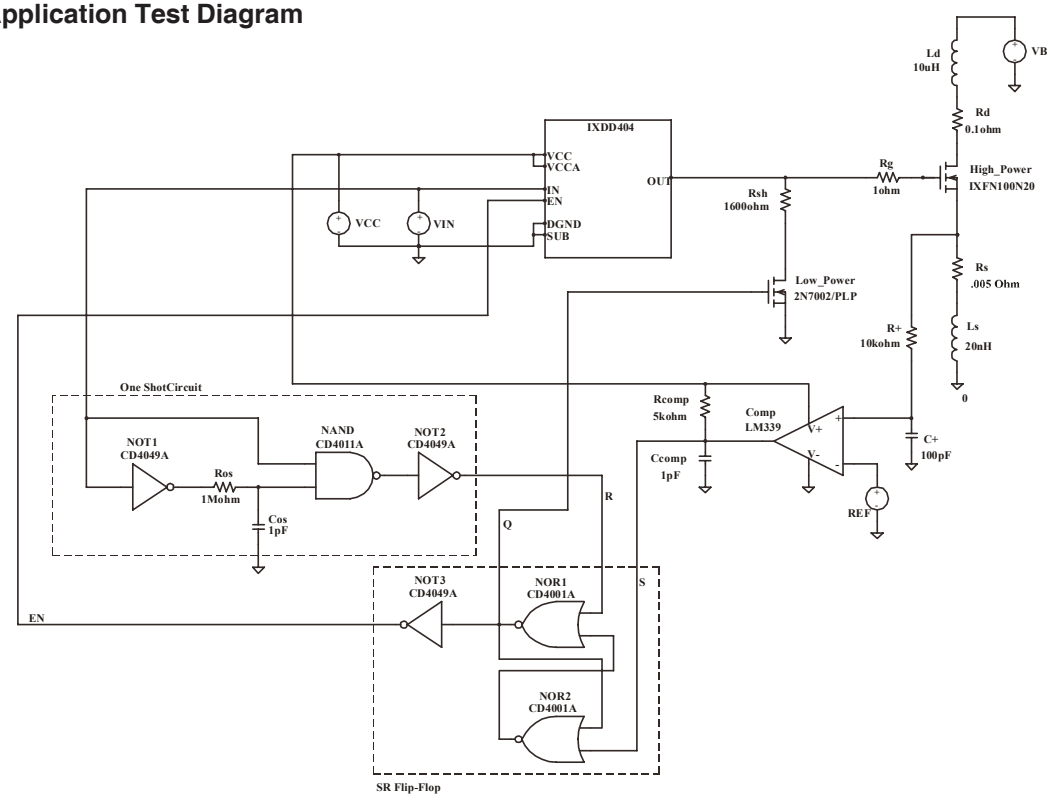
A low power MOSFET, such as the 2N7000, in series with a resistor, will enable the IXFN100N20 gate voltage to drop gradually. The resistor should be chosen so that the RC time constant will be 100us, where "C" is the Miller capacitance of the IXFN100N20.

For resuming normal operation, a Reset signal is needed at the SRFF's input to enable the IXDD404 again. This Reset can be generated by connecting a One Shot circuit between the IXDD408 Input signal and the SRFF restart input. The One Shot will create a pulse on the rise of the IXDD404 input, and this pulse will reset the SRFF outputs to normal operation.

When a short circuit occurs, the voltage drop across the low-value, current-sensing resistor, (Rs=0.005 Ohm), connected between the MOSFET Source and ground, increases. This triggers the comparator at a preset level. The SRFF drives a low input into the Enable pin disabling the IXDD404 output. The SRFF also turns on the low power MOSFET, (2N7000).

In this way, the high-power MOSFET module is softly turned off by the IXDD404, preventing its destruction.

Figure 29 - Application Test Diagram



Supply Bypassing and Grounding Practices, Output Lead inductance

When designing a circuit to drive a high speed MOSFET utilizing the IXDD404, it is very important to keep certain design criteria in mind, in order to optimize performance of the driver. Particular attention needs to be paid to **Supply Bypassing**, **Grounding**, and minimizing the **Output Lead Inductance**.

Say, for example, we are using the IXDD404 to charge a 2500pF capacitive load from 0 to 25 volts in 25ns.

Using the formula: I= ΔV C / Δt, where ΔV=25V C=2500pF & Δt=25ns we can determine that to charge 2500pF to 25 volts in 25ns will take a constant current of 2.5A. (In reality, the charging current won't be constant, and will peak somewhere around 4A).

SUPPLY BYPASSING

In order for our design to turn the load on properly, the IXDD404 must be able to draw this 2.5A of current from the power supply in the 25ns. This means that there must be very low impedance between the driver and the power supply. The most common method of achieving this low impedance is to bypass the power supply at the driver with a capacitance value that is a magnitude larger than the load capacitance. Usually, this would be achieved by placing two different types of bypassing capacitors, with complementary impedance curves, very close to the driver itself. (These capacitors should be carefully selected, low inductance, low resistance, high-pulse current-service capacitors). Lead lengths may radiate at high frequency due to inductance, so care should be taken to keep the lengths of the leads between these bypass capacitors and the IXDD404 to an absolute minimum.

GROUNDING

In order for the design to turn the load off properly, the IXDD404 must be able to drain this 2.5A of current into an adequate grounding system. There are three paths for returning current that need to be considered: Path #1 is between the IXDD404 and it's load. Path #2 is between the IXDD404 and it's power supply. Path #3 is between the IXDD404 and whatever logic is driving it. All three of these paths should be as low in resistance and inductance as possible, and thus as short as practical. In addition, every effort should be made to keep these three ground paths distinctly separate. Otherwise, (for instance), the returning ground current from the load may develop a voltage that would have a detrimental effect on the logic line driving the IXDD404.

OUTPUT LEAD INDUCTANCE

Of equal importance to Supply Bypassing and Grounding are issues related to the Output Lead Inductance. Every effort should be made to keep the leads between the driver and it's load as short and wide as possible. If the driver must be placed farther than 2" from the load, then the output leads should be treated as transmission lines. In this case, a twisted-pair should be considered, and the return line of each twisted pair should be placed as close as possible to the ground pin of the driver, and connect directly to the ground terminal of the load.

TTL to High Voltage CMOS Level Translation

The enable (EN) input to the IXDD404 is a high voltage CMOS logic level input where the EN input threshold is ½ V_{CC}, and may not be compatible with 5V CMOS or TTL input levels. The IXDD404 EN input was intentionally designed for enhanced noise immunity with the high voltage CMOS logic levels. In a typical gate driver application, V_{CC} =15V and the EN input threshold at 7.5V, a 5V CMOS logical high input applied to this typical IXDD404 application's EN input will be misinterpreted as a logical low, and may cause undesirable or unexpected results. The note below is for optional adaptation of TTL or 5V CMOS levels.

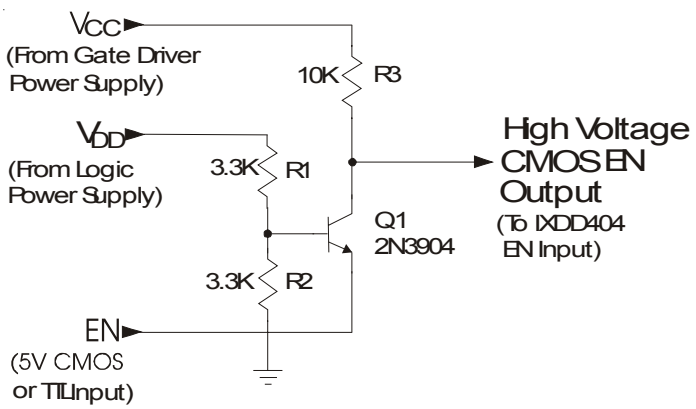
The circuit in Figure 28 alleviates this potential logic level misinterpretation by translating a TTL or 5V CMOS logic input to high voltage CMOS logic levels needed by the IXDD404 EN input. From the figure, V_{CC} is the gate driver power supply, typically set between 8V to 20V, and V_{DD} is the logic power supply, typically between 3.3V to 5.5V. Resistors R1 and R2 form a voltage divider network so that the Q1 base is positioned at the midpoint of the expected TTL logic transition levels.

A TTL or 5V CMOS logic low, V_{TTLLOW}=~<0.8V, input applied to the Q1 emitter will drive it on. This causes the level translator output, the Q1 collector output to settle to $V_{CESATQ1}$ + V_{TTLLOW}=<~2V, which is sufficiently low to be correctly interpreted as a high voltage CMOS logic low (<1/3V_{CC}=5V for V_{CC} =15V given in the IXDD404 data sheet.)

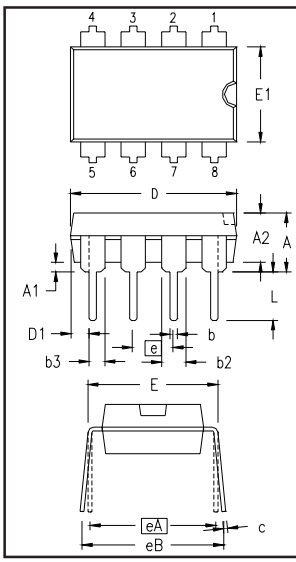
A TTL high, $V_{TTLHIGH}$=>~2.4V, or a 5V CMOS high, $V_{5VCMOSHIGH}$=~>3.5V, applied to the EN input of the circuit in Figure 28 will cause Q1 to be biased off. This results in Q1 collector being pulled up by R3 to V_{CC}=15V, and provides a high voltage CMOS logic high output. The high voltage CMOS logical EN output applied to the IXDD404 EN input will enable it, allowing the gate driver to fully function as a ±4 Amp output driver.

The total component cost of the circuit in Figure 28 is less than $0.10 if purchased in quantities >1K pieces. It is recommended that the physical placement of the level translator circuit be placed close to the source of the TTL or CMOS logic circuits to maximize noise rejection.

Figure 30 - TTL to High Voltage CMOS Level Translator



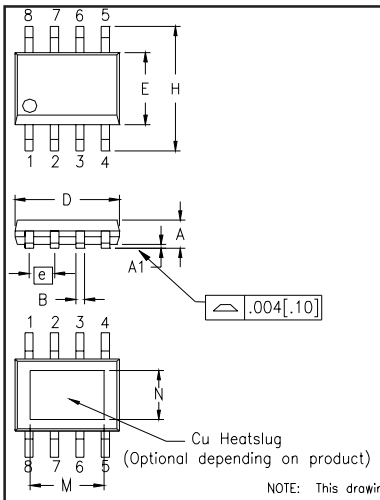
Dimenional Outline: IXDD404PI



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.355	.400	9.02	10.16
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 BA.

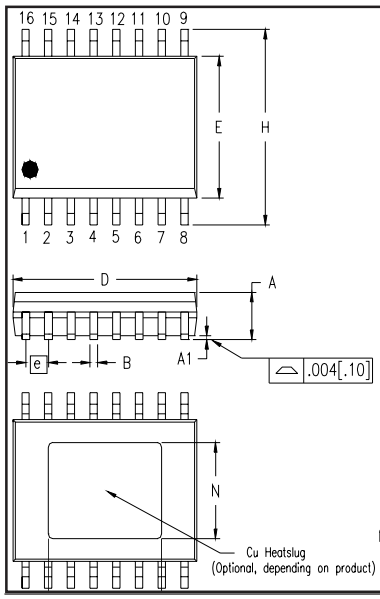
Dimenional Outlines: IXDD404SI-CT and IXDD404SIA



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
B	.013	.020	0.33	0.51
C	.008	.010	0.19	0.25
D	.189	.197	4.80	5.00
E	.150	.157	3.80	4.00
e	.050BSC		1.27BSC	
H	.228	.244	5.80	6.20
h	.010	.020	0.25	0.50
L	.016	.050	0.40	1.27
M	.135	.155	3.43	3.94
N	.095	.115	2.41	2.92
α	0°	8°	0°	8°

NOTE: This drawing will meet all dimensions requirement of JEDEC MS-012 AA.

Dimenional Outlines: IXDD404SI-16CT and IXDD404SIA-16



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
B	.013	.020	0.33	0.51
C	.009	.013	0.23	0.32
D	.398	.413	10.10	10.50
E	.291	.299	7.40	7.60
e	.050BSC		1.27BSC	
H	.394	.419	10.00	10.65
h	.010	.029	0.25	0.75
L	.016	.050	0.40	1.27
M	.240	.260	6.10	6.60
N	.190	.210	4.83	5.33
α	0°	8°	0°	8°

NOTE: 1. This drawing will meet all dimensions requirement of JEDEC MS-013 AA case outline.
2. Cu heatslug is attached to the die attach pad.

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