

**N-channel silicon field-effect transistors**

**J111; J112; J113**

**DESCRIPTION**

Symmetrical silicon n-channel junction FETs in plastic TO-92 envelopes. They are intended for applications such as analog switches, choppers, commutators etc.

**FEATURES**

- High speed switching
- Interchangeability of drain and source connections
- Low  $R_{DS\ on}$  at zero gate voltage

**PINNING**

- 1 = gate
- 2 = source
- 3 = drain

Note: Drain and source are interchangeable.

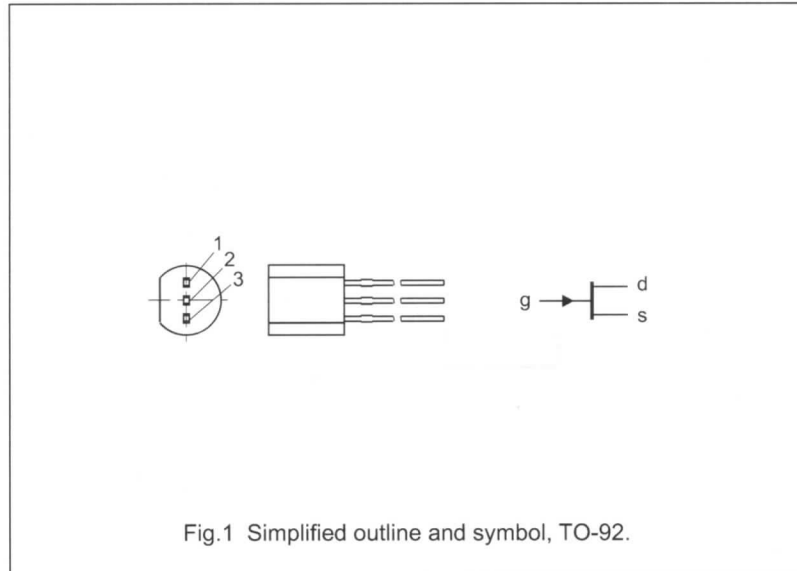


Fig.1 Simplified outline and symbol, TO-92.

**QUICK REFERENCE DATA**

			J111	J112	J113	
Drain-source voltage	$\pm V_{DS}$	max.	40	40	40	V
Drain current						
$V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	min.	20	5	2	mA
Total power dissipation						
up to $T_{amb} = 50\text{ }^\circ\text{C}$	$P_{tot}$	max.	400	400	400	mW
Gate-source cut-off voltage						
$V_{DS} = 5\text{ V}; I_D = 1\text{ }\mu\text{A}$	$-V_{GS\ off}$	min.	3	1	0.5	V
		max.	10	5	3	V
Drain-source on-state resistance						
$V_{DS} = 0.1\text{ V}; V_{GS} = 0$	$R_{DS\ on}$	max.	30	50	100	$\Omega$



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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40 V
Gate-source voltage	$-V_{GSO}$	max.	40 V
Gate-drain voltage	$-V_{GDO}$	max.	40 V
Gate forward current (DC)	$I_G$	max.	50 mA
Total power dissipation up to $T_{amb} = 50\text{ }^\circ\text{C}$	$P_{tot}$	max.	400 mW
Storage temperature range	$T_{stg}$		-65 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	150 $^\circ\text{C}$

### THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	250 K/W
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### STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

			J111	J112	J113
Gate reverse current $-V_{GS} = 15\text{ V}; V_{DS} = 0$	$-I_{GSS}$	max.	1	1	1 nA
Drain cut-off current $V_{DS} = 5\text{ V}; -V_{GS} = 10\text{ V}$	$-I_{DSX}$	max.	1	1	1 nA
Drain saturation current $V_{DS} = 15\text{ V}; V_{GS} = 0$	$I_{DSS}$	min.	20	5	2 mA
Gate-source breakdown voltage $-I_G = 1\text{ }\mu\text{A}; V_{DS} = 0$	$-V_{(BR)GSS}$	min.	40	40	40 V
Gate-source cut-off voltage $V_{DS} = 5\text{ V}; I_D = 1\text{ }\mu\text{A}$	$-V_{GS\ off}$	min. max.	3 10	1 5	0.5 3 V
Drain-source on-state resistance $V_{DS} = 0.1\text{ V}; V_{GS} = 0$	$R_{DSon}$	max.	30	50	100 $\Omega$