

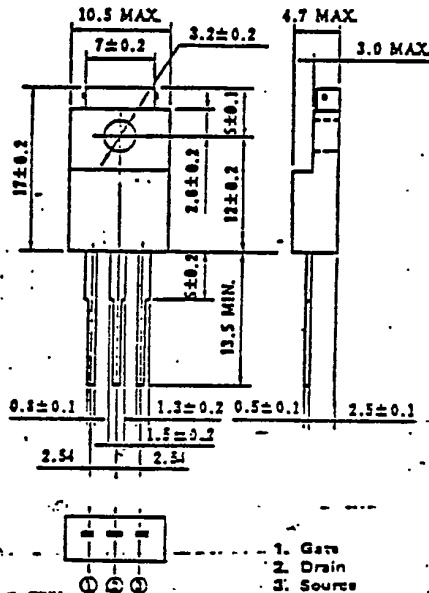


MOS FIELD EFFECT TRANSISTOR

2SJ135

FAST SWITCHING P-CHANNEL SILICON POWER MOS FET

PACKAGE DIMENSIONS
(Unit: mm)



Features

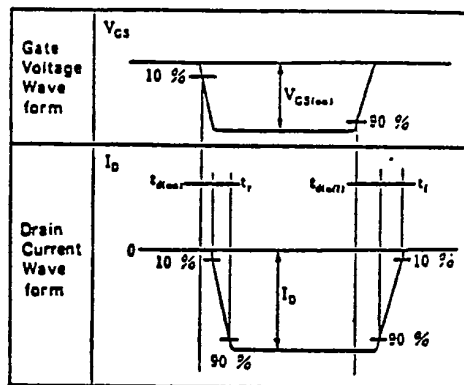
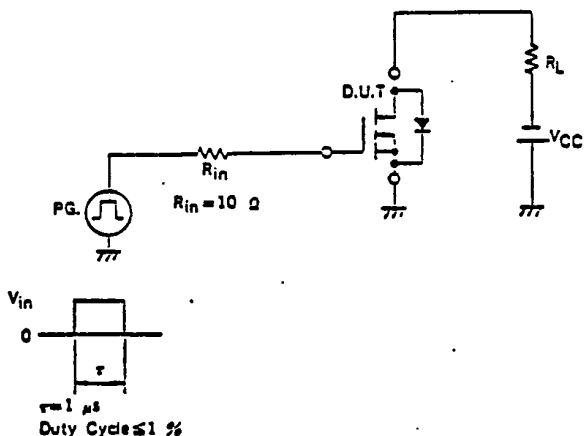
- Suitable for switching power supplies, actuator controls and pulse circuits
 - 4V Gate Drive — Logic Level —
 - Large current switching : $I_D(DC) = 5A$
 - Low $R_{DS(on)}$
 - No Secondary Breakdown
- Absolute Maximum Ratings ($T_a = 25^\circ C$)
- | | | |
|--------------------------|--------------|----------------|
| Drain to Source Voltage | V_{DS} | -100V |
| Gate to Source Voltage | V_{GS} | ± 20V |
| Continuous Drain Current | $I_D(DC)$ | ± 5.0A |
| Pulse Drain Current | $I_D(pulse)$ | * ± 20A |
| Total Power Dissipation | PT | 2.0W |
| Total Power Dissipation | PT** | 30W |
| Channel Temperature | T_{ch} | 150 °C |
| Storage Temperature | T_{stg} | -55 to +150 °C |
- * $T_{ch} \leq 150^\circ C$
** $T_c = 25^\circ C$

Electrical Characteristics ($T_a = 25^\circ C$)

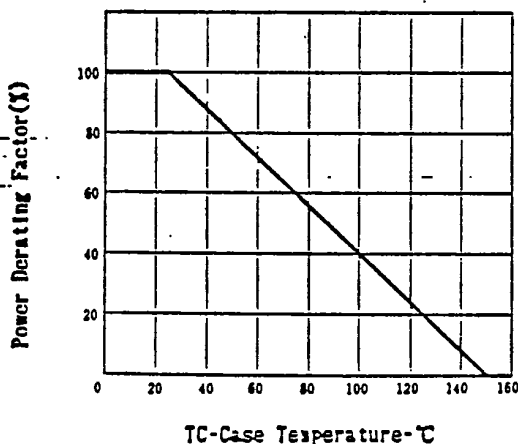
Characteristics	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain Leakage Current	I_{DSS}			- 10	μA	$V_{DS} = -100V, V_{GS} = 0$
Gate to Source Leakage Current	I_{GSS}			100	nA	$V_{GS} = 20V, V_{DS} = 0$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-1.0		-3.0	V	$V_{DS} = -10V, I_D = -1.0A$
Forward Transfer Admittance	$ y_{fs} $	1.0			S	$V_{DS} = -10V, I_D = -3.5A$
Drain to Source On-State Resistance	$R_{DS(on)}$			0.6	Ω	$V_{GS} = -10V, I_D = -3.5A$
Drain to Source On-State Resistance	$R_{DS(on)}$			0.9	Ω	$V_{GS} = -4.0V, I_D = -3.5A$
Input Capacitance	C_{iss}		1600		pF	$V_{DS} = -10V, V_{GS} = 0$
Output Capacitance	C_{oss}		400		pF	$V_{GS} = 0, f = 1.0MHz$
Reverse Transfer Capacitance	C_{rss}		65		pF	$f = 1.0MHz$
Turn-On Delay Time	$t_{d(on)}$		9		ns	$I_D = -3.5A, V_{GS(on)} = -10V$
Rise Time	t_r		35		ns	$V_{cc} = -50V, R_L = 15 \Omega$
Turn-Off Delay Time	$t_{d(off)}$		55		ns	
Fall Time	t_f		40		ns	

NEC cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

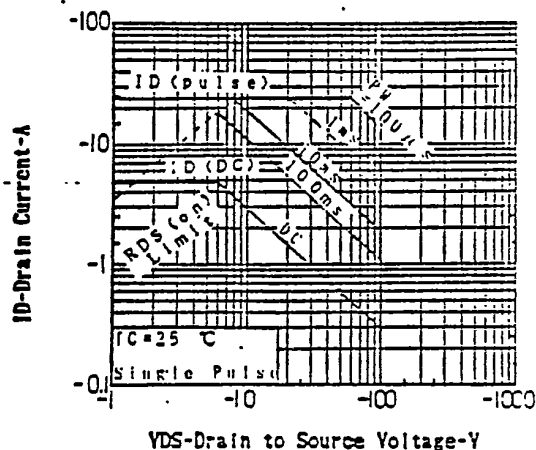
TURN-ON AND TURN-OFF TIME TEST CIRCUIT



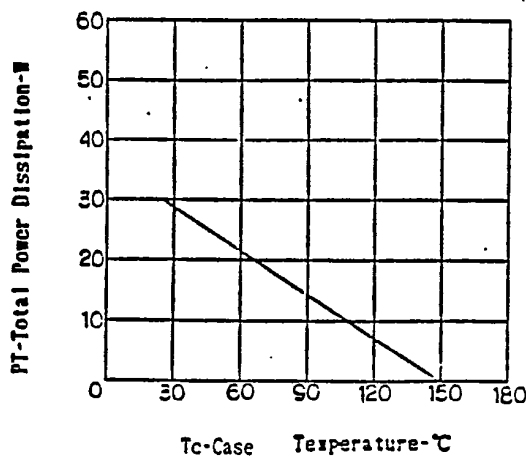
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



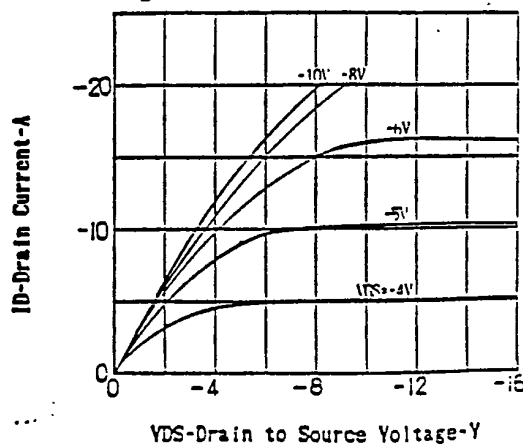
FORWARD BIAS SAFE OPERATING AREA

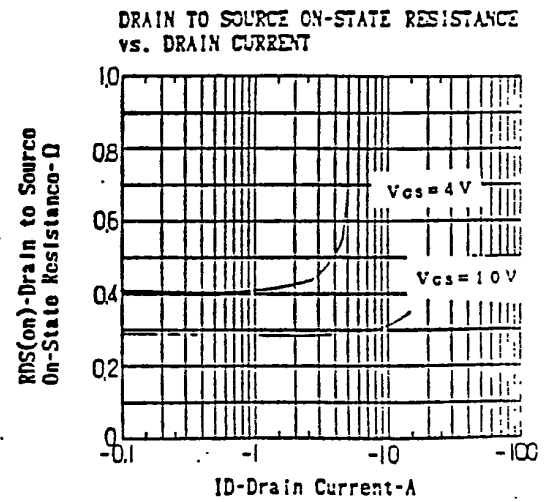
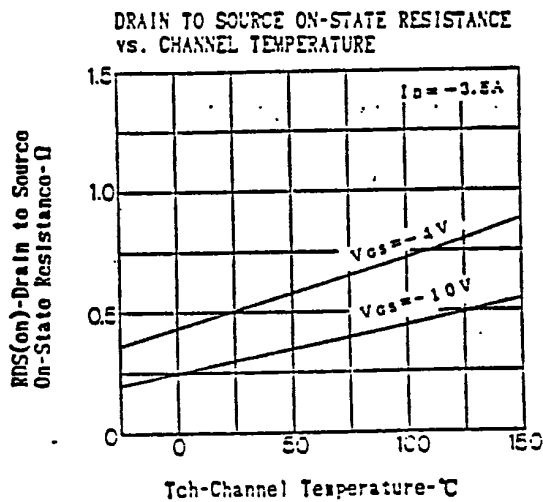
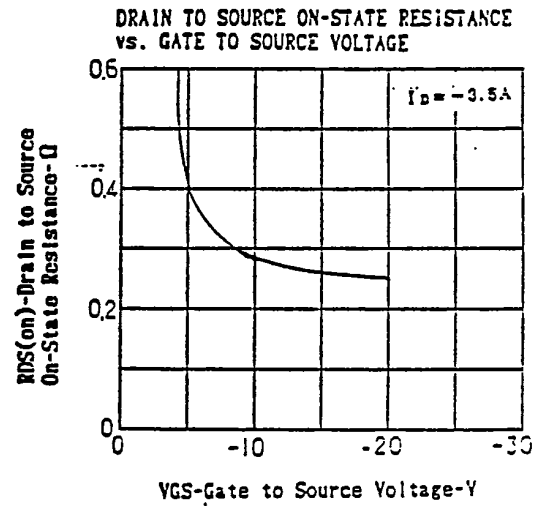
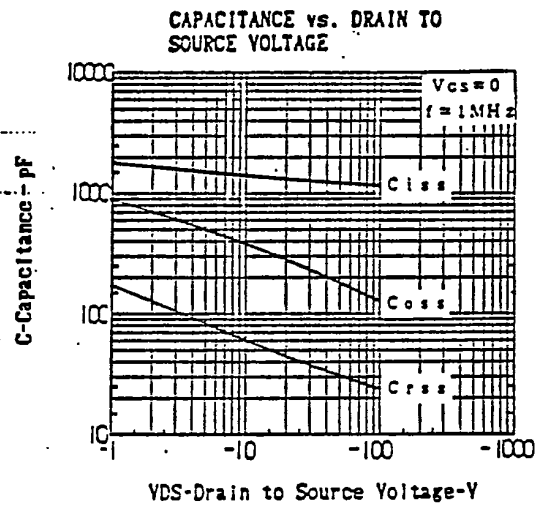
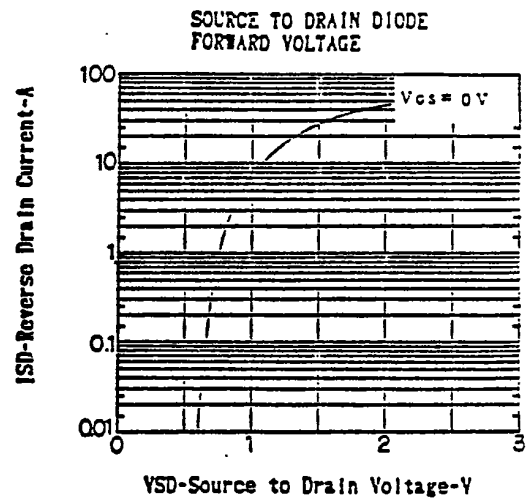
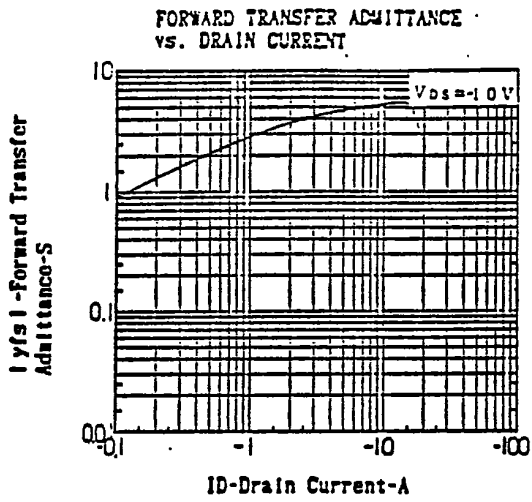


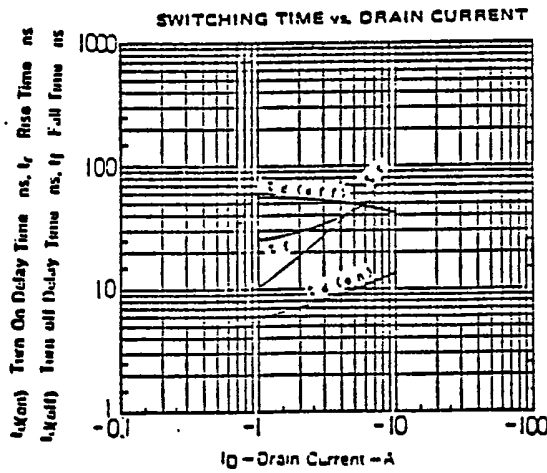
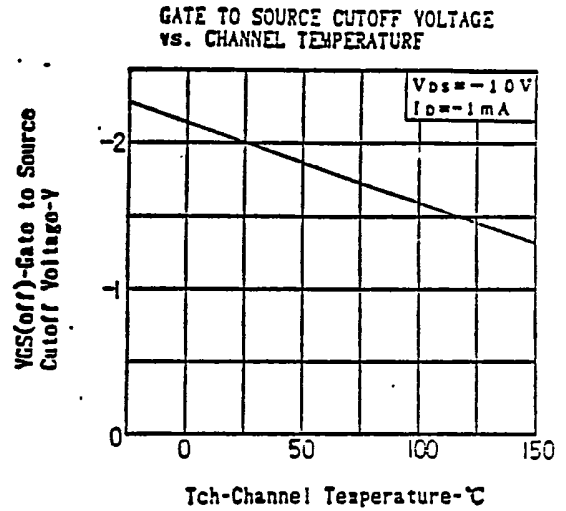
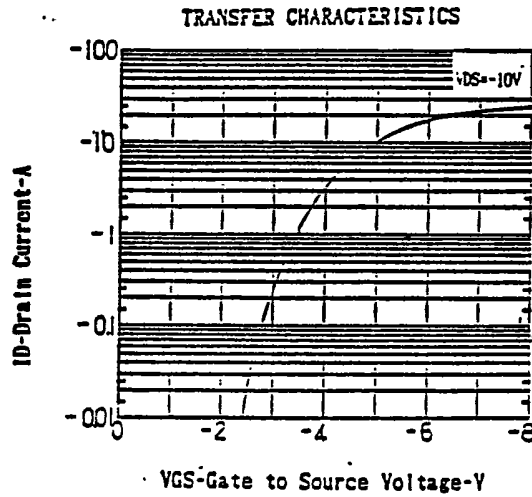
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE







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