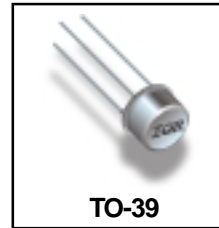


REPETITIVE AVALANCHE AND dv/dt RATED HEXFET[®] TRANSISTORS THRU-HOLE (TO-205AF)

IRFF9130
JANTX2N6849
JANTXV2N6849
JANS2N6849
REF:MIL-PRF-19500/564
100V, P-CHANNEL

Product Summary

Part Number	BVDSS	RDS(on)	ID
IRFF9130	-100V	0.30Ω	-6.5A



The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters. They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers and high energy pulse circuits.

Features:

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Hermetically Sealed
- Simple Drive Requirements
- Ease of Paralleling

Absolute Maximum Ratings

	Parameter		Units
I_D @ $V_{GS} = -10V, T_C = 25^\circ C$	Continuous Drain Current	-6.5	A
I_D @ $V_{GS} = -10V, T_C = 100^\circ C$	Continuous Drain Current	-4.1	
I_{DM}	Pulsed Drain Current ①	-25	
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	25	W
	Linear Derating Factor	0.20	W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20	V
EAS	Single Pulse Avalanche Energy ②	92	mJ
I_{AR}	Avalanche Current ①	—	A
EAR	Repetitive Avalanche Energy ①	—	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.5	V/ns
T_J	Operating Junction	-55 to 150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)	
	Weight	0.98(typical)	g

For footnotes refer to the last page

Electrical Characteristics @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBV _{DSS} /ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.10	—	V/°C	Reference to 25°C, I _D = -1.0mA
R _{DSON}	Static Drain-to-Source On-State Resistance	—	—	0.30	Ω	V _{GS} = -10V, I _D = -4.1A ④
		—	—	0.345		V _{GS} = -10V, I _D = -6.5A ④
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	2.5	—	—	S (r)	V _{DS} > -15V, I _{DS} = -4.1A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-250		V _{DS} = -80V V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	14.7	—	34.8	nC	V _{GS} = -10V, I _D = -6.5A
Q _{gs}	Gate-to-Source Charge	1.0	—	7.1		V _{DS} = -50V
Q _{gd}	Gate-to-Drain ('Miller') Charge	2.0	—	21		
t _{d(on)}	Turn-On Delay Time	—	—	60	ns	V _{DD} = -50V, I _D = -6.5A, V _{GS} = -10V, R _G = 7.5Ω
t _r	Rise Time	—	—	140		
t _{d(off)}	Turn-Off Delay Time	—	—	140		
t _f	Fall Time	—	—	140		
LS + LD	Total Inductance	—	7.0	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C _{iss}	Input Capacitance	—	800	—	pF	V _{GS} = 0V, V _{DS} = -25V f = 1.0MHz
C _{oss}	Output Capacitance	—	350	—		
C _{rss}	Reverse Transfer Capacitance	—	125	—		

Source-Drain Diode Ratings and Characteristics

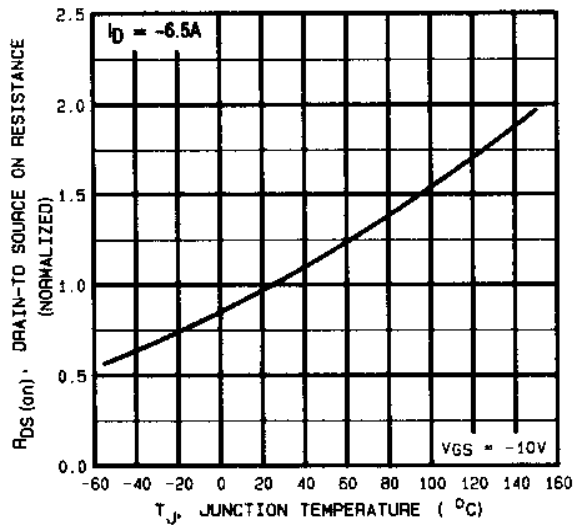
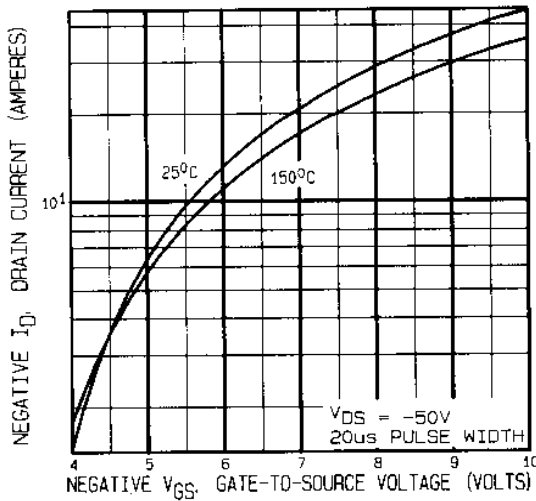
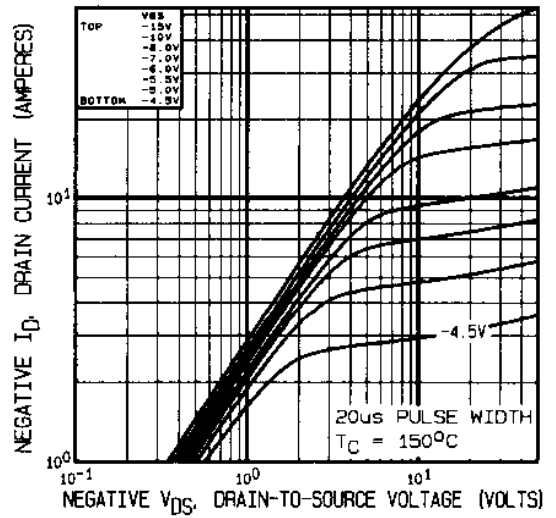
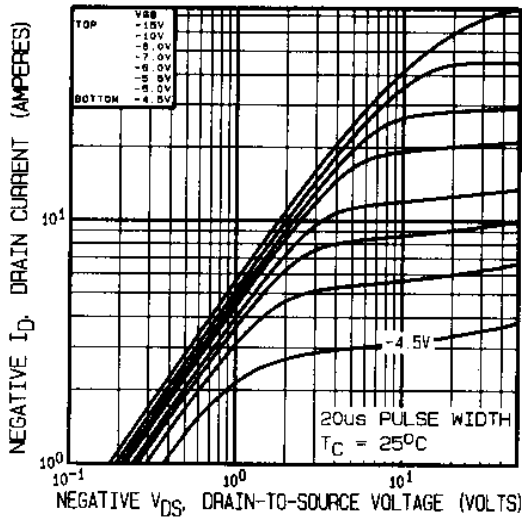
	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-6.5	A	T _J = 25°C, I _S = -6.5A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-25		
V _{SD}	Diode Forward Voltage	—	—	-4.7	V	T _J = 25°C, I _F = -6.5A, di/dt ≤ -100A/μs V _{DD} ≤ -50V ④
t _{rr}	Reverse Recovery Time	—	—	250	nS	
Q _{RR}	Reverse Recovery Charge	—	—	3.0	μC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	5.0	°C/W	Typical socket mount
R _{thJA}	Junction-to-Ambient	—	—	175		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page



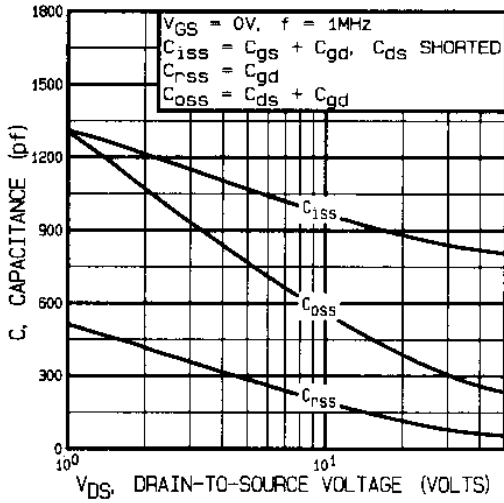


Fig5. Typical Capacitance Vs. Drain-to-Source Voltage

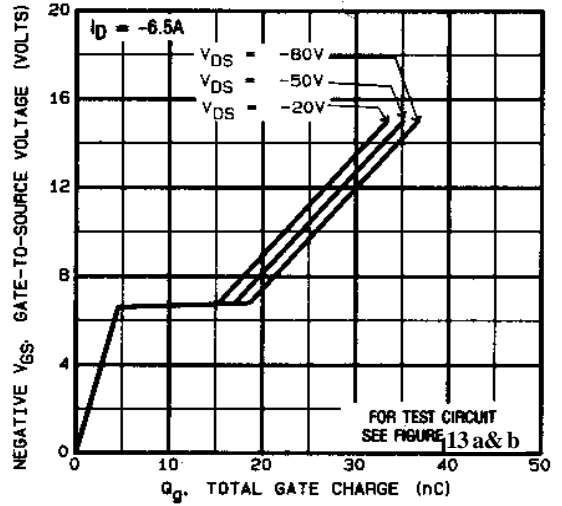


Fig6. Typical Gate Charge Vs. Gate-to-Source Voltage

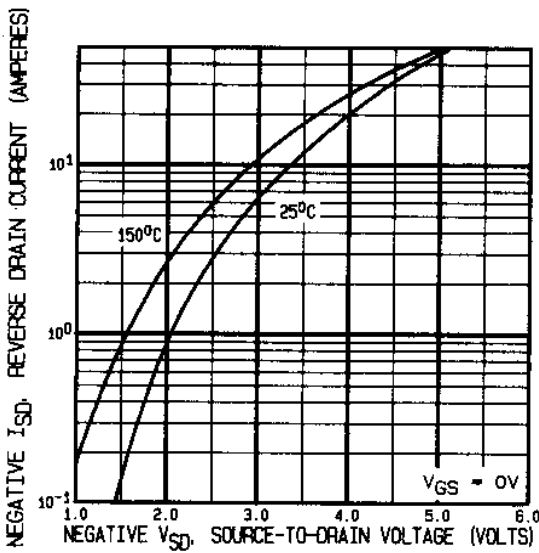


Fig7. Typical Source-Drain Diode Forward Voltage

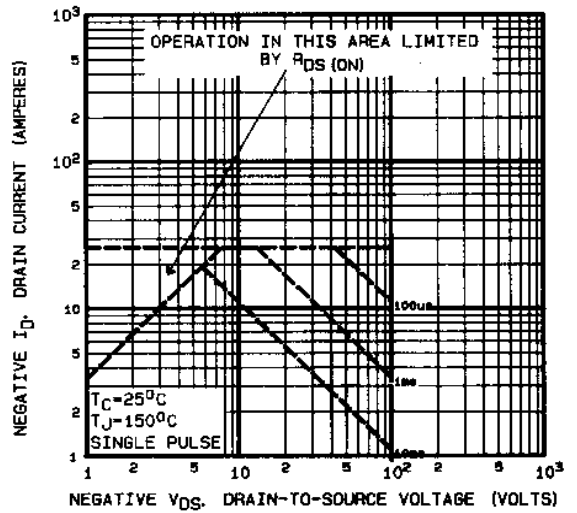


Fig8. Maximum Safe Operating Area

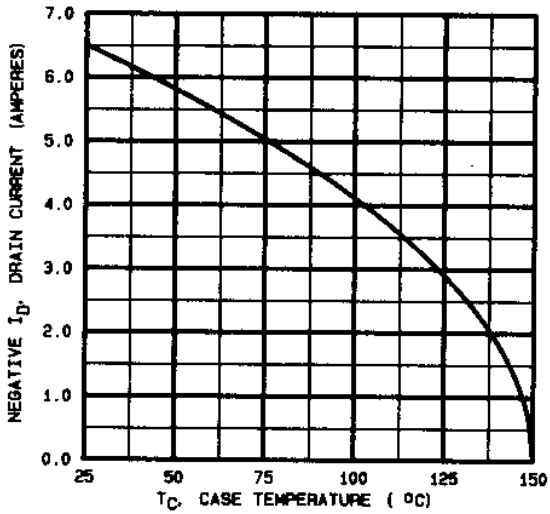


Fig9. Maximum Drain Current Vs. Case Temperature

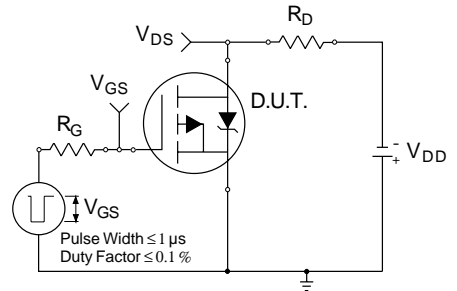


Fig 10a. Switching Time Test Circuit

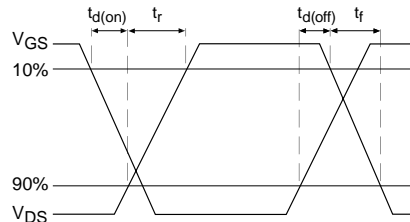


Fig 10b. Switching Time Waveforms

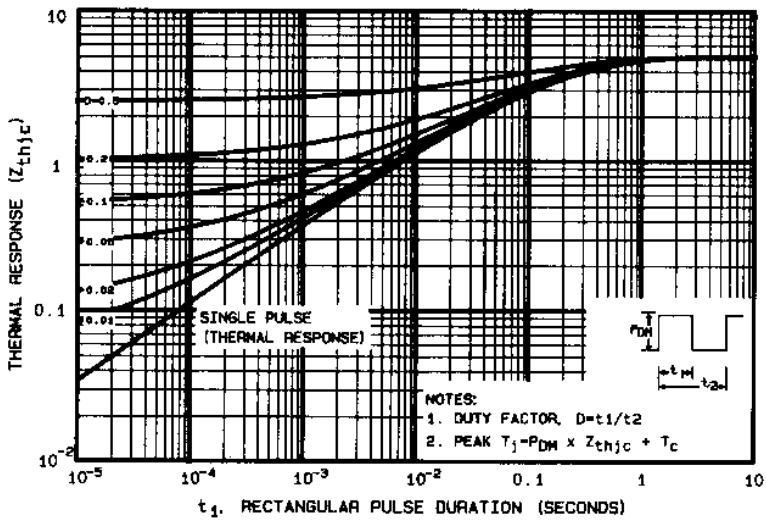


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

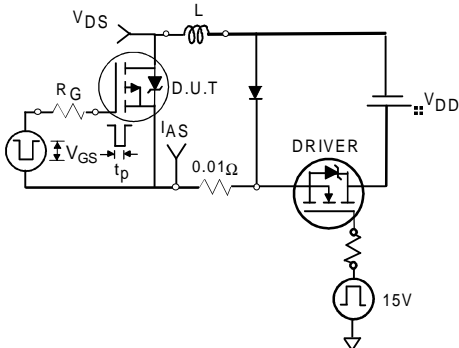


Fig 12a. Unclamped Inductive Test Circuit

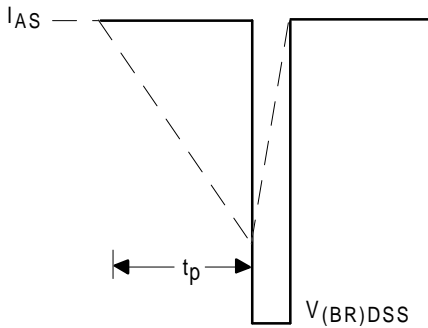


Fig 12b. Unclamped Inductive Waveforms

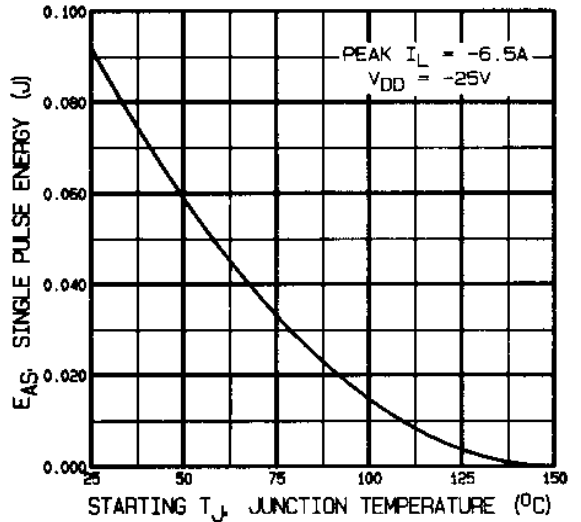


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

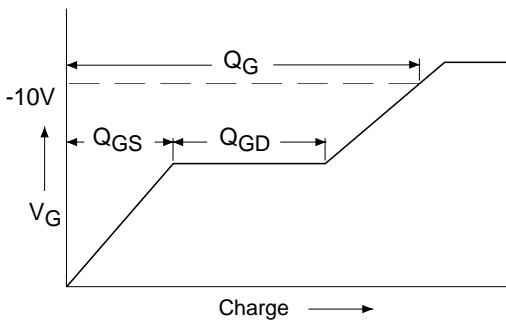


Fig 13a. Basic Gate Charge Waveform

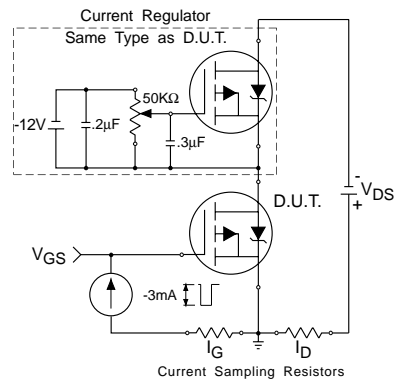
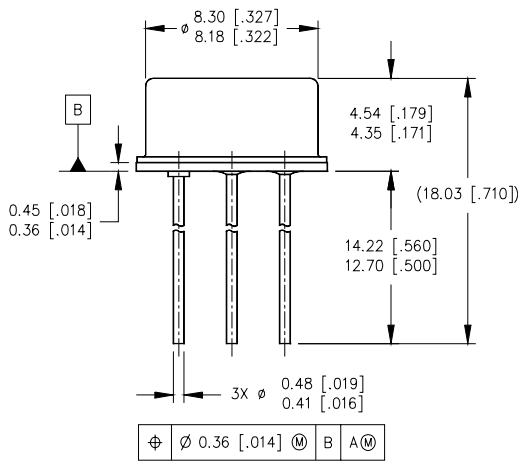


Fig 13b. Gate Charge Test Circuit

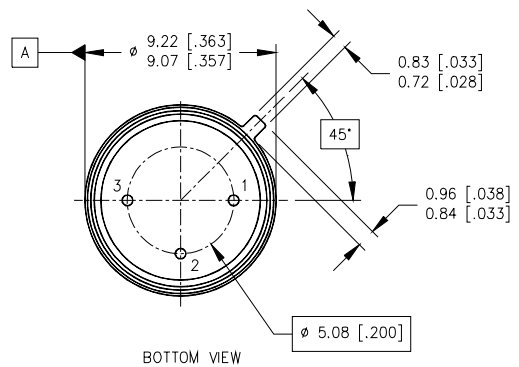
Foot Notes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ C$,
 Peak $I_L = -6.5A$, $V_{GS} = -10V$
- ③ $I_{SD} \leq -6.5A$, $di/dt \leq -140A/\mu s$,
 $V_{DD} \leq -100V$, $T_J \leq 150^\circ C$
 Suggested $R_G = 7.5 \Omega$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$

Case Outline and Dimensions —TO-205AF



SIDE VIEW



BOTTOM VIEW

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. CONTROLLING DIMENSION: INCH.
- 4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN