256Mb C-die NOR FLASH

16M x16, Synch Burst
Multi Bank SLC NOR Flash

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- Initial Draft.	Jul. 2010	Target	-
0.5	- Preliminary datasheet.	14, Oct. 2010	Preliminary	-
0.6	- Added NOTE "Not 100% tested." for parameter "32-word Buffer Programming Time" in 18.4 Erase/Program Performance table.	2, Nov. 2010	Preliminary	-
1.0	- Specification is finalized.	18, Nov. 2010	Final	-

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256M Bit (16M x16) Synch Burst , Multi Bank SLC NOR Flash Memory

1.0 FEATURES

- Single Voltage, 1.7V to 1.95V for Read and Write operations
- Organization
  - 16,777,216 x 16 bit (Word Mode Only)
- Read While Program/Erase Operation
- Multiple Bank Architecture
  - 16 Banks (16Mb Partition)
- OTP Block : Extra 512-Word block
- Read Access Time (@ CL=30pF)
  - Asynchronous Random Access Time : 100ns
  - Synchronous Random Access Time :95ns
  - Burst Access Time :
    11ns(66Mhz) / 9ns(83Mhz) / 7ns (108MHz) / 6ns (133MHz)
- Page Mode Operation
  16Words Page access allows fast asynchronous read
  Page Read Access Time :
  18ns(66/83Mhz) / 15ns(108/133Mhz)
- Burst Length :
  - Continuous Linear Burst
  - Linear Burst : 8-word & 16-word with Wrap
- Block Architecture
  - Uniform block part (K8A(56/57)15EZC) : Two hundred fifty-six 64Kword blocks
  - Boot block part (K8A(56/57)15ET(B)C) : Four 16Kword blocks and two hundred fifty-five 64Kword blocks (Bank 0 contains four 16 Kword blocks and fifteen 64Kword blocks, Bank 1 ~ Bank 15 contain two hundred forty 64Kword blocks)
- Reduce program time using the VPP
- Support 32-word Buffer Program
- Power Consumption (Typical value, CL=30pF)
  - Synchronous Read Current : 35mA
  - Program/Erase Current : 25mA
  - Read While Program/Erase Current : 45mA
  - Standby Mode/Auto Sleep Mode : 30uA
- Block Protection/Unprotection
  - Using the software command sequence
  - Last two boot blocks are protected by WP=VIL
    (Boot block part : K8A(56/57)15ET(B)C)
  - Last one block (BA255) is protected by WP=VIL
    (Uniform block part : K8A(56/57)15EZC)
  - All blocks are protected by VPP=VIL
- Handshaking Feature
  - Provides host system with minimum latency by monitoring RDY
- Erase Suspend/Resume
- Program Suspend/Resume
- Unlock Bypass Program/Erase
- Hardware Reset (RESET)
- Deep Power Down Mode
- Data Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase completion
- Endurance
  - 100K Program/Erase Cycles Minimum
- Extended Temperature : -25°C ~ 85°C
- Support Common Flash Memory Interface
- Output Driver Control by Configuration Register
- Low Vcc Write Inhibit
- Package : TBD

2.0 GENERAL DESCRIPTION

The K8A(56/57)15E featuring single 1.8V power supply is a 256Mbit Burst Multi Bank Flash Memory organized as 16Mx16. The memory architecture of the device is designed to divide its memory arrays into 256 blocks(Uniform block part)/259 blocks(Boot block part) with independent hardware protection. This block architecture provides highly flexible erase and program capability. The K8A(56/57)15E NOR Flash consists of sixteen banks. This device is capable of reading data from one bank while programming or erasing in the other bank.

Regarding read access time, the K8A5615E provides an 11ns burst access time and an 95ns initial access time at 66MHz. At 83MHz, the K8A5615E provides an 9ns burst access time and an 95ns initial access time. At 108MHz, the K8A5715E provides an 7ns burst access time and an 95ns initial access time. At 133MHz, the K8A5715E provides an 6ns burst access time and an 95ns initial access time.

The device performs a program operation in units of 16 bits (Word) and erases in units of a block. Single or multiple blocks can be erased. The block erase operation is completed within typically 0.6sec. The device requires 25mA as program/erase current in the extended temperature ranges.

The K8A(56/57)15E NOR Flash Memory is created by using Samsung's advanced CMOS process technology.

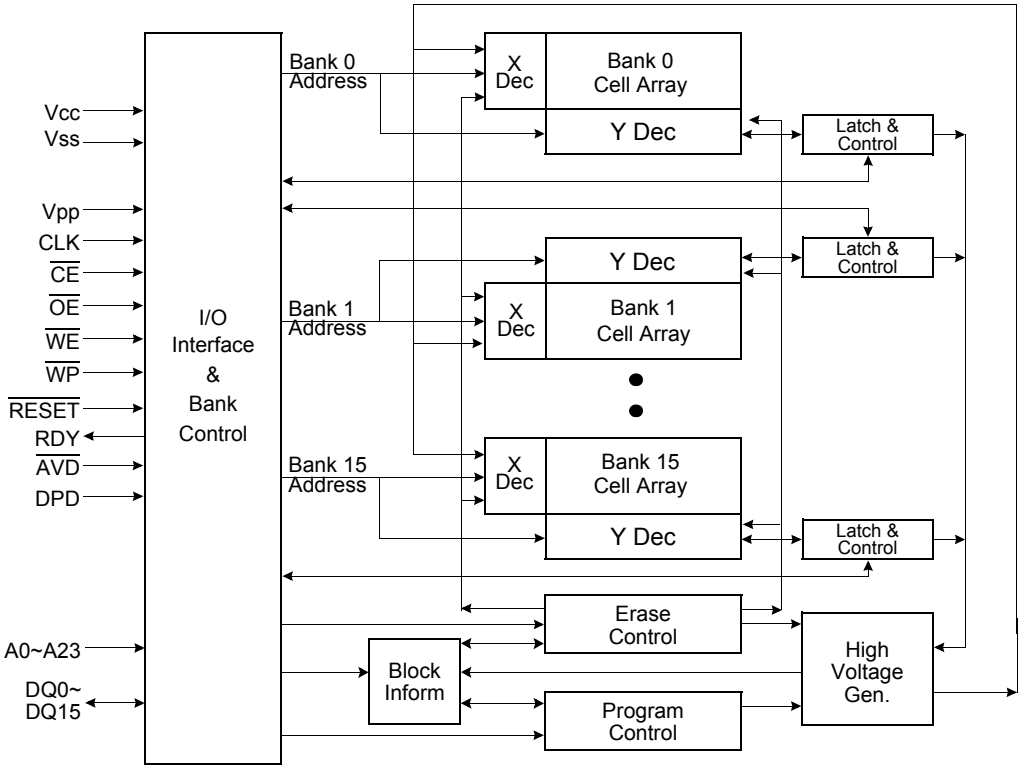
3.0 PIN DESCRIPTION

Pin Name	Pin Function
A0 - A23	Address Inputs
DQ0 - DQ15	Data input/output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset Pin
VPP	Accelerates Programming
$\overline{WE}$	Write Enable
$\overline{WP}$	Hardware Write Protection Input
CLK	Clock
RDY	Ready Output
$\overline{AVD}$	Address Valid Input
DPD	Deep Power Down
Vcc	Power Supply
VSS	Ground

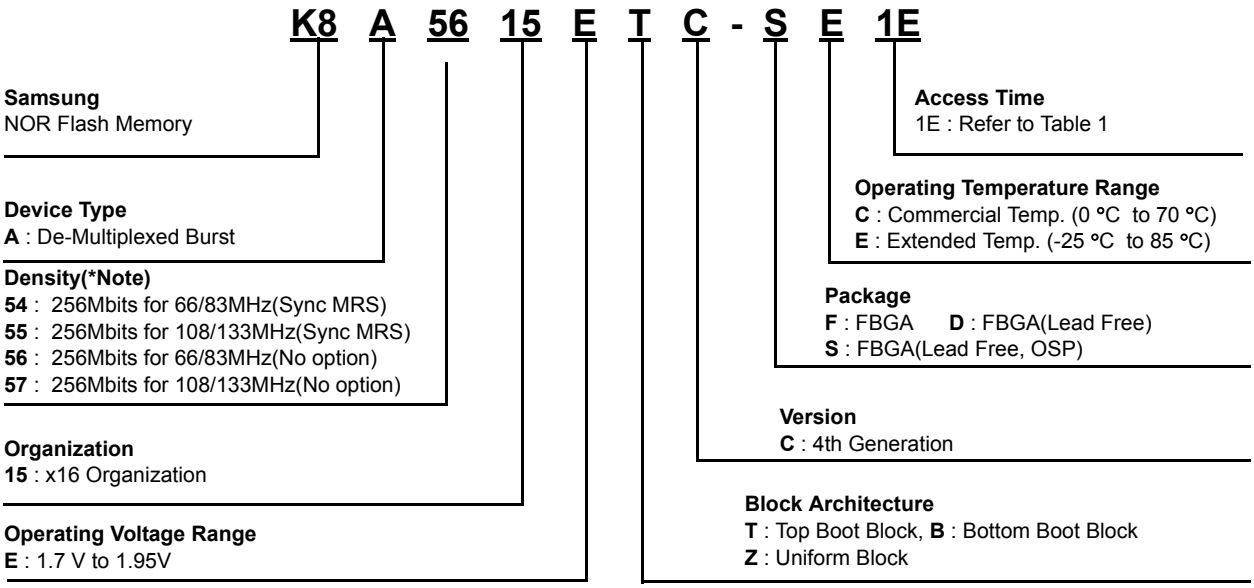
4.0 BALL FBGA TOP VIEW (BALL DOWN)

TBD

5.0 FUNCTIONAL BLOCK DIAGRAM



6.0 ORDERING INFORMATION



NOTE :
Density : (1) 54 : 256Mb for 66/83Mhz with the Sync MRS option
(2) 55 : 256Mb for 108/133Mhz with the Sync MRS option
(3) 56 : 256Mb for 66/83Mhz with no option
(4) 57 : 256Mb for 108/133Mhz with no option

[Table 1] PRODUCT LINE-UP

K8A(56/57)15E						
	Mode	**Speed Option**	**1C (66MHz)**	**1D (83MHz)**	**1E (108MHz)**	**1F (133MHz)**
V_{CC}=1.7V -1.95V	Synchronous/ Burst	Max. Initial Access Time (t_{IAA}, ns)	95	95	95	95
		Max. Burst Access Time (t_{BA}, ns)	11	9	7	6
	Asynchronous	Max. Access Time (t_{AA}, ns)	100	100	100	100
		Max. $\overline{CE}$ Access Time (t_{CE}, ns)	100	100	100	100
		Max. $\overline{OE}$ Access Time (t_{OE}, ns)	15	15	15	15

[Table 2] PRODUCT Classification

Speed/Boot Option	Top	Bottom	Uniform
256Mb for 66/83MHz	K8A5615ETC	K8A5615EBC	K8A5615EZC
256Mb for 108/133MHz	K8A5715ETC	K8A5715EBC	K8A5715EZC

[Table 3] K8A(56/57)15E DEVICE BANK DIVISIONS

Bank 0 ~ Bank 15	
Mbit	**Block Sizes**
256Mbit (Boot block part)	Four 16Kword blocks and two hundred fifty-five 64Kword blocks
256Mbit (Uniform block part)	Two hundred fifty-six 64Kword blocks

[Table 4] K8A(56/57)15EZC DEVICE BANK DIVISIONS (Uniform block)

Bank	Bank size	Quantity of Blocks	Block Size
0	16Mb	16	64 Kwords
1	16Mb	16	64 Kwords
2	16Mb	16	64 Kwords
3	16Mb	16	64 Kwords
4	16Mb	16	64 Kwords
5	16Mb	16	64 Kwords
6	16Mb	16	64 Kwords
7	16Mb	16	64 Kwords
8	16Mb	16	64 Kwords
9	16Mb	16	64 Kwords
10	16Mb	16	64 Kwords
11	16Mb	16	64 Kwords
12	16Mb	16	64 Kwords
13	16Mb	16	64 Kwords
14	16Mb	16	64 Kwords
15	16Mb	16	64 Kwords

[Table 5] K8A(56/57)15ETC DEVICE BANK DIVISIONS (Top Boot block)

Bank	Bank size	Quantity of Blocks	Block Size
0	16Mb	4	16 Kwords
		15	64 Kwords
1	16Mb	16	64 Kwords
2	16Mb	16	64 Kwords
3	16Mb	16	64 Kwords
4	16Mb	16	64 Kwords
5	16Mb	16	64 Kwords
6	16Mb	16	64 Kwords
7	16Mb	16	64 Kwords
8	16Mb	16	64 Kwords
9	16Mb	16	64 Kwords
10	16Mb	16	64 Kwords
11	16Mb	16	64 Kwords
12	16Mb	16	64 Kwords
13	16Mb	16	64 Kwords
14	16Mb	16	64 Kwords
15	16Mb	16	64 Kwords

[Table 6] K8A(56/57)15EBC DEVICE BANK DIVISIONS (Bottom Boot block)

Bank	Bank size	Quantity of Blocks	Block Size
15	16Mb	16	64 Kwords
14	16Mb	16	64 Kwords
13	16Mb	16	64 Kwords
12	16Mb	16	64 Kwords
11	16Mb	16	64 Kwords
10	16Mb	16	64 Kwords
9	16Mb	16	64 Kwords
8	16Mb	16	64 Kwords
7	16Mb	16	64 Kwords
6	16Mb	16	64 Kwords
5	16Mb	16	64 Kwords
4	16Mb	16	64 Kwords
3	16Mb	16	64 Kwords
2	16Mb	16	64 Kwords
1	16Mb	16	64 Kwords
0	16Mb	15	64 Kwords
		4	16 Kwords

7.0 PRODUCT INTRODUCTION

The K8A(56/57)15E is 256Mbit (268,435,456 bits) NOR-type Burst Flash memory. The device features 1.8V single voltage power supply operating within the range of 1.7V to 1.95V. The device is programmed by using the Channel Hot Electron (CHE) injection mechanism which is used to program EPROMs. The device is erased electrically by using Fowler-Nordheim tunneling mechanism. To provide highly flexible erase and program capability, the device adapts a block memory architecture that divides its memory array into 256 blocks (64-Kword x 256 blocks, Uniform block part) / 259 blocks (16-Kword x 4 + 64-Kword x 255, Boot block part). Programming is done in units of 16 bits (Word). Programming is done in units of 16 bits (Word). All bits of data in one or multiple blocks can be erased when the device executes the erase operation. To prevent the device from accidental erasing or over-writing the programmed data, 256 / 259 memory blocks can be hardware protected. Regarding read access time, the K8A5615E provides 11ns burst access time and 95ns initial access time at 66MHz. At the K8A5615E provides 9ns burst access time and 95ns initial access time at 83MHz. At the K8A5715E provides 7ns burst access time and 95ns initial access time at 108MHz. At 133MHz, the K8A5715E provides 6ns burst access time and 95ns initial access time. The command set of K8A(56/57)15E is compatible with standard Flash devices. The device uses Chip Enable (CE), Write Enable (WE), Output Enable (OE) to control asynchronous read and write operation. For burst operations, the device additionally requires Ready (RDY) and Clock (CLK). Device operations are executed by selective command codes. The command codes to be combined with addresses and data are sequentially written to the command registers using microprocessor write timing. The command codes serve as inputs to an internal state machine which controls the program/erase circuitry. Register contents also internally latch addresses and data necessary to execute the program and erase operations. The K8A(56/57)15E is implemented with Internal Program/Erase Routines to execute the program/erase operations. The Internal Program/Erase Routines are invoked by program/erase command sequences. The Internal Program Routine automatically programs and verifies data at specified addresses. The Internal Erase Routine automatically pre-programs the memory cell which is not programmed and then executes the erase operation. The K8A(56/57)15E has means to indicate the status of completion of program/erase operations. The status can be indicated via Data polling of DQ7, or the Toggle bit (DQ6). Once the operations have been completed, the device automatically resets itself to the read mode. The device requires only 35mA as burst and asynchronous mode read current and 25 mA for program/erase operations.

[Table 7] Device Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0-23	DQ0-15	$\overline{RESET}$	CLK	$\overline{AVD}$
Asynchronous Read Operation	L	L	H	Add In	I/O	H	L	L
Write	L	H	⊓	Add In	I/O	H	L	X
Standby	H	X	X	X	High-Z	H	X	X
Hardware Reset	X	X	X	X	High-Z	L	X	X
Load Initial Burst Address	L	H	H	Add In	X	H	↑	⊓
Burst Read Operation	L	L	H	X	Burst DOUT	H	↑	H
Terminate Burst Read Cycle	H	X	X	X	High-Z	H	X	X
Terminate Burst Read Cycle via $\overline{RESET}$	X	X	X	X	High-Z	L	X	X
Terminate Current Burst Read Cycle and Start New Burst Read Cycle	L	H	H	Add In	I/O	H	↑	⊓

NOTE : L=VIL (Low), H=VIH (High), X=Don't Care.

8.0 COMMAND DEFINITIONS

The K8A(56/57)15E operates by selecting and executing its operational modes. Each operational mode has its own command set. In order to select a certain mode, a proper command with specific address and data sequences must be written into the command register. Writing incorrect information which include address and data or writing an improper command will reset the device to the read mode. The defined valid register command sequences are stated in Table 8.

[Table 8] Command Sequences

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Asynchronous Read	Add	1	RA					
	Data		RD					
Reset [5),20)]	Add	1	XXXH					
	Data		F0H					
Autoselect Manufacturer ID [6)]	Add	4	555H	2AAH	(DA)555H	(DA)X00H		
	Data		AAH	55H	90H	ECH		
Autoselect Device ID [6)]	Add	4	555H	2AAH	(DA)555H	(DA)X01H		
	Data		AAH	55H	90H	Note6		
Autoselect Block Protection Verify [7)]	Add	4	555H	2AAH	(BA)555H	(BA)X02H		
	Data		AAH	55H	90H	00H/01H		
Autoselect Handshaking[6), 8)]	Add	4	555H	2AAH	(DA)555H	(DA)X03H		
	Data		AAH	55H	90H	0H/1H		
Program	Add	4	555H	2AAH	555H	PA		
	Data		AAH	55H	A0H	PD		
Unlock Bypass	Add	3	555H	2AAH	555H			
	Data		AAH	55H	20H			
Unlock Bypass Program[9)]	Add	2	XXX	PA				
	Data		A0H	PD				
Unlock Bypass Block Erase [9)]	Add	2	XXX	BA				
	Data		80H	30H				
Unlock Bypass Chip Erase [9)]	Add	2	XXXH	XXXH				
	Data		80H	10H				
Unlock Bypass Reset	Add	2	XXXH	XXXH				
	Data		90H	00H				
Chip Erase	Add	6	555H	2AAH	555H	555H	2AAH	555H
	Data		AAH	55H	80H	AAH	55H	10H
Block Erase	Add	6	555H	2AAH	555H	555H	2AAH	BA
	Data		AAH	55H	80H	AAH	55H	30H
Erase Suspend [10)]	Add	1	(DA)XXXH					
	Data		B0H					
Erase Resume [11)]	Add	1	(DA)XXXH					
	Data		30H					
Program Suspend [12)]	Add	1	(DA)XXXH					
	Data		B0H					
Program Resume [11)]	Add	1	(DA)XXXH					
	Data		30H					
Block Protection/Unprotection [13)]	Add	3	XXX	XXX	ABP			
	Data		60H	60H	60H			
CFI Query [14)]	Add	1	(DA)X55H					
	Data		98H					

Command Definitions		Cycle	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
Write to Buffer 15)	Add	3	555H	2AAH	BA	BA	PA	WBL
	Data		AAH	55H	25H	WC	PD	PD
Program buffer to Flash 15)	Add	1	BA					
	Data		29H					
Write to Buffer Abort Reset 16),19)	Add	3	555H	2AAH	XXX			
	Data		AAH	55H	F0H			
Set Burst Mode Configuration Register 17),18)	Add	3	555H	2AAH	Note 18			
	Data		AAH	55H	C0H			
Enter OTP Block Region	Add	3	555H	2AAH	XXX			
	Data		AAH	55H	70H			
Exit OTP Block Region	Add	4	555H	2AAH	555H	XXX		
	Data		AAH	55H	75H	00H		

NOTE :

1) RA : Read Address , PA : Program Address, RD : Read Data, PD : Program Data , BA : Block Address (A23 ~ A14), DA : Bank Address (A23 ~ A20)
ABP : Address of the block to be protected or unprotected , CR : Configuration Register Setting
WBL : Write Buffer Location, WC : Word Count
2) The 4th cycle data of autoselect mode and RD are output data. The others are input data.
3) Data bits DQ15–DQ8 are don't care in command sequences, except for RD, PD and Device ID.
4) Unless otherwise noted, address bits A23–A11 are don't cares.
5) The reset command is required to return to read mode.
If a bank entered the autoselect mode during the erase suspend mode, writing the reset command returns that bank to the erase suspend mode.
If a bank entered the autoselect mode during the program suspend mode, writing the reset command returns that bank to the program suspend mode.
If DQ5 goes high during the program or erase operation, writing the reset command returns that bank to read mode or erase suspend mode if that bank was in erase suspend mode.
6) The 3rd and 4th cycle bank address of autoselect mode must be same.
Device ID Data : "2206H" for Top Boot Block Device, "2207H" for Bottom Boot Block Device, "301BH" for Uniform Block Device
7) Normal Block Protection Verify : 00H for an unprotected block and 01H for a protected block.
OTP Block Protect verify (with OTP Block Address after Entering OTP Block) : 00H for unlocked, and 01H for locked.
8) 0H for handshaking, 1H for non-handshaking
9) The unlock bypass command sequence is required prior to this command sequence.
10) The system may read and program in non-erasing blocks when in the erase suspend mode.
The system may enter the autoselect mode when in the erase suspend mode.
The erase suspend command is valid only during a block erase operation, and requires the bank address.
11) The erase/program resume command is valid only during the erase/program suspend mode, and requires the bank address.
12) This mode is used only to enable Data Read by suspending the Program operation.
13) Set ABP(Address of the block to be protected or unprotected) as either A6 = VIH, A1 = VIH and A0 = VIL for unprotected or A6 = VIL, A1 = VIH and A0 = VIL for protected.
14) Command is valid when the device is in Read mode or Autoselect mode.
15) For Buffer Program, Firstly Enter "Write to Buffer" Command sequence and then Enter Block Address and Word Count which is the number of word data will be programmed. Word Count is smaller than the number of data wanted to program by one, Example if 15 words are wanted to program then WC (Word Count) is 14. After Entering Command, Enter PA/PD's (Program Addresses/ Program Data). Finally Enter "Program buffer to Flash" Command sequence, This starts a buffer program operation. This Device supports 32-word Buffer Program.
There is some caution points.
- The number of PA/PD's which are entered must be same to WC+1
- PA's which are entered must be same A23~A5 address bits because Buffer Address is A23~A5 address and decided by PA entered firstly.
- If PA which are entered isn't same Buffer Address, then PA/PD which is entered may be ignored and this buffer programming operation is aborted. To return to normal operation, hardware reset or "Write to Buffer Abort Reset" command is issued.
- Overwrite for program buffer is also prohibited.
16) Command sequence resets device for next command after aborted write-to-buffer operation.
17) See "Set Burst Mode Configuration Register" for details.
18) On the third cycle, the data should be "C0h", address bits A10-A0 should be 101_0101_0101b, and address bits A21-A11 set the code to be latched.
19) After software reset and write to buffer abort reset command, min. 5us recovery time is needed for normal read mode.

9.0 DEVICE OPERATION

The device has inputs/outputs that accept both address and data information. To write a command or command sequence (which includes programming data to the device and erasing blocks of memory), the system must drive CLK, WE and CE to VIL and OE to VIH when writing commands or data. The device provides the unlock bypass mode to save its program time for program operation. Unlike the standard program command sequence which is comprised of four bus cycles, only two program cycles are required to program a word in the unlock bypass mode. One block, multiple blocks, or the entire device can be erased. Table 16 indicates the address space that each block occupies. The device's address space is divided into sixteen banks. A "bank address" is the address bits required to uniquely select a bank. Similarly, a "block address" is the address bits required to uniquely select a block. ICC2 in the DC Characteristics table represents the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

9.1 Read Mode

The device automatically enters to asynchronous read mode after device power-up. For synchronous read, the device needs to be set mode register prior to read operation. After completing an Internal Program/Erase Routine, each bank is ready to read array data. The reset command is required to return a bank to the read(or erase-suspend-read)mode if DQ5 goes high during an active program/erase operation, or if the bank is in the autoselect mode.

(1) K8A5415ET(B)(Z)C : 66/83Mhz with the Sync MRS option
(2) K8A5515ET(B)(Z)C : 108/133Mhz with the Sync MRS option
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while $\overline{AVD}$ is held low *after Burst Mode Configuration Register Setting to A19=1.* If several CLKs exist in $\overline{AVD}$ low, the last rising edge is valid CLK.

(3) K8A5615ET(B)(Z)C : 66/83Mhz with no option
(4) K8A5715ET(B)(Z)C : 108/133Mhz with no option
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while $\overline{AVD}$ is held low. If several CLKs exist in $\overline{AVD}$ low, the last rising edge is valid CLK.

9.1.1 Asynchronous Read Mode

For the asynchronous read mode a valid address should be asserted on A0-A23, while driving $\overline{AVD}$ and CE to VIL. WE should remain at VIH. The data will appear on DQ0-DQ15. Since the memory array is divided into sixteen banks, each bank remains enabled for read access until the command register contents are altered.
Address access time (tAA) is equal to the delay from valid addresses to valid output data. The chip enable access time(tCE) is the delay from the falling edge of CE to valid data at the outputs. The output enable access time(tOE) is the delay from the falling edge of OE to valid data at the output. To prevent the memory content from spurious altering during power transition, the initial state machine is set for reading array data upon device power-up, or after a hardware reset.

9.1.1.1 Asynchronous Page Read Mode

16-Words Page mode is supported for fast asynchronous read. After address access time(tAA), sixteen data words are loaded into an internal page buffer. A0~A3 bits determine which page word is output during a read operation. A4~A23 and $\overline{AVD}$ must be stable throughout the page read access. Figure 11 shows the Asynchronous Page Read Mode timing.

9.1.2 Synchronous (Burst) Read Mode

The device is capable of continuous linear burst operation and linear burst operation of a preset length. For the burst mode, the system should determine how many clock cycles are desired for the initial word(tIAA) of each burst access and what mode of burst operation is desired using "Burst Mode Configuration Register" command sequences. See "Set Burst Mode Configuration" for further details. The status data also can be read during burst read mode by using $\overline{AVD}$ signal with a bank address which is programming or erasing. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation.

9.1.2.1 Continuous Linear Burst Read

(1) K8A5415ET(B)(Z)C : 66/83Mhz with the Sync MRS option
(2) K8A5515ET(B)(Z)C : 108/133Mhz with the Sync MRS option
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while $\overline{AVD}$ is held low *after Burst Mode Configuration Register Setting to A19=1.* If several CLKs exist in $\overline{AVD}$ low, the last rising edge is valid CLK.

(3) K8A5615ET(B)(Z)C : 66/83Mhz with no option
(4) K8A5715ET(B)(Z)C : 108/133Mhz with no option
The synchronous(burst) mode will automatically start on the rising edge of the CLK input while $\overline{AVD}$ is held low. If several CLKs exist in $\overline{AVD}$ low, the last rising edge is valid CLK.

The initial word is output tIAA after the rising edge of the last CLK cycle. Subsequent words are output tBA after the rising edge of each successive clock

cycle, which automatically increase the internal address counter. Note that the device has internal address boundary that occurs every 16 words. When the device is crossing the first word boundary, additional clock cycles are needed before data appears for the next address. The number of additional clock cycle can vary from zero to thirteen cycles, and the exact number of additional clock cycle depends on the starting address of burst read. The RDY output indicates this condition to the system by pulsing low. The device will continue to output sequential burst data, wrapping around to address 0000000h after it reaches the highest addressable memory location until the system asserts CE high, RESET low or $\overline{AVD}$ low in conjunction with a new address.(Refer to Table 7.) The reset command does not terminate the burst read operation. When it accesses the bank is programming or erasing, continuous burst read mode will output status data. And status data will be sustained until the system asserts CE high or RESET low or $\overline{AVD}$ low in conjuction with a new address. Note that at least 10ns is needed to start next burst read operation from terminating previous burst read operation in the case of asserting CE high.

8-, 16-Word Linear Burst Read

As well as the Continuous Linear Burst Mode, there are two(8 & 16 word) linear wrap, in which a fixed number of words are read from consecutive addresses. In these modes, the addresses for burst read are determined by the group within which the starting address falls. The groups are sized according to the number of words read in a single burst sequence for a given mode. (Refer to Table 9)

[Table 9] Burst Address Groups(Wrap mode)

Burst Mode	Group Size	Group Address Ranges
8 word	8 words	0-7h, 8-Fh, 10-17h, ...
16 word	16 words	0-Fh, 10-1Fh, 20-2Fh, ...

As an example: In wrap mode case, if the starting address in the 8-word mode is 2h, the address range to be read would be 0-7h, and the wrap burst sequence would be 2-3-4-5-6-7-0-1h. The burst sequence begins with the starting address written to the device, but wraps back to the first address in the selected group. In a similar manner, 16-word wrap mode begins its burst sequence on the starting address written to the device, and then wrap back to the first address in the selected address group.

9.2 Programmable Wait State

The programmable wait state feature indicates to the device the number of additional clock cycles that must elapse after $\overline{AVD}$ is driven from low to high for burst read mode. Upon power up, the number of total initial access cycles defaults to fourteen.

9.3 Handshaking

The handshaking feature allows the host system to simply monitor the RDY signal from the device to determine when the initial word of burst data is ready to be read. To set the number of initial cycle for optimal burst mode, the host should use the programmable wait state configuration.(See "Set Burst Mode Configuration Register" for details.) The rising edge of RDY after OE goes low indicates the initial word of valid burst data.(RDY can be low active by Extended configuration register A11 settng : RDY low indicates data valid) Using the autoselect command sequence, the handshaking feature will be verified in the device.

9.4 Set Burst Mode Configuration Register

The device uses a configuration register to set the various burst parameters : the number of initial cycles for burst and burst read mode. The burst mode configuration register must be set before the device enters burst mode. The burst mode configuration register is loaded with a three-cycle command sequences. On the third cycle, the data should be C0h, address bits A10-A0 should be 101_0101_0101b, and address bits A21-A11 set the code to be latched. The device returns to default setting after power up or hardware reset.

9.4.1 Programmable Wait State Configuration

This feature informs the device the number of clock cycles that must elapse after $\overline{AVD}$ is driven from low to high before data will be available. This value is determined by the input frequency of the device. Address bits A14-A11 determine the setting. (See Configuration Register Table 10.) The Programmable wait state setting instructs the device to set a particular number of clock cycles for the initial access in burst mode. Note that hardware reset will revert the wait state to the default setting, that is 14 initial cycles.

9.4.2 Burst Read Mode Setting

The device supports three different burst read modes : continuous linear mode, 8 and 16 word linear burst modes with wrap.

9.4.3 RDY Configuration

By default, the RDY pin will be high whenever there is valid data on the output. (RDY can be low active by configuration register A11 settng : RDY low indicates data valid) The device can be set so that RDY goes active one data cycle before active data. Address bit A18 determines this setting. The RDY pin behaves same way in word boundary crossing case.

[Table 10] Burst Mode Configuration Register Table : K8A54(55)15ET(B)(Z)C : 66/83/108/133Mhz with the Sync MRS option

Address Bit	Function	Settings(Binary)
A19	Read Mode	1 = Synchronous Burst Read Mode 0 = Asynchronous Read Mode (default)
A18	RDY Active	1 = RDY active one clock cycle before data 0 = RDY active with data(default)
A17 A16 A15	Burst Read Mode	000 = Continuous(default) 001 = 8-word linear with wrap 010 = 16-word linear with wrap 011~111 = Reserve
A14 A13 A12 A11	Programmable Wait State	0000 = Data is valid on the 4th active CLK edge after $\overline{AVD}$ transition to VIH 0001 = Data is valid on the 5th active CLK edge after $\overline{AVD}$ transition to VIH (40Mhz*) 0010 = Data is valid on the 6th active CLK edge after $\overline{AVD}$ transition to VIH (50/54Mhz*) 0011 = Data is valid on the 7th active CLK edge after $\overline{AVD}$ transition to VIH (60/66Mhz*) 0100 = Data is valid on the 8th active CLK edge after $\overline{AVD}$ transition to VIH (70Mhz*) 0101 = Data is valid on the 9th active CLK edge after $\overline{AVD}$ transition to VIH (80/83Mhz*) 0110 = Data is valid on the 10th active CLK edge after $\overline{AVD}$ transition to VIH (90/100Mhz*) 0111 = Data is valid on the 11th active CLK edge after $\overline{AVD}$ transition to VIH (108/110Mhz*) 1000 = Data is valid on the 12th active CLK edge after $\overline{AVD}$ transition to VIH (120Mhz*) 1001 = Data is valid on the 13th active CLK edge after $\overline{AVD}$ transition to VIH (133Mhz*,default) 1010 = Data is valid on the 14th active CLK edge after $\overline{AVD}$ transition to VIH 1011 = Data is valid on the 15th active CLK edge after $\overline{AVD}$ transition to VIH

NOTE :
Initial wait state should be set according to it's clock frequency. Table 10 recommend the program wait state for each clock frequencies.
Not 100% tested

[Table 11] Burst Mode Configuration Register Table : K8A56(57)15ET(B)(Z)C : 66/83/108/133Mhz with no option

Address Bit	Function	Settings(Binary)
A18	RDY Active	1 = RDY active one clock cycle before data 0 = RDY active with data(default)
A17 A16 A15	Burst Read Mode	000 = Continuous(default) 001 = 8-word linear with wrap 010 = 16-word linear with wrap 011~111 = Reserve
A14 A13 A12 A11	Programmable Wait State	0000 = Data is valid on the 4th active CLK edge after $\overline{AVD}$ transition to VIH 0001 = Data is valid on the 5th active CLK edge after $\overline{AVD}$ transition to VIH (40Mhz*) 0010 = Data is valid on the 6th active CLK edge after $\overline{AVD}$ transition to VIH (50/54Mhz*) 0011 = Data is valid on the 7th active CLK edge after $\overline{AVD}$ transition to VIH (60/66Mhz*) 0100 = Data is valid on the 8th active CLK edge after $\overline{AVD}$ transition to VIH (70Mhz*) 0101 = Data is valid on the 9th active CLK edge after $\overline{AVD}$ transition to VIH (80/83Mhz*) 0110 = Data is valid on the 10th active CLK edge after $\overline{AVD}$ transition to VIH (90/100Mhz*) 0111 = Data is valid on the 11th active CLK edge after $\overline{AVD}$ transition to VIH (108/110Mhz*) 1000 = Data is valid on the 12th active CLK edge after $\overline{AVD}$ transition to VIH (120Mhz*) 1001 = Data is valid on the 13th active CLK edge after $\overline{AVD}$ transition to VIH (133Mhz*,default) 1010 = Data is valid on the 14th active CLK edge after $\overline{AVD}$ transition to VIH 1011 = Data is valid on the 15th active CLK edge after $\overline{AVD}$ transition to VIH

[Table 12] Burst Address Sequences

	Start Addr.	Burst Address Sequence		
		Continuous Burst	8-word Burst	16-word Burst
Wrap	0	0-1-2-3-4-5-6...	0-1-2-3-4-5-6-7	0-1-2-3 ... -D-E-F
	1	1-2-3-4-5-6-7...	1-2-3-4-5-6-7-0	1-2-3-4 ... -E-F-0
	2	2-3-4-5-6-7-8...	2-3-4-5-6-7-0-1	2-3-4-5 ... -F-0-1
	. .	. .	. .	. .

9.5 Autoselect Mode

By writing the autoselect command sequences to the system, the device enters the autoselect mode. This mode can be read only by asynchronous read mode. The system can then read autoselect codes from the internal register(which is separate from the memory array). Standard asynchronous read cycle timings apply in this mode. The device offers the Autoselect mode to identify manufacturer and device type by reading a binary code. In addition, this mode allows the host system to verify the block protection or unprotection. Table 13 shows the address and data requirements. The autoselect command sequence may be written to an address within a bank that is in the read mode, erase-suspend-read mode or program-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the device. The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the address and the autoselect command. Note that the block address is needed for the verification of block protection. The system may read at any address within the same bank any number of times without initiating another autoselect command sequence. And the burst read should be prohibited during Autoselect Mode. To terminate the autoselect operation, write Reset command(F0H) into the command register.

[Table 13] Autoselect Mode Description

Description	Address	Read Data
Manufacturer ID	(DA) + 00H	ECH
Device ID	(DA) + 01H	2206H (Top Boot Block), 2207H (Bottom Boot Block), 301BH (Uniform Block)
Block Protection/Unprotection	(BA) + 02H	01H (protected), 00H (unprotected)
Handshaking	(DA) + 03H	0H : handshaking, 1H : non-handshaking

9.6 Standby Mode

When the CE inputs is held at VCC ± 0.2V, and the system is not reading or writing, the device enters Stand-by mode to minimize the power consumption. In this mode, the device outputs are placed in the high impedence state, independent of the OE input. When the device is in either of these standby modes, the device requires standard access time (tCE) for read access before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. ICC5 in the DC Characteristics table represents the standby current specification.

9.7 Automatic Sleep Mode

The device features Automatic Sleep Mode to minimize the device power consumption during both asynchronous and burst mode. When addresses remain stable for tAA+60ns, the device automatically enables this mode. The Automatic sleep mode is depends on the CE, WE and OE signal, so CE, WE and OE signals are held at any state. In a sleep mode, output data is latched and always available to the system. When OE is active, the device provides new data without wait time. Automatic sleep mode current is equal to standby mode current.

9.8 Output Disable Mode

When the OE input is at VIH , output from the device is disabled. The outputs are placed in the high impedance state.

9.9 Block Protection & Unprotection

To protect the block from accidental writes, the block protection/unprotection command sequence is used. On power up, all blocks in the device are protected. To unprotect a block, the system must write the block protection/unprotection command sequence. The first two cycles are written: addresses are don't care and data is 60h. Using the third cycle, the block address (ABP) and command (60h) is written, while specifying with addresses A6, A1 and A0 whether that block should be protected (A6 = VIL, A1 = VIH, A0 = VIL) or unprotected (A6 = VIH, A1 = VIH, A0 = VIL). After the third cycle, the system can continue to protect or unprotect additional cycles, or exit the sequence by writing F0h (reset command).
The device offers three types of data protection at the block level:

- The block protection/unprotection command sequence disables or re-enables both program and erase operations in any block.
- When WP is at VIL, the two outermost blocks are protected.(Boot block part : K8A(54/55/56/57)15ET(B)C)
- When WP is at VIL, the last one block (BA255) is protected.(Uniform block part :K8A(54/55/56/57)15EZC)
- When VPP is at VIL, all blocks are protected.

Note that user never float the Vpp and WP, that is, Vpp is always connected with VIH, VIL or VID and WP is VIH or VIL.

9.10 Hardware Reset

The device features a hardware method of resetting the device by the RESET input. When the RESET pin is held low(VIL) for at least a period of tRP, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write commands for the duration of the RESET pulse.

The device also resets the internal state machine to asynchronous read mode. To ensure data integrity, the interrupted operation should be reinitiated once the device is ready to accept another command sequence. The RESET pin may be tied to the system reset pin. If a system reset occurs during the Internal Program or Erase Routine, the device will be automatically reset to the asynchronous read mode; this will enable the systems microprocessor to read the boot-up firmware from the Flash memory. If RESET is asserted during a program or erase operation, the device requires a time of tREADY (during Internal Routines) before the device is ready to read data again. If RESET is asserted when a program or erase operation is not executing, the reset operation is completed within a time of tREADY (not during Internal Routines). tRH is needed to read data after RESET returns to VIH. Refer to the AC Characteristics tables for RESET parameters and to Figure 12 for the timing diagram. When RESET is at logic high, the device is in standard operation. When RESET transitions from logic-low to logic-high, the device resets all blocks to locked and defaults to the read array mode.

9.11 Software Reset

The reset command provides that the bank is reseted to read mode, erase-suspend-read mode or program-suspend-read mode. The addresses are in Don't Care state. The reset command may be written between the sequence cycles in an erase command sequence before erasing begins, or in an program command sequence before programming begins. If the device begins erasure or programming, the reset command is ignored until the operation is completed. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. The reset command valid between the sequence cycles in an autoselect command sequence. In an autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Also, if a bank entered the autoselect mode while in the Program Suspend mode, writing the reset command returns that bank to the program-suspend-read mode. If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode. (or erase-suspend-read mode if the bank was in Erase Suspend)

9.12 Program

The K8A(56/57)E can be programmed in units of a word. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings. During the Internal Program Routine, commands written to the device will be ignored.
Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

9.13 Accelerated Program

The device provides accelerated program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When VID is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. In accelerated program mode, the system would use a two-cycle program command sequence for only a word program. By removing VID returns the device to normal operation mode.
Note that Read While Accelerated Program(Erase) and Program suspend(Erase suspend) mode are not guaranteed.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : TA = 30°C±10°C

9.14 Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 32-word in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initi-ated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the block address in which programming will occur. The fourth cycle writes the block address and the number of word locations, minus one, to be programmed. For example, if the system will program 19 unique address locations, then 12h should be written to the device. This tells the device how many write buffer addresses will be loaded with data. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A23(max.) ~ A5 entered at fifth cycle. All subsequent address/ data pairs must fall within the selected write-buffer-page, so that all subsequent addresses must have the same address bit A23(max.) ~ A5 as those entered at fifth cycle. Write buffer locations may be loaded in any order.
Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" com mand at the block address. Any other command address/data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming. The write-buffer programming operation can be suspended using the standard program suspend/ resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.
Note also that an address loaction cannot be loaded more than once into the write-buffer-page.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Loading a value that is greater than the buffer size(32-word) during then number of word locations to Program step.
  (In case, WC > 1FH @Table 8)
- The number of Program address/data pairs entered is different to the number of word locations initially defined with WC (@ Table 8)

- Writing a Program address to have a different write-buffer-page with selected write-buffer-page (Address bits A23(max) ~ A5 are different)
- Writing non-exact "Program Buffer to Flash" command

The abort condition is indicated by DQ1 = 1, DQ7 = DATA (for the last address location loaded), DQ6 = toggle, and DQ5=0. A "Write-to-Buffer-Abort Reset" command sequence must be written to reset the device for the next operation. Note that the third cycle of Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

And from the third cycle to the last cycle of Write to Buffer command is also required when using Write-Buffer-Programming features in Unlock Bypass mode. A bit cannot be programmed from “0” back to a “1.” Attempting to do so may cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still “0.” Only erase operations can convert a “0” to a “1."

9.15 Accelerated Write Buffer Programming

The device provides accelerated Write Buffer Program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When VID is asserted on the Vpp input, the device temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. In accelerated Write Buffer Program mode, the system must enter "Write to Buffer" and "Program Buffer to Flash" command sequence to be same as them of normal Write Buffer Programming. Note that the third cycle of "Write to Buffer Abort Reset" command sequence is required in an accelerated mode.

Note that Read While Accelerated Write Buffer Program and Program suspend mode are not guaranteed.

- Program/Erase cycling must be limited below 100cycles for optimum performance.
- Ambient temperature requirements : TA = 30°C±10°C

9.16 Chip Erase

To erase a chip is to write 1′s into the entire memory array by executing the Internal Erase Routine. The Chip Erase requires six bus cycles to write the command sequence. The erase set-up command is written after first two "unlock" cycles. Then, there are two more write cycles prior to writing the chip erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory for an all zero data pattern prior to erasing. The automatic erase begins on the rising edge of the last WE pulse in the command sequence and terminates when DQ7 is "1". After that the device returns to the read mode.

9.17 Block Erase

To erase a block is to write 1′s into the desired memory block by executing the Internal Erase Routine. The Block Erase requires six bus cycles to write the command sequence shown in Table 8. After the first two "unlock" cycles, the erase setup command (80H) is written at the third cycle. Then there are two more "unlock" cycles followed by the Block Erase command. The Internal Erase Routine automatically pre-programs and verifies the entire memory prior to erasing it. Multiple blocks can be erased sequentially by writing the sixth bus-cycle. Upon completion of the last cycle for the Block Erase, additional block address and the Block Erase command (30H) can be written to perform the Multi-Block Erase. For the Multi-Block Erase, only sixth cycle(block address and 30H) is needed.(Similarly, only second cycle is needed in unlock bypass block erase.) An 50us (typical) "time window" is required between the Block Erase command writes. The Block Erase command must be written within the 50us "time window", otherwise the Block Erase command will be ignored. The 50us "time window" is reset when the falling edge of the WE occurs within the 50us of "time window" to latch the Block Erase command. During the 50us of "time window", any command other than the Block Erase or the Erase Suspend command written to the device will reset the device to read mode. After the 50 us of "time window", the Block Erase command will initiate the Internal Erase Routine to erase the selected blocks. Any Block Erase address and command following the exceeded "time window" may or may not be accepted. No other commands will be recognized except the Erase Suspend command during Block Erase operation.

9.18 Unlock Bypass

The K8A(56/57)E provides the unlock bypass mode to save its operation time. This mode is possible for program, block erase, chip erase, write to buffer and write to buffer abort reset operation. There are two methods to enter the unlock bypass mode. The mode is invoked by the unlock bypass command sequence or the assertion of VID on VPP pin. Unlike the standard program/erase command sequence that contains four bus cycles, the unlock bypass program/erase command sequence comprises only two bus cycles. The unlock bypass mode is engaged by issuing the unlock bypass command sequence which is comprised of three bus cycles. Writing first two unlock cycles is followed by a third cycle containing the unlock bypass command (20H). Once the device is in the unlock bypass mode, the unlock bypass program/erase command sequence is necessary. The unlock bypass program command sequence is comprised of only two bus cycles; writing the unlock bypass program command (A0H) is followed by the program address and data. This command sequence is the only valid one for programming the device in the unlock bypass mode. Also, The unlock bypass erase command sequence is comprised of two bus cycles; writing the unlock bypass block erase command(80H-30H) or writing the unlock bypass chip erase command(80H-10H). This command sequences are the only valid ones for erasing the device in the unlock bypass mode. The unlock bypass reset command sequence is the only valid command sequence to exit the unlock bypass mode. The unlock bypass reset command sequence consists of two bus cycles. The first cycle must contain the data (90H). The second cycle contains only the data (00H). Then, the device returns to the read mode.

To enter the unlock bypass mode in hardware level, the VID also can be used. By assertion VID on the VPP pin, the device enters the unlock bypass mode. Also, the all blocks are temporarily unprotected when the device using the VID for unlock bypass mode. To exit the unlock bypass mode, just remove the asserted VID from the VPP pin.(Note that user never float the Vpp, that is, Vpp is always connected with VIH, VIL or VID.).

9.19 Erase Suspend / Resume

The Erase Suspend command interrupts the Block Erase to read or program data in a block that is not being erased. Also, it is possible to protect or unprotect of the block that is not being erased in erase suspend mode. The Erase Suspend command is only valid during the Block Erase operation including the time window of 50us. The Erase Suspend command is not valid while the Chip Erase or the Internal Program Routine sequence is running. When the Erase Suspend command is written during a Block Erase operation, the device requires a maximum of 30us(recovery time) to suspend the erase operation. Therefore system must wait for 30us(recovery time) to read the data from the bank which include the block being erased. Otherwise, system can read the data immediately from a bank which don't include the block being erased without recovery time(max. 30us) after Erase Suspend command. And, after the maximum 30us recovery time, the device is availble for programming data in a block that is not being erased. But, when the Erase Suspend command is written during the block erase time window (50us), the device terminates the block erase time window and suspends the erase operation in about 2us. The system may also write the autoselect command sequence when the device is in the Erase Suspend mode. When the Erase Resume command is executed, the Block Erase operation will resume. When the Erase Suspend or Erase Resume command is executed, the addresses are in the bank address which is operating in Erase Suspend or Erase Resume. While erase can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.

9.20 Program Suspend / Resume

The device provides the Program Suspend/Resume mode. This mode is used to enable Data Read by suspending the Program operation. The device accepts a Program Suspend command in Program mode(including Program operations performed during Erase Suspend) but other commands are ignored. After input of the Program Suspend command, 10us is needed to enter the Program Suspend Read mode. Therefore system must wait for 10us(recovery time) to read the data from the bank which include the block being programmed. Otherwise, system can read the data immediately from a bank which don't include block being programmed without recovery time(max. 10us) after Program Suspend command. Like an Erase Suspend mode, the device can be returned to Program mode by using a Program Resume command. In the program suspend mode, protect/unprotect command is prohibited.
While program can be suspended and resumed multiple times, a minimum 30us is required from resume to the next suspend.

9.21 Read While Write Operation

The device is capable of reading data from one bank while writing in the other banks. This is so called the Read While Write operation. An erase operation may also be suspended to read from or program to another location within the same bank(except the block being erased). The Read While Write operation is prohibited during the chip erase operation. Figure 19 shows how read and write cycles may be initiated for simultaneous operation with zero latency. Refer to the DC Characteristics table for read-while-write current specifications.

9.22 OTP Block Region

The OTP Block feature provides a 512-word Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The OTP Block is customer lockable and shipped with itself unlocked, allowing customers to untilize the that block in any manner they choose. The customer-lockable OTP Block has the Protection Verify Bit (DQ0) set to a "0" for Unlocked state or a "1" for Locked state.
The system accesses the OTP Block through a command sequence (see "Enter OTP Block / Exit OTP Block Command sequence" at Table 8). After the system has written the "Enter OTP Block" Command sequence, it may read the OTP Block by using the addresses (FFFE00h~FFFFFFh : Top Boot block device/Uniform block device, 000000h-0001FFh : Bottom Boot block device) normally and may check the Protection Verify Bit (DQ0) by using the "Autoselect Block Protection Verify" Command sequence with OTP Block address. This mode of operation continues until the system issues the "Exit OTP Block" Command suquence, a hardware reset or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to main blocks. Note that the Accelerated function and unlock bypass modes are not available when the OTP Block is enabled.

Customer Lockable
In a Customer lockable device, The OTP Block is one-time programmable and can be locked only once. Note that the Accelerated programming and Unlock bypass functions are not available when programming the OTP Block. Locking operation to the OTP Block is started by writing the "Enter OTP Block" Command sequence, and then the "Block Protection" Command seqeunce (Table 8) with an OTP Block address. The Locking operation has to be above 100us. "Exit OTP Block" commnad sequence and Hardware reset makes locking operation finished and then exiting from OTP Block after 30us.

The OTP Block Lock operation must be used with caution since, once locked, there is no procedure available for unlocking and none of the bits in the OTP Block space can be modified in any way.
Suspend and resume operation are not supported during OTP protect, nor is OTP protect supported during any suspend operations.
After entering OTP block, program/erase operation on main blocks is prohibited. Enter OTP block command is not allowed while other operation is excuting.

9.23 Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during Vcc power-up and power-down, a write cycle is locked out for Vcc less than VLKO. If the Vcc < VLKO (Lock-Out Voltage), the command register and all internal program/erase circuits are disabled. Under this condition the device will reset itself to the read mode.Subsequent writes will be ignored until the Vcc level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above VLKO.

9.24 Write Pulse "Glitch" Protection

Noise pulses of less than 5ns (typical) on OE, CE, $\overline{AVD}$ or WE do not initiate a write cycle.

9.25 Logical Inhibit

Write cycles are inhibited by holding any one of OE = VIL , CE = VIH or WE = VIH. To initiate a write cycle, CE and WE must be a logical zero while OE is a logical one

10.0 FLASH MEMORY STATUS FLAGS

The K8A(56/57)E has means to indicate its status of operation in the bank where a program or erase operation is in processes. Address must include bank address being executed internal routine operation. The status is indicated by raising the device status flag via corresponding DQ pins. The status data can be read during burst read mode by using $\overline{AVD}$ signal with a bank address. That means status read is supported in synchronous mode. If status read is performed, the data provided in the burst read is identical to the data in the initial access. To initiate the synchronous read again, a new address and $\overline{AVD}$ pulse is needed after the host has completed status reads or the device has completed the program or erase operation. The corresponding DQ pins are DQ7, DQ6, DQ5, DQ3, DQ2 and DQ1.

[Table 14] Hardware Sequence Flags

	Status		DQ7	DQ6	DQ5	DQ3	DQ2	DQ1
In Progress	Programming		$\overline{DQ7}$	Toggle	0	0	1	0
	Block Erase or Chip Erase		0	Toggle	0	1	Toggle	0
	Erase Suspend Read	Erase Suspended Block	1	1	0	0	Toggle 1)	0
	Erase Suspend Read	Non-Erase Suspended Block	Data	Data	Data	Data	Data	Data
	Erase Suspend Program	Non-Erase Suspended Block	$\overline{DQ7}$	Toggle	0	0	1	0
	Program Suspend Read	Program Suspended Block	DQ7	1	0	0	Toggle 1)	0
	Program Suspend Read	Non- program Suspended Block	Data	Data	Data	Data	Data	Data
Exceeded Time Limits	Programming		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	Block Erase or Chip Erase		0	Toggle	1	1	NOTE2	0
	Erase Suspend Program		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
Write-to-Buffer3)	BUSY state		$\overline{DQ7}$	Toggle	0	0	No Toggle	0
	Exceeded Timing Limits		$\overline{DQ7}$	Toggle	1	0	No Toggle	0
	ABORT State		$\overline{DQ7}$	Toggle	0	0	No Toggle	1

NOTE :
1) DQ2 will toggle when the device performs successive read operations from the erase/program suspended block.
2) If DQ5 is High (exceeded timing limits), successive reads from a problem block will cause DQ2 to toggle.
3) Note that DQ7 during Write-to-Buffer-Programming indicates the data-bar for DQ7 data for the last loaded write-buffer address location.

DQ7 : $\overline{\text{Data}}$ Polling

When an attempt to read the device is made while executing the Internal Program, the complement of the data is written to DQ7 as an indication of the Routine in progress. When the Routine is completed an attempt to access to the device will produce the true data written to DQ7. When a user attempts to read the block being erased or bank contains the block, DQ7 will be low. If the device is placed in the Erase/Program Suspend Mode, the status can be detected via the DQ7 pin. If the system tries to read an address which belongs to a block that is being erase suspended, DQ7 will be high. And, if the system tries to read an address which belongs to a block that is being program suspended, the output will be the true data of DQ7 itself. If a non-erase-suspended or non-program-suspended block address is read, the device will produce the true data to DQ7. If an attempt is made to program a protected block, DQ7 outputs complements the data for approximately 2us and the device then returns to the Read Mode without changing data in the block. If an attempt is made to erase a protected block, DQ7 outputs complement data in approximately 100us and the device then returns to the Read Mode without erasing the data in the block.

DQ6 : Toggle Bit

Toggle bit is another option to detect whether an Internal Routine is in progress or completed. Once the device is at a busy state, DQ6 will toggle. Toggling DQ6 will stop after the device completes its Internal Routine. If the device is in the Erase/Program Suspend Mode, an attempt to read an address that belongs to a block that is being erased or programmed will produce a high output of DQ6. If an address belongs to a block that is not being erased or programmed, toggling is halted and valid data is produced at DQ6. If an attempt is made to program a protected block, DQ6 toggles for approximately 2us and the device then returns to the Read Mode without changing the data in the block. If an attempt is made to erase a protected block, DQ6 toggles for approximately 100μs and the device then returns to the Read Mode without erasing the data in the block. #OE or #CE should be toggled in each toggle bit status read.

DQ5 : Exceed Timing Limits

If the Internal Program/Erase Routine extends beyond the timing limits, DQ5 will go High, indicating program/erase failure.

DQ3 : Block Erase Timer

The status of the multi-block erase operation can be detected via the DQ3 pin. DQ3 will go High if 50μs of the block erase time window expires. In this case, the Internal Erase Routine will initiate the erase operation.Therefore, the device will not accept further write commands until the erase operation is completed. DQ3 is Low if the block erase time window is not expired. Within the block erase time window, an additional

block erase command (30H) can be accepted. To confirm that the block erase command has been accepted, the software may check the status of DQ3 following each block erase command.

DQ2 : Toggle Bit 2

The device generates a toggling pulse in DQ2 only if an Internal Erase Routine or an Erase/Program Suspend is in progress. When the device executes the Internal Erase Routine, DQ2 toggles if the bank including an erasing block is read. Although the Internal Erase Routine is in the Exceeded Time Limits, DQ2 toggles only if an erasing block in the Exceeded Time Limits is read. When the device is in the Erase/Program Suspend mode, DQ2 toggles only if an address in the erasing or programming block is read. If a non-erasing or non-programmed block address is read during the Erase/Program Suspend mode, then DQ2 will produce valid data. DQ2 will go High if the user tries to program a non-erase suspend block while the device is in the Erase Suspend mode. #OE or #CE should be toggled in each toggle bit status read.

DQ1 : Buffer Program Abort Indicator

DQ1 indocates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data.

RDY: Ready

Normally the RDY signal is used to indicate if new burst data is available at the rising edge of the clock cycle or not. If RDY is low state, data is not valid at expected time, and if high state, data is valid. Note that, if CE is low and OE is high, the RDY is high state.

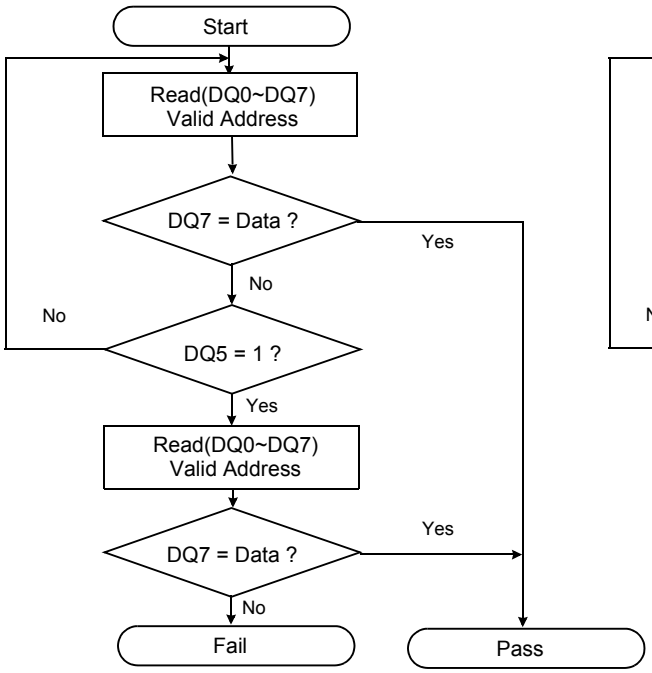


Figure 1: Data Polling Algorithms

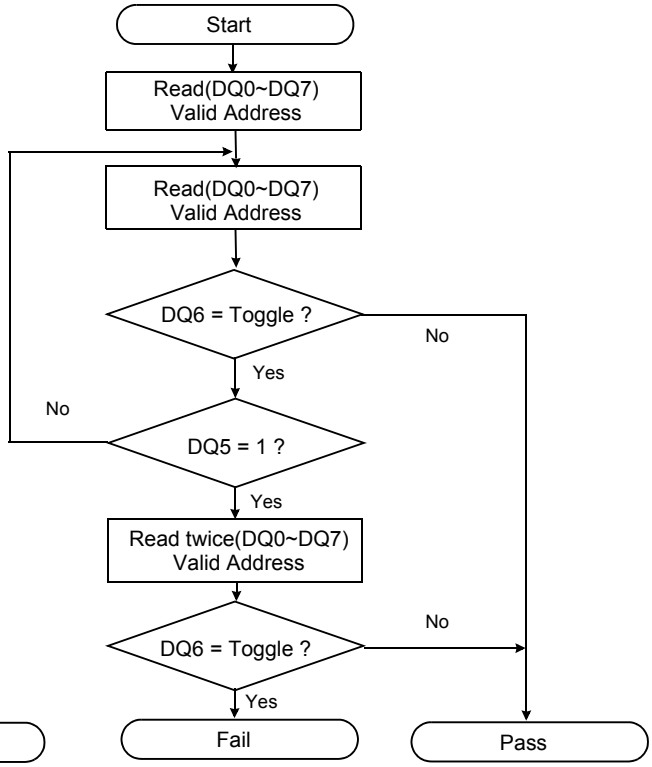


Figure 2: Toggle Bit Algorithms

11.0 DEEP POWER DOWN

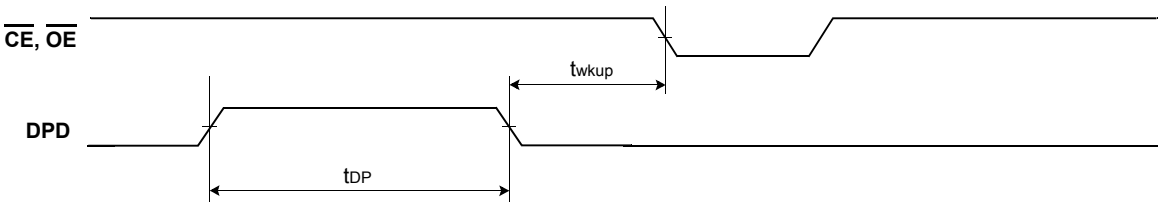
In order to reduce the power consumption of the device, it shall a deep power down mode inplemented on a seperate pin. The deep power down mode is active when the deep power down signal is activated, high state. In deep power down the device shall turn off all circuitry in order to reach a power consumption of 2uA(tpy). The device shall exit the deep power down mode within 75us after that the deep power down signal has been de-activated, set to low. In deep power down the state of the device chip select shall have no impact on the device power consumption. All programming capabilities of the device are inhibited.
At the power up, the device shall accept any order of activation of the reset and deep power down signal. The device shall respond within the specified time for the signal that was deactivated/activated latest. The deep power down mode is activated when DPD pin high state only. If DPD is asserted during a program or erase operation, the device requires a time of tDP(During Internal Routines) before the device is ready to enter DPD mode.

Note that user never float the DPD that is, DPD is always connected with V_{IH}, V_{IL}.Deep Power Down (DPD)

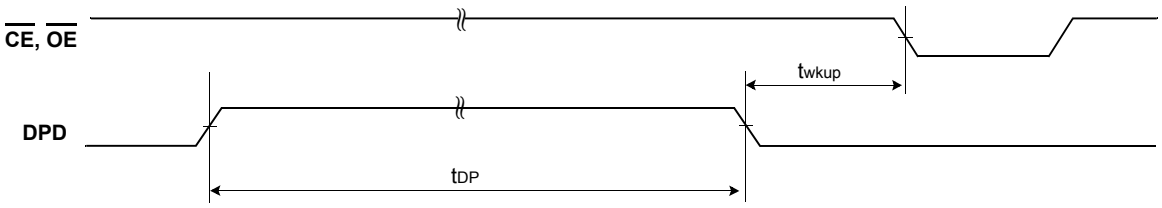
Parameter	Symbol	All Speed Options			Unit
		Min	Typ	Max	
DPD Pin High(NOT During Internal Routines) to DPD Mode*	t_{DP}	100	-	-	ns
DPD Pin High(During Internal Routines) to DPD Mode*	t_{DP}	20	-	-	µs
DPD Low Time Before Read*	t_{wkup}	75	-	-	µs

NOTE :
Not 100% tested.

SWITCHING WAVEFORMS



DPD Timings NOT during Internal Routines



DPD Timings during Internal Routines

Figure 3: DPD Timings

12.0 COMMON FLASH MEMORY INTERFACE

Common Flash Memory Interface is contrived to increase the compatibility of host system software. It provides the specific information of the device, such as memory size and electrical features. Once this information has been obtained, the system software will know which command sets to use to enable flash writes, block erases, and control the flash component.
When the system writes the CFI command(98H) to address 55H , the device enters the CFI mode. And then if the system writes the address shown in Table 15, the system can read the CFI data. Query data are always presented on the lowest-order data outputs(DQ0-7) only. In word(x16) mode, the upper data outputs(DQ8-15) is 00h. To terminate this operation, the system must write the reset command.

[Table 15] Common Flash Memory Interface Code

Description	Addresses (Word Mode)	Data
Query Unique ASCII string "QRY"	10H 11H 12H	0051H 0052H 0059H
Primary OEM Command Set	13H 14H	0002H 0000H
Address for Primary Extended Table	15H 16H	0040H 0000H
Alternate OEM Command Set (00h = none exists)	17H 18H	0000H 0000H
Address for Alternate OEM Extended Table (00h = none exists)	19H 1AH	0000H 0000H
Vcc Min. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1BH	0017H
Vcc Max. (write/erase) D7-D4: volt, D3-D0: 100 millivolt	1CH	0019H
Vpp(Acceleration Program) Supply Minimum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1DH	0085H
Vpp(Acceleration Program) Supply Maximum 00 = Not Supported, D7 - D4 : Volt, D3 - D0 : 100mV	1EH	0095H
Typical timeout per single word write 2^N us	1FH	0008H
Typical timeout for Max buffer write 2^N us(00H = not supported)	20H	0009H
Typical timeout per individual block erase 2^N ms	21H	000AH
Typical timeout for full chip erase 2^N ms(00H = not supported)	22H	0012H
Max. timeout for word write 2^N times typical	23H	0001H
Max. timeout for buffer write 2^N times typical	24H	0001H
Max. timeout per individual block erase 2^N times typical	25H	0004H
Max. timeout for full chip erase 2^N times typical(00H = not supported)	26H	0000H
Device Size = 2^N byte	27H	0019H
Flash Device Interface description	28H 29H	0000H 0000H
Max. number of byte in multi-byte write = 2^N	2AH 2BH	0006H 0000H
Number of Erase Block Regions within device (Note 1)	2CH	0002H
Erase Block Region 1 Information (Boot block part : **(K8A(56/57)15ET(B)C)**) Bits 0~15: y+1=block number Bits 16~31: block size= z x 256bytes	2DH 2EH 2FH 30H	0003H 0000H 0080H 0000H

Description	Addresses (Word Mode)	Data
Erase Block Region 1 Information (Uniform block part : **(K8A(56/57)15EZC)**) Bits 0~15: y+1=block number Bits 16~31: block size= z x 256bytes	2DH 2EH 2FH 30H	00FFH 0000H 0000H 0002H
Erase Block Region 2 Information (Boot block part : **(K8A(56/57)15ET(B)C)**)	31H 32H 33H 34H	00FEH 0000H 0000H 0002H
Erase Block Region 2 Information (Uniform block part : **(K8A(56/57)15EZC)**)	31H 32H 33H 34H	0000H 0000H 0000H 0000H
Erase Block Region 3 Information	35H 36H 37H 38H	0000H 0000H 0000H 0000H
Erase Block Region 4 Information	39H 3AH 3BH 3CH	0000H 0000H 0000H 0000H
Query-unique ASCII string "PRI"	40H 41H 42H	0050H 0052H 0049H
Major version number, ASCII	43H	0030H
Minor version number, ASCII	44H	0030H
Address Sensitive Unlock(Bits 1-0) 0 = Required, 1= Not Required Silcon Revision Number(Bits 7-2)	45H	0000H
Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write	46H	0002H
Block Protect 00 = Not Supported, 01 = Supported	47H	0001H
Block Temporary Unprotect 00 = Not Supported, 01 = Supported	48H	0000H
Block Protect/Unprotect scheme 00 = Not Supported, 01 = Supported	49H	0001H
Simultaneous Operation 00 = Not Supported, 01 = Supported	4AH	0001H
Burst Mode Type 00 = Not Supported, 01 = Supported	4BH	0001H
Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page, 03 = 16 Word Page	4CH	0003H
Top/Bottom Boot/Uniform Block Flag 02H = Bottom Boot Device, 03H = Top Boot Device, 04H = Uniform Device	4DH	0003H
Max. Operating Clock Frequency (MHz) (Note 2)	4EH	0085H
RWW(Read While Write) Functionality Restriction (00H = non exists , 01H = exists)	4FH	0000H
Handshaking 00 = Not Supported at both mode, 01 = Supported at Sync. Mode 10 = Supported at Async. Mode, 11 = Supported at both Mode	50H	0001H

NOTE :
1) Uniform block part (K8A(56/57)15EZC) : Data is 01H
Boot block part (K8A(56/57)15ET(B)C) : Data is 02H
2) Max. Operating Clock Frequency : Data is 85H in 108/133Mhz part (K8A5715E(T/B/Z)C), Data is 53H in 66/83Mhz part (K8A5615E(T/B/Z)C)

13.0 ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	Vcc	Vcc	-0.5 to +2.5	V
	V_{PP}	V_{IN}	-0.5 to +9.5	
	All Other Pins		-0.5 to +2.5	
Storage Temperature		T_{stg}	-65 to +100	°C
Short Circuit Output Current		I_{OS}	5	mA
Operating Temperature		T_A (Commercial Temp.)	0 to +70	°C
		T_A (Extended Temp.)	-25 to + 85	°C

NOTE :
1) Minimum DC voltage is -0.5V on Input/ Output pins. During transitions, this level may fall to -2.0V for periods <20ns.
Maximum DC voltage is Vcc+0.6V on input / output pins which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2) Minimum DC input voltage is -0.5V on VPP . During transitions, this level may fall to -2.0V for periods <20ns.
Maximum DC input voltage is +9.5V on VPP which, during transitions, may overshoot to +12.0V for periods <20ns.
3) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

14.0 RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	Vcc	1.7	1.8	1.95	V
Supply Voltage	Vss	0	0	0	V

NOTE :
1) Data retention is not guaranteed on Operating condition Extended temperature(-25'C~85'C) over.

15.0 DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}, V_{CC}=V_{CC}max	- 1.0	-	+ 1.0	μA
VPP Leakage Current	I_{LIP}	V_{CC}=V_{CC}max , V_{PP}=V_{CC}max	- 1.0	-	+ 1.0	μA
		V_{CC}=V_{CC}max , V_{PP}=9.5V	-	-	35	μA
Output Leakage Current	I_{LO}	V_{OUT}=V_{SS} to V_{CC}, V_{CC}=V_{CC}max, $\overline{OE}$=V_{IH}	- 1.0	-	+ 1.0	μA
Active Burst Read Current	I_{CCB1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} (@133MHz)	-	35	55	mA
Active Asynchronous Read Current	I_{CC1}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} 10MHz	-	35	55	mA
Active Write Current [2]	I_{CC2}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, $\overline{WE}$=V_{IL}, VPP=V_{IH}	-	25	40	mA
Read While Write Current	I_{CC3}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}	-	45	70	mA
Accelerated Program Current	I_{CC4}	$\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH} , V_{PP}=9.5V	-	20	30	mA
Standby Current	I_{CC5}	$\overline{CE}$= $\overline{RESET}$=V_{CC} ± 0.2V	-	30	120	μA
Standby Current During Reset	I_{CC6}	$\overline{RESET}$ = V_{SS} ± 0.2V	-	30	120	μA
Automatic Sleep Mode [3]	I_{CC7}	$\overline{CE}$=V_{SS} ± 0.2V, Other Pins=V_{IL} or V_{IH} V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V	-	30	120	μA
Deep Power Down Mode	I_{CC8}		-	2	20	μA
Input Low Voltage	V_{IL}		-0.5	-	0.4	V
Input High Voltage	V_{IH}		V_{CC}-0.4	-	V_{CC}+0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 μA , V_{CC}=V_{CC}min	-	-	0.1	V
Output High Voltage	V_{OH}	I_{OH} = -100 μA , V_{CC}=V_{CC}min	V_{CC}-0.1	-	-	V
Voltage for Accelerated Program	V_{ID}		8.5	9.0	9.5	V
Low VCC Lock-out Voltage	V_{LKO}		-	-	1.4	V
Vpp current in program/erase	I_{vpp}	V_{pp} = 9.5V	-	0.8	5	mA
		V_{pp} = 1.95V	-	-	50	μA

NOTE :

1) Maximum ICC specifications are tested with VCC = VCCmax.

2) ICC active while Internal Erase or Internal Program is in progress.

3) Device enters automatic sleep mode when addresses are stable for tAA + 60ns.

Vcc Power-up

Parameter	Symbol	All Speed Options		Unit
		Min	Max	
Vcc Setup Time	t_{VCS}	200	-	µs
Time between $\overline{RESET}$ (high) and $\overline{CE}$ (low)	t_{RH}	200	-	ns

NOTE: Not 100% tested.

SWITCHING WAVEFORMS

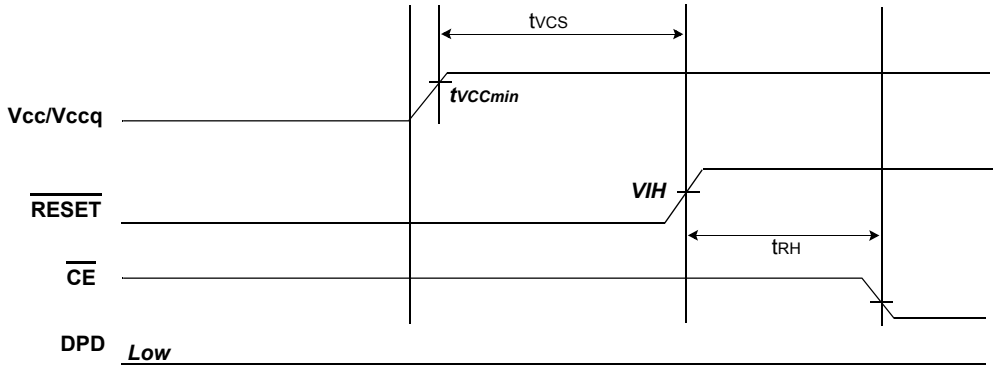


Figure 4: Vcc Power-up Diagram

NOTE : DPD should be low during power-up sequence.

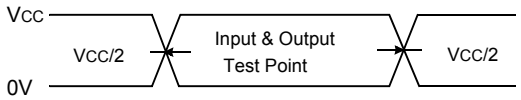
16.0 CAPACITANCE (TA = 25 °C, VCC = 1.8V, f = 1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	10	pF
Control Pin Capacitance	C_{IN2}	V_{IN}=0V	-	10	pF

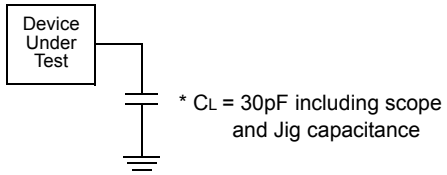
NOTE : Capacitance is periodically sampled and not 100% tested.

17.0 AC TEST CONDITION

Parameter	Value
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	3ns(max)@66Mhz, 2.5ns(max)@83Mhz, 1.5ns(max)@108Mhz, 1ns(max)@133Mhz
Input and Output Timing Levels	VCC/2
Output Load	C_L = 30pF
Address to Address Skew	3ns(max)



Input Pulse and Test Point (including CLK characterization)



Output Load

18.0 AC CHARACTERISTICS

18.1 Synchronous/Burst Read

Parameter	Symbol	1B (54 MHz)		1C (66 MHz)		1D (83 MHz)		1E (108 MHz)		1F (133 MHz)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Initial Access Time	t_{IAA}	-	95	-	95	-	95	-	95	-	95	ns
Burst Access Time Valid Clock to Output Delay	t_{BA}	-	14.5	-	11	-	9	-	7	-	6	ns
$\overline{AVD}$ Setup Time to CLK	t_{AVDS}	5	-	5	-	4	-	3.5	-	2.5	-	ns
$\overline{AVD}$ Hold Time from CLK	t_{AVDH}	2	-	2	-	2	-	2	-	2	-	ns
$\overline{AVD}$ High to $\overline{OE}$ Low	t_{AVDO}	0	-	0	-	0	-	0	-	0	-	ns
Address Setup Time to CLK	t_{ACS}	5	-	5	-	4	-	3.5	-	2.5	-	ns
Address Hold Time from CLK	t_{ACH}	7	-	6	-	5	-	2	-	2	-	ns
Data Hold Time from Next Clock Cycle	t_{BDH}	4	-	3	-	3	-	2	-	2	-	ns
Output Enable to RDY valid	t_{OER}	-	14.5	-	11	-	9	-	7	-	6	ns
$\overline{CE}$ Disable to High Z	t_{CEZ}	-	9	-	9	-	9	-	9	-	9	ns
$\overline{OE}$ Disable to High Z	t_{OEZ}	-	9	-	9	-	9	-	9	-	9	ns
$\overline{CE}$ Setup Time to CLK	t_{CES}	6	-	6	-	4.5	-	4	-	3.5	-	ns
$\overline{CE}$ Enable to RDY active	t_{RDY}	-	14.5	-	11	-	9	-	7	-	6	ns
CLK to RDY Setup Time	t_{RDYA}	-	14.5	-	11	-	9	-	7	-	6	ns
RDY Setup Time to CLK	t_{RDYS}	4	-	3	-	3	-	2	-	2	-	ns
CLK period	t_{CLK}	18.5	-	15.1	-	12.05	-	9.26	-	7.52	-	ns
CLK High or Low Time	$t_{CLKH/L}$	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	0.4x t_{CLK}	0.6x t_{CLK}	ns
CLK Fall or Rise Time	t_{CLKHCL}	-	3	-	3	-	2.5	-	1.5	-	1	ns

SWITCHING WAVEFORMS

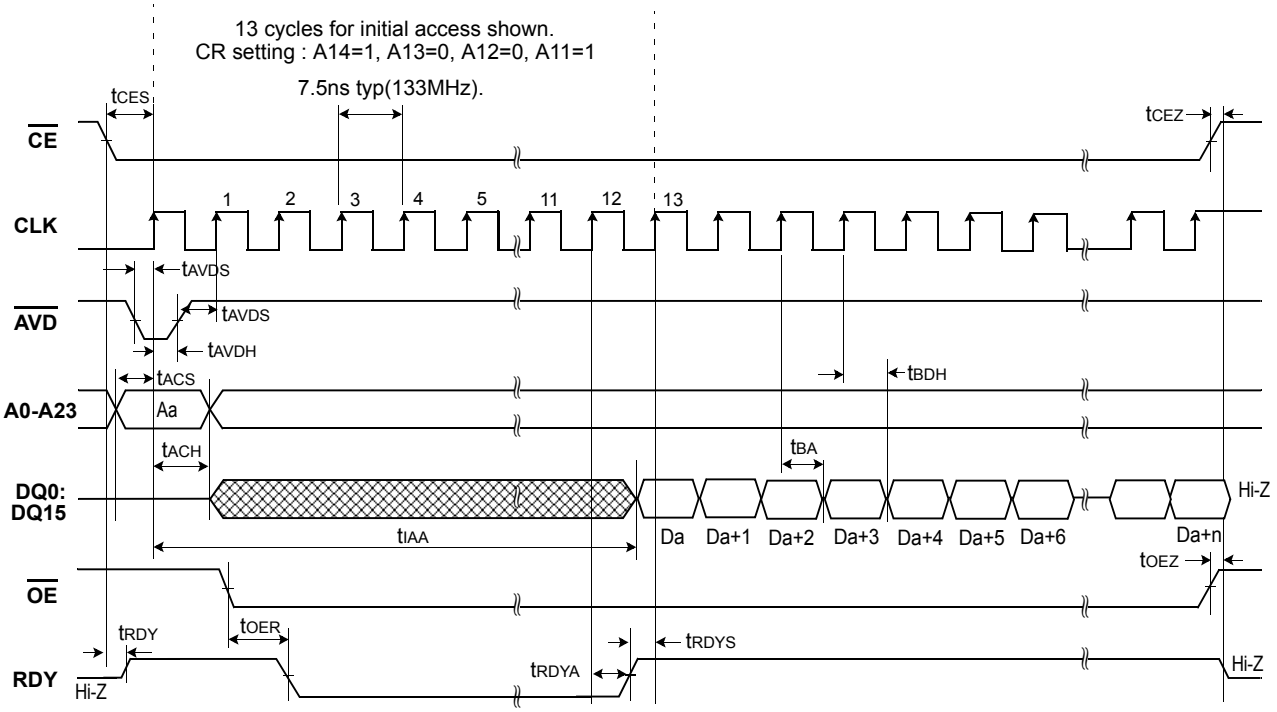


Figure 5: Continuous Burst Mode Read (133 MHz)

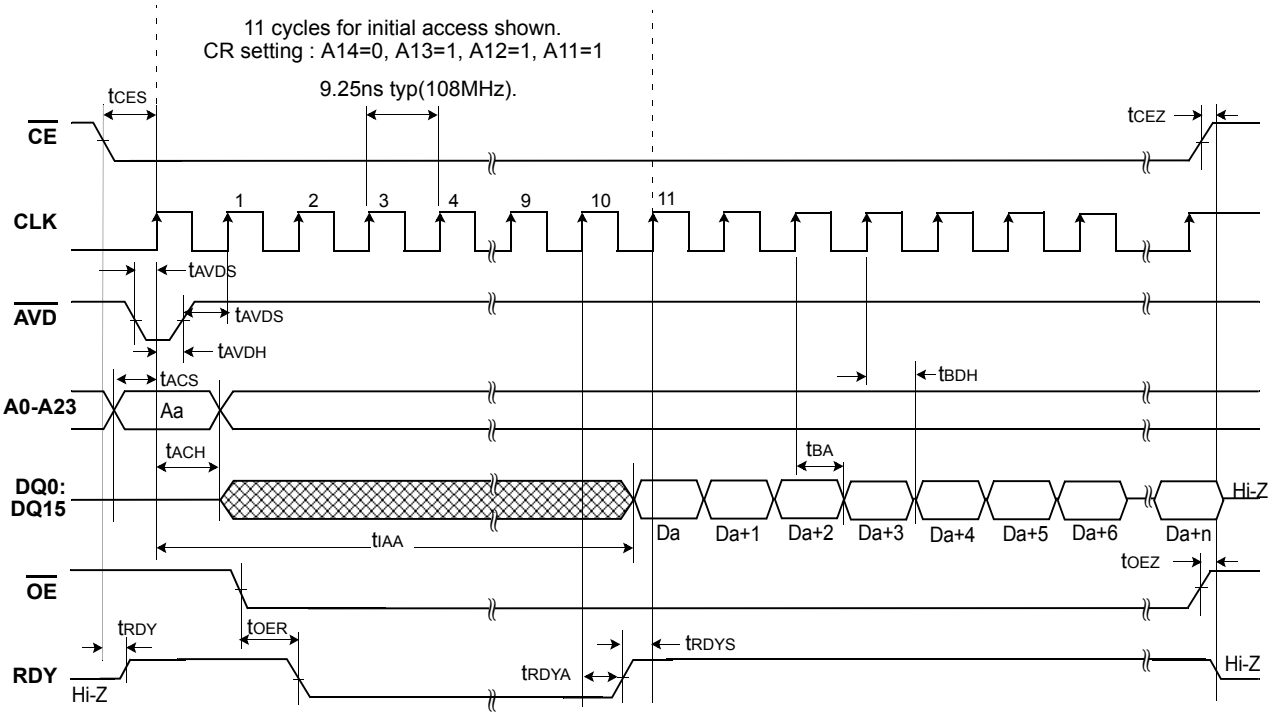


Figure 6: Continuous Burst Mode Read (108 MHz)

SWITCHING WAVEFORMS

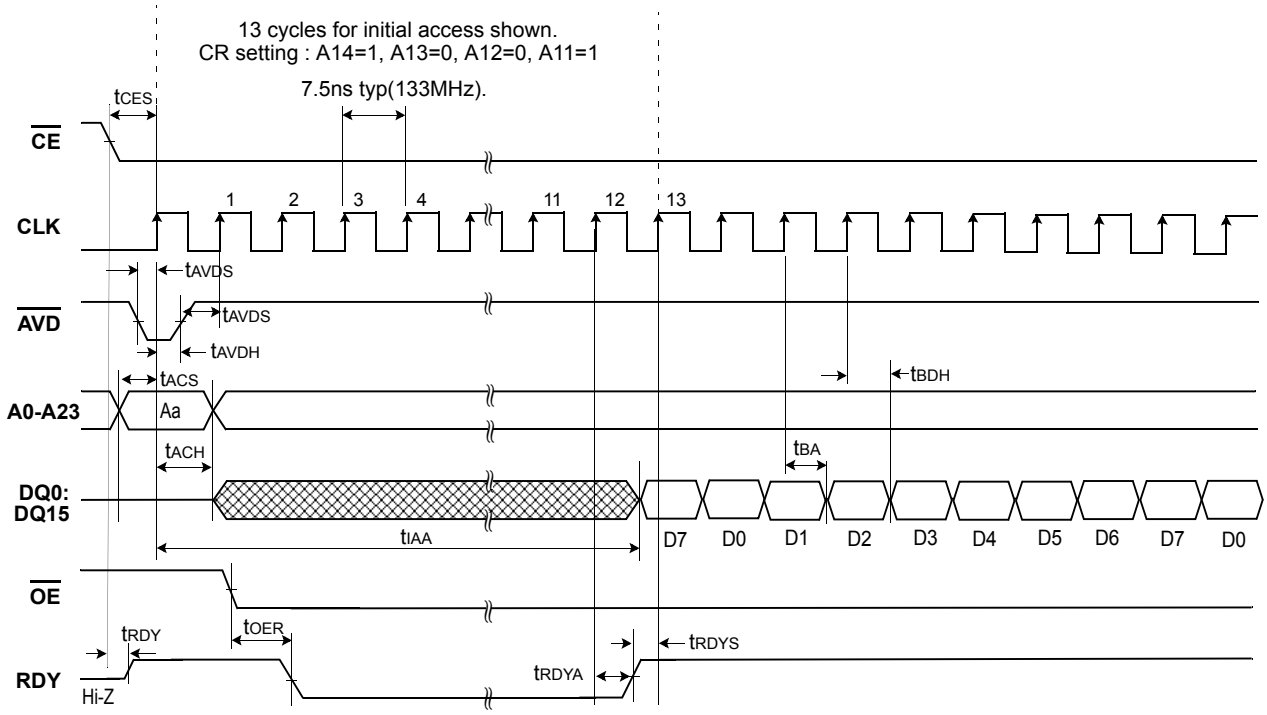


Figure 7: 8 word Linear Burst Mode with Wrap Around (133MHz)

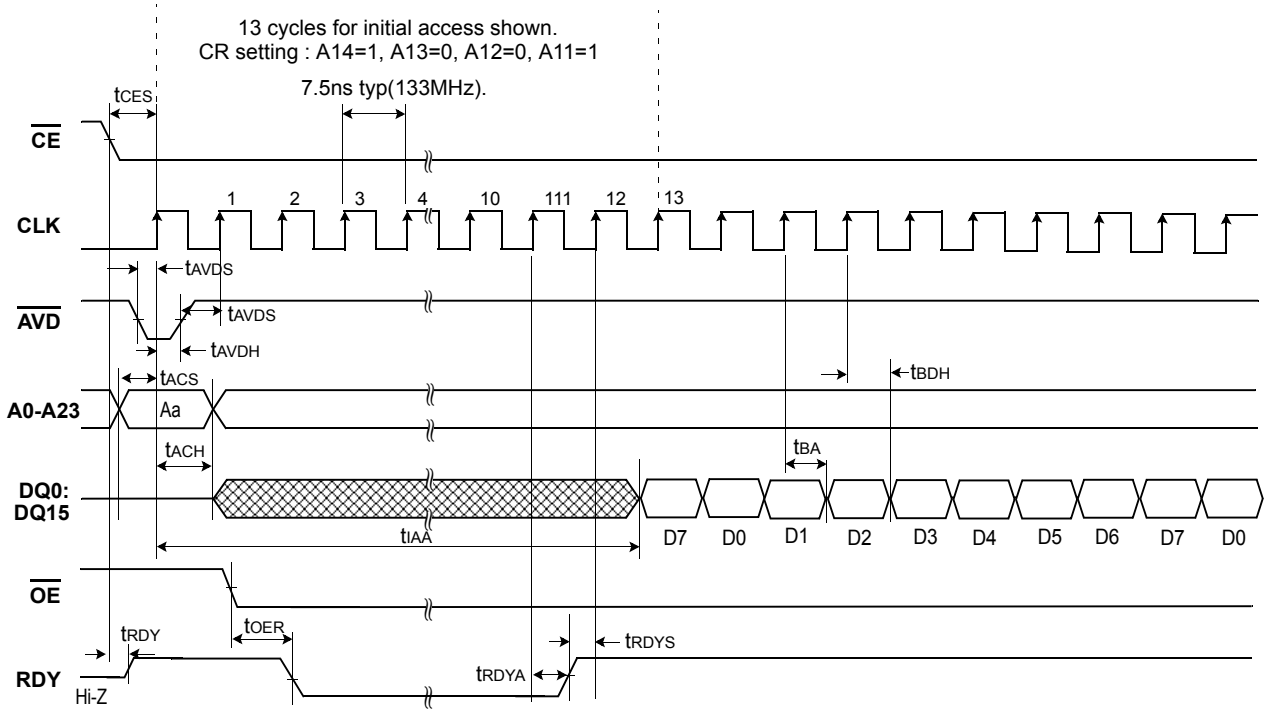


Figure 8: 8 word Linear Burst with RDY Set One Cycle Before Data

(Wrap Around Mode, CR setting : A18=1)

SWITCHING WAVEFORMS

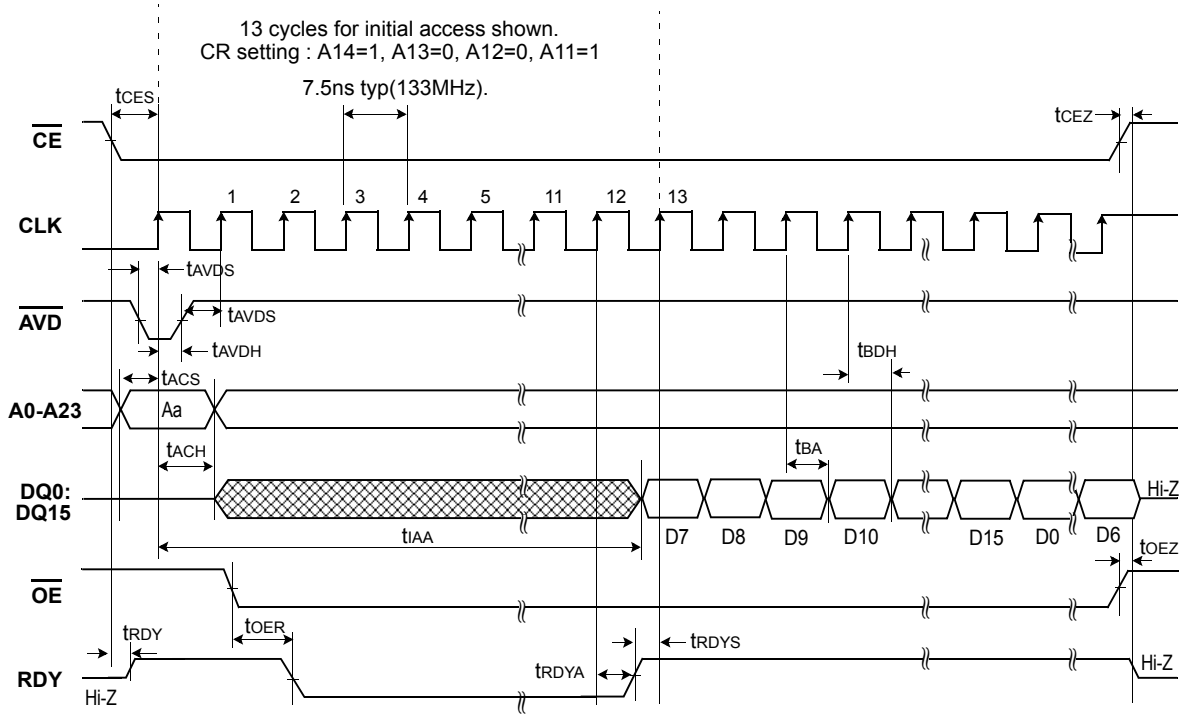


Figure 9: 16 word Linear Burst Mode with Wrap Around (133Mhz)

18.2 Asynchronous Read

Parameter		Symbol	All Speed option		Unit
			Min	Max	
Access Time from $\overline{CE}$ Low		t_{CE}	-	100	ns
Asynchronous Access Time		t_{AA}	-	100	ns
Page Address Access Time		t_{PA}	-	15	ns
Output Hold Time from Address, $\overline{CE}$ or $\overline{OE}$		t_{OH}	3	-	ns
$\overline{AVD}$ Low Setup Time to $\overline{CE}$ Enable		t_{AVDCS}	0	-	ns
$\overline{AVD}$ Low Hold Time from $\overline{CE}$ Enable		t_{AVDCH}	0	-	ns
Output Enable to Output Valid		t_{OE}	-	15	ns
Output Enable Hold Time	Read	t_{OEH}	0	-	ns
	Toggle and $\overline{Data}$ Polling		10	-	ns
Output Disable to High Z*		t_{OEZ}	-	9	ns

NOTE: Not 100% tested.

SWITCHING WAVEFORMS

Asynchronous Mode Read

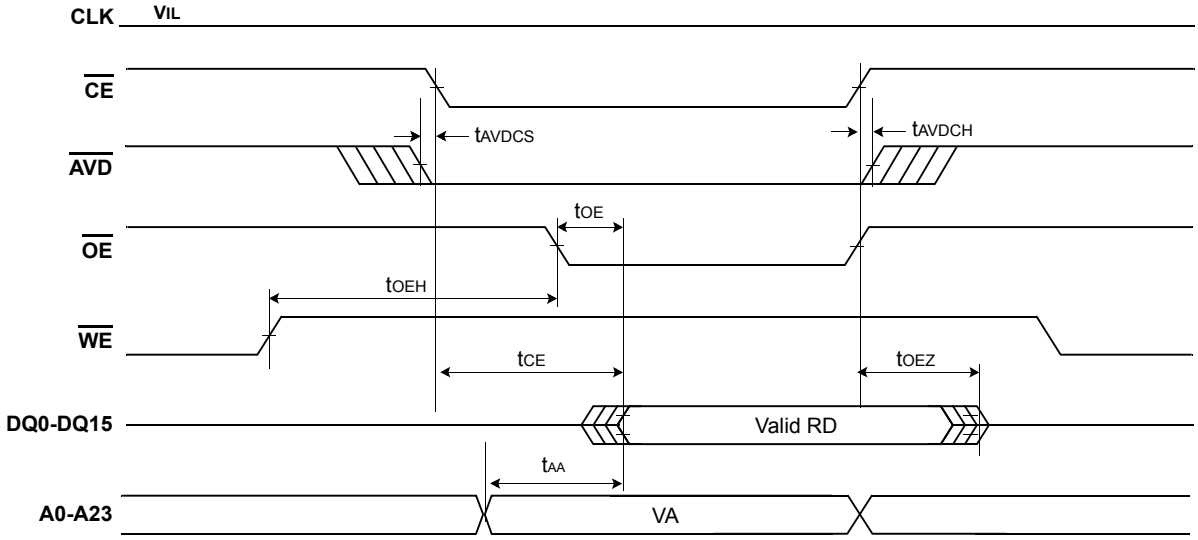


Figure 10: Asynchronous Mode Read

NOTE :
1) VA=Valid Read Address, RD=Read Data.
2) $\overline{AVD}$ should be held VIL in asynchronous read mode.
3) Asynchronous mode may not support read following four sequential invalid read condition within 200ns.
4) CLK "HIGH" should be prohibited in asynchronous read mode start (From $\overline{CE}$ LOW).

SWITCHING WAVEFORMS
Page Read Operations

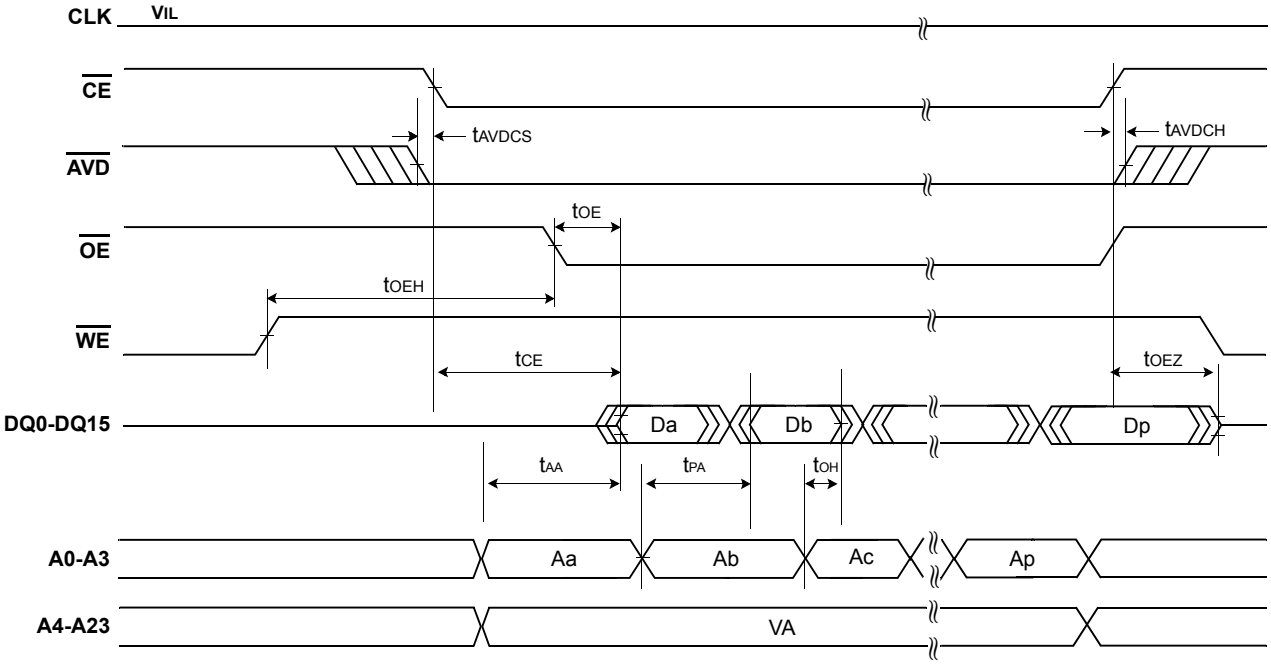


Figure 11: Asynchronous Page Mode Read

NOTE: CLK "HIGH" should be prohibited in asynchronous read mode start (From $\overline{CE}$ LOW).

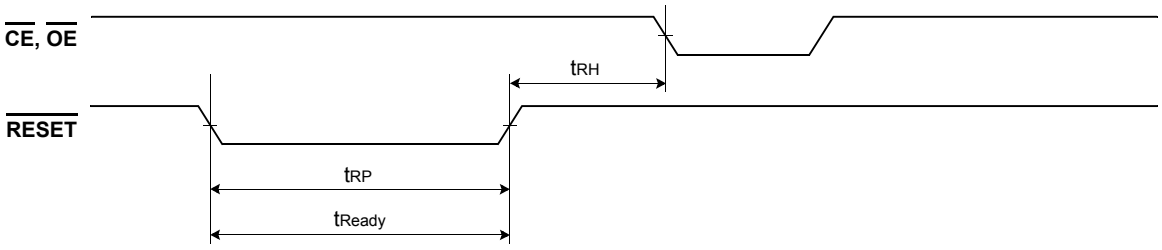
AC CHARACTERISTICS

Hardware Reset($\overline{RESET}$)

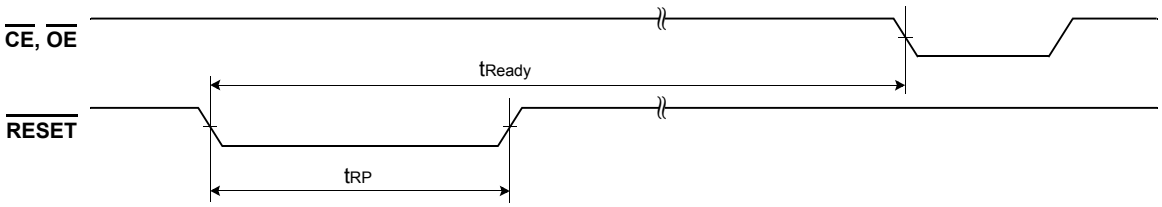
Parameter	Symbol	All Speed Options		Unit
		Min	Max	
$\overline{RESET}$ Pin Low(During Internal Routines) to Read Mode (Note)	t_{Ready}	-	20	μs
$\overline{RESET}$ Pin Low(NOT During Internal Routines) to Read Mode (Note)	t_{Ready}	-	500	ns
$\overline{RESET}$ Pulse Width*	t_{RP}	200	-	ns
Reset High Time Before Read (Note)	t_{RH}	200	-	ns

NOTE :
1) Not 100% tested.

SWITCHING WAVEFORMS



Reset Timings NOT during Internal Routines



Reset Timings during Internal Routines

Figure 12: Reset Timings

AC CHARACTERISTICS

18.3 Erase/Program Operation

Parameter	Symbol	All Speed Option			Unit
		Min	Typ	Max	
$\overline{WE}$ Cycle Time[1]	t_{WC}	75	-	-	ns
Address Setup Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	30	-	-	ns
Data Setup Time	t_{DS}	30	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Read Recovery Time Before Write	t_{GHWL}	0	-	-	ns
$\overline{CE}$ Setup Time	t_{CS}	0	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	0	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	30	-	-	ns
$\overline{WE}$ Pulse Width High	t_{WPH}	45	-	-	ns
Latency Between Read and Write Operations	$t_{SR/W}$	0	-	-	ns
Word Programming Operation [2]	t_{PGM}	-	80	-	µs
Single word Buffer Program [2]	t_{PGM_BP}	-	250	-	µs
32-word Buffer Program [3]	t_{PGM_BP}	-	89.6	-	µs
Accelerated Programming Operation	t_{ACCPGM}	-	80	-	µs
Accelerated Single word Buffer Program	t_{ACCPGM_BP}	-	1.4	-	µs
Accelerated 32-word Buffer Program [3]	t_{ACCPGM_BP}	-	44.8	-	µs
Block Erase Operation (64KW block)	t_{BERS}	-	0.6	-	sec
VPP Rise and Fall Time	t_{VPP}	500	-	-	ns
VPP Setup Time (During Accelerated Programming)	t_{VPS}	1	-	-	µs

NOTE :
1) Not 100% tested.
2) Internal programming algorithm is optimized for Buffer Program, so Normal word programming or Single word Buffer Program use Buffer Program algorithm.
3) Typical 32-word Buffer Program time pays due regard to that Each program data pattern ("11", "10". "01", "00") has a same portion in 32-word Buffer.

18.4 Erase/Program Performance

Parameter		Limits			Unit	Comments
		Min.	Typ.	Max.		
Block Erase Time	64 Kword	-	0.6	3.0	sec	Includes 00h programming prior to erasure
	16 Kword	-	0.3	1.5		
Chip Erase Time 3)		-	154.2	771		
Accelerated Block Erase Time (4)	64 Kword	-	0.4	3.0		
	16 Kword	-	0.2	1.5		
Accelerated Chip Erase Time 3),4)		-	103	515		
Word Programming Time		-	80	550	µs / word	Excludes system level over-head
32-word Buffer Programming Time 5)		-	2.8	14		
Accelerated Word Programming Time		-	80	550		
Accelerated 32-word Buffer Programming Time		-	1.4	7		
Chip Buffer Programming Time		-	47	235	sec	Excludes system level over-head
Accelerated Buffer Chip Programming Time		-	23.4	117		

NOTE :

1) 25ºC, VCC = 1.8V, 100,000 cycles, typical pattern.

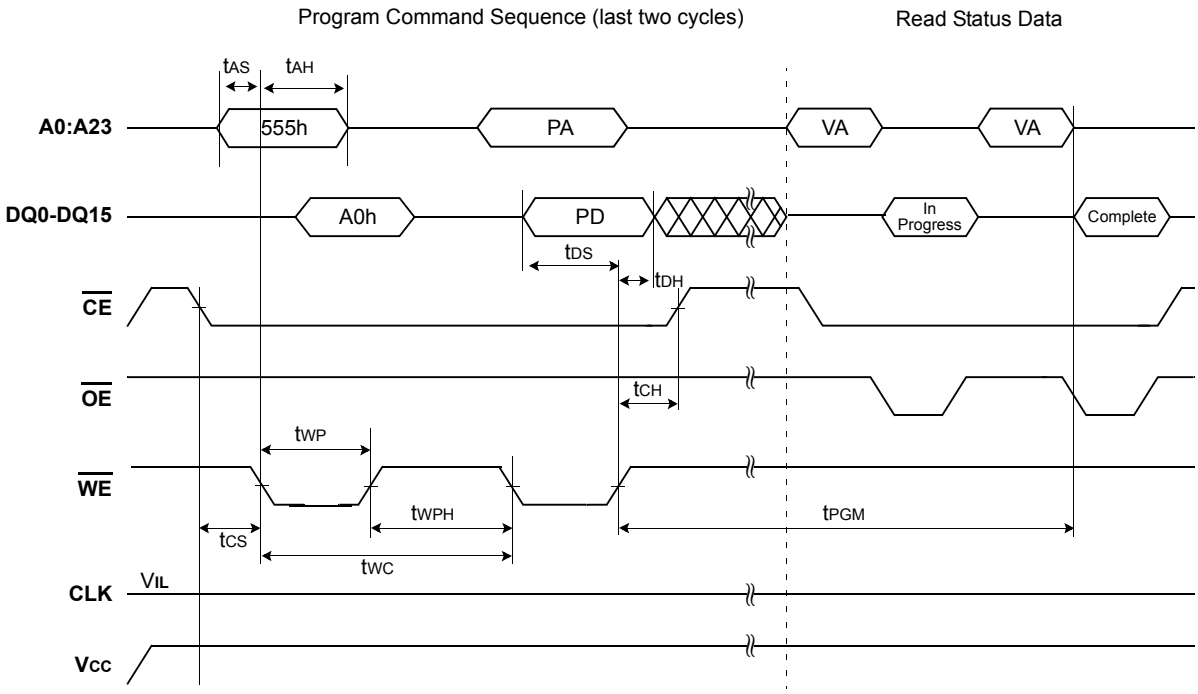
2) System-level overhead is defined as the time required to execute the two or four bus cycle command necessary to program each word.

3) Chip Erase time & Accel. Chip Erase time for boot block part : K8A(56)(57)15ET(B)C

4) Accelerated Program/Erase cycling must be limited below 100cycles for optimum performance. Ambient temperature requirements : TA = 30°C±10°C

5) Not 100% tested.

SWITCHING WAVEFORMS
Program Operations



NOTE :

1) PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.

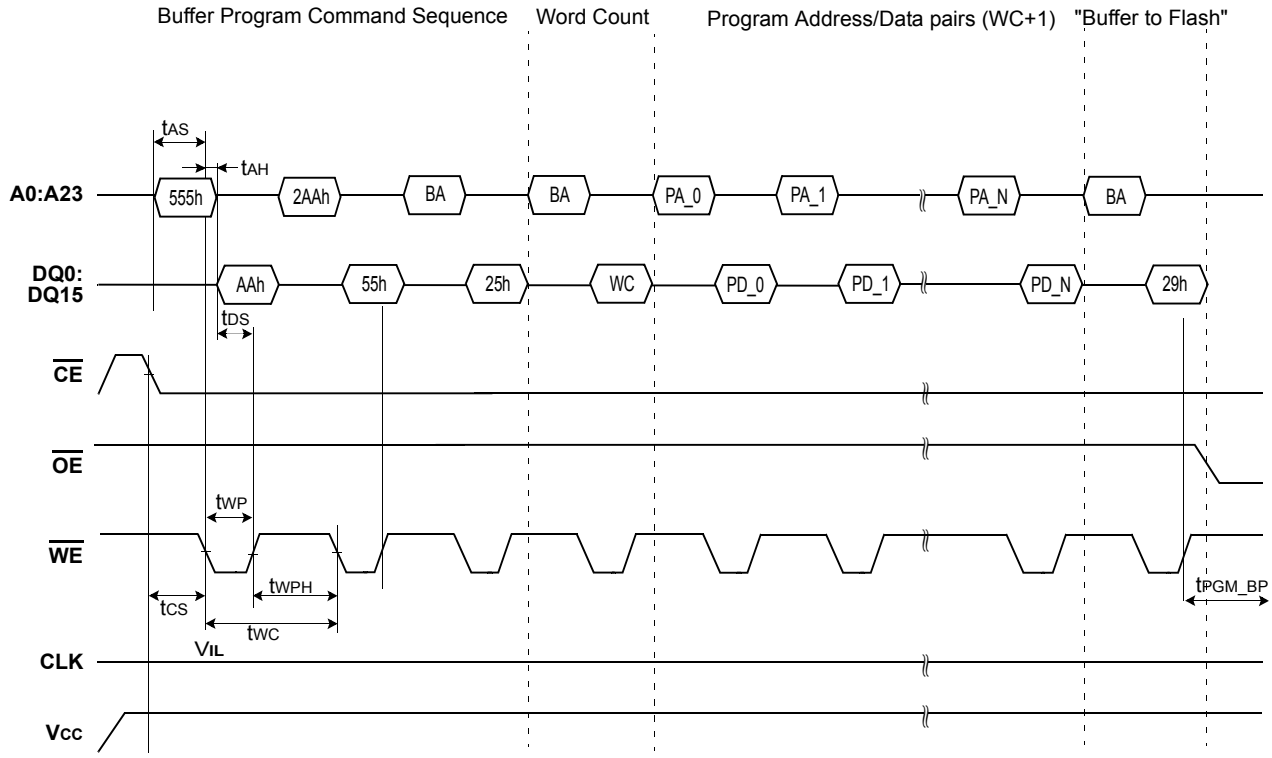
2) “In progress” and “complete” refer to status of program operation.

3) A16–A23 are don’t care during command sequence unlock cycles.

4) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

Figure 13: Program Operation Timing

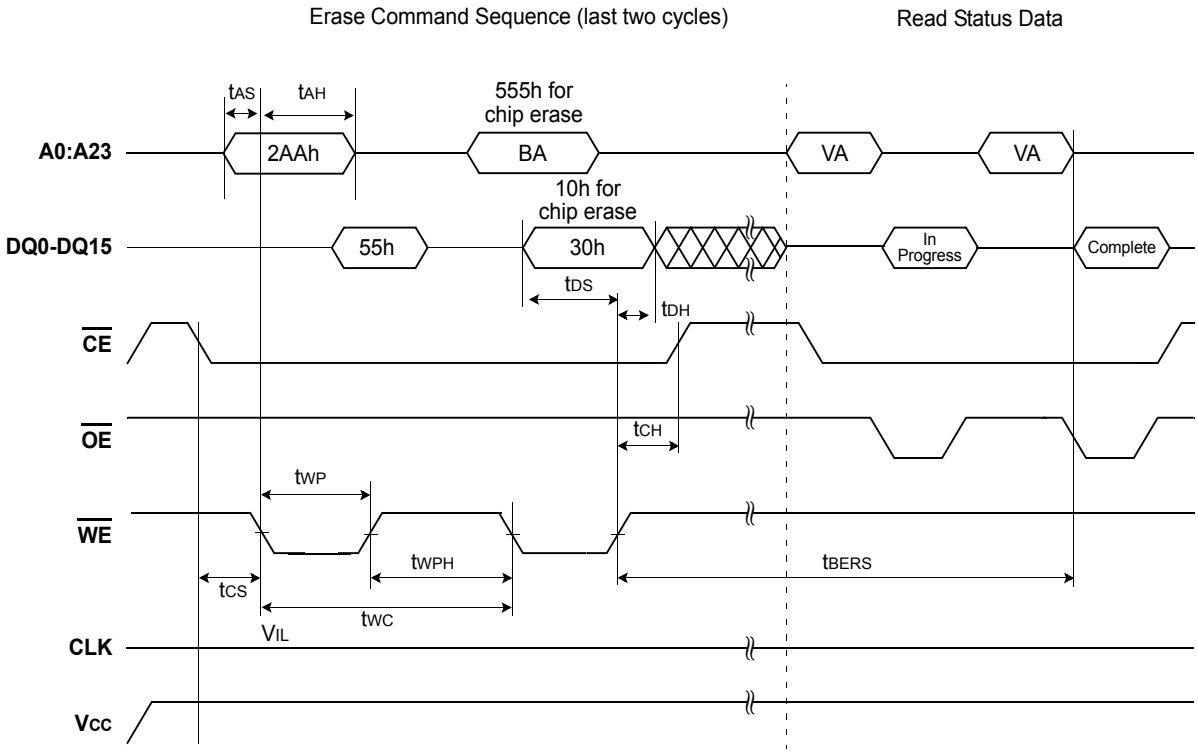
SWITCHING WAVEFORMS
Buffer Program Operations



NOTE :
1) BA = Block Address, WC = Word Count, PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.
2) Sequential PA_1, PA_2, ... , PA_N must have same address bits A23(max.) ~ A5 as PA_0 entered firstly
3) The number of Program/Data pairs entered must be same as WC+1 because WC = N.
4) “In progress” and “complete” refer to status of program operation.
5) A16–A23 are don’t care during command sequence unlock cycles.
6) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

Figure 14: Buffer Program Operation Timing

SWITCHING WAVEFORMS
Erase Operation

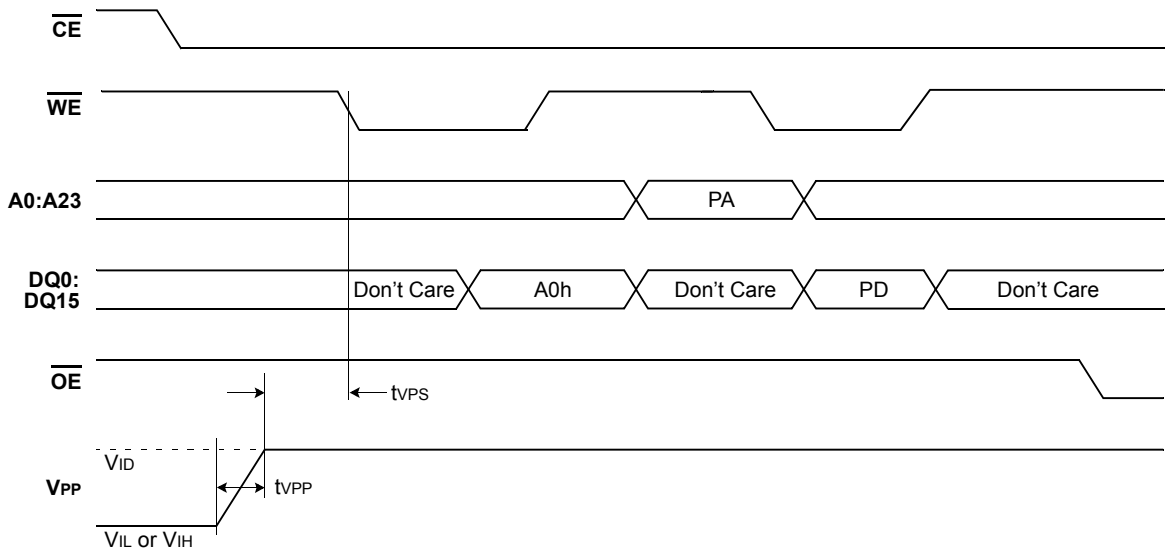


NOTE :
1) BA is the block address for Block Erase.
2) Address bits A16–A23 are don't cares during unlock cycles in the command sequence.
3) Status reads in this figure is asynchronous read, but status read in synchronous mode is also supported.

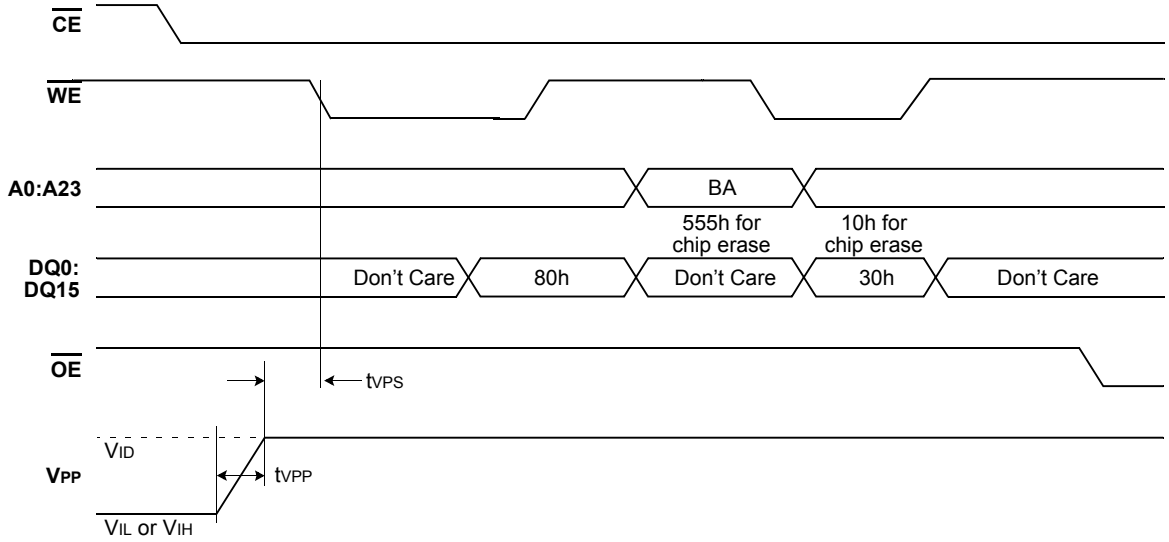
Figure 15: Chlp/Block Erase Operations

SWITCHING WAVEFORMS

Unlock Bypass Program Operations(Accelerated Program)



Unlock Bypass Block Erase Operations



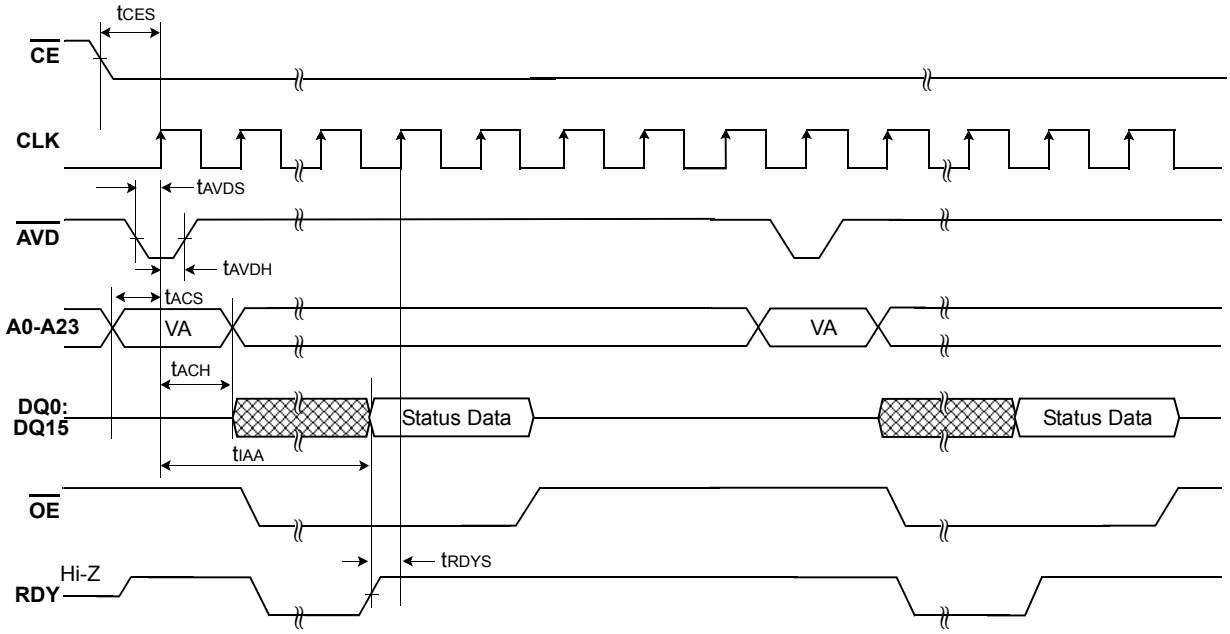
NOTE :

1) VPP can be left high for subsequent programming pulses.
2) Use setup and hold times from conventional program operations.
3) Conventional Program/Erase commands as well as Unlock Bypass Program/Erase commands can be used when the VID is applied to Vpp.

Figure 16: Unlock Bypass Operation Timings

SWITCHING WAVEFORMS

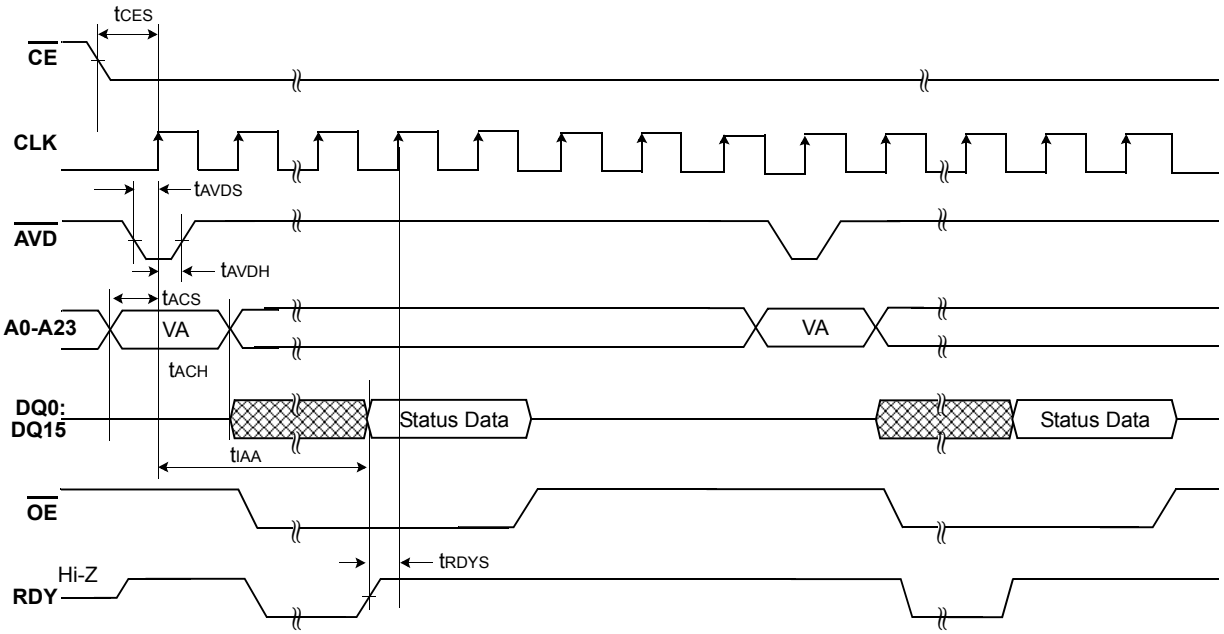
Data Polling Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, and Data Polling will output true data.

Figure 17: Data Polling Timings (During Internal Routine)

Toggle Bit Operations



NOTE :
1) VA = Valid Address. When the Internal Routine operation is complete, the toggle bits will stop toggling.

Figure 18: Toggle Bit Timings(During Internal Routine)

SWITCHING WAVEFORMS

Read While Write Operations

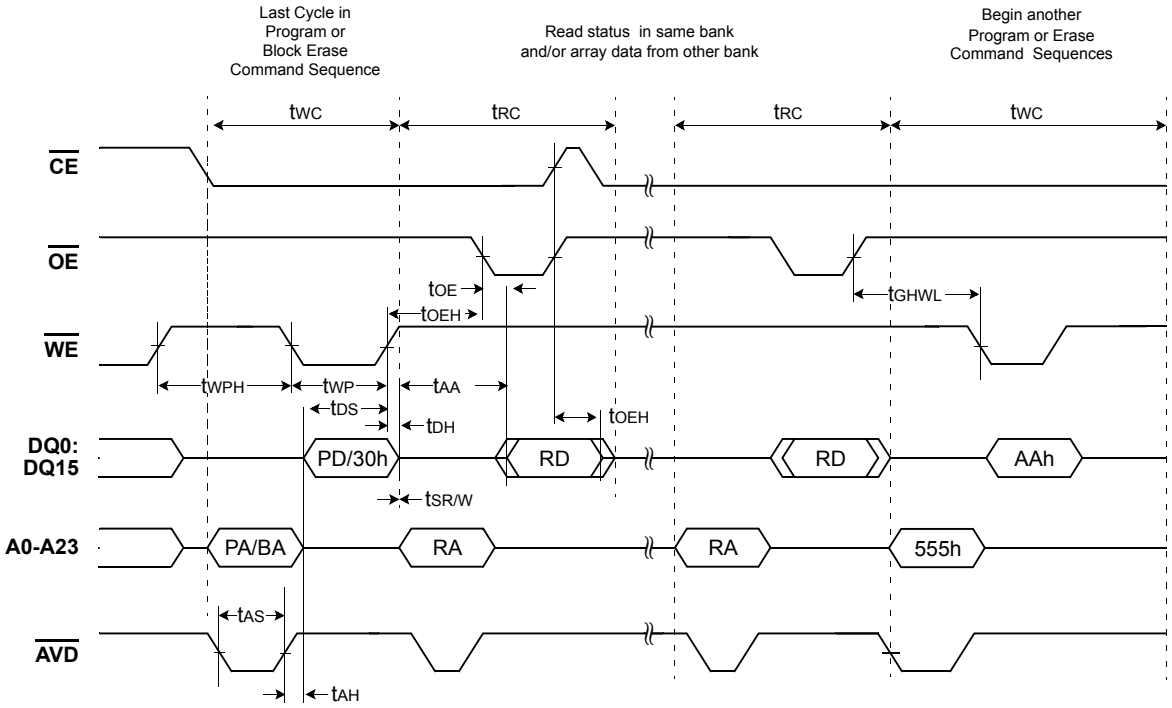


Figure 19: Read While Write Operation

NOTE :
Breakpoints in waveforms indicate that system may alternately read array data from the “non-busy bank” and checking the status of the program or erase operation in the “busy” bank.

19.0 CROSSING OF FIRST WORD BOUNDARY IN BURST READ MODE

The additional clock insertion for word boundary is needed only at the first crossing of word boundary. This means that no additional clock cycle is needed from 2nd word boundary crossing to the end of continuous burst read. Also, the number of additional clock cycle for the first word boundary can varies from zero to thirteen cycles, and the exact number of additional clock cycle depends on the starting address of burst read and programmable wait state settings.

For example, if the starting address is 16N+15 (the worst case) and programmable wait state setting(A<14:11>) is "0011" (which means data is valid on the 7th active CLK edge after $\overline{AVD}$ transition to Vih), six additional clock cycle is needed.

Similarly, if the starting address is 16N+15 (the worst case) and programmable wait state setting(A<14:11>) is "0010" (which means data is valid on the 6th active CLK edge after $\overline{AVD}$ transition to Vih), five additional clock cycle is needed.

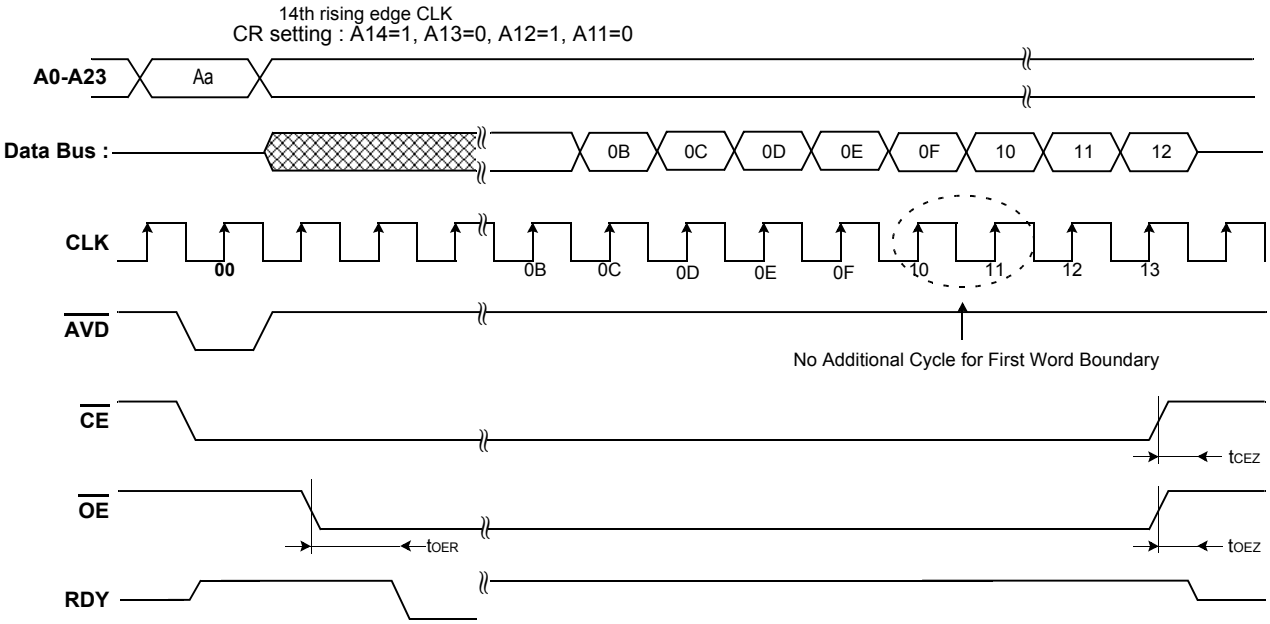
Below table shows the starting address vs. additional clock cycles for first word boundary.

Starting Address vs. Additional Clock Cycles for first word boundary

Srarting Address Group for Burst Read	The Residue of (Address/16)	LSB Bits of Address	Additional Clock Cycles for First Word Boundary (note1)				
			A<14:11> "0000" Valid data : 4th CLK	A<14:11> "0001" Valid data : 5th CLK	A<14:11> "0010" Valid data : 6th CLK	...	A<14:11> "1010" Valid data : 14th CLK
16N	0	0000	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+1	1	0001	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+2	2	0010	0 cycle	0 cycle	0 cycle	...	0 cycle
16N+3	3	0011	0 cycle	0 cycle	0 cycle	...	1 cycle
16N+4	4	0100	0 cycle	0 cycle	0 cycle	...	2 cycle
16N+5	5	0101	0 cycle	0 cycle	0 cycle	...	3 cycle
16N+6	6	0110	0 cycle	0 cycle	0 cycle	...	4 cycle
16N+7	7	0111	0 cycle	0 cycle	0 cycle	...	5 cycle
16N+8	8	1000	0 cycle	0 cycle	0 cycle	...	6 cycle
16N+9	9	1001	0 cycle	0 cycle	0 cycle	...	7 cycle
16N+10	10	1010	0 cycle	0 cycle	0 cycle	...	8 cycle
16N+11	11	1011	0 cycle	0 cycle	1 cycle	...	9 cycle
16N+12	12	1100	0 cycle	1 cycle	2 cycle	...	10 cycle
16N+13	13	1101	1 cycle	2 cycle	3 cycle	...	11 cycle
16N+14	14	1110	2 cycle	3 cycle	4 cycle	...	12 cycle
16N+15	15	1111	3 cycle	4 cycle	5 cycle	...	13 cycle

NOTE :
Address bit A<14:11> means the programmable wait state on burst mode configuration register. Refer to Table 10.

Case 1 : Start from "16N" address group

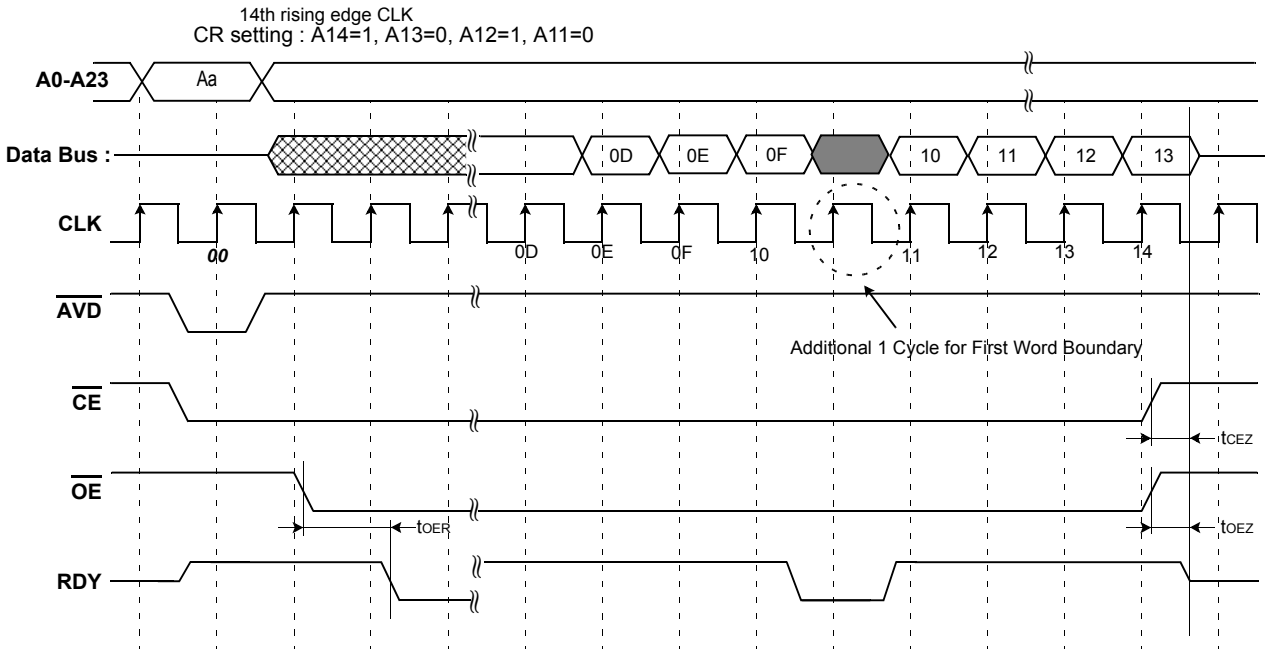


NOTE :

1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 20: Crossing of first word boundary in burst read mode.

Case 2 : Start from "16N+3" address group

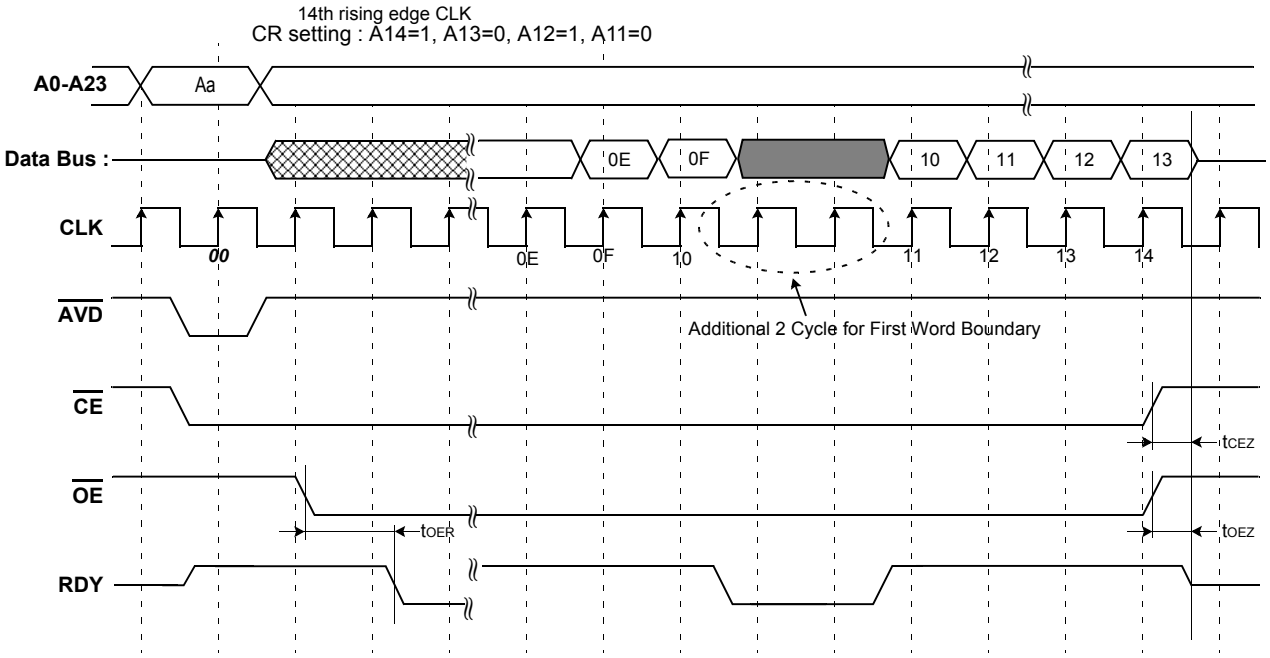


NOTE :

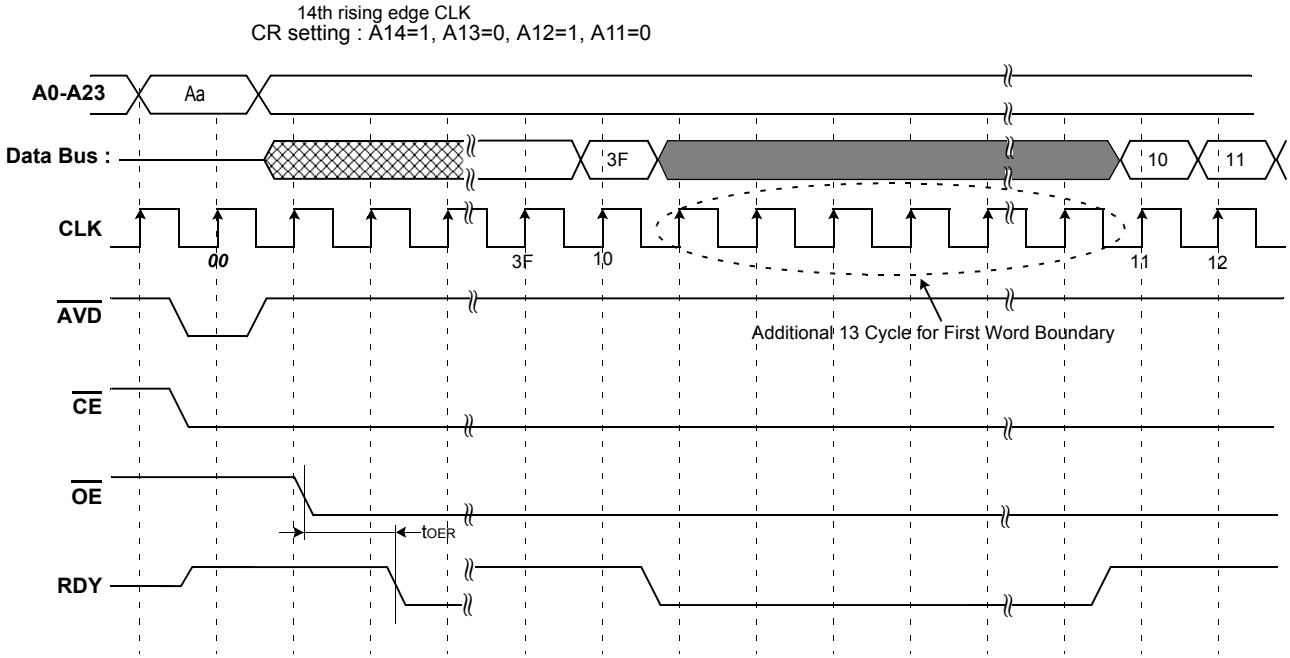
1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 21: Crossing of first word boundary in burst read mode.

Case3 : Start from "16N+4" address group



Case 4 : Start from "16N+15" address group



NOTE :

1) Address boundary occurs every 16 words beginning at address 000000FH , 000001FH , 000002FH , etc.
2) Address 000000H is also a boundary crossing.
3) No additional clock cycles are needed except for 1st boundary crossing.

Figure 22: Crossing of first word boundary in burst read mode.

[Table 16] Top Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA258	16 kwords	FFC000h-FFFFFFh
	BA257	16 kwords	FF8000h-FFBFFFh
	BA256	16 kwords	FF4000h-FF7FFFh
	BA255	16 kwords	FF0000h-FF3FFFh
	BA254	64 kwords	FE0000h-FEFFFFh
	BA253	64 kwords	FD0000h-FDFFFFh
	BA252	64 kwords	FC0000h-FCFFFFh
	BA251	64 kwords	FB0000h-FBFFFFh
	BA250	64 kwords	FA0000h-FAFFFFh
	BA249	64 kwords	F90000h-F9FFFFh
	BA248	64 kwords	F80000h-F8FFFFh
	BA247	64 kwords	F70000h-F7FFFFh
	BA246	64 kwords	F60000h-F6FFFFh
	BA245	64 kwords	F50000h-F5FFFFh
	BA244	64 kwords	F40000h-F4FFFFh
	BA243	64 kwords	F30000h-F3FFFFh
	BA242	64 kwords	F20000h-F2FFFFh
	BA241	64 kwords	F10000h-F1FFFFh
	BA240	64 kwords	F00000h-F0FFFFh
Bank 1	BA239	64 kwords	EF0000h-EFFFFFh
	BA238	64 kwords	EE0000h-EEFFFFh
	BA237	64 kwords	ED0000h-EDFFFFh
	BA236	64 kwords	EC0000h-ECFFFFh
	BA235	64 kwords	EB0000h-EBFFFFh
	BA234	64 kwords	EA0000h-EAFFFFh
	BA233	64 kwords	E90000h-E9FFFFh
	BA232	64 kwords	E80000h-E8FFFFh
	BA231	64 kwords	E70000h-E7FFFFh
	BA230	64 kwords	E60000h-E6FFFFh
	BA229	64 kwords	E50000h-E5FFFFh
	BA228	64 kwords	E40000h-E4FFFFh
	BA227	64 kwords	E30000h-E3FFFFh
	BA226	64 kwords	E20000h-E2FFFFh
	BA225	64 kwords	E10000h-E1FFFFh
	BA224	64 kwords	E00000h-E0FFFFh
Bank 2	BA223	64 kwords	DF0000h-DFFFFFh
	BA222	64 kwords	DE0000h-DEFFFFh
	BA221	64 kwords	DD0000h-DDFFFFh
	BA220	64 kwords	DC0000h-DCFFFFh
	BA219	64 kwords	DB0000h-DBFFFFh
	BA218	64 kwords	DA0000h-DAFFFFh
	BA217	64 kwords	D90000h-D9FFFFh
	BA216	64 kwords	D80000h-D8FFFFh
	BA215	64 kwords	D70000h-D7FFFFh
	BA214	64 kwords	D60000h-D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA213	64 kwords	D50000h-D5FFFFh
	BA212	64 kwords	D40000h-D4FFFFh
	BA211	64 kwords	D30000h-D3FFFFh
	BA210	64 kwords	D20000h-D2FFFFh
	BA209	64 kwords	D10000h-D1FFFFh
	BA208	64 kwords	D00000h-D0FFFFh
Bank 3	BA207	64 kwords	CF0000h-CFFFFFh
	BA206	64 kwords	CE0000h-CEFFFFh
	BA205	64 kwords	CD0000h-CDFFFFh
	BA204	64 kwords	CC0000h-CCFFFFh
	BA203	64 kwords	CB0000h-CBFFFFh
	BA202	64 kwords	CA0000h-CAFFFFh
	BA201	64 kwords	C90000h-C9FFFFh
	BA200	64 kwords	C80000h-C8FFFFh
	BA199	64 kwords	C70000h-C7FFFFh
	BA198	64 kwords	C60000h-C6FFFFh
	BA197	64 kwords	C50000h-C5FFFFh
	BA196	64 kwords	C40000h-C4FFFFh
	BA195	64 kwords	C30000h-C3FFFFh
	BA194	64 kwords	C20000h-C2FFFFh
	BA193	64 kwords	C10000h-C1FFFFh
	BA192	64 kwords	C00000h-C0FFFFh
Bank 4	BA191	64 kwords	BF0000h-BFFFFFh
	BA190	64 kwords	BE0000h-BEFFFFh
	BA189	64 kwords	BD0000h-BDFFFFh
	BA188	64 kwords	BC0000h-BCFFFFh
	BA187	64 kwords	BB0000h-BBFFFFh
	BA186	64 kwords	BA0000h-BAFFFFh
	BA185	64 kwords	B90000h-B9FFFFh
	BA184	64 kwords	B80000h-B8FFFFh
	BA183	64 kwords	B70000h-B7FFFFh
	BA182	64 kwords	B60000h-B6FFFFh
	BA181	64 kwords	B50000h-B5FFFFh
	BA180	64 kwords	B40000h-B4FFFFh
	BA179	64 kwords	B30000h-B3FFFFh
	BA178	64 kwords	B20000h-B2FFFFh
	BA177	64 kwords	B10000h-B1FFFFh
	BA176	64 kwords	B00000h-B0FFFFh
Bank 5	BA175	64 kwords	AF0000h-AFFFFFh
	BA174	64 kwords	AE0000h-AEFFFFh
	BA173	64 kwords	AD0000h-ADFFFFh
	BA172	64 kwords	AC0000h-ACFFFFh
	BA171	64 kwords	AB0000h-ABFFFFh
	BA170	64 kwords	AA0000h-AAFFFFh
	BA169	64 kwords	A90000h-A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 5	BA168	64 kwords	A80000h-A8FFFFh
	BA167	64 kwords	A70000h-A7FFFFh
	BA166	64 kwords	A60000h-A6FFFFh
	BA165	64 kwords	A50000h-A5FFFFh
	BA164	64 kwords	A40000h-A4FFFFh
	BA163	64 kwords	A30000h-A3FFFFh
	BA162	64 kwords	A20000h-A2FFFFh
	BA161	64 kwords	A10000h-A1FFFFh
	BA160	64 kwords	A00000h-A0FFFFh
Bank 6	BA159	64 kwords	9F0000h-9FFFFFh
	BA158	64 kwords	9E0000h-9EFFFFh
	BA157	64 kwords	9D0000h-9DFFFFh
	BA156	64 kwords	9C0000h-9CFFFFh
	BA155	64 kwords	9B0000h-9BFFFFh
	BA154	64 kwords	9A0000h-9AFFFFh
	BA153	64 kwords	990000h-99FFFFh
	BA152	64 kwords	980000h-98FFFFh
	BA151	64 kwords	970000h-97FFFFh
	BA150	64 kwords	960000h-96FFFFh
	BA149	64 kwords	950000h-95FFFFh
	BA148	64 kwords	940000h-94FFFFh
	BA147	64 kwords	930000h-93FFFFh
	BA146	64 kwords	920000h-92FFFFh
	BA145	64 kwords	910000h-91FFFFh
	BA144	64 kwords	900000h-90FFFFh
Bank 7	BA143	64 kwords	8F0000h-8FFFFFh
	BA142	64 kwords	8E0000h-08EFFFFh
	BA141	64 kwords	8D0000h-8DFFFFh
	BA140	64 kwords	8C0000h-8CFFFFh
	BA139	64 kwords	8B0000h-8BFFFFh
	BA138	64 kwords	8A0000h-8AFFFFh
	BA137	64 kwords	890000h-89FFFFh
	BA136	64 kwords	880000h-88FFFFh
	BA135	64 kwords	870000h-87FFFFh
	BA134	64 kwords	860000h-86FFFFh
	BA133	64 kwords	850000h-85FFFFh
	BA132	64 kwords	840000h-84FFFFh
	BA131	64 kwords	830000h-83FFFFh
	BA130	64 kwords	820000h-82FFFFh
	BA129	64 kwords	810000h-81FFFFh
	BA128	64 kwords	800000h-80FFFFh
Bank 8	BA127	64 kwords	7F0000h-7FFFFFh
	BA126	64 kwords	7E0000h-7EFFFFh
	BA125	64 kwords	7D0000h-7DFFFFh
	BA124	64 kwords	7C0000h-7CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 8	BA123	64 kwords	7B0000h-7BFFFFh
	BA122	64 kwords	7A0000h-7AFFFFh
	BA121	64 kwords	790000h-79FFFFh
	BA120	64 kwords	780000h-78FFFFh
	BA119	64 kwords	770000h-77FFFFh
	BA118	64 kwords	760000h-76FFFFh
	BA117	64 kwords	750000h-75FFFFh
	BA116	64 kwords	740000h-74FFFFh
	BA115	64 kwords	730000h-73FFFFh
	BA114	64 kwords	720000h-72FFFFh
	BA113	64 kwords	710000h-71FFFFh
	BA112	64 kwords	700000h-70FFFFh
Bank 9	BA111	64 kwords	6F0000h-6FFFFFh
	BA110	64 kwords	6E0000h-6EFFFFh
	BA109	64 kwords	6D0000h-6DFFFFh
	BA108	64 kwords	6C0000h-6CFFFFh
	BA107	64 kwords	6B0000h-6BFFFFh
	BA106	64 kwords	6A0000h-6AFFFFh
	BA105	64 kwords	690000h-69FFFFh
	BA104	64 kwords	680000h-68FFFFh
	BA103	64 kwords	670000h-67FFFFh
	BA102	64 kwords	660000h-66FFFFh
	BA101	64 kwords	650000h-65FFFFh
	BA100	64 kwords	640000h-64FFFFh
	BA99	64 kwords	630000h-63FFFFh
	BA98	64 kwords	620000h-62FFFFh
	BA97	64 kwords	610000h-61FFFFh
	BA96	64 kwords	600000h-60FFFFh
Bank10	BA95	64 kwords	5F0000h-5FFFFFh
	BA94	64 kwords	5E0000h-5EFFFFh
	BA93	64 kwords	5D0000h-5DFFFFh
	BA92	64 kwords	5C0000h-5CFFFFh
	BA91	64 kwords	5B0000h-5BFFFFh
	BA90	64 kwords	5A0000h-5AFFFFh
	BA89	64 kwords	590000h-59FFFFh
	BA88	64 kwords	580000h-58FFFFh
	BA87	64 kwords	570000h-57FFFFh
	BA86	64 kwords	560000h-56FFFFh
	BA85	64 kwords	550000h-55FFFFh
	BA84	64 kwords	540000h-54FFFFh
	BA83	64 kwords	530000h-53FFFFh
	BA82	64 kwords	520000h-52FFFFh
	BA81	64 kwords	510000h-51FFFFh
	BA80	64 kwords	500000h-50FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 11	BA79	64 kwords	4F0000h-4FFFFFh
	BA78	64 kwords	4E0000h-4EFFFFh
	BA77	64 kwords	4D0000h-4DFFFFh
	BA76	64 kwords	4C0000h-4CFFFFh
	BA75	64 kwords	4B0000h-4BFFFFh
	BA74	64 kwords	4A0000h-4AFFFFh
	BA73	64 kwords	490000h-49FFFFh
	BA72	64 kwords	480000h-48FFFFh
	BA71	64 kwords	470000h-47FFFFh
	BA70	64 kwords	460000h-46FFFFh
	BA69	64 kwords	450000h-45FFFFh
	BA68	64 kwords	440000h-44FFFFh
	BA67	64 kwords	430000h-43FFFFh
	BA66	64 kwords	420000h-42FFFFh
	BA65	64 kwords	410000h-41FFFFh
	BA64	64 kwords	400000h-40FFFFh
Bank 12	BA63	64 kwords	3F0000h-3FFFFFh
	BA62	64 kwords	3E0000h-3EFFFFh
	BA61	64 kwords	3D0000h-3DFFFFh
	BA60	64 kwords	3C0000h-3CFFFFh
	BA59	64 kwords	3B0000h-3BFFFFh
	BA58	64 kwords	3A0000h-3AFFFFh
	BA57	64 kwords	390000h-39FFFFh
	BA56	64 kwords	380000h-38FFFFh
	BA55	64 kwords	370000h-37FFFFh
	BA54	64 kwords	360000h-36FFFFh
	BA53	64 kwords	350000h-35FFFFh
	BA52	64 kwords	340000h-34FFFFh
	BA51	64 kwords	330000h-33FFFFh
	BA50	64 kwords	320000h-32FFFFh
	BA49	64 kwords	310000h-31FFFFh
	BA48	64 kwords	300000h-30FFFFh
Bank 13	BA47	64 kwords	2F0000h-2FFFFFh
	BA46	64 kwords	2E0000h-2EFFFFh
	BA45	64 kwords	2D0000h-2DFFFFh
	BA44	64 kwords	2C0000h-2CFFFFh
	BA43	64 kwords	2B0000h-2BFFFFh
	BA42	64 kwords	2A0000h-2AFFFFh
	BA41	64 kwords	290000h-29FFFFh
	BA40	64 kwords	280000h-28FFFFh
	BA39	64 kwords	270000h-27FFFFh
	BA38	64 kwords	260000h-26FFFFh
	BA37	64 kwords	250000h-25FFFFh
	BA36	64 kwords	240000h-24FFFFh
	BA35	64 kwords	230000h-23FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA34	64 kwords	220000h-22FFFFh
	BA33	64 kwords	210000h-21FFFFh
	BA32	64 kwords	200000h-20FFFFh
Bank 14	BA31	64 kwords	1F0000h-1FFFFFh
	BA30	64 kwords	1E0000h-1EFFFFh
	BA29	64 kwords	1D0000h-1DFFFFh
	BA28	64 kwords	1C0000h-1CFFFFh
	BA27	64 kwords	1B0000h-1BFFFFh
	BA26	64 kwords	1A0000h-1AFFFFh
	BA25	64 kwords	190000h-19FFFFh
	BA24	64 kwords	180000h-18FFFFh
	BA23	64 kwords	170000h-17FFFFh
	BA22	64 kwords	160000h-16FFFFh
	BA21	64 kwords	150000h-15FFFFh
	BA20	64 kwords	140000h-14FFFFh
	BA19	64 kwords	130000h-13FFFFh
	BA18	64 kwords	120000h-12FFFFh
	BA17	64 kwords	110000h-11FFFFh
	BA16	64 kwords	100000h-10FFFFh
Bank 15	BA15	64 kwords	0F0000h-0FFFFFh
	BA14	64 kwords	0E0000h-0EFFFFh
	BA13	64 kwords	0D0000h-0DFFFFh
	BA12	64 kwords	0C0000h-0CFFFFh
	BA11	64 kwords	0B0000h-0BFFFFh
	BA10	64 kwords	0A0000h-0AFFFFh
	BA9	64 kwords	090000h-09FFFFh
	BA8	64 kwords	080000h-08FFFFh
	BA7	64 kwords	070000h-07FFFFh
	BA6	64 kwords	060000h-06FFFFh
	BA5	64 kwords	050000h-05FFFFh
	BA4	64 kwords	040000h-04FFFFh
	BA3	64 kwords	030000h-03FFFFh
	BA2	64 kwords	020000h-02FFFFh
	BA1	64 kwords	010000h-01FFFFh
	BA0	64 kwords	000000h-00FFFFh

[Table 17] OTP Block Addresses

	Block Address A23 ~ A8	Block Size	(x16) Address Range*
OTP	FFFFh	512words	FFFE00h-FFFFFFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.

[Table 18] Bottom Boot Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 15	BA258	64 kwords	FF0000h-FFFFFFh
	BA257	64 kwords	FE0000h-FEFFFFh
	BA256	64 kwords	FD0000h-FDFFFFh
	BA255	64 kwords	FC0000h-FCFFFFh
	BA254	64 kwords	FB0000h-FBFFFFh
	BA253	64 kwords	FA0000h-FAFFFFh
	BA252	64 kwords	F90000h-F9FFFFh
	BA251	64 kwords	F80000h-F8FFFFh
	BA250	64 kwords	F70000h-F7FFFFh
	BA249	64 kwords	F60000h-F6FFFFh
	BA248	64 kwords	F50000h-F5FFFFh
	BA247	64 kwords	F40000h-F4FFFFh
	BA246	64 kwords	F30000h-F3FFFFh
	BA245	64 kwords	F20000h-F2FFFFh
	BA244	64 kwords	F10000h-F1FFFFh
	BA243	64 kwords	F00000h-F0FFFFh
Bank 14	BA242	64 kwords	EF0000h-EFFFFFh
	BA241	64 kwords	EE0000h-EEFFFFh
	BA240	64 kwords	ED0000h-EDFFFFh
	BA239	64 kwords	EC0000h-ECFFFFh
	BA238	64 kwords	EB0000h-EBFFFFh
	BA237	64 kwords	EA0000h-EAFFFFh
	BA236	64 kwords	E90000h-E9FFFFh
	BA235	64 kwords	E80000h-E8FFFFh
	BA234	64 kwords	E70000h-E7FFFFh
	BA233	64 kwords	E60000h-E6FFFFh
	BA232	64 kwords	E50000h-E5FFFFh
	BA231	64 kwords	E40000h-E4FFFFh
	BA230	64 kwords	E30000h-E3FFFFh
	BA229	64 kwords	E20000h-E2FFFFh
	BA228	64 kwords	E10000h-E1FFFFh
	BA227	64 kwords	E00000h-E0FFFFh
Bank 13	BA226	64 kwords	DF0000h-DFFFFFh
	BA225	64 kwords	DE0000h-DEFFFFh
	BA224	64 kwords	DD0000h-DDFFFFh
	BA223	64 kwords	DC0000h-DCFFFFh
	BA222	64 kwords	DB0000h-DBFFFFh
	BA221	64 kwords	DA0000h-DAFFFFh
	BA220	64 kwords	D90000h-D9FFFFh
	BA219	64 kwords	D80000h-D8FFFFh
	BA218	64 kwords	D70000h-D7FFFFh
	BA217	64 kwords	D60000h-D6FFFFh
	BA216	64 kwords	D50000h-D5FFFFh
	BA215	64 kwords	D40000h-D4FFFFh
	BA214	64 kwords	D30000h-D3FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA213	64 kwords	D20000h-D2FFFFh
	BA212	64 kwords	D10000h-D1FFFFh
	BA211	64 kwords	D00000h-D0FFFFh
Bank 12	BA210	64 kwords	CF0000h-CFFFFFh
	BA209	64 kwords	CE0000h-CEFFFFh
	BA208	64 kwords	CD0000h-CDFFFFh
	BA207	64 kwords	CC0000h-CCFFFFh
	BA206	64 kwords	CB0000h-CBFFFFh
	BA205	64 kwords	CA0000h-CAFFFFh
	BA204	64 kwords	C90000h-C9FFFFh
	BA203	64 kwords	C80000h-C8FFFFh
	BA202	64 kwords	C70000h-C7FFFFh
	BA201	64 kwords	C60000h-C6FFFFh
	BA200	64 kwords	C50000h-C5FFFFh
	BA199	64 kwords	C40000h-C4FFFFh
	BA198	64 kwords	C30000h-C3FFFFh
	BA197	64 kwords	C20000h-C2FFFFh
	BA196	64 kwords	C10000h-C1FFFFh
	BA195	64 kwords	C00000h-C0FFFFh
Bank 11	BA194	64 kwords	BF0000h-BFFFFFh
	BA193	64 kwords	BE0000h-BEFFFFh
	BA192	64 kwords	BD0000h-BDFFFFh
	BA191	64 kwords	BC0000h-BCFFFFh
	BA190	64 kwords	BB0000h-BBFFFFh
	BA189	64 kwords	BA0000h-BAFFFFh
	BA188	64 kwords	B90000h-B9FFFFh
	BA187	64 kwords	B80000h-B8FFFFh
	BA186	64 kwords	B70000h-B7FFFFh
	BA185	64 kwords	B60000h-B6FFFFh
	BA184	64 kwords	B50000h-B5FFFFh
	BA183	64 kwords	B40000h-B4FFFFh
	BA182	64 kwords	B30000h-B3FFFFh
	BA181	64 kwords	B20000h-B2FFFFh
	BA180	64 kwords	B10000h-B1FFFFh
	BA179	64 kwords	B00000h-B0FFFFh
Bank 10	BA178	64 kwords	AF0000h-AFFFFFh
	BA177	64 kwords	AE0000h-AEFFFFh
	BA176	64 kwords	AD0000h-ADFFFFh
	BA175	64 kwords	AC0000h-ACFFFFh
	BA174	64 kwords	AB0000h-ABFFFFh
	BA173	64 kwords	AA0000h-AAFFFFh
	BA172	64 kwords	A90000h-A9FFFFh
	BA171	64 kwords	A80000h-A8FFFFh
	BA170	64 kwords	A70000h-A7FFFFh
	BA169	64 kwords	A60000h-A6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 10	BA168	64 kwords	A50000h-A5FFFFh
	BA167	64 kwords	A40000h-A4FFFFh
	BA166	64 kwords	A30000h-A3FFFFh
	BA165	64 kwords	A20000h-A2FFFFh
	BA164	64 kwords	A10000h-A1FFFFh
	BA163	64 kwords	A00000h-A0FFFFh
Bank 9	BA162	64 kwords	9F0000h-9FFFFFh
	BA161	64 kwords	9E0000h-9EFFFFh
	BA160	64 kwords	9D0000h-9DFFFFh
	BA159	64 kwords	9C0000h-9CFFFFh
	BA158	64 kwords	9B0000h-9BFFFFh
	BA157	64 kwords	9A0000h-9AFFFFh
	BA156	64 kwords	990000h-99FFFFh
	BA155	64 kwords	980000h-98FFFFh
	BA154	64 kwords	970000h-97FFFFh
	BA153	64 kwords	960000h-96FFFFh
	BA152	64 kwords	950000h-95FFFFh
	BA151	64 kwords	940000h-94FFFFh
	BA150	64 kwords	930000h-93FFFFh
	BA149	64 kwords	920000h-92FFFFh
	BA148	64 kwords	910000h-91FFFFh
	BA147	64 kwords	900000h-90FFFFh
Bank 8	BA146	64 kwords	8F0000h-8FFFFFh
	BA145	64 kwords	8E0000h-08EFFFFh
	BA144	64 kwords	8D0000h-8DFFFFh
	BA143	64 kwords	8C0000h-8CFFFFh
	BA142	64 kwords	8B0000h-8BFFFFh
	BA141	64 kwords	8A0000h-8AFFFFh
	BA140	64 kwords	890000h-89FFFFh
	BA139	64 kwords	880000h-88FFFFh
	BA138	64 kwords	870000h-87FFFFh
	BA137	64 kwords	860000h-86FFFFh
	BA136	64 kwords	850000h-85FFFFh
	BA135	64 kwords	840000h-84FFFFh
	BA134	64 kwords	830000h-83FFFFh
	BA133	64 kwords	820000h-82FFFFh
	BA132	64 kwords	810000h-81FFFFh
	BA131	64 kwords	800000h-80FFFFh
Bank 7	BA130	64 kwords	7F0000h-7FFFFFh
	BA129	64 kwords	7E0000h-7EFFFFh
	BA128	64 kwords	7D0000h-7DFFFFh
	BA127	64 kwords	7C0000h-7CFFFFh
	BA126	64 kwords	7B0000h-7BFFFFh
	BA125	64 kwords	7A0000h-7AFFFFh
	BA124	64 kwords	790000h-79FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 7	BA123	64 kwords	780000h-78FFFFh
	BA122	64 kwords	770000h-77FFFFh
	BA121	64 kwords	760000h-76FFFFh
	BA120	64 kwords	750000h-75FFFFh
	BA119	64 kwords	740000h-74FFFFh
	BA118	64 kwords	730000h-73FFFFh
	BA117	64 kwords	720000h-72FFFFh
	BA116	64 kwords	710000h-71FFFFh
	BA115	64 kwords	700000h-70FFFFh
Bank 6	BA114	64 kwords	6F0000h-6FFFFFh
	BA113	64 kwords	6E0000h-6EFFFFh
	BA112	64 kwords	6D0000h-6DFFFFh
	BA111	64 kwords	6C0000h-6CFFFFh
	BA110	64 kwords	6B0000h-6BFFFFh
	BA109	64 kwords	6A0000h-6AFFFFh
	BA108	64 kwords	690000h-69FFFFh
	BA107	64 kwords	680000h-68FFFFh
	BA106	64 kwords	670000h-67FFFFh
	BA105	64 kwords	660000h-66FFFFh
	BA104	64 kwords	650000h-65FFFFh
	BA103	64 kwords	640000h-64FFFFh
	BA102	64 kwords	630000h-63FFFFh
	BA101	64 kwords	620000h-62FFFFh
	BA100	64 kwords	610000h-61FFFFh
	BA99	64 kwords	600000h-60FFFFh
Bank5	BA98	64 kwords	5F0000h-5FFFFFh
	BA97	64 kwords	5E0000h-5EFFFFh
	BA96	64 kwords	5D0000h-5DFFFFh
	BA95	64 kwords	5C0000h-5CFFFFh
	BA94	64 kwords	5B0000h-5BFFFFh
	BA93	64 kwords	5A0000h-5AFFFFh
	BA92	64 kwords	590000h-59FFFFh
	BA91	64 kwords	580000h-58FFFFh
	BA90	64 kwords	570000h-57FFFFh
	BA89	64 kwords	560000h-56FFFFh
	BA88	64 kwords	550000h-55FFFFh
	BA87	64 kwords	540000h-54FFFFh
	BA86	64 kwords	530000h-53FFFFh
	BA85	64 kwords	520000h-52FFFFh
	BA84	64 kwords	510000h-51FFFFh
	BA83	64 kwords	500000h-50FFFFh
Bank4	BA82	64 kwords	4F0000h-4FFFFFh
	BA81	64 kwords	4E0000h-4EFFFFh
	BA80	64 kwords	4D0000h-4DFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 4	BA79	64 kwords	4C0000h-4CFFFFh
	BA78	64 kwords	4B0000h-4BFFFFh
	BA77	64 kwords	4A0000h-4AFFFFh
	BA76	64 kwords	490000h-49FFFFh
	BA75	64 kwords	480000h-48FFFFh
	BA74	64 kwords	470000h-47FFFFh
	BA73	64 kwords	460000h-46FFFFh
	BA72	64 kwords	450000h-45FFFFh
	BA71	64 kwords	440000h-44FFFFh
	BA70	64 kwords	430000h-43FFFFh
	BA69	64 kwords	420000h-42FFFFh
	BA68	64 kwords	410000h-41FFFFh
	BA67	64 kwords	400000h-40FFFFh
Bank 3	BA66	64 kwords	3F0000h-3FFFFFh
	BA65	64 kwords	3E0000h-3EFFFFh
	BA64	64 kwords	3D0000h-3DFFFFh
	BA63	64 kwords	3C0000h-3CFFFFh
	BA62	64 kwords	3B0000h-3BFFFFh
	BA61	64 kwords	3A0000h-3AFFFFh
	BA60	64 kwords	390000h-39FFFFh
	BA59	64 kwords	380000h-38FFFFh
	BA58	64 kwords	370000h-37FFFFh
	BA57	64 kwords	360000h-36FFFFh
	BA56	64 kwords	350000h-35FFFFh
	BA55	64 kwords	340000h-34FFFFh
	BA54	64 kwords	330000h-33FFFFh
	BA53	64 kwords	320000h-32FFFFh
	BA52	64 kwords	310000h-31FFFFh
	BA51	64 kwords	300000h-30FFFFh
Bank 2	BA50	64 kwords	2F0000h-2FFFFFh
	BA49	64 kwords	2E0000h-2EFFFFh
	BA48	64 kwords	2D0000h-2DFFFFh
	BA47	64 kwords	2C0000h-2CFFFFh
	BA46	64 kwords	2B0000h-2BFFFFh
	BA45	64 kwords	2A0000h-2AFFFFh
	BA44	64 kwords	290000h-29FFFFh
	BA43	64 kwords	280000h-28FFFFh
	BA42	64 kwords	270000h-27FFFFh
	BA41	64 kwords	260000h-26FFFFh
	BA40	64 kwords	250000h-25FFFFh
	BA39	64 kwords	240000h-24FFFFh
	BA38	64 kwords	230000h-23FFFFh
	BA37	64 kwords	220000h-22FFFFh
	BA36	64 kwords	210000h-21FFFFh
	BA35	64 kwords	200000h-20FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 1	BA34	64 kwords	1F0000h-1FFFFFh
	BA33	64 kwords	1E0000h-1EFFFFh
	BA32	64 kwords	1D0000h-1DFFFFh
	BA31	64 kwords	1C0000h-1CFFFFh
	BA30	64 kwords	1B0000h-1BFFFFh
	BA29	64 kwords	1A0000h-1AFFFFh
	BA28	64 kwords	190000h-19FFFFh
	BA27	64 kwords	180000h-18FFFFh
	BA26	64 kwords	170000h-17FFFFh
	BA25	64 kwords	160000h-16FFFFh
	BA24	64 kwords	150000h-15FFFFh
	BA23	64 kwords	140000h-14FFFFh
	BA22	64 kwords	130000h-13FFFFh
	BA21	64 kwords	120000h-12FFFFh
	BA20	64 kwords	110000h-11FFFFh
	BA19	64 kwords	100000h-10FFFFh
Bank 0	BA18	64 kwords	0F0000h-0FFFFFh
	BA17	64 kwords	0E0000h-0EFFFFh
	BA16	64 kwords	0D0000h-0DFFFFh
	BA15	64 kwords	0C0000h-0CFFFFh
	BA14	64 kwords	0B0000h-0BFFFFh
	BA13	64 kwords	0A0000h-0AFFFFh
	BA12	64 kwords	090000h-09FFFFh
	BA11	64 kwords	080000h-08FFFFh
	BA10	64 kwords	070000h-07FFFFh
	BA9	64 kwords	060000h-06FFFFh
	BA8	64 kwords	050000h-05FFFFh
	BA7	64 kwords	040000h-04FFFFh
	BA6	64 kwords	030000h-03FFFFh
	BA5	64 kwords	020000h-02FFFFh
	BA4	64 kwords	010000h-01FFFFh
	BA3	16 kwords	00C000h-00FFFFh
	BA2	16 kwords	008000h-00BFFFh
	BA1	16 kwords	004000h-007FFFh
	BA0	16 kwords	000000h-003FFFh

[Table 19] Bottom Boot OTP Block Addresses

	Block Address A23 ~ A8	Block Size	(x16) Address Range*
OTP	0000h	512 words	000000h-0001FFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.

[Table 20] Uniform Block Address Table

Bank	Block	Block Size	(x16) Address Range
Bank 0	BA255	64 kwords	0FF0000h-0FFFFFFh
	BA254	64 kwords	0FE0000h-0FEFFFFh
	BA253	64 kwords	0FD0000h-0FDFFFFh
	BA252	64 kwords	0FC0000h-0FCFFFFh
	BA251	64 kwords	0FB0000h-0FBFFFFh
	BA250	64 kwords	0FA0000h-0FAFFFFh
	BA249	64 kwords	0F90000h-0F9FFFFh
	BA248	64 kwords	0F80000h-0F8FFFFh
	BA247	64 kwords	0F70000h-0F7FFFFh
	BA246	64 kwords	0F60000h-0F6FFFFh
	BA245	64 kwords	0F50000h-0F5FFFFh
	BA244	64 kwords	0F40000h-0F4FFFFh
	BA243	64 kwords	0F30000h-0F3FFFFh
	BA242	64 kwords	0F20000h-0F2FFFFh
	BA241	64 kwords	0F10000h-0F1FFFFh
	BA240	64 kwords	0F00000h-0F0FFFFh
Bank 1	BA239	64 kwords	0EF0000h-0EFFFFFh
	BA238	64 kwords	0EE0000h-0EEFFFFh
	BA237	64 kwords	0ED0000h-0EDFFFFh
	BA236	64 kwords	0EC0000h-0ECFFFFh
	BA235	64 kwords	0EB0000h-0EBFFFFh
	BA234	64 kwords	0EA0000h-0EAFFFFh
	BA233	64 kwords	0E90000h-0E9FFFFh
	BA232	64 kwords	0E80000h-0E8FFFFh
	BA231	64 kwords	0E70000h-0E7FFFFh
	BA230	64 kwords	0E60000h-0E6FFFFh
	BA229	64 kwords	0E50000h-0E5FFFFh
	BA228	64 kwords	0E40000h-0E4FFFFh
	BA227	64 kwords	0E30000h-0E3FFFFh
	BA226	64 kwords	0E20000h-0E2FFFFh
	BA225	64 kwords	0E10000h-0E1FFFFh
	BA224	64 kwords	0E00000h-0E0FFFFh
Bank 2	BA223	64 kwords	0DF0000h-0DFFFFFh
	BA222	64 kwords	0DE0000h-0DEFFFFh
	BA221	64 kwords	0DD0000h-0DDFFFFh
	BA220	64 kwords	0DC0000h-0DCFFFFh
	BA219	64 kwords	0DB0000h-0DBFFFFh
	BA218	64 kwords	0DA0000h-0DAFFFFh
	BA217	64 kwords	0D90000h-0D9FFFFh
	BA216	64 kwords	0D80000h-0D8FFFFh
	BA215	64 kwords	0D70000h-0D7FFFFh
	BA214	64 kwords	0D60000h-0D6FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 2	BA213	64 kwords	0D50000h-0D5FFFFh
	BA212	64 kwords	0D40000h-0D4FFFFh
	BA211	64 kwords	0D30000h-0D3FFFFh
	BA210	64 kwords	0D20000h-0D2FFFFh
	BA209	64 kwords	0D10000h-0D1FFFFh
	BA208	64 kwords	0D00000h-0D0FFFFh
Bank 3	BA207	64 kwords	0CF0000h-0CFFFFFh
	BA206	64 kwords	0CE0000h-0CEFFFFh
	BA205	64 kwords	0CD0000h-0CDFFFFh
	BA204	64 kwords	0CC0000h-0CCFFFFh
	BA203	64 kwords	0CB0000h-0CBFFFFh
	BA202	64 kwords	0CA0000h-0CAFFFFh
	BA201	64 kwords	0C90000h-0C9FFFFh
	BA200	64 kwords	0C80000h-0C8FFFFh
	BA199	64 kwords	0C70000h-0C7FFFFh
	BA198	64 kwords	0C60000h-0C6FFFFh
	BA197	64 kwords	0C50000h-0C5FFFFh
	BA196	64 kwords	0C40000h-0C4FFFFh
	BA195	64 kwords	0C30000h-0C3FFFFh
	BA194	64 kwords	0C20000h-0C2FFFFh
	BA193	64 kwords	0C10000h-0C1FFFFh
	BA192	64 kwords	0C00000h-0C0FFFFh
Bank 4	BA191	64 kwords	0BF0000h-0BFFFFFh
	BA190	64 kwords	0BE0000h-0BEFFFFh
	BA189	64 kwords	0BD0000h-0BDFFFFh
	BA188	64 kwords	0BC0000h-0BCFFFFh
	BA187	64 kwords	0BB0000h-0BBFFFFh
	BA186	64 kwords	0BA0000h-0BAFFFFh
	BA185	64 kwords	0B90000h-0B9FFFFh
	BA184	64 kwords	0B80000h-0B8FFFFh
	BA183	64 kwords	0B70000h-0B7FFFFh
	BA182	64 kwords	0B60000h-0B6FFFFh
	BA181	64 kwords	0B50000h-0B5FFFFh
	BA180	64 kwords	0B40000h-0B4FFFFh
	BA179	64 kwords	0B30000h-0B3FFFFh
	BA178	64 kwords	0B20000h-0B2FFFFh
	BA177	64 kwords	0B10000h-0B1FFFFh
	BA176	64 kwords	0B00000h-0B0FFFFh
Bank 5	BA175	64 kwords	0AF0000h-0AFFFFFh
	BA174	64 kwords	0AE0000h-0AEFFFFh
	BA173	64 kwords	0AD0000h-0ADFFFFh
	BA172	64 kwords	0AC0000h-0ACFFFFh
	BA171	64 kwords	0AB0000h-0ABFFFFh
	BA170	64 kwords	0AA0000h-0AAFFFFh
	BA169	64 kwords	0A90000h-0A9FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 5	BA168	64 kwords	0A80000h-0A8FFFFh
	BA167	64 kwords	0A70000h-0A7FFFFh
	BA166	64 kwords	0A60000h-0A6FFFFh
	BA165	64 kwords	0A50000h-0A5FFFFh
	BA164	64 kwords	0A40000h-0A4FFFFh
	BA163	64 kwords	0A30000h-0A3FFFFh
	BA162	64 kwords	0A20000h-0A2FFFFh
	BA161	64 kwords	0A10000h-0A1FFFFh
	BA160	64 kwords	0A00000h-0A0FFFFh
Bank 6	BA159	64 kwords	09F0000h-09FFFFFh
	BA158	64 kwords	09E0000h-09EFFFFh
	BA157	64 kwords	09D0000h-09DFFFFh
	BA156	64 kwords	09C0000h-09CFFFFh
	BA155	64 kwords	09B0000h-09BFFFFh
	BA154	64 kwords	09A0000h-09AFFFFh
	BA153	64 kwords	0990000h-099FFFFh
	BA152	64 kwords	0980000h-098FFFFh
	BA151	64 kwords	0970000h-097FFFFh
	BA150	64 kwords	0960000h-096FFFFh
	BA149	64 kwords	0950000h-095FFFFh
	BA148	64 kwords	0940000h-094FFFFh
	BA147	64 kwords	0930000h-093FFFFh
	BA146	64 kwords	0920000h-092FFFFh
	BA145	64 kwords	0910000h-091FFFFh
	BA144	64 kwords	0900000h-090FFFFh
Bank 7	BA143	64 kwords	08F0000h-08FFFFFh
	BA142	64 kwords	08E0000h-08EFFFFh
	BA141	64 kwords	08D0000h-08DFFFFh
	BA140	64 kwords	08C0000h-08CFFFFh
	BA139	64 kwords	08B0000h-08BFFFFh
	BA138	64 kwords	08A0000h-08AFFFFh
	BA137	64 kwords	0890000h-089FFFFh
	BA136	64 kwords	0880000h-088FFFFh
	BA135	64 kwords	0870000h-087FFFFh
	BA134	64 kwords	0860000h-086FFFFh
	BA133	64 kwords	0850000h-085FFFFh
	BA132	64 kwords	0840000h-084FFFFh
	BA131	64 kwords	0830000h-083FFFFh
	BA130	64 kwords	0820000h-082FFFFh
	BA129	64 kwords	0810000h-081FFFFh
	BA128	64 kwords	0800000h-080FFFFh
Bank 8	BA127	64 kwords	07F0000h-07FFFFFh
	BA126	64 kwords	07E0000h-07EFFFFh
	BA125	64 kwords	07D0000h-07DFFFFh
	BA124	64 kwords	07C0000h-07CFFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 8	BA123	64 kwords	07B0000h-07BFFFFh
	BA122	64 kwords	07A0000h-07AFFFFh
	BA121	64 kwords	0790000h-079FFFFh
	BA120	64 kwords	0780000h-078FFFFh
	BA119	64 kwords	0770000h-077FFFFh
	BA118	64 kwords	0760000h-076FFFFh
	BA117	64 kwords	0750000h-075FFFFh
	BA116	64 kwords	0740000h-074FFFFh
	BA115	64 kwords	0730000h-073FFFFh
	BA114	64 kwords	0720000h-072FFFFh
	BA113	64 kwords	0710000h-071FFFFh
	BA112	64 kwords	0700000h-070FFFFh
Bank 9	BA111	64 kwords	06F0000h-06FFFFFh
	BA110	64 kwords	06E0000h-06EFFFFh
	BA109	64 kwords	06D0000h-06DFFFFh
	BA108	64 kwords	06C0000h-06CFFFFh
	BA107	64 kwords	06B0000h-06BFFFFh
	BA106	64 kwords	06A0000h-06AFFFFh
	BA105	64 kwords	0690000h-069FFFFh
	BA104	64 kwords	0680000h-068FFFFh
	BA103	64 kwords	0670000h-067FFFFh
	BA102	64 kwords	0660000h-066FFFFh
	BA101	64 kwords	0650000h-065FFFFh
	BA100	64 kwords	0640000h-064FFFFh
	BA99	64 kwords	0630000h-063FFFFh
	BA98	64 kwords	0620000h-062FFFFh
	BA97	64 kwords	0610000h-061FFFFh
	BA96	64 kwords	0600000h-060FFFFh
Bank10	BA95	64 kwords	05F0000h-05FFFFFh
	BA94	64 kwords	05E0000h-05EFFFFh
	BA93	64 kwords	05D0000h-05DFFFFh
	BA92	64 kwords	05C0000h-05CFFFFh
	BA91	64 kwords	05B0000h-05BFFFFh
	BA90	64 kwords	05A0000h-05AFFFFh
	BA89	64 kwords	0590000h-059FFFFh
	BA88	64 kwords	0580000h-058FFFFh
	BA87	64 kwords	0570000h-057FFFFh
	BA86	64 kwords	0560000h-056FFFFh
	BA85	64 kwords	0550000h-055FFFFh
	BA84	64 kwords	0540000h-054FFFFh
	BA83	64 kwords	0530000h-053FFFFh
	BA82	64 kwords	0520000h-052FFFFh
	BA81	64 kwords	0510000h-051FFFFh
	BA80	64 kwords	0500000h-050FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 11	BA79	64 kwords	04F0000h-04FFFFFh
	BA78	64 kwords	04E0000h-04EFFFFh
	BA77	64 kwords	04D0000h-04DFFFFh
	BA76	64 kwords	04C0000h-04CFFFFh
	BA75	64 kwords	04B0000h-04BFFFFh
	BA74	64 kwords	04A0000h-04AFFFFh
	BA73	64 kwords	0490000h-049FFFFh
	BA72	64 kwords	0480000h-048FFFFh
	BA71	64 kwords	0470000h-047FFFFh
	BA70	64 kwords	0460000h-046FFFFh
	BA69	64 kwords	0450000h-045FFFFh
	BA68	64 kwords	0440000h-044FFFFh
	BA67	64 kwords	0430000h-043FFFFh
	BA66	64 kwords	0420000h-042FFFFh
	BA65	64 kwords	0410000h-041FFFFh
	BA64	64 kwords	0400000h-040FFFFh
Bank 12	BA63	64 kwords	03F0000h-03FFFFFh
	BA62	64 kwords	03E0000h-03EFFFFh
	BA61	64 kwords	03D0000h-03DFFFFh
	BA60	64 kwords	03C0000h-03CFFFFh
	BA59	64 kwords	03B0000h-03BFFFFh
	BA58	64 kwords	03A0000h-03AFFFFh
	BA57	64 kwords	0390000h-039FFFFh
	BA56	64 kwords	0380000h-038FFFFh
	BA55	64 kwords	0370000h-037FFFFh
	BA54	64 kwords	0360000h-036FFFFh
	BA53	64 kwords	0350000h-035FFFFh
	BA52	64 kwords	0340000h-034FFFFh
	BA51	64 kwords	0330000h-033FFFFh
	BA50	64 kwords	0320000h-032FFFFh
	BA49	64 kwords	0310000h-031FFFFh
	BA48	64 kwords	0300000h-030FFFFh
Bank 13	BA47	64 kwords	02F0000h-02FFFFFh
	BA46	64 kwords	02E0000h-02EFFFFh
	BA45	64 kwords	02D0000h-02DFFFFh
	BA44	64 kwords	02C0000h-02CFFFFh
	BA43	64 kwords	02B0000h-02BFFFFh
	BA42	64 kwords	02A0000h-02AFFFFh
	BA41	64 kwords	0290000h-029FFFFh
	BA40	64 kwords	0280000h-028FFFFh
	BA39	64 kwords	0270000h-027FFFFh
	BA38	64 kwords	0260000h-026FFFFh
	BA37	64 kwords	0250000h-025FFFFh
	BA36	64 kwords	0240000h-024FFFFh
	BA35	64 kwords	0230000h-023FFFFh

Bank	Block	Block Size	(x16) Address Range
Bank 13	BA34	64 kwords	0220000h-022FFFFh
	BA33	64 kwords	0210000h-021FFFFh
	BA32	64 kwords	0200000h-020FFFFh
Bank 14	BA31	64 kwords	01F0000h-01FFFFFh
	BA30	64 kwords	01E0000h-01EFFFFh
	BA29	64 kwords	01D0000h-01DFFFFh
	BA28	64 kwords	01C0000h-01CFFFFh
	BA27	64 kwords	01B0000h-01BFFFFh
	BA26	64 kwords	01A0000h-01AFFFFh
	BA25	64 kwords	0190000h-019FFFFh
	BA24	64 kwords	0180000h-018FFFFh
	BA23	64 kwords	0170000h-017FFFFh
	BA22	64 kwords	0160000h-016FFFFh
	BA21	64 kwords	0150000h-015FFFFh
	BA20	64 kwords	0140000h-014FFFFh
	BA19	64 kwords	0130000h-013FFFFh
	BA18	64 kwords	0120000h-012FFFFh
	BA17	64 kwords	0110000h-011FFFFh
	BA16	64 kwords	0100000h-010FFFFh
Bank 15	BA15	64 kwords	00F0000h-00FFFFFh
	BA14	64 kwords	00E0000h-00EFFFFh
	BA13	64 kwords	00D0000h-00DFFFFh
	BA12	64 kwords	00C0000h-00CFFFFh
	BA11	64 kwords	00B0000h-00BFFFFh
	BA10	64 kwords	00A0000h-00AFFFFh
	BA9	64 kwords	0090000h-009FFFFh
	BA8	64 kwords	0080000h-008FFFFh
	BA7	64 kwords	0070000h-007FFFFh
	BA6	64 kwords	0060000h-006FFFFh
	BA5	64 kwords	0050000h-005FFFFh
	BA4	64 kwords	0040000h-004FFFFh
	BA3	64 kwords	0030000h-003FFFFh
	BA2	64 kwords	0020000h-002FFFFh
	BA1	64 kwords	0010000h-001FFFFh
	BA0	64 kwords	0000000h-000FFFFh

[Table 21] Uniform OTP Block Addresses

	Block Address A23 ~ A8	Block Size	(x16) Address Range*
OTP	FFFFh	512 words	FFFE00h-FFFFFFh

After entering OTP Block, any issued addresses should be in the range of OTP block address.