K9XXG08UXD

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Document Title

4G x 8 Bit/ 8G x 8 Bit/ 16G x 8 Bit NAND Flash Memory

Revision History

Revision No	History	Draft Date	Remark
0.0	1. Initial issue	Mar. 14th 2008	Advance
0.1	1. K9PDG08U5D-L's package thickness is changed. 2. $\overline{CE}$ and R/$\overline{B}$ pin location of K9PDG08U5D-L is changed.	Oct. 16th 2008	Preliminary
0.2	1. Interleaving operation is modified. 2. Interleaving page read operation is added.		

4G x 8 Bit/ 8G x 8 Bit/ 16G x 8 Bit NAND Flash Memory

PRODUCT LIST

Part Number	Vcc Range	Organization	PKG Type
K9LBG08U0D-P	2.7V ~ 3.6V	x8	TSOP1
K9HCG08U1D-P			
K9MDG08U5D-P			TSOP1-DSP
K9HCG08U1D-I			52TLGA
K9PDG08U5D-L			52TLGA(14x18)

FEATURES

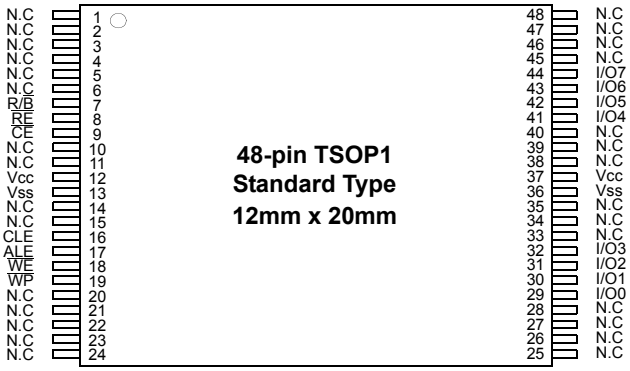
- Voltage Supply
  - 3.3V Device : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (2G + 109M) x 8bit
  - Data Register : (4K + 218) x 8bit
- Automatic Program and Erase
  - Page Program : (4K + 218)Byte
  - Block Erase : (512K + 27.25K)Byte
- Page Read Operation
  - Page Size : (4K + 218)Byte
  - Random Read : 60μs(Max.)
  - Serial Access : 30ns(Min.)
  *K9XDG08U5D: 50ns(Min.)
- Memory Cell : 2bit / Memory Cell
- Fast Write Cycle Time
  - Program time : 800μs(Typ.)
  - Block Erase Time : 1.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance : TBD Cycles(with TBD ECC)
  - Data Retention : TBD Years
- Command Register Operation
- Unique ID for Copyright Protection
- Package :
  - K9LBG08U0D-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9HCG08U1D-PCB0/PIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9MDG08U5D-PCB0/PIB0: Two K9HCG08U1D packages stacked
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch) : Pb-FREE PACKAGE
  - K9HCG08U1D-ICB0/IIB0
    52 - Pin TLGA (12 x 17 / 1.00 mm pitch)
  - K9PDG08U5D-LCB0/LIB0 : Pb/Halogen-FREE PACKAGE
    52 - Pin TLGA (14 x 18 / 1.00 mm pitch)

GENERAL DESCRIPTION

Offered in 4Gx8bit, the K9LBG08U0D is a 32G-bit NAND Flash Memory with spare 1,744M-bit. The device is offered in 3.3V Vcc. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. A program operation can be performed in typical 800μs on the 4,314-byte page and an erase operation can be performed in typical 1.5ms on a (512K+27.25K)byte block. Data in the data register can be read out at 30ns(K9XDG08U5D: 50ns) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9LBG08U0D's extended reliability of TBD cycles by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9LBG08U0D is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

PIN CONFIGURATION (TSOP1)

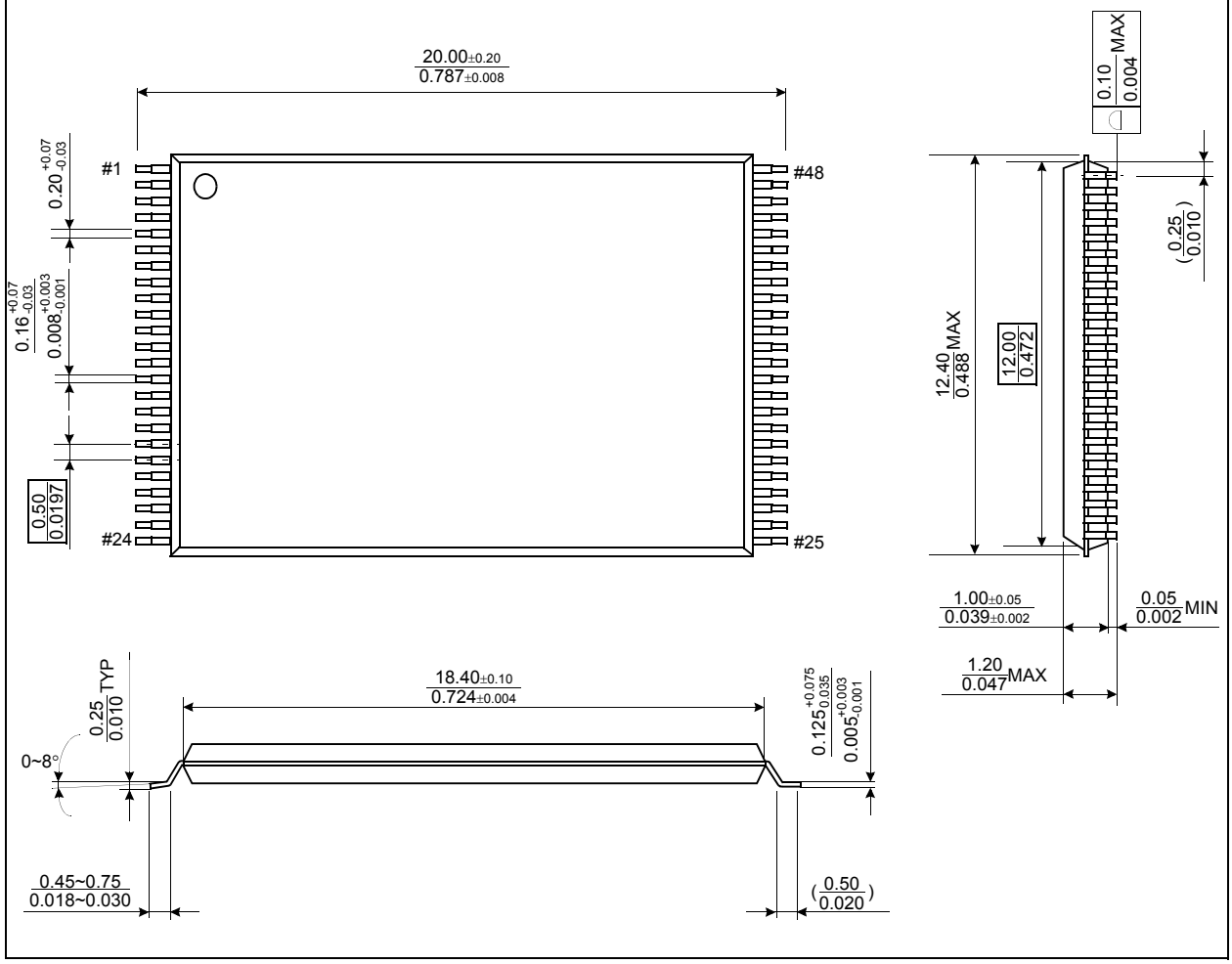
K9LBG08U0D-PCB0/PIB0



PACKAGE DIMENSIONS

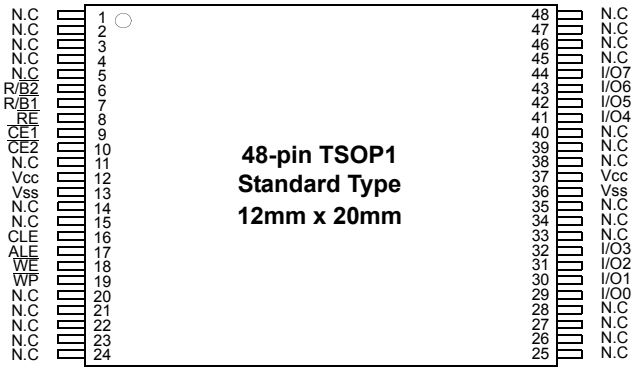
48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



PIN CONFIGURATION (TSOP1)

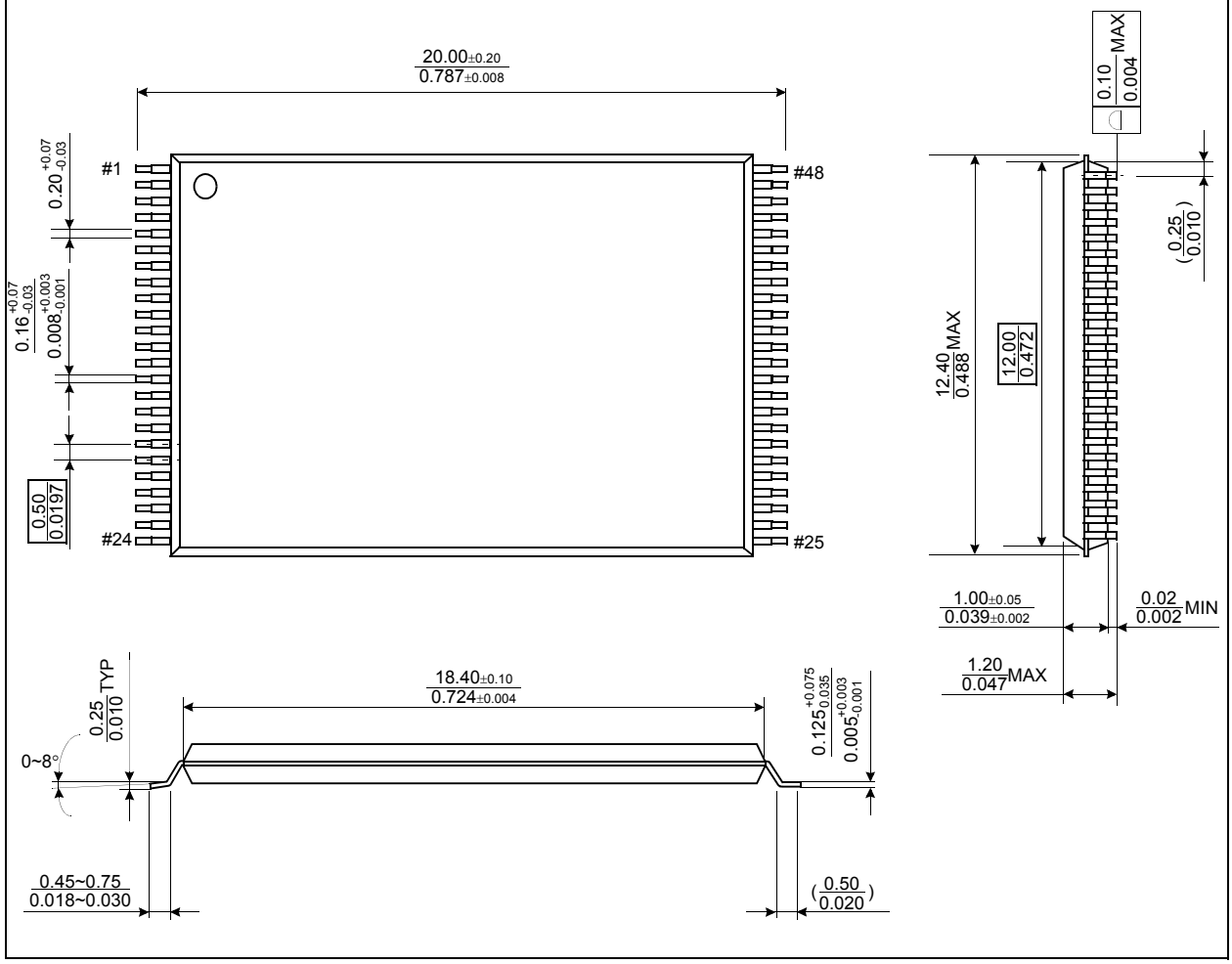
K9HCG08U1D-PCB0/PIB0



PACKAGE DIMENSIONS

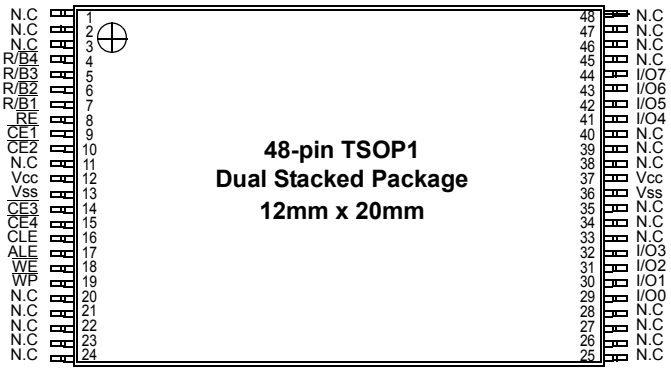
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



PIN CONFIGURATION (TSOP1-DSP)

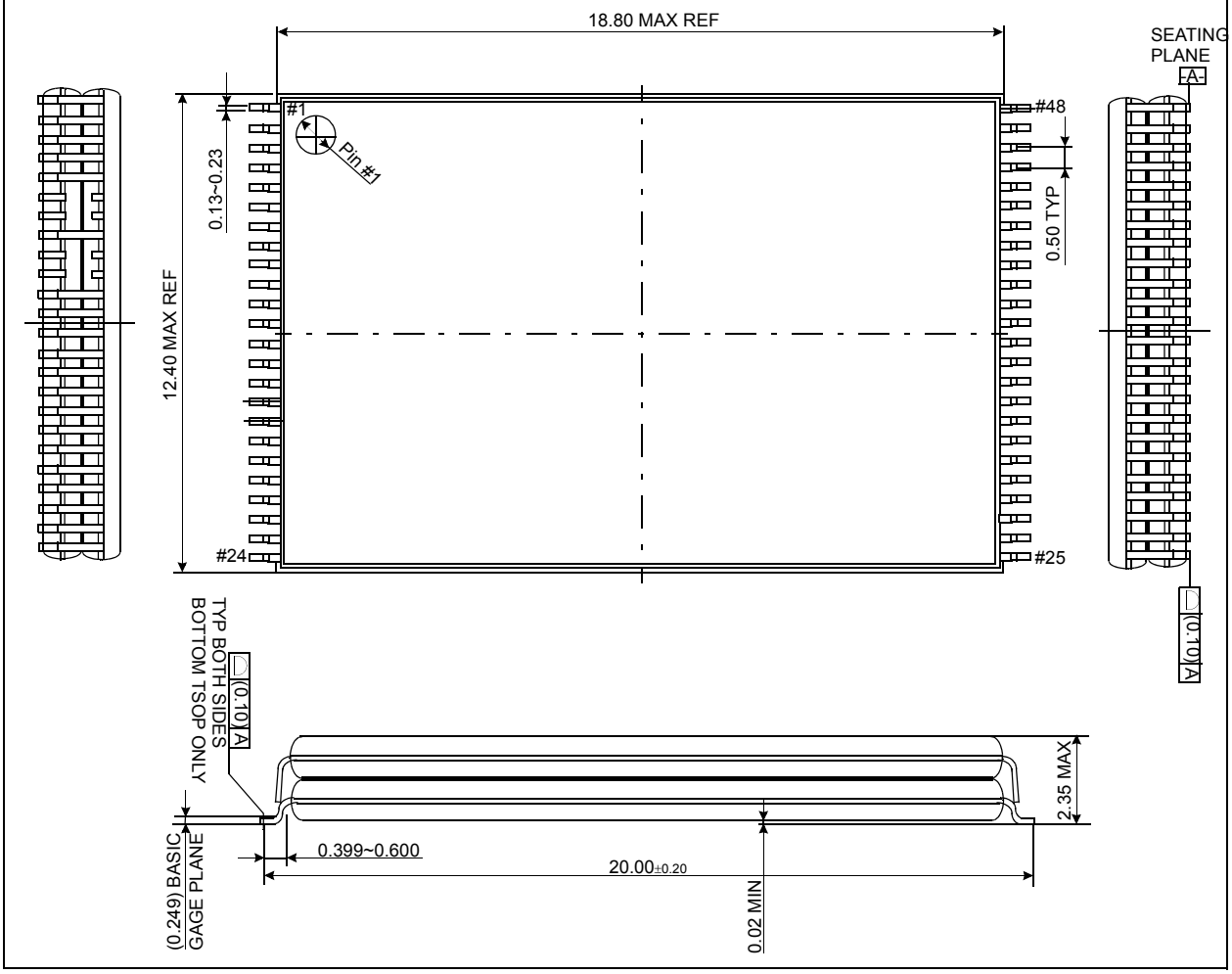
K9MDG08U5D-PCB0/PIB0



PACKAGE DIMENSIONS

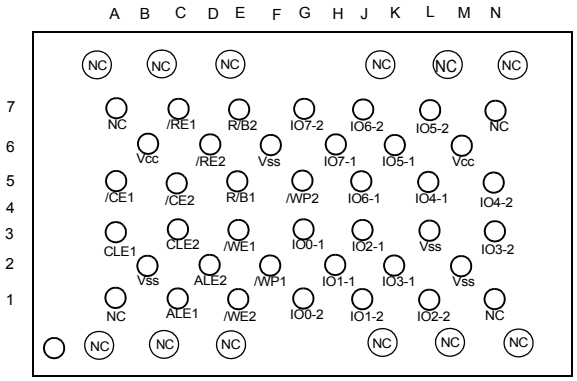
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

48 - TSOP1 - 1220AF Unit :mm/Inch



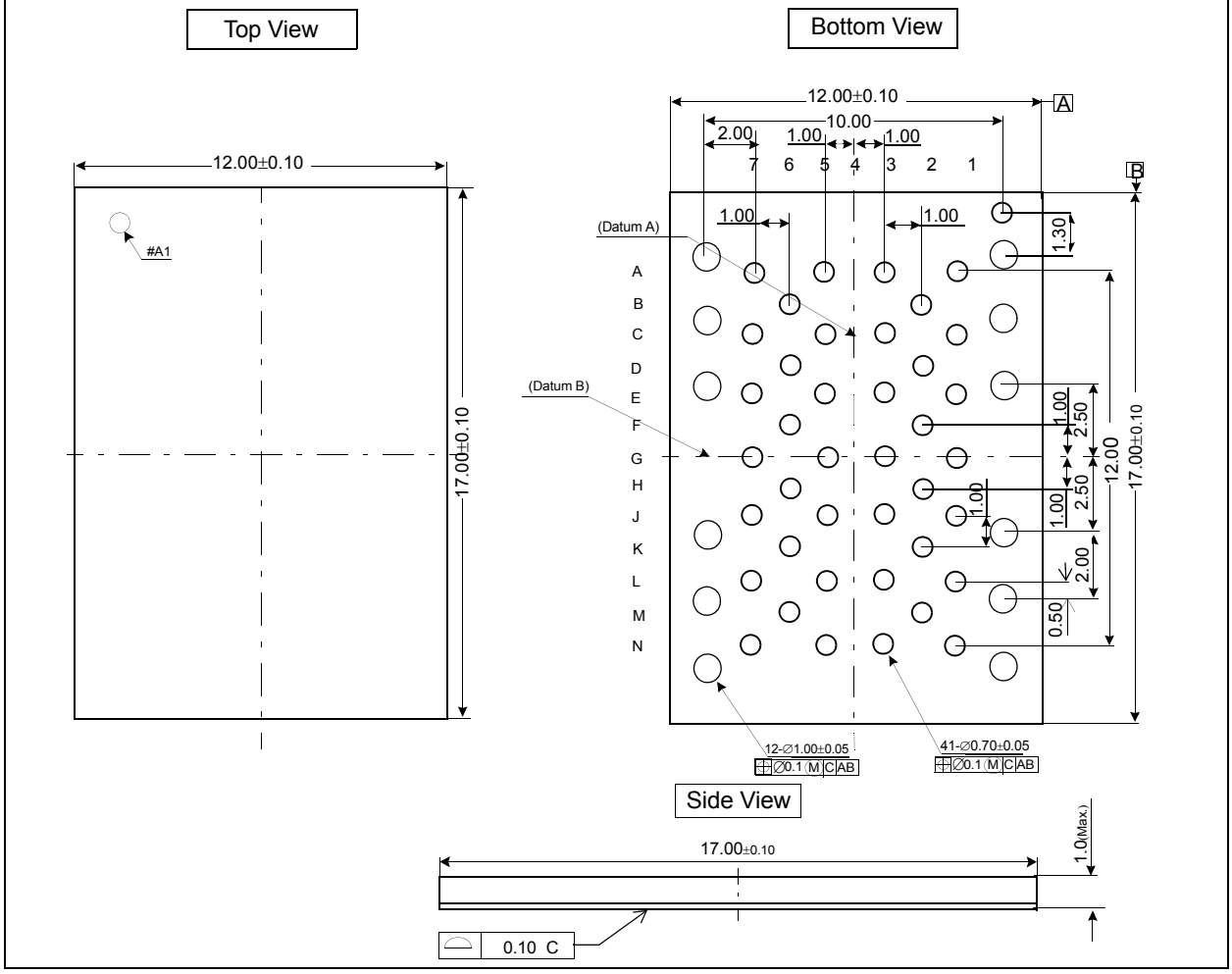
PIN CONFIGURATION (TLGA)

K9HCG08U1D - ICB0 / IIB0

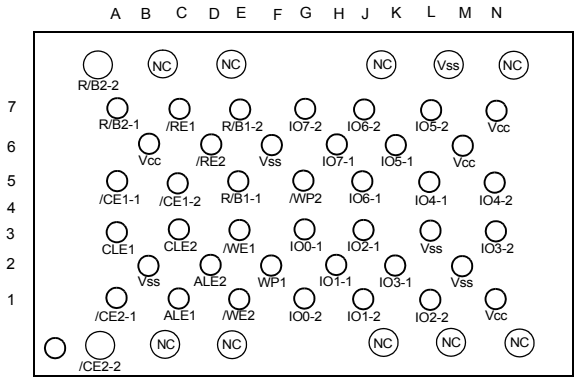


PACKAGE DIMENSIONS

52-TLGA (measured in millimeters)

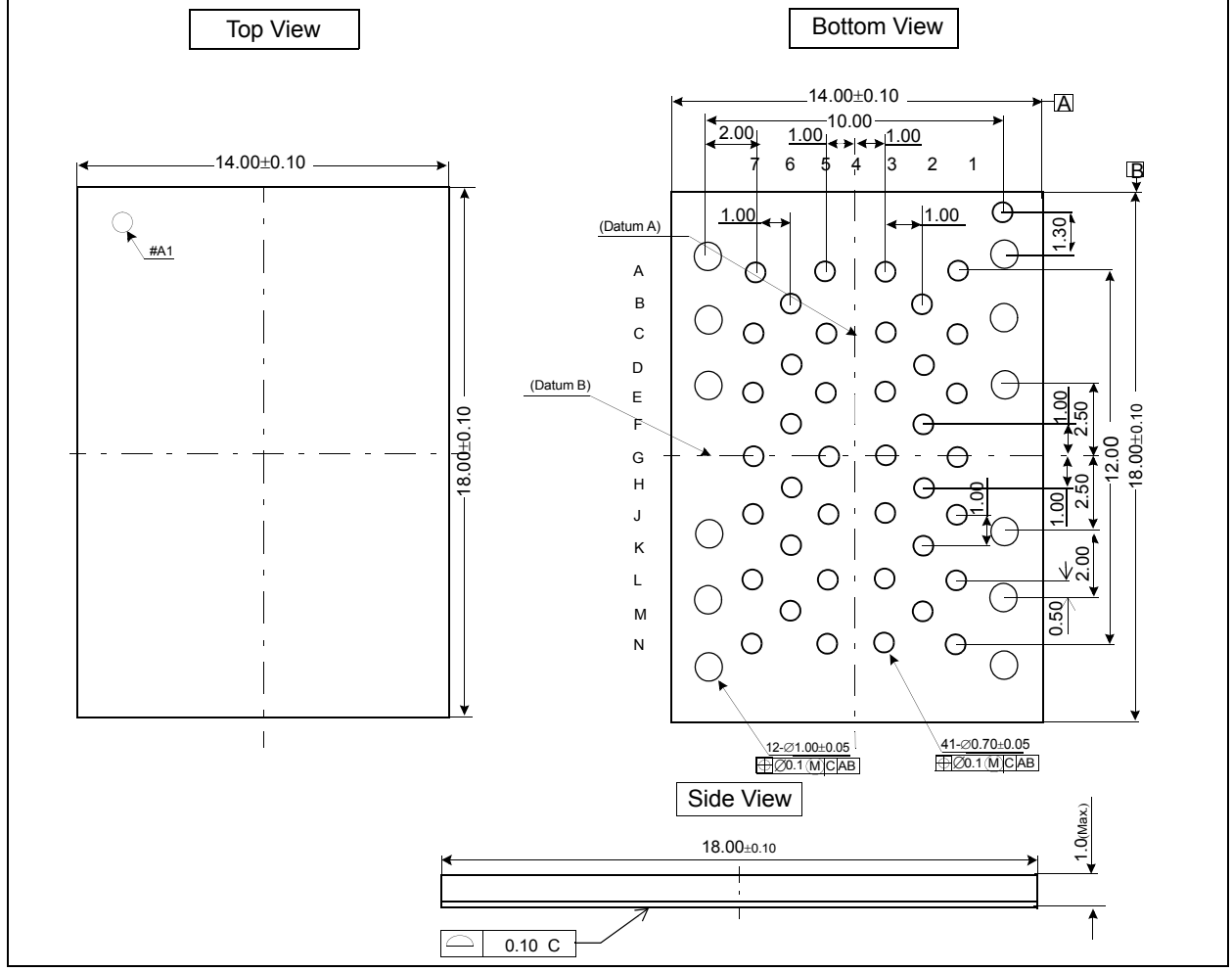


K9PDG08U5D-LCB0/LIB0



PACKAGE DIMENSIONS

52-TLGA (measured in millimeters)



PIN DESCRIPTION

Pin Name	Pin Function
I/O_0 ~ I/O_7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high.
$\overline{CE}$ / $\overline{CE1}$	**CHIP ENABLE** The $\overline{CE}$ / $\overline{CE}$ 1 input is the device selection control. When the device is in the Busy state, $\overline{CE}$ / $\overline{CE1}$ high is ignored, and the device does not return to standby mode in program or erase operation. Regarding $\overline{CE}$ / $\overline{CE}$1 control during read operation , refer to 'Page Read' section of Device operation
$\overline{CE2}$	**CHIP ENABLE** The $\overline{CE}$2 input enables the second K9LBG08U0D
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WE}$	**WRITE ENABLE** The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.
R/$\overline{B}$ / R/$\overline{B}$1	**READY/BUSY OUTPUT** The R/$\overline{B}$ / R/$\overline{B}$1 output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
R/$\overline{B}$2	**READY/BUSY OUTPUT** The R/$\overline{B}$2 output indicates the status of the second K9LBG08U0D.
Vcc	**POWER** Vcc is the power supply for device.
Vss	**GROUND**
N.C	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all Vcc and Vss pins of each device to common power supply outputs.
Do not leave Vcc or Vss disconnected.

There are two $\overline{CE}$ pins ($\overline{CE}$1 & $\overline{CE}$2) in the K9HCG08U1D, and four $\overline{CE}$ pins ($\overline{CE}$1 & $\overline{CE}$2 & $\overline{CE}$3 & $\overline{CE}$4) in the K9XDG08U5D.
There are two R/$\overline{B}$ pins (R/$\overline{B}$1 & R/$\overline{B}$2) in the K9HCG08U1D, and four R/$\overline{B}$ pins (R/$\overline{B}$1 & R/$\overline{B}$2 & R/$\overline{B}$3 & R/$\overline{B}$4) in the K9XDG08U5D.

Figure 1. K9LBG08U0D Functional Block Diagram

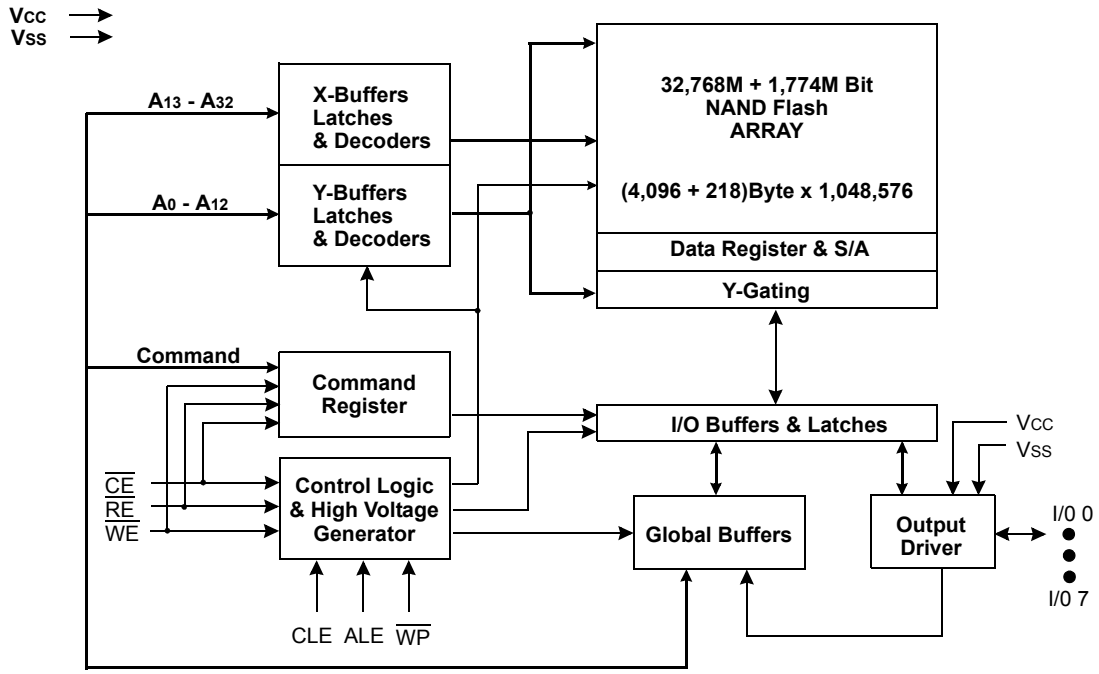
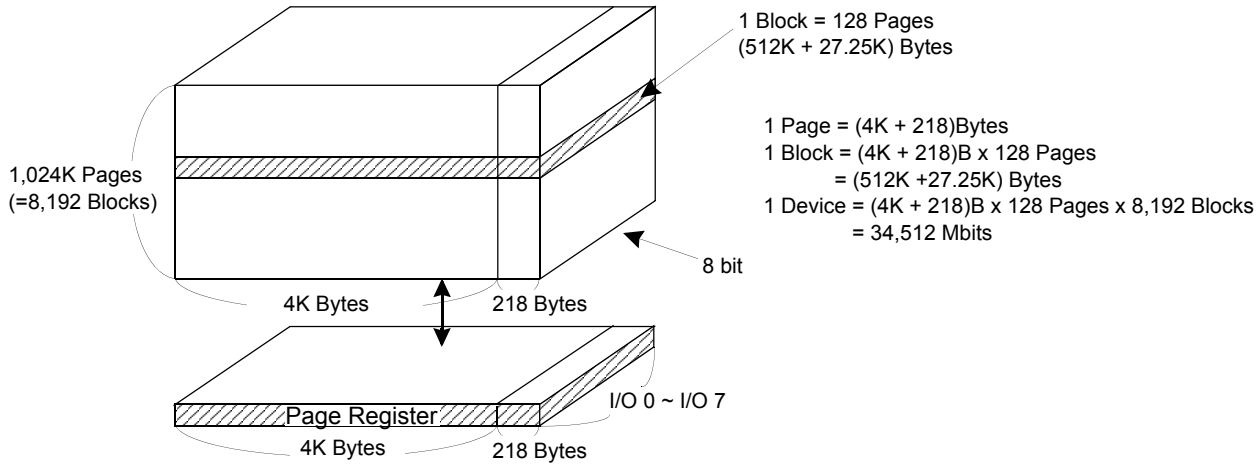


Figure 2. K9LBG08U0D Array Organization



	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	A12	*L	*L	*L	
3rd Cycle	A13	A14	A15	A16	A17	A18	A19	A20	Row Address; Page Address : A13 ~ A19, Plane Address : A20, Block Address : A21 ~ the last Address
4th Cycle	A21	A22	A23	A24	A25	A26	A27	A28	
5th Cycle	A29	A30	A31	A32	*L	*L	*L	*L	

NOTE : Column Address : Starting Address of the Register.

* L must be set to 'Low'.

* The device ignores any additional input of address cycles than required.

* Row Address consists of Page address (A13 ~ A19) & Plane address(A20) & Block address(A21 ~ the last Address)

Product Introduction

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Those are latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution. Page Read and Page Program need the same five address cycles following the required command input. In Block Erase operation, however, only the three row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 1 defines the specific commands of the K9LBG08U0D.

Table 1. Command Sets

Function	1st Set	2nd Set	
Read	00h	30h	
Read for Copy Back	00h	35h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	
Page Program	80h	10h	
Cache Program	80h	15h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input(1)	85h	-	
Random Data Output(1)	05h	E0h	
Two-Plane Read (3)	60h----60h	30h	
Two-Plane Read for Copy-Back(3)	60h----60h	35h	
Two-Plane Random Data Output (1) (3)	00h----05h	E0h	
Two-Plane Cache Read(3)	60h----60h	33h	
Two-Plane Page Program(2)	80h----11h	81h----10h	
Two-Plane Copy-Back Program(2)	85h----11h	81h----10h	
Two-Plane Cache Program(2)	80h----11h	81h----15h	
Two-Plane Block Erase	60h----60h	D0h	
Read ID	90h	-	
Read Status	70h	-	O
Chip1 Status	F1h		O
Chip2 Status	F2h		O
Reset	FFh	-	O

NOTE : 1. Random Data Input/Output can be executed in a page.

2. Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h/F2h and FFh.

3. Two-Plane Random Data out must be used after Two-Plane Read or Two-Plane Cache Read operation

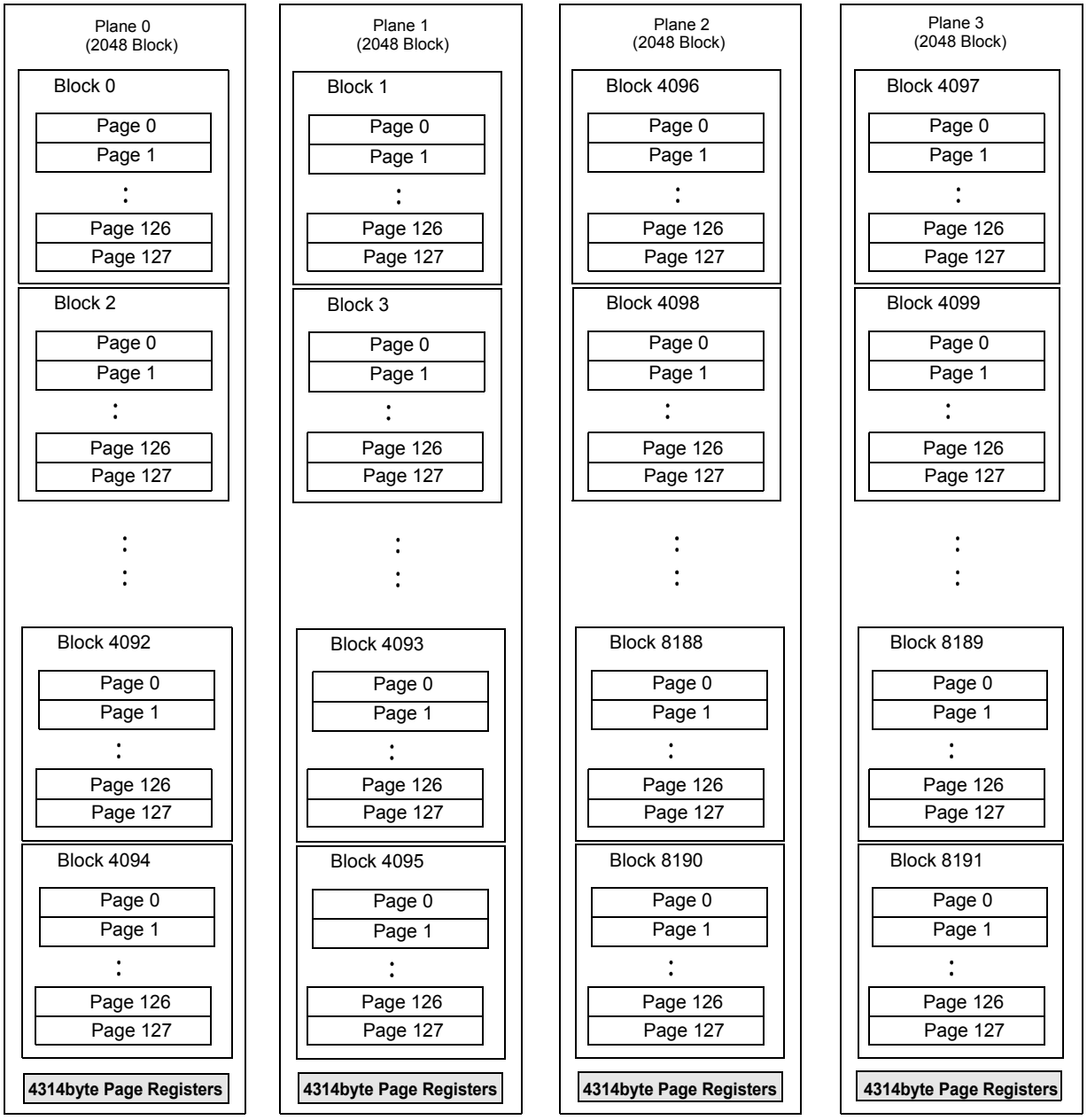
4. Interleave-operation between two chips is allowed.

Caution : Any undefined command inputs are prohibited except for above command set of Table 1.

Memory Map

K9LBG08U0D is arranged in four 8Gb memory planes. Each plane contains 2,048 blocks and 4314 byte page registers. This allows it to perform simultaneous page program and block erase by selecting one page or block from each plane. The block address map is configured so that two-plane program/erase operations can be executed by dividing the memory array into plane 0~1 or plane 2~3 separately.

For example, two-plane program/erase operation into plane 0 and plane 2 is prohibited. That is to say, two-plane program/erase operation into plane 0 and plane 1 or into plane 2 and plane 3 is allowed.



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}		V_{CC}	-0.6 to + 4.6	V
		V_{IN}	-0.6 to + 4.6	
		$V_{I/O}$	-0.6 to Vcc+0.3 (<4.6V)	
Temperature Under Bias	K9XXG08UXD-XCB0	T_{BIAS}	-10 to +125	°C
	K9XXG08UXD-XIB0		-40 to +125	
Storage Temperature	K9XXG08UXD-XCB0	T_{STG}	-65 to +150	°C
	K9XXG08UXD-XIB0			
Short Circuit Current		Ios	5	mA

NOTE :
1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is V_{CC}+0.3V which, during transitions, may overshoot to V_{CC}+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, K9XXG08UXD-XCB0 :T_A=0 to 70°C, K9XXG08UXD-XIB0:T_A=-40 to 85°C)

Parameter	Symbol	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATING CHARACTERISTICS(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Current	Page Read with Serial Access	$I_{CC}1$	tRC=30ns (K9XDG08U5D: 50ns) $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	35	mA
	Program	$I_{CC}2$	-				
	Erase	$I_{CC}3$	-				
Stand-by Current(TTL)		$I_{SB}1$	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/V_{CC}	-	-	1	
Stand-by Current(CMOS)		$I_{SB}2$	$\overline{CE}$=V_{CC}-0.2, $\overline{WP}$=0V/V_{CC}	-	20	100	µA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc(max)	-	-	±20	
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±20	
Input High Voltage		V_{IH}(1)	-	0.8 xVcc	-	Vcc +0.3	V
Input Low Voltage, All inputs		V_{IL}(1)	-	-0.3	-	0.2 xVcc	
Output High Voltage Level		V_{OH}	I_{OH}=-400µA	2.4	-	-	
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	
Output Low Current(R/$\overline{B}$)		I_{OL}(R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

NOTE : 1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC} +0.4V for durations of 20 ns or less.
2. Typical value is measured at Vcc=3.3V, T_A=25°C. Not 100% tested.
3. The typical value of the K9HCG08U1D's $I_{SB}2$ is 40µA and the maximum value is 200µA.
4. The typical value of the K9XDG08U5D's $I_{SB}2$ is 80µA and the maximum value is 400µA.
5. The maximum value of K9HCG08U1D-P's I_{LI} and I_{LO} is ±40µA.
6. The maximum value of K9PDG08U5D-L's I_{LI} and I_{LO} is ±40µA and K9MDG08U5D-P's I_{LI} and I_{LO} is ±80µA.

VALID BLOCK

Parameter	Symbol	Min	Typ.	Max	Unit
K9LBG08U0D	N_{VB}	7,992	-	8,192	Blocks
K9HCG08U1D		15,984	-	16,384	
K9XDG08U5D		31,968	-	32,768	

NOTE :
1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment
3. The number of valid blocks is on the basis of single plane operations, and this may be decreased with two plane operations.

* : Each K9LBG08U0D chip in the K9HCG08U1D, K9XDG08U5D has maximum 200 invalid blocks.

AC TEST CONDITION

(K9XXG08UXD-XCB0 :T_A=0 to 70°C, K9XXG08UXD-XIB0:T_A=-40 to 85°C, K9XXG08UXD: Vcc=2.7V ~ 3.6V,unless otherwise noted)

Parameter	K9XXG08UXD
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and CL=50pF (K9LBG08U0D-P, K9HCG08U1D-I)
	1 TTL GATE and CL=30pF (K9HCG08U1D-P, K9XDG08U5D-P/L)

CAPACITANCE(T_A=25°C, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	K9LBG08U0D		K9HCG08U1D		K9MDG08U5D		Unit
			Min	Max	Min	Max	Min	Max	
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	13	-	23	-	43	pF
	$C_{I/O(W)}$*		-	10	-	20	-	40	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	13	-	23	-	43	pF
	$C_{IN(W)}$*		-	10	-	20	-	40	pF

NOTE : 1. Capacitance is periodically sampled and not 100% tested.
2. $C_{I/O(W)}$ and $C_{IN(W)}$ are tested at wafer level.
3. K9HCG08U1D-IXB0's capacitance(I/O, Input) is 13pF and K9PDG08U5D-LXB0's capacitance(I/O, Input) is 23pF.

MODE SELECTION

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode	
H	L	L	⎍	H	X	Read Mode	Command Input
L	H	L	⎍	H	X		Address Input(5clock)
H	L	L	⎍	H	H	Write Mode	Command Input
L	H	L	⎍	H	H		Address Input(5clock)
L	L	L	⎍	H	H	Data Input	
L	L	L	H	⎎	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE : 1. X can be V_{IL} or V_{IH}.
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	0.8	3	ms
Dummy Busy Time for Two-Plane Program	t_{DBSY}	-	0.5	1	μs
Dummy Busy Time for Cache Program	t_{CBSY}	-	-	3	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	1	cycle
Block Erase Time	t_{BERS}	-	1.5	10	ms

NOTE: 1.Typical program time is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

2. Typical Program time is defined as the time within which more than 50% of the whole pages are programed at 3.3V Vcc and 25°C temperature.

3. Within a same block, program time(tPROG) of page group A is faster than that of page group B. Typical tPROG is the average program time of the page group A and B(Table 5).

Page Group A: Page 0, 1, 2, 3, 6, 7, 10, 11, ... , 110, 111, 114, 115, 118, 119, 122, 123

Page Group B: Page 4, 5, 8, 9, 12, 13, 16, 17, ... , 116, 117, 120, 121, 124, 125, 126, 127

4. t_{CBSY} depends on the timing between internal programming time and data in time.

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min		Max		Unit
		K9LBG08U0D K9HCG08U1D	K9XDG08U5D	K9LBG08U0D K9HCG08U1D	K9XDG08U5D	
CLE Setup Time	t_{CLS}(1)	15	25	-	-	ns
CLE Hold Time	t_{CLH}	5	10	-	-	ns
$\overline{CE}$ Setup Time	t_{CS}(1)	20	35	-	-	ns
$\overline{CE}$ Hold Time	t_{CH}	5	10	-	-	ns
$\overline{WE}$ Pulse Width	t_{WP}	15	25	-	-	ns
ALE Setup Time	t_{ALS}(1)	15	25	-	-	ns
ALE Hold Time	t_{ALH}	5	10	-	-	ns
Data Setup Time	t_{DS}(1)	15	20	-	-	ns
Data Hold Time	t_{DH}	5	10	-	-	ns
Write Cycle Time	t_{WC}	30	45	-	-	ns
$\overline{WE}$ High Hold Time	t_{WH}	10	15	-	-	ns
Address to Data Loading Time	t_{ADL}(2)	100	100	-	-	ns

NOTES : 1. The transition of the corresponding control pins must occur only once while $\overline{WE}$ is held low

2. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle

AC Characteristics for Operation

Parameter	Symbol	Min		Max		Unit
		K9LBG08U0D K9HCG08U1D	K9XDG08U5D	K9LBG08U0D K9HCG08U1D	K9XDG08U5D	
Data Transfer from Cell to Register	t_R	-		60	60	µs
ALE to $\overline{RE}$ Delay	t_{AR}	10	10	-		ns
CLE to $\overline{RE}$ Delay	t_{CLR}	10	10	-		ns
Ready to $\overline{RE}$ Low	t_{RR}	20	20	-		ns
$\overline{RE}$ Pulse Width	t_{RP}	15	25	-		ns
$\overline{WE}$ High to Busy	t_{WB}	-	-	100	100	ns
$\overline{WP}$ High to $\overline{WE}$ Low	t_{WW}	100	100			ns
Read Cycle Time	t_{RC}	30	50	-		ns
$\overline{RE}$ Access Time	t_{REA}	-	-	20	30	ns
$\overline{CE}$ Access Time	t_{CEA}	-	-	25	45	ns
$\overline{RE}$ High to Output Hi-Z	t_{RHZ}	-	-	100	100	ns
$\overline{CE}$ High to Output Hi-Z	t_{CHZ}	-	-	30	30	ns
$\overline{CE}$ High to ALE or CLE Don't Care	t_{CSD}	0	0	-		ns
$\overline{RE}$ High to Output Hold	t_{RHOH}	15	15	-		ns
$\overline{RE}$ Low to Output Hold	t_{RLOH}	5	-	-		ns
$\overline{RE}$ High Hold Time	t_{REH}	10	15	-		ns
Output Hi-Z to $\overline{RE}$ Low	t_{IR}	0	0	-		ns
$\overline{RE}$ High to $\overline{WE}$ Low	t_{RHW}	100	100	-		ns
$\overline{WE}$ High to $\overline{RE}$ Low	t_{WHR}	60	60	-		ns
Device Resetting Time(Read/Program/Erase)	t_{RST}	-	-	5/10/500(1)	5/10/500(1)	µs
Cache Busy in Read Cache (following 31h and 3Fh)	t_{DCBSYR}	-	-	65	65	µs

NOTE: 1. If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5µs.

NAND Flash Technical Notes

Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that the last page of every initial invalid block has non-FFh data at the column address of 4,096.The initial invalid block information is also erasable in most cases, and it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the initial invalid block information is prohibited.

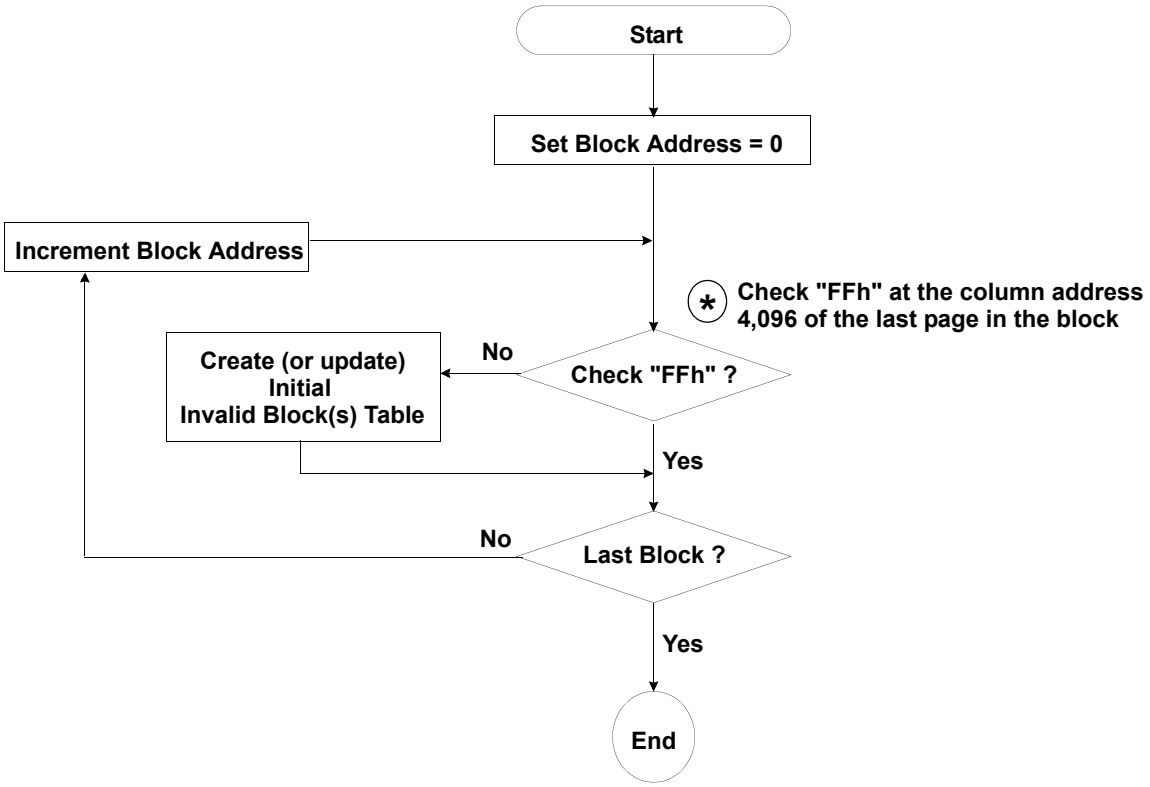


Figure 3. Flow chart to create initial invalid block table.

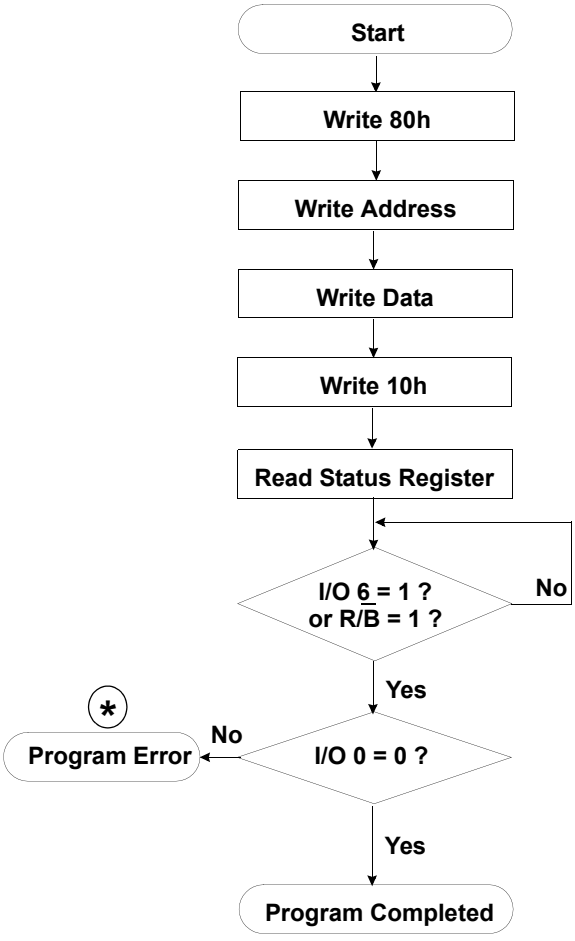
Error in write or read operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. Block replacement should be done upon erase or program error.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Up to Eight Bit Failure	Verify ECC -> ECC Correction

ECC : Error Correcting Code --> RS Code or BCH Code etc.
Example) 8bit correction / 512-byte

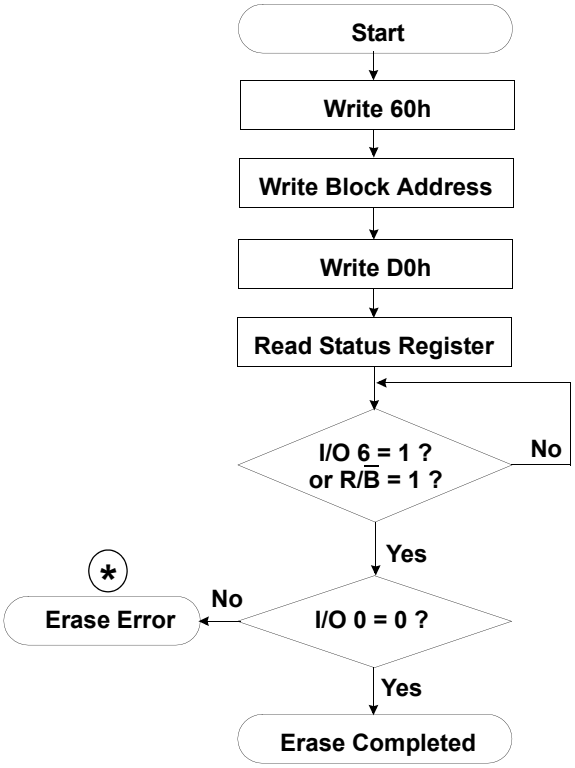
Program Flow Chart



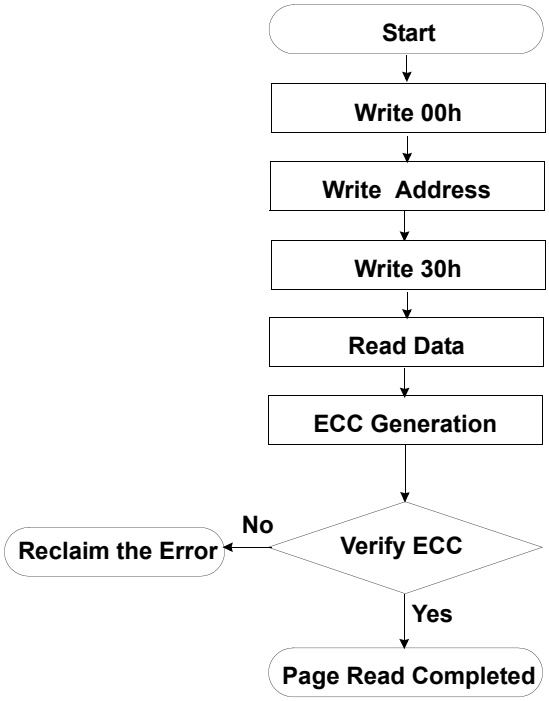
(*) : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

NAND Flash Technical Notes *(Continued)*

Erase Flow Chart

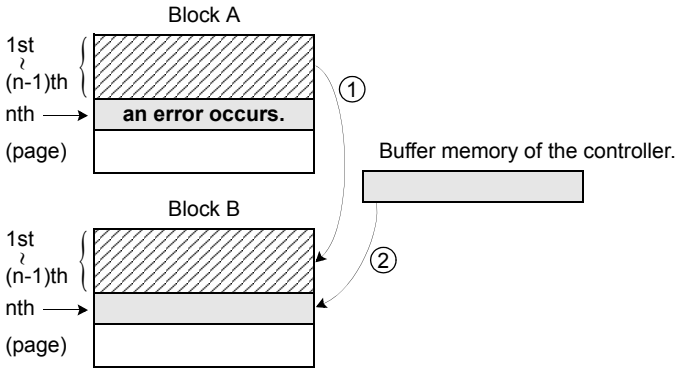


Read Flow Chart



(*) : If erase operation results in an error, map out the failing block and replace it with another block.

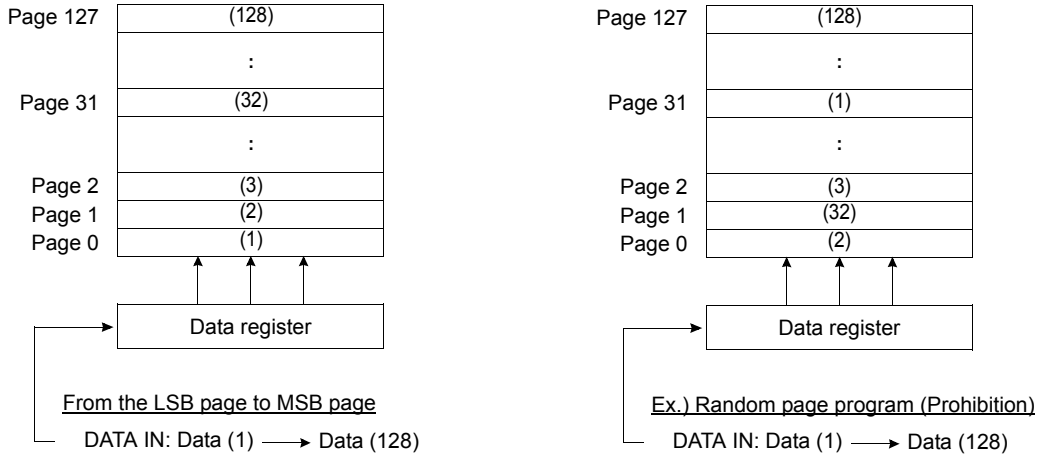
Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing for program operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.



Interleaving operation

DDP device is composed of two chips sharing CE pin. DDP device provides interleaving operation between two chips
This interleaving operation improves the system throughput almost twice compared to non-interleaving operation.

At first, the host issues a operation command to one of the LSB chips, say (chip #1). Due to DDP device goes into busy state. During this time, MSB chip (chip #2) is in ready state. So it can execute the operation command issued by the host.

After the execution of operation by LSB chip (chip #1), it can execute another operation regardless of MSB chip (chip #2). Before that the host needs to check the status of LSB chip (chip #1) by issuing F1h command. Only when the status of LSB chip (chip #1) becomes ready status, host can issue another operation command. If LSB chip (chip #1) is in busy state, the host has to wait for LSB chip (chip #1) to get into ready state.

Similarly, MSB chip (chip #2) can execute another operation after the completion of the previous operation. The host can monitor the status of MSB chip (chip #2) by issuing F2h command. When MSB chip (chip #2) shows ready state, host can issue another operation command to MSB chip (chip #2).

This interleaving algorithm improves the system throughput almost twice. The host can issue page operation command to each chip individually. This reduces the time lag for the completion of operation.

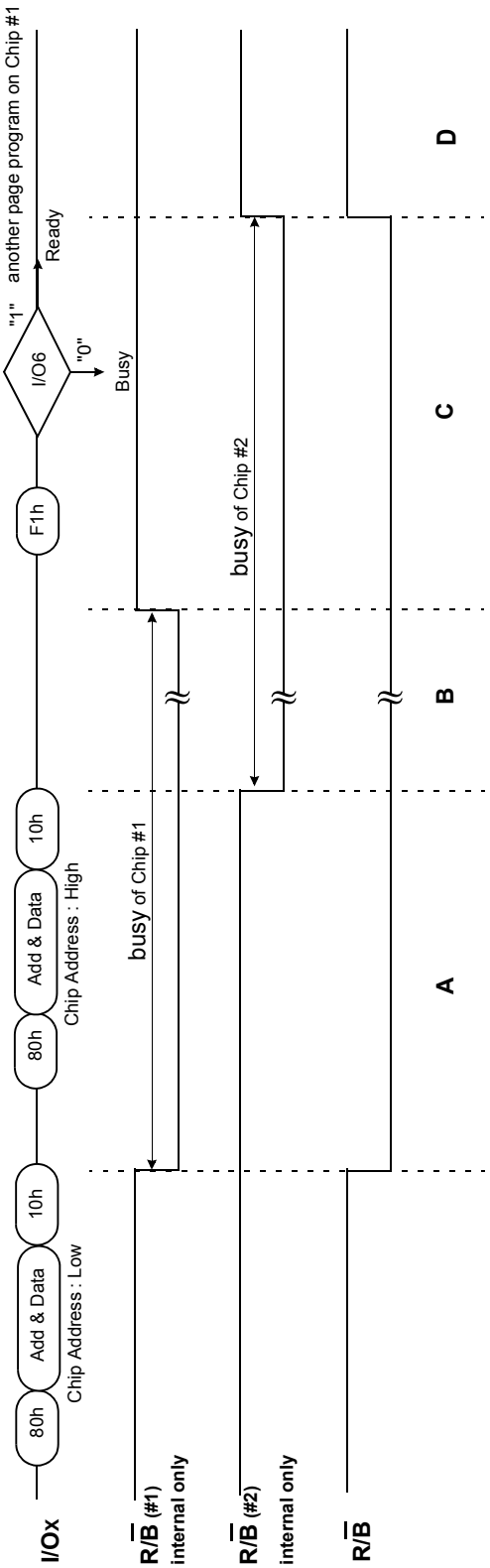
NOTES : During interleave operations, 70h command is prohibited.

Table . F1h/F2h Read Status Register Definition

I/O No.	Page Program	Block Erase	Read	Definition	
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Not use	Pass : "0"	Fail : "1"
I/O 3	Not Use	Not Use	Not Use	Don't -cared	
I/O 4	Not Use	Not Use	Not Use	Don't -cared	
I/O 5	Not Use	Not Use	Not Use	Don't -cared	
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0"	Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0"	Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

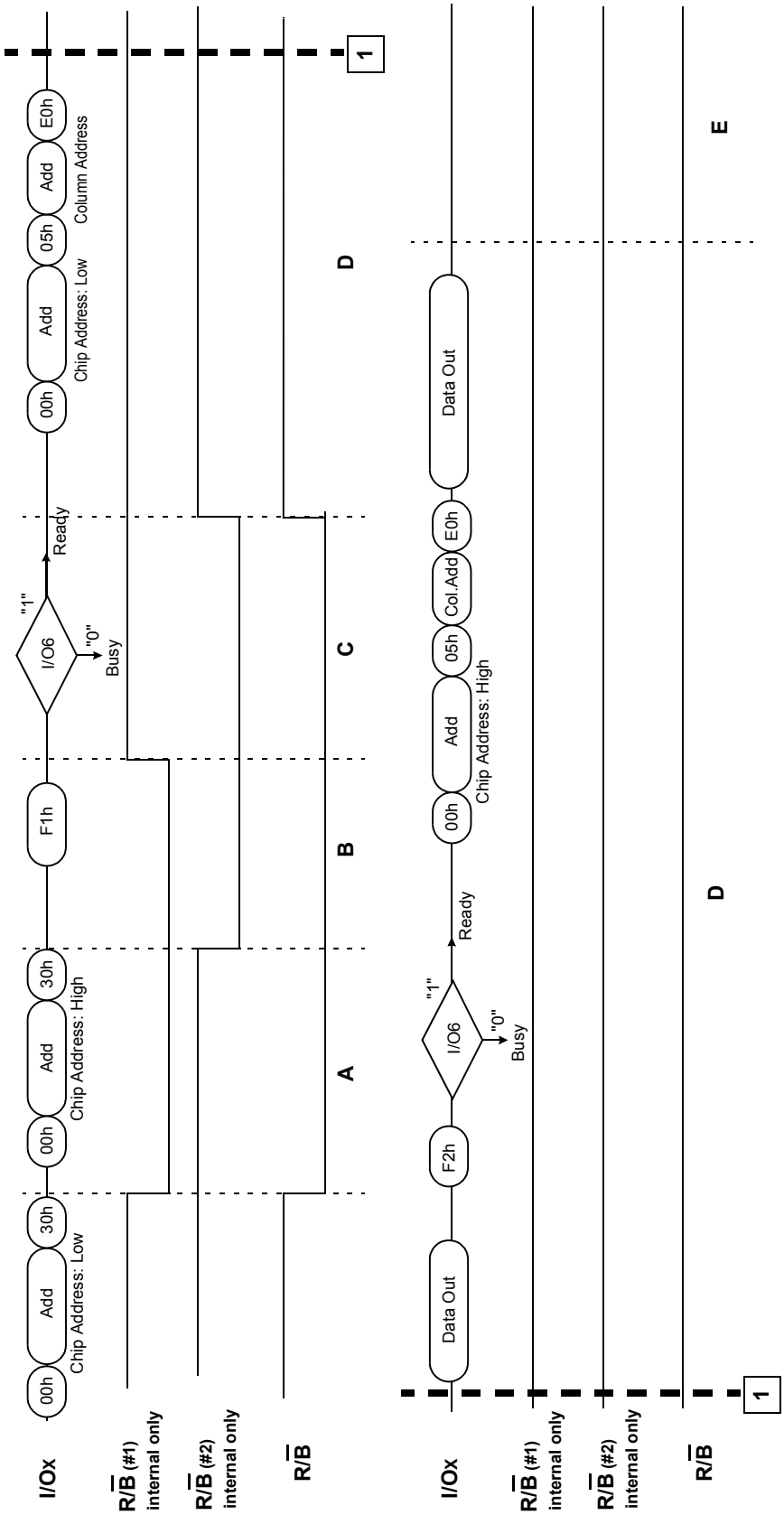
Interleaving Page Program



State A : Chip #1 is executing page program operation and chip #2 is in ready state. So the host can issue page program command to chip #2.
State B : Both chip #1 and chip #2 are executing page program operation.
State C : Page program on chip #1 is terminated, but page program on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another page program command to chip #1.
State D : Chip #1 and Chip #2 are ready.

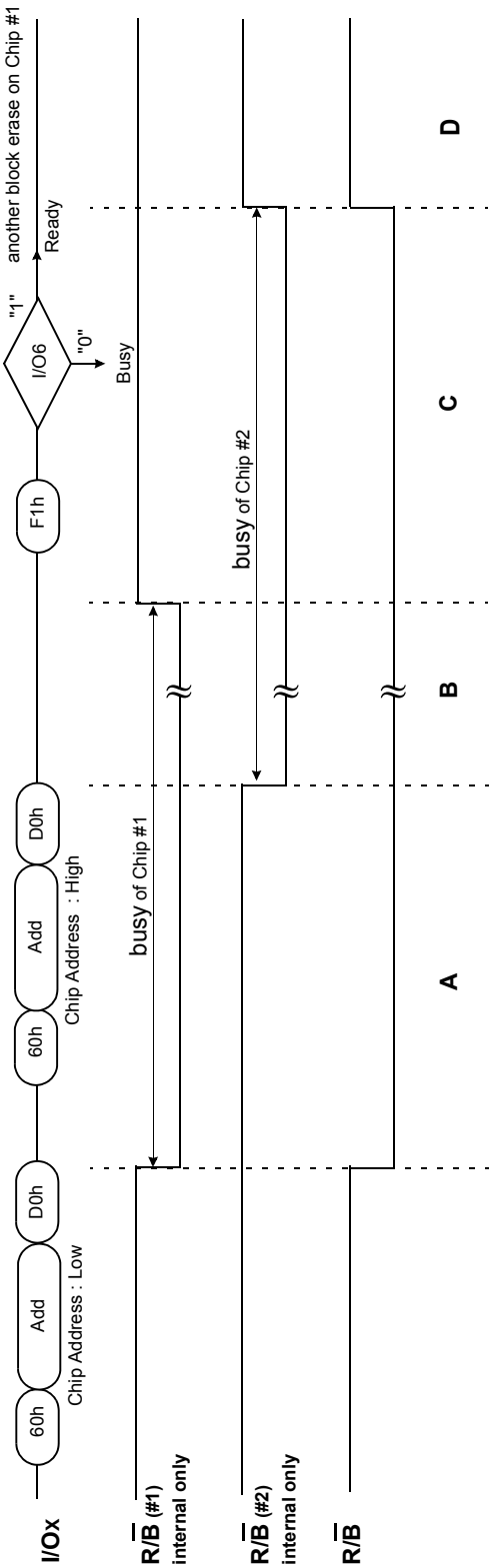
According to the above process, the system can operate page program on chip #1 and chip #2 alternately.

Interleaving Page Read Operation



State A : Chip #1 is executing page read operation, and chip #2 is in ready state. So the host can issue page read command to chip #2.
State B : Both chip #1 and chip #2 are executing page read operation.
State C : Page read on chip #1 is completed and chip #2 is still executing page read operation.
State D : Data out of chip #1 and chip #2 is executing.
State E : Chip #1 and Chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the data out command to chip #1.
F2h command is required to check the status of chip #2 to issue the data out command to chip #2.
According to the above process, the system can operate page read on chip #1 and chip #2 alternately.

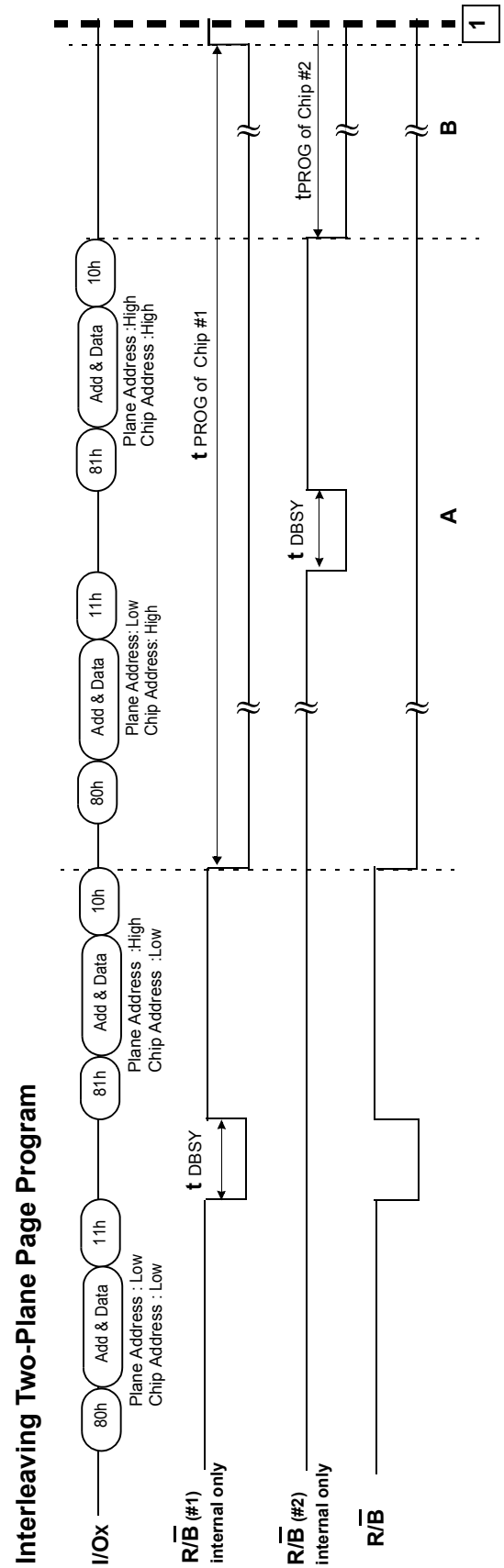
Interleaving Block Erase



State A : Chip #1 is executing block erase operation, and chip #2 is in ready state. So the host can issue block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing block erase operation.
State C : Block erase on chip #1 is terminated, but block erase on chip #2 is still operating. And the system should issue F1h command to detect the status of chip #1. If chip #1 is ready, status I/O6 is "1" and the system can issue another block erase command to chip #1.
State D : Chip #1 and Chip #2 are ready.

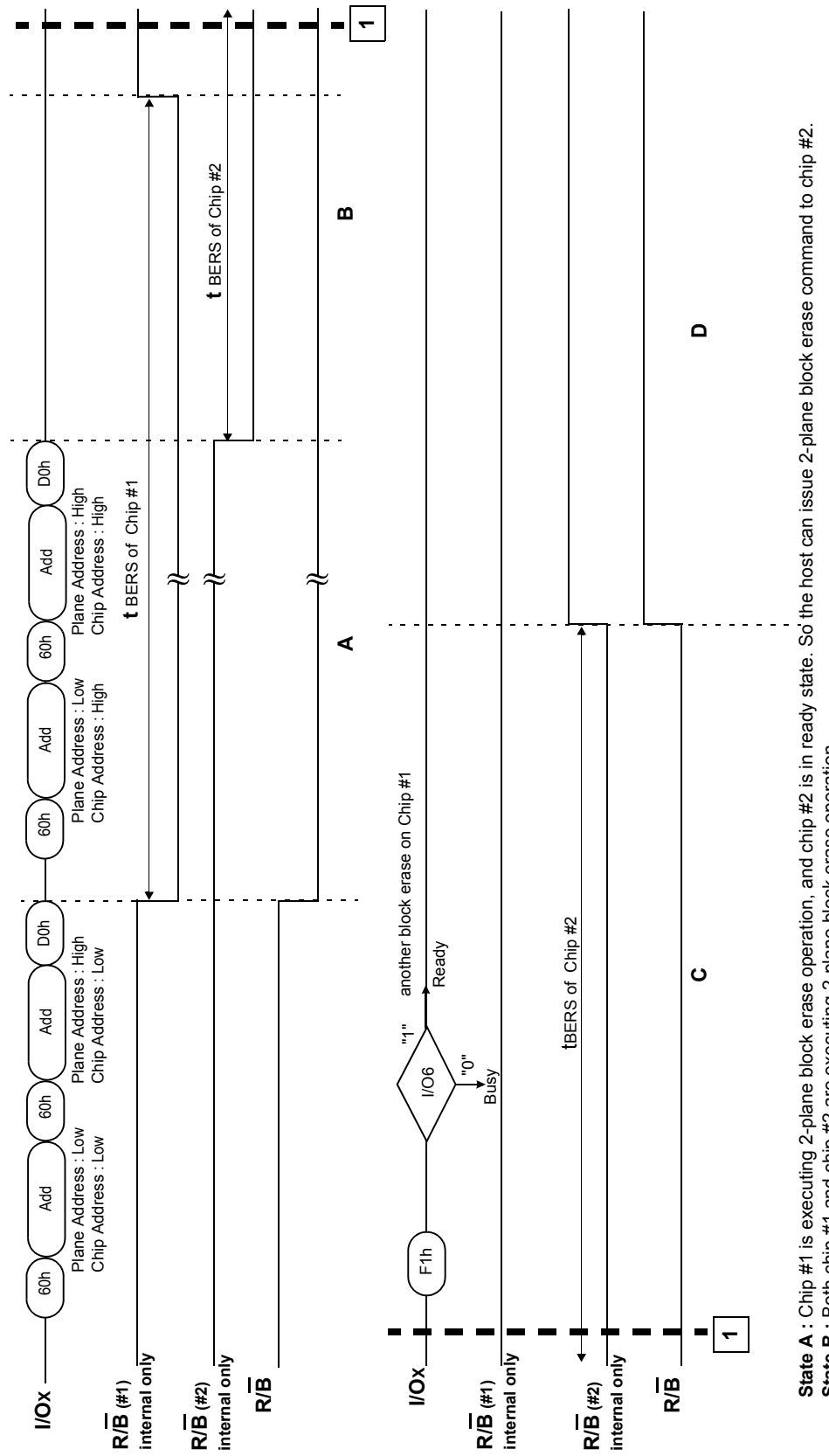
According to the above process, the system can operate block erase on chip #1 and chip #2 alternately.

Interleaving Two-Plane Page Program



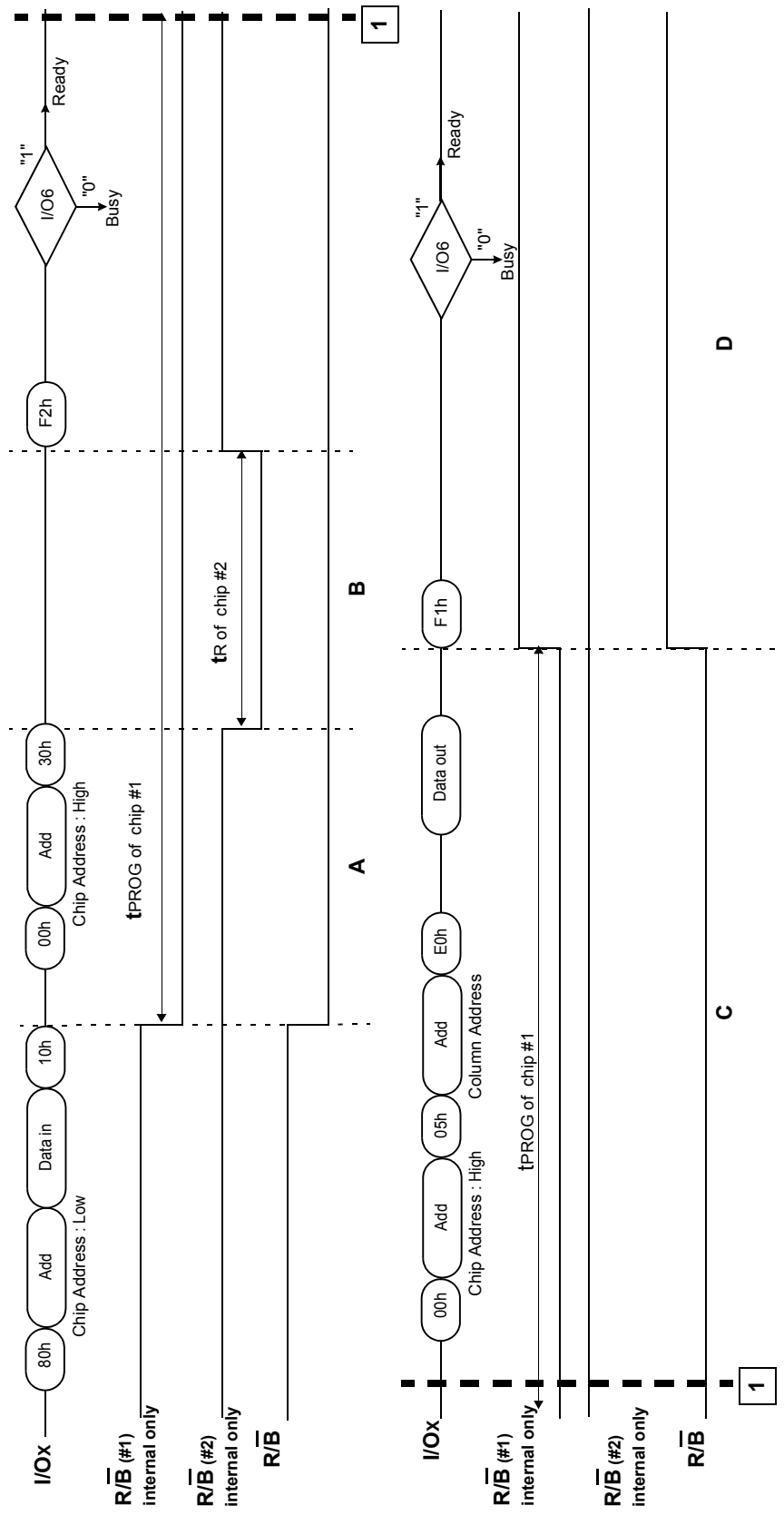
State A : Chip #1 is executing 2-plane page program operation, and chip #2 is in ready state. So the host can issue 2-plane page program command to chip #2.
State B : Both chip #1 and chip #2 are executing 2-plane page program operation.
State C : 2-plane page program on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing 2-plane page program operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next page program command to chip #1.
F2h command is required to check the status of chip #2 to issue the next page program command to chip #2.
According to the above process, the system can operate two-plane page program on chip #1 and chip #2 alternately.

Interleaving Two-Plane Block Erase



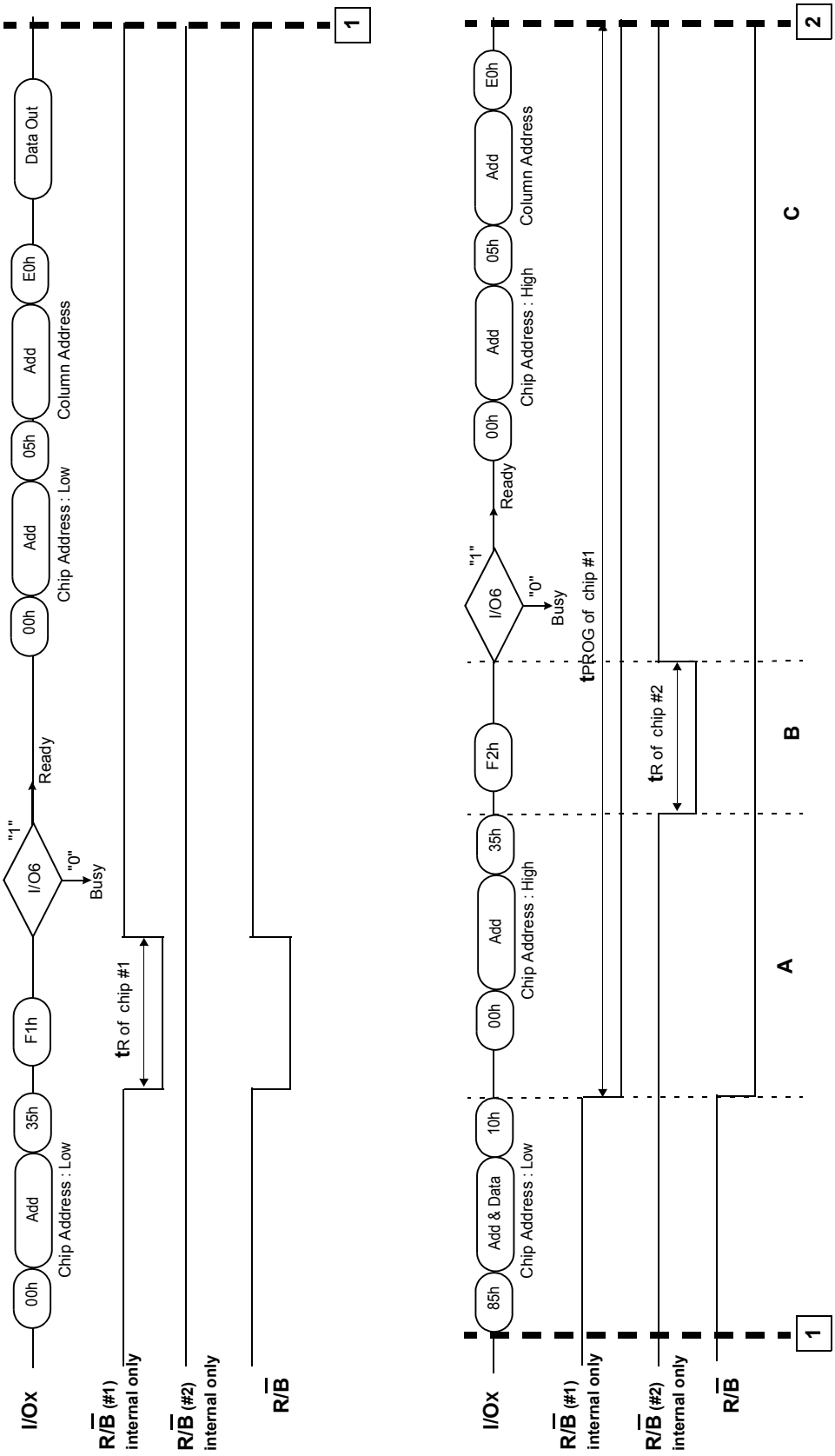
State A : Chip #1 is executing 2-plane block erase operation, and chip #2 is in ready state. So the host can issue 2-plane block erase command to chip #2.
State B : Both chip #1 and chip #2 are executing 2-plane block erase operation.
State C : 2-plane block erase on chip #1 is completed and chip #1 is ready for the next operation. Chip #2 is still executing 2-plane block erase operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next block erase command to chip #1.
F2h command is required to check the status of chip #2 to issue the next block erase command to chip #2.
According to the above process, the system can operate two-plane block erase on chip #1 and chip #2 alternately.

Interleaving Read to Page Program Operation

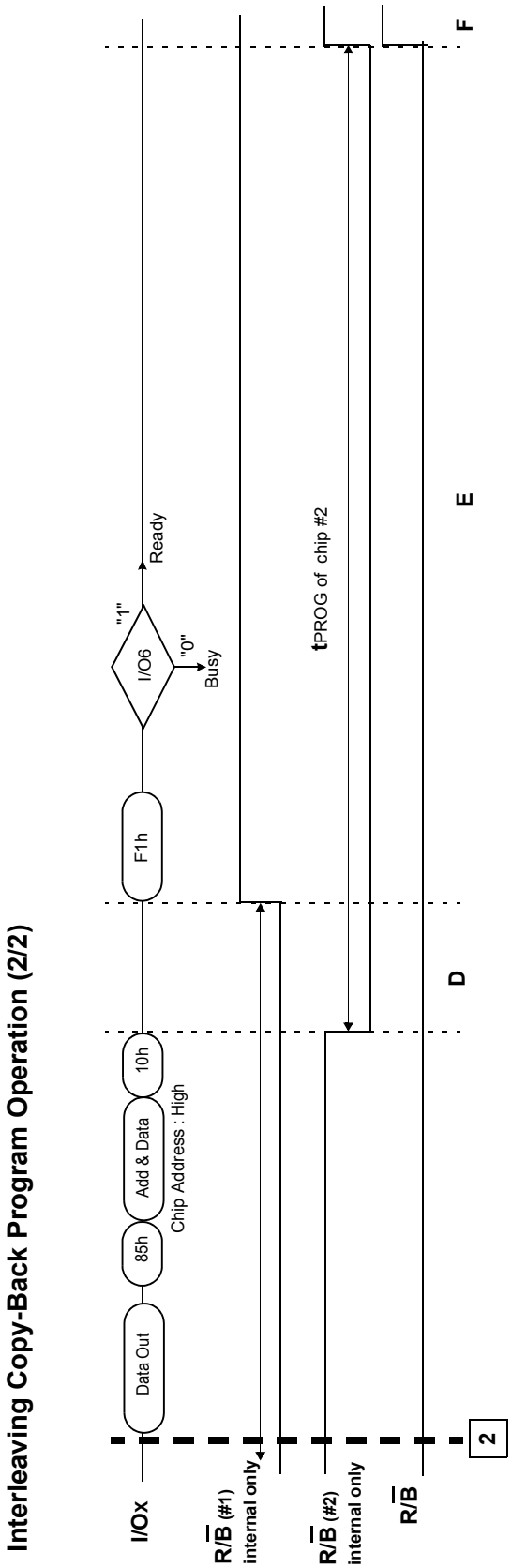


State A : Chip #1 is executing page program operation, and chip #2 is in ready state. So the host can issue read command to chip #2.
State B : Both chip #1 is executing page program operation and chip #2 is executing read operation.
State C : Read operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing page program operation.
State D : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave read to page porgram on chip #1 and chip #2 alternatively.

Interleaving Copy-Back Program Operation (1/2)

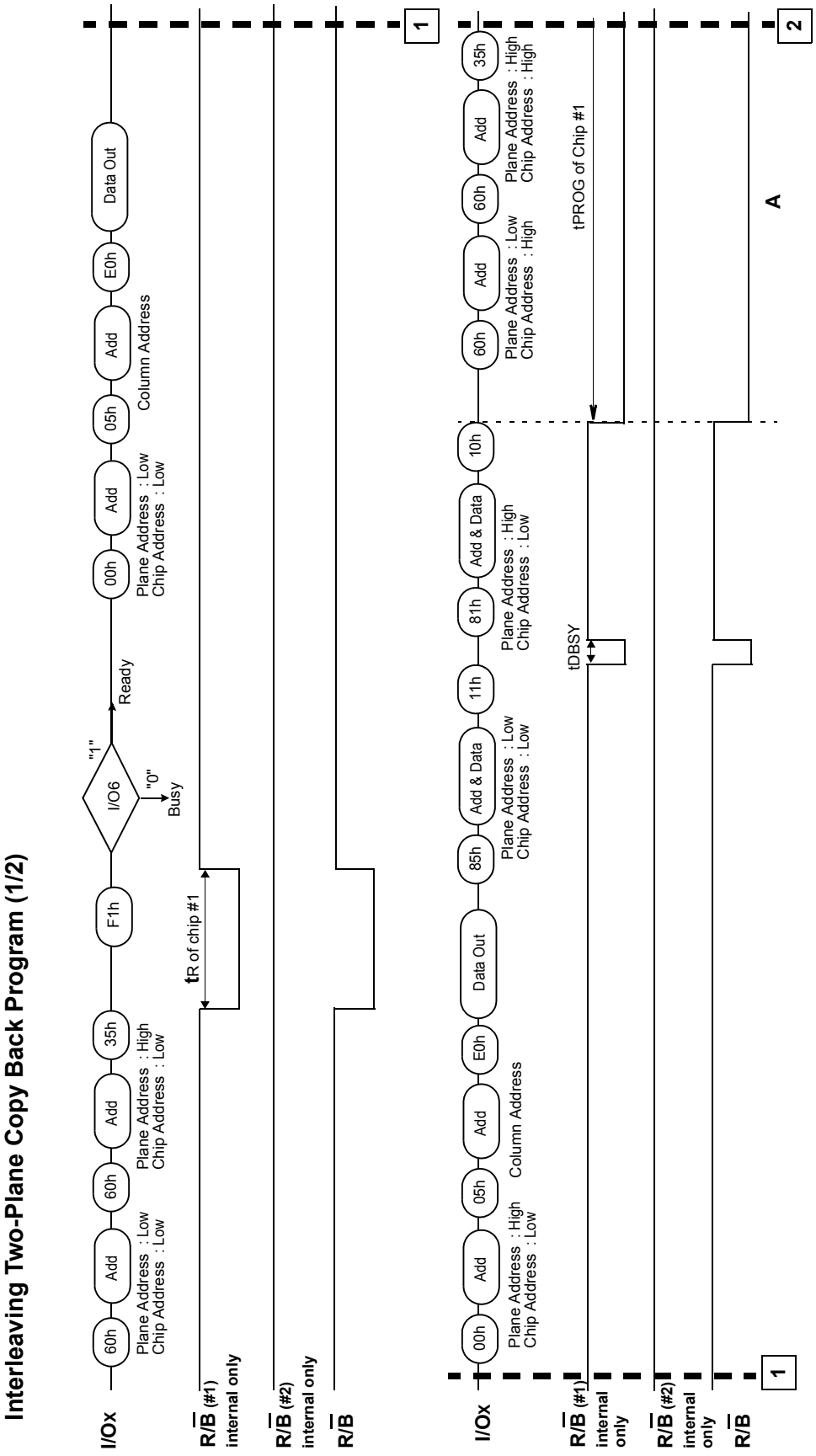


Interleaving Copy-Back Program Operation (2/2)

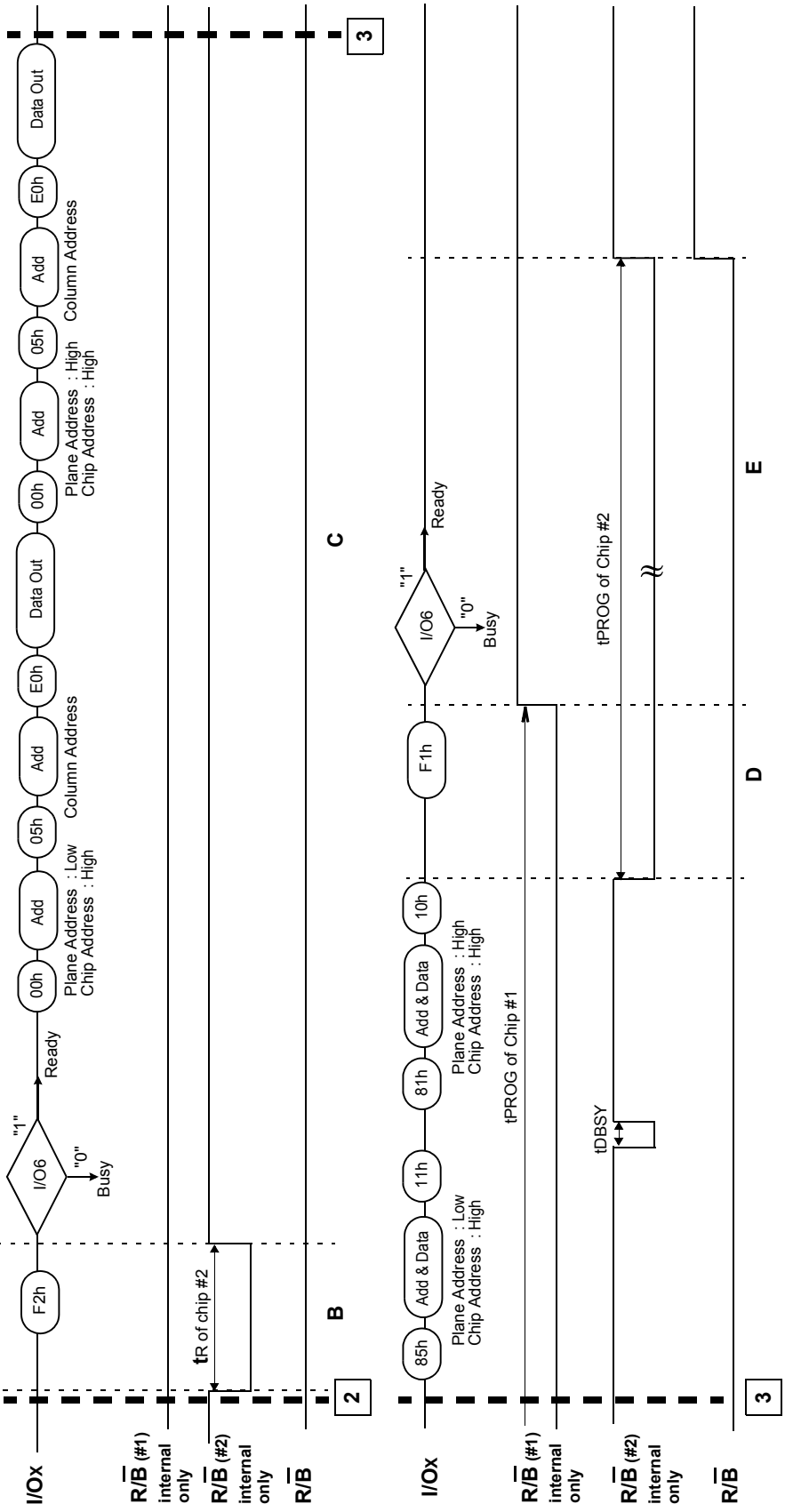


State A : Chip #1 is executing copy-back program operation, and chip #2 is in ready state. So the host can issue read for copy-back command to chip #2.
State B : Chip #1 is executing copy-back program operation and chip #2 is executing read for copy-back operation.
State C : Read for copy-back operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing copy-back program operation.
State D : Both chip #1 and chip #2 are executing copy-back program operation.
State E : Chip #2 is still executing a copy-back program operation, and chip #1 is in ready for the next operation.
State F : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave copy-back program on chip #1 and chip #2 alternatively.

Interleaving Two-Plane Copy Back Program (1/2)



Interleaving Two-Plane Copy Back Program (2/2)



State A : Chip #1 is executing 2-plane copy-back program operation, and chip #2 is in ready state. So the host can issue 2-plane read for copy-back command to chip #2.
State B : Chip #1 is executing 2-plane copy-back program operation and chip #2 is executing 2-plane read for copy-back operation.
State C : 2-plane read for copy-back operation on chip #2 is completed and chip #2 is ready for the next operation. Chip #1 is still executing 2-plane copy-back program operation.
State D : Both chip #1 and chip #2 are executing 2-plane copy-back program operation.
State E : Chip #2 is still executing a 2-plane copy-back program operation, and chip #1 is in ready for the next operation.
State F : Both chip #1 and chip #2 are ready.
Note : *F1h command is required to check the status of chip #1 to issue the next command to chip #1.
F2h command is required to check the status of chip #2 to issue the next command to chip #2.
As the above process, the system can operate Interleave 2-plane copy-back program on chip #1 and chip #2 alternatively.

System Interface Using $\overline{CE}$ don't-care.

For an easier system interface, $\overline{CE}$ may be inactive during the data-loading or serial access as shown below. The internal 4,314byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ-seconds, de-activating $\overline{CE}$ during the data-loading and serial access would provide significant savings in power consumption.

Figure 4. Program Operation with $\overline{CE}$ don't-care.

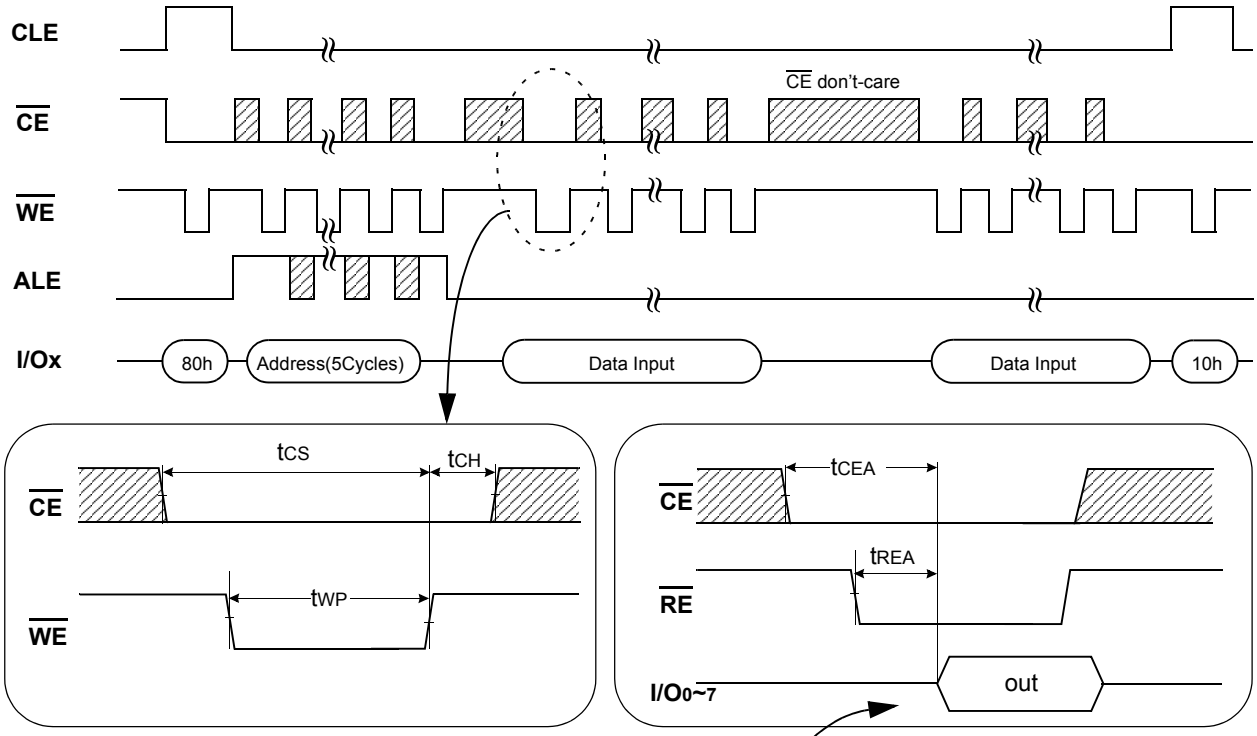
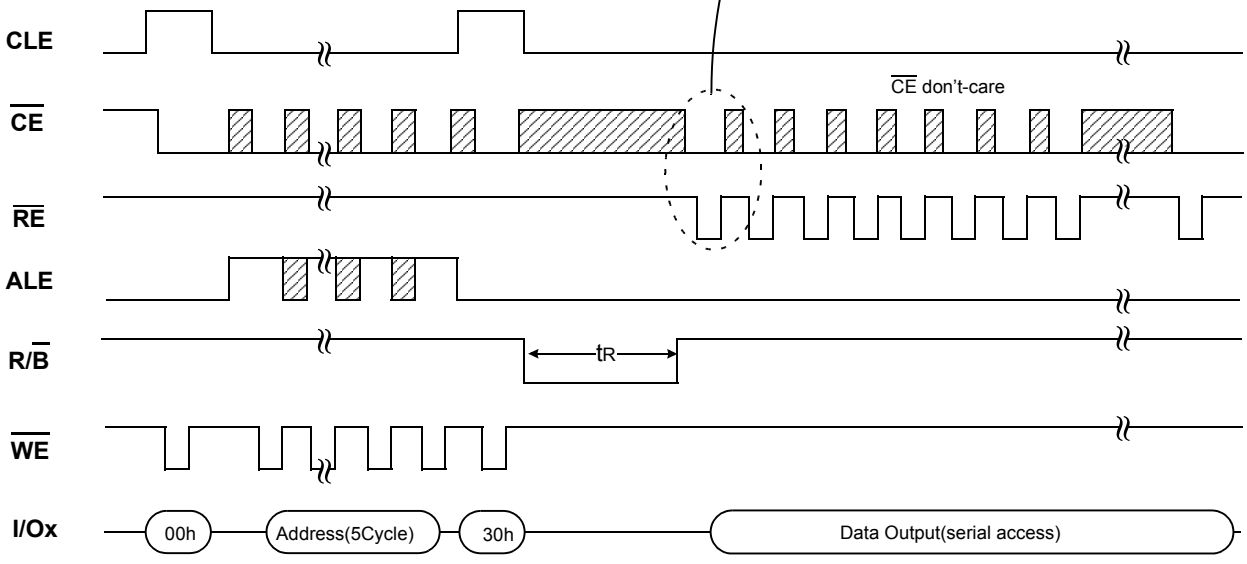


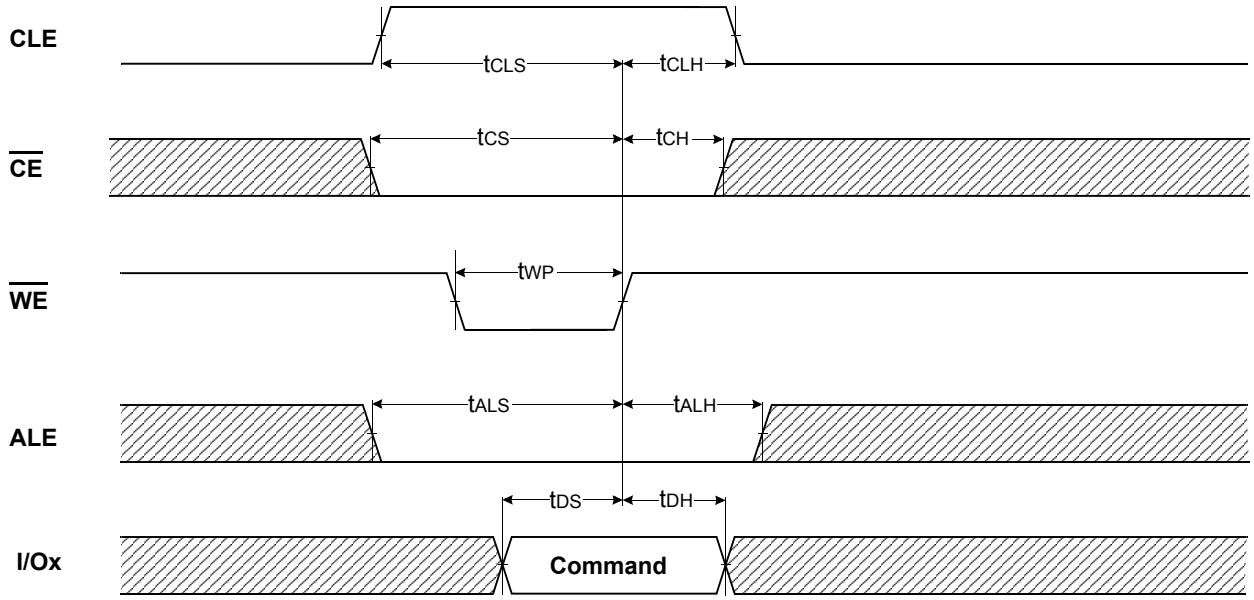
Figure 5. Read Operation with $\overline{CE}$ don't-care.



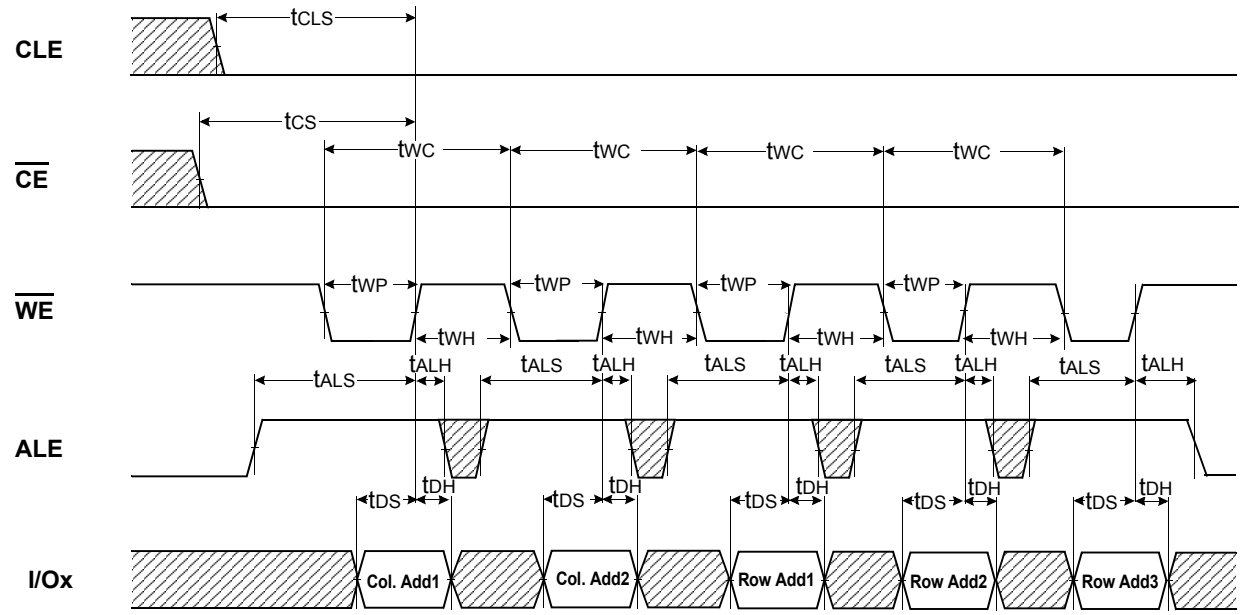
NOTE

Device	I/O	DATA	ADDRESS				
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
K9LBG08U0D	I/O 0 ~ I/O 7	4,314byte	A0~A7	A8~A12	A13~A20	A21~A28	A29~A32

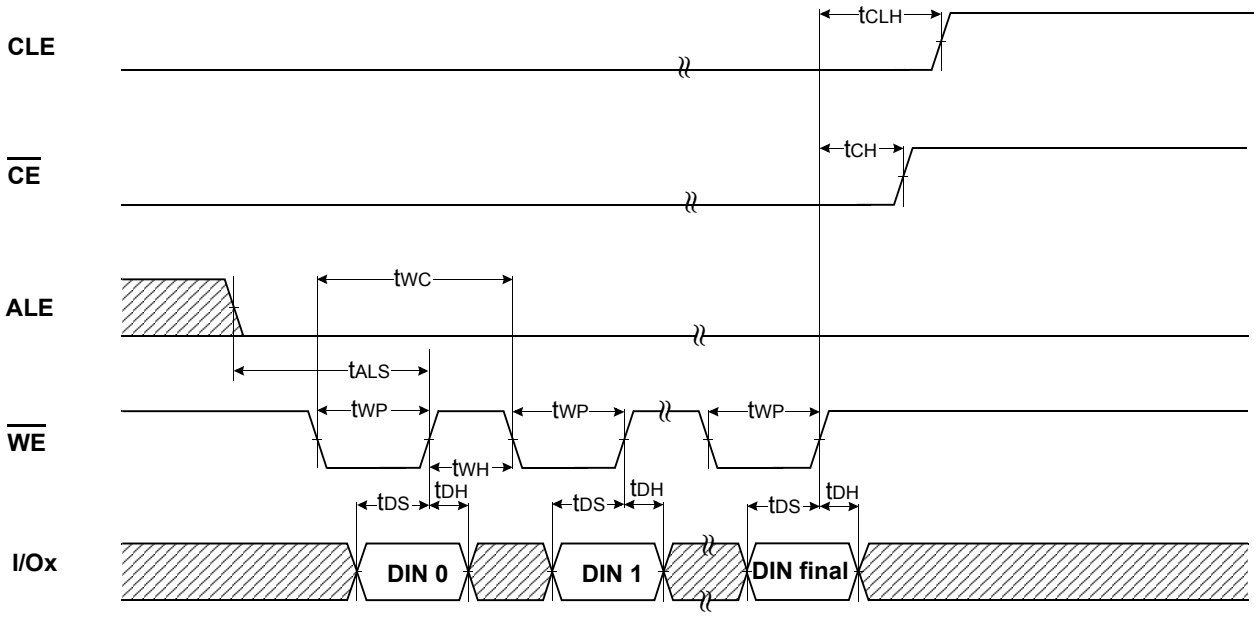
Command Latch Cycle



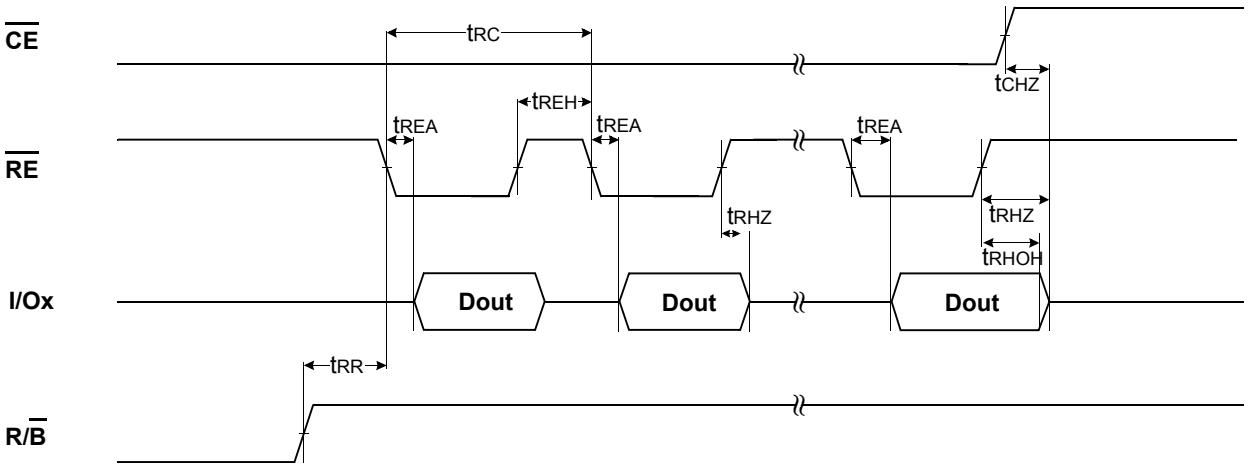
Address Latch Cycle



Input Data Latch Cycle

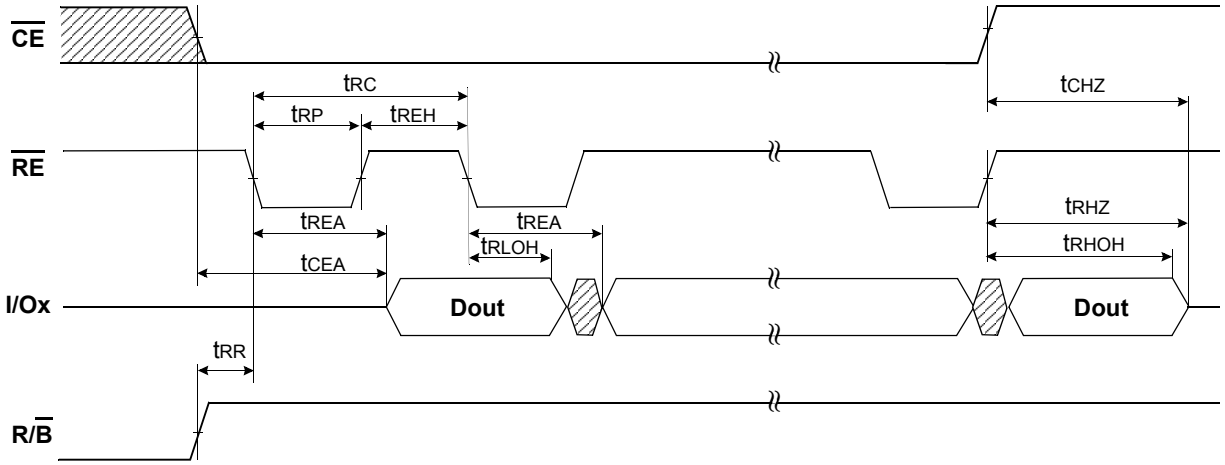


* Serial Access Cycle after Read(CLE=L, $\overline{WE}$=H, ALE=L)



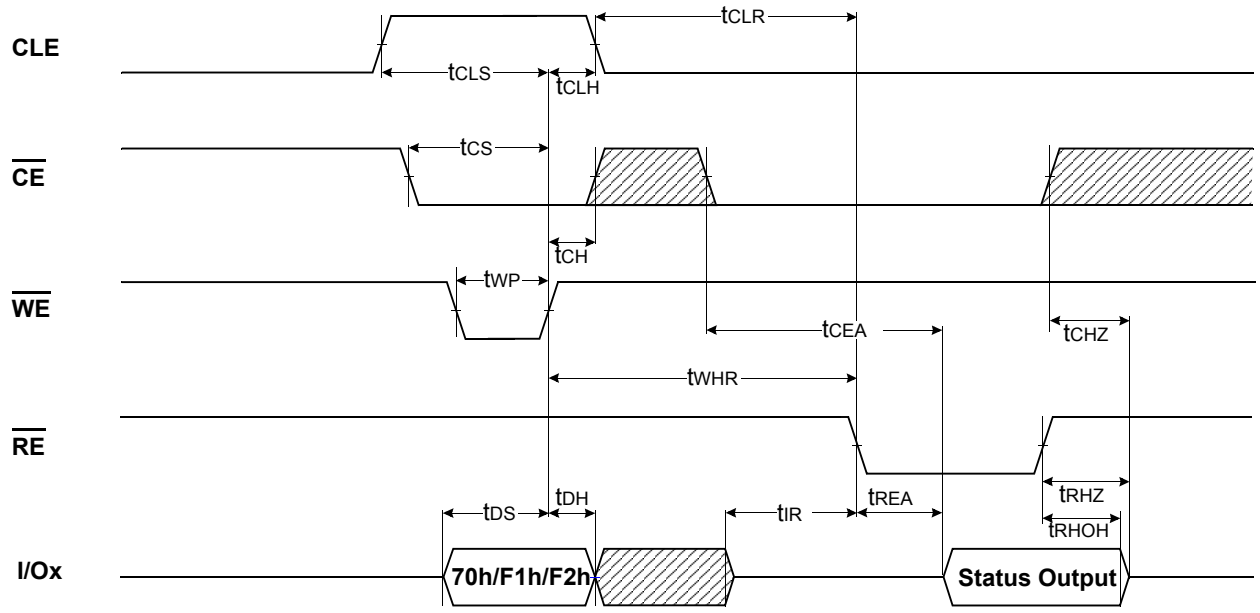
NOTES : 1.Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
2. tRLOH is valid when frequency is higher than 20MHz.
tRHOH starts to be valid when frequency is lower than 20MHz.

Serial Access Cycle after Read(EDO Type, CLE=L, $\overline{WE}$=H, ALE=L)

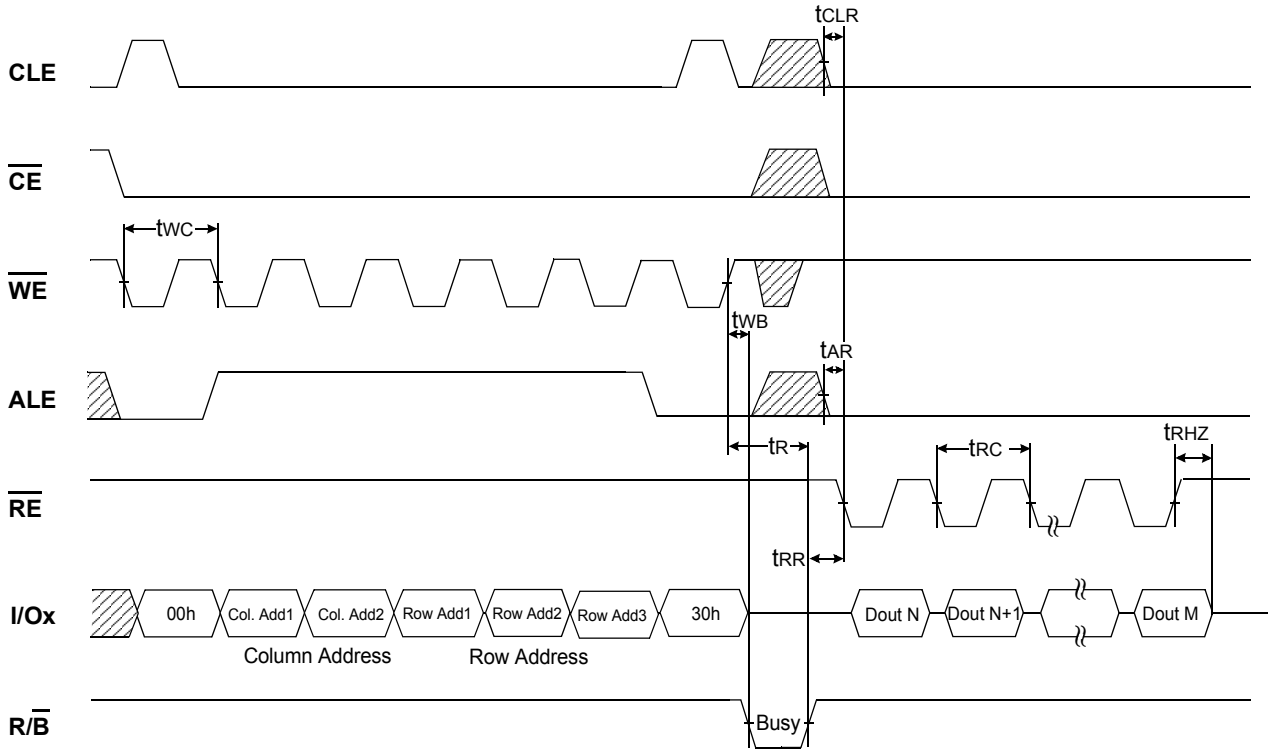


NOTES : 1. Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
2. tRLOH is valid when frequency is higher than 20MHz.
tRHOH starts to be valid when frequency is lower than 20MHz.

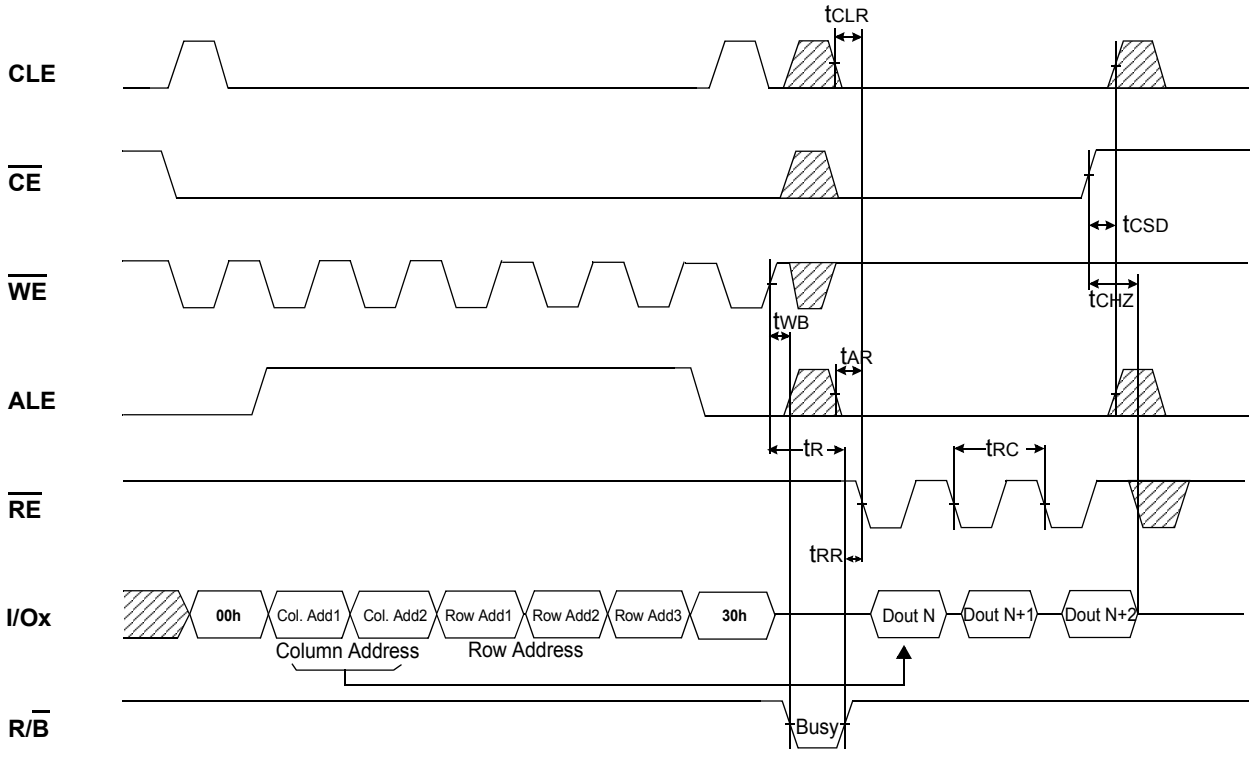
Status Read Cycle



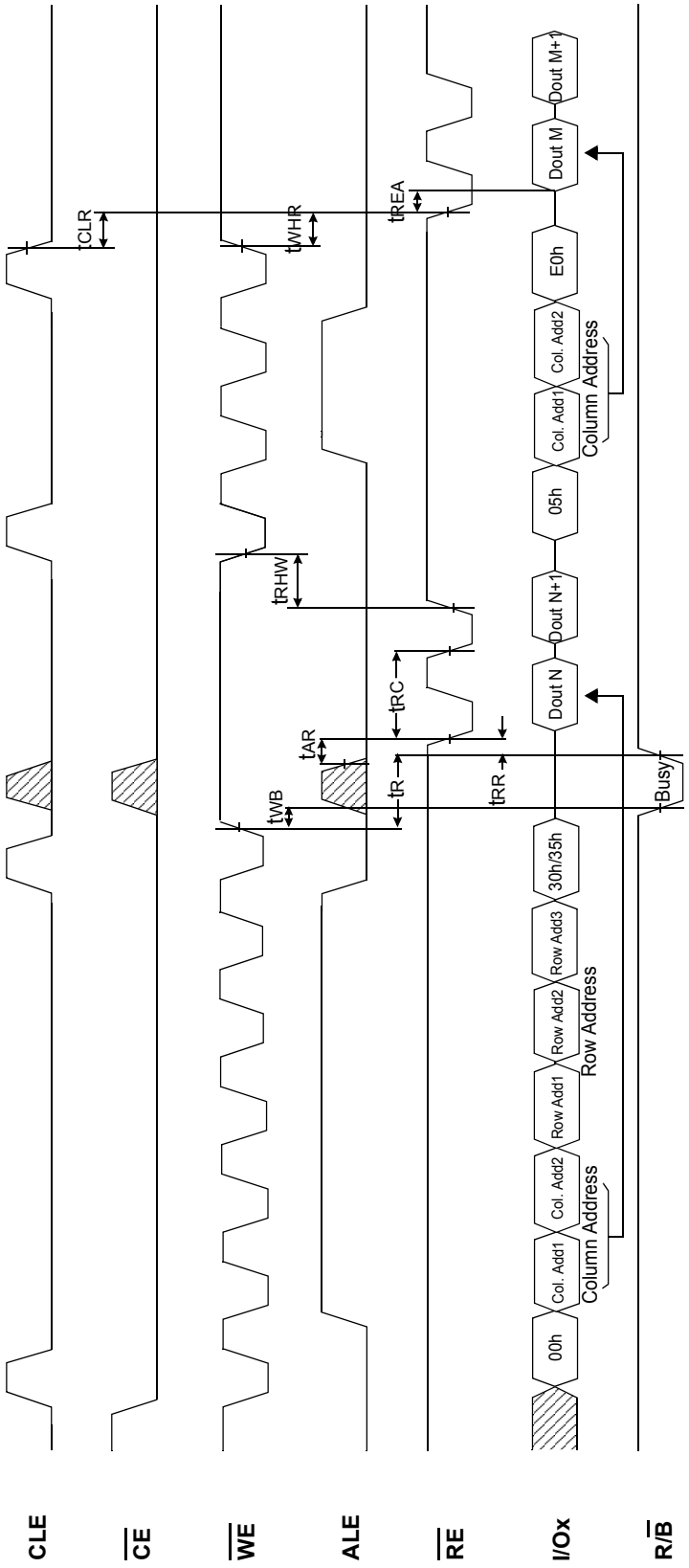
Read Operation



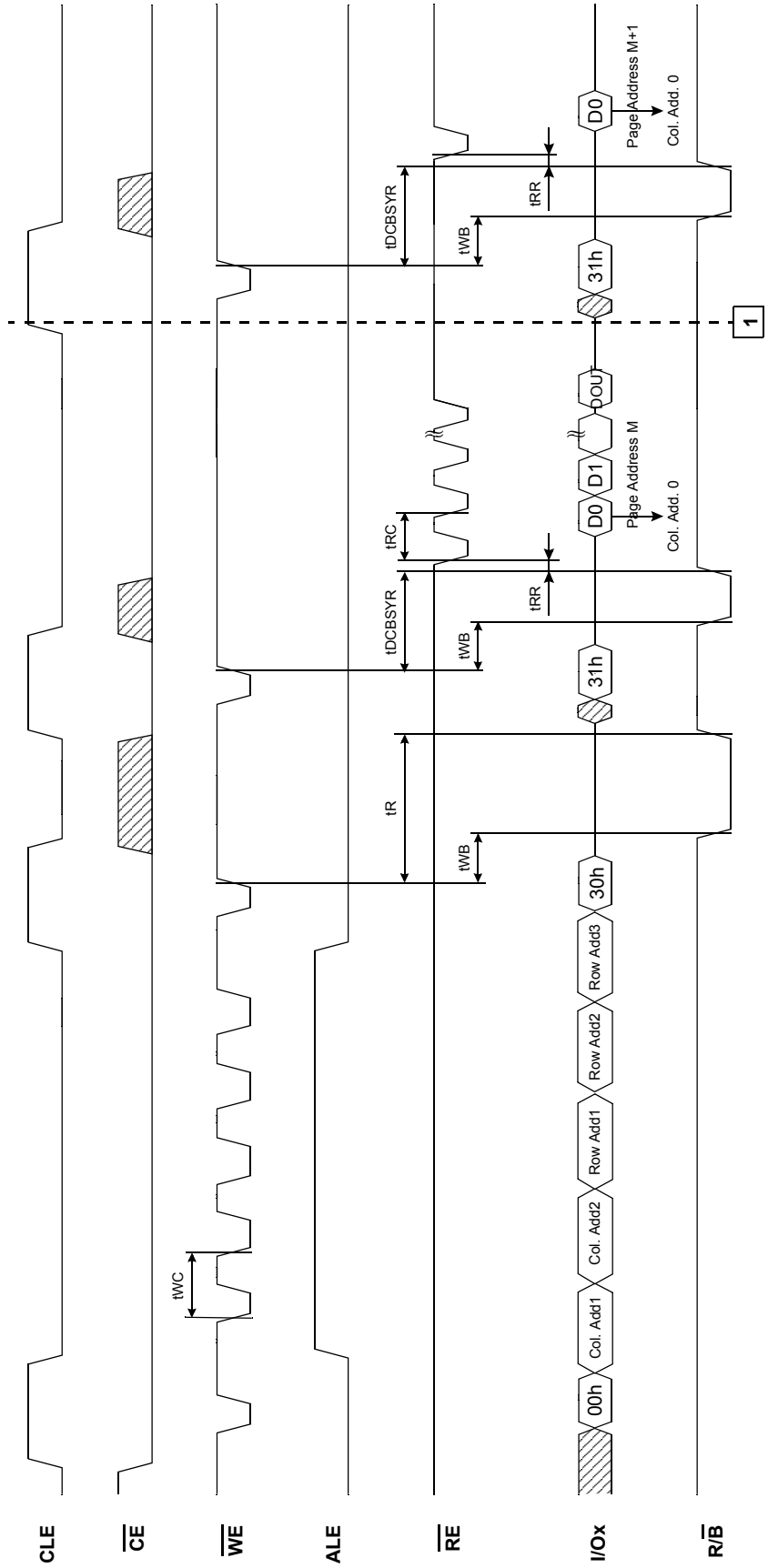
Read Operation(Intercepted by $\overline{CE}$)



Random Data Output In a Page

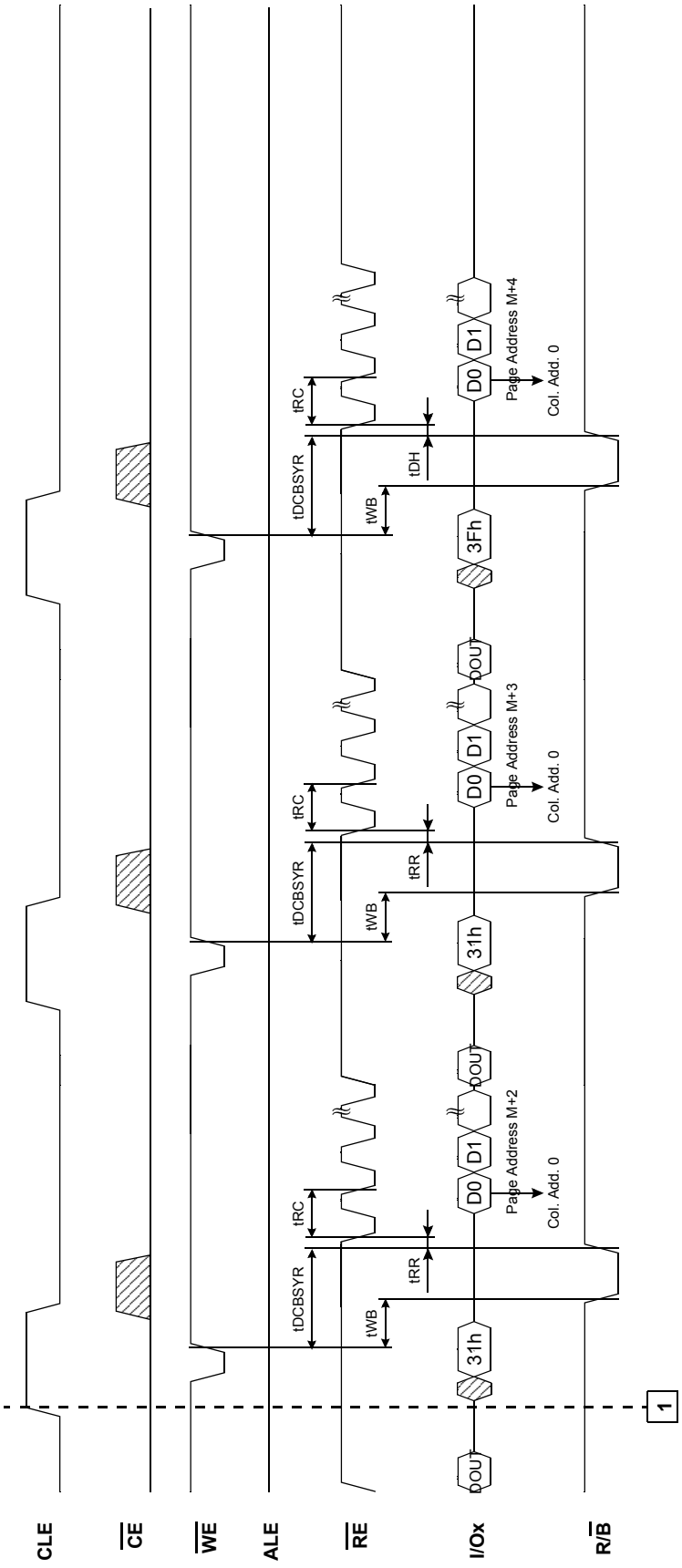


Cache Read Operation(1/2)



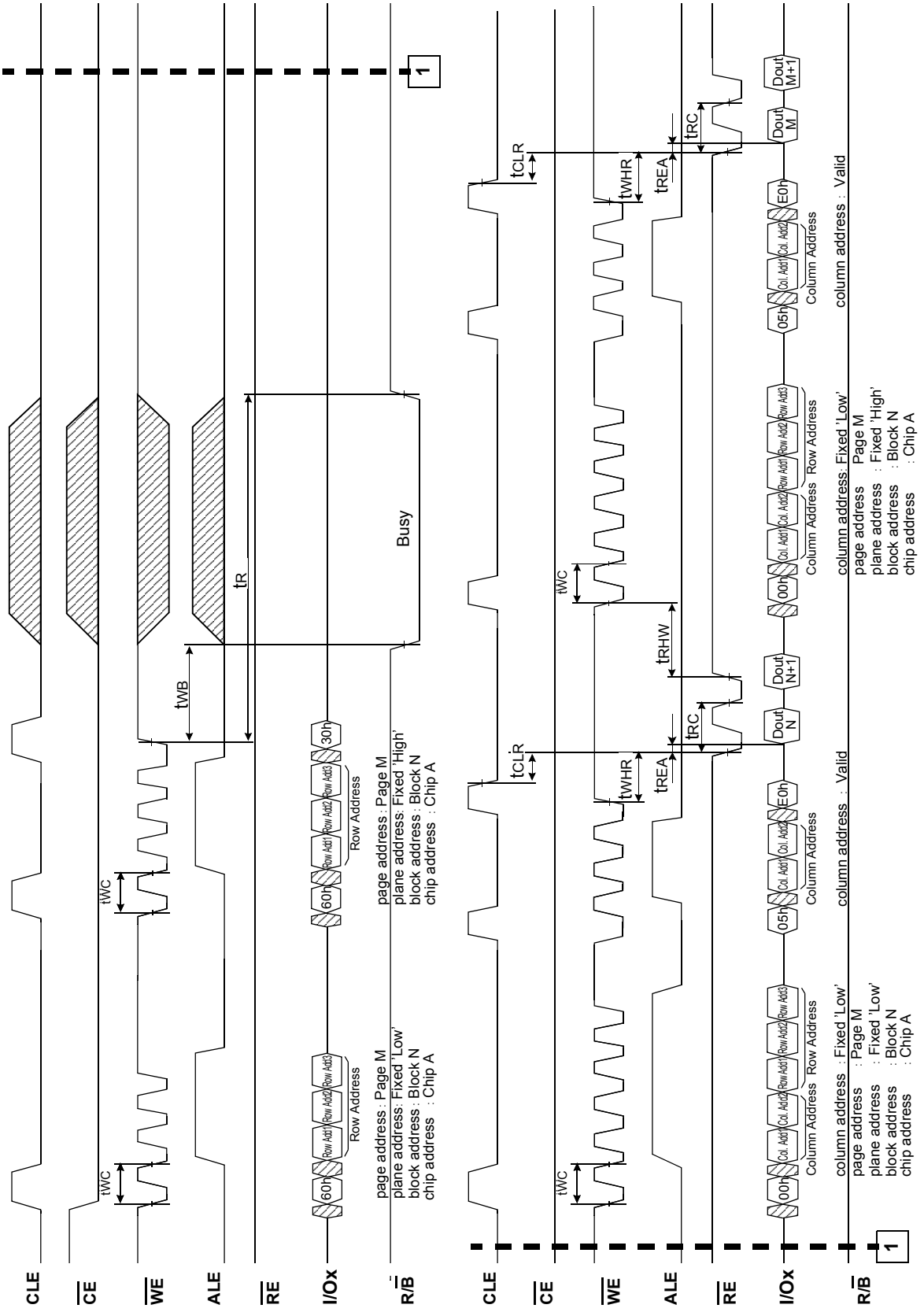
NOTES : 1. The column address will be reset to 0 by the 31h command input.
2. Cache Read operation is available only within a block.

Cache Read Operation(2/2)

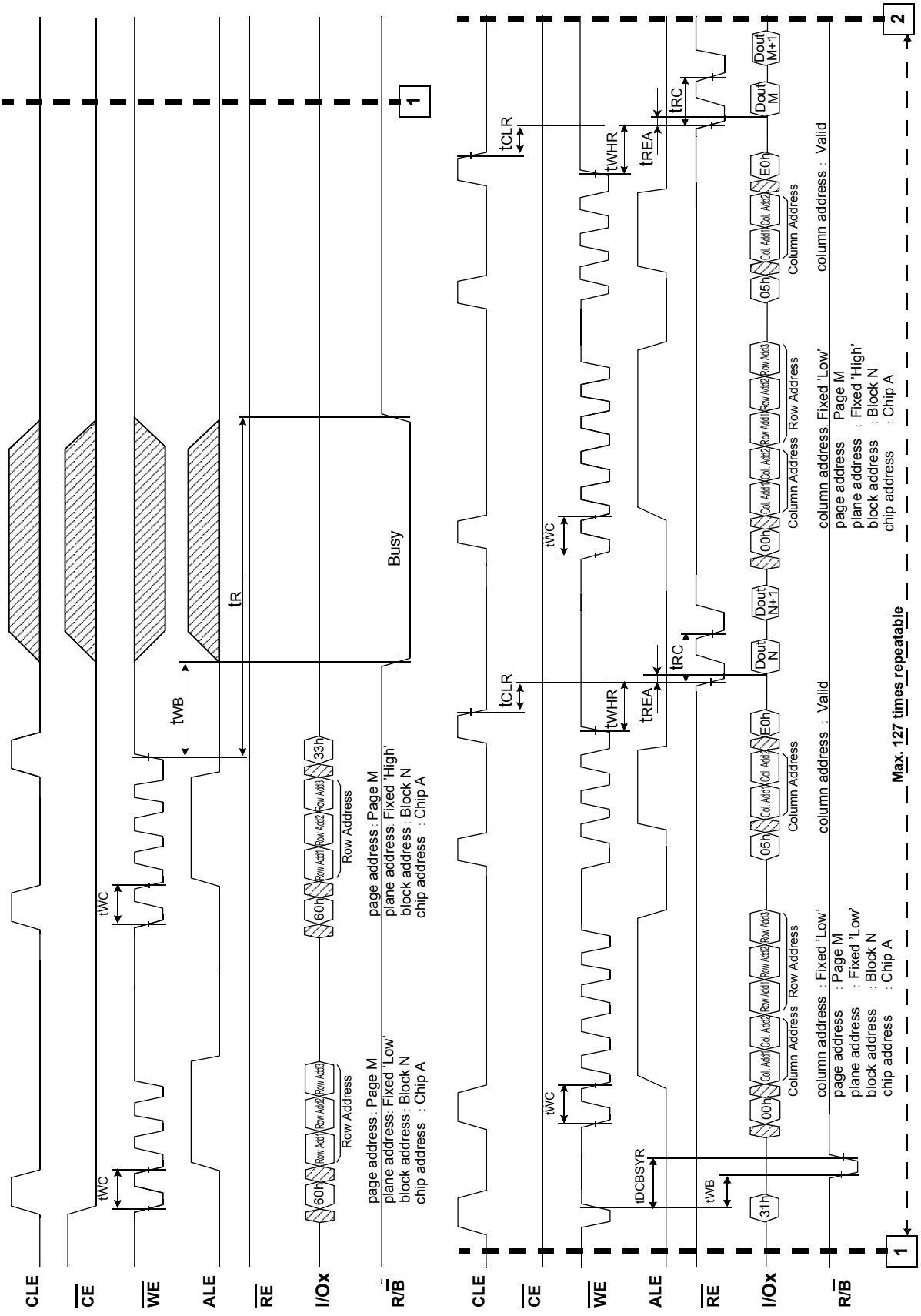


NOTES : 1. The column address will be reset to 0 by the 31h and 3Fh command input.
2. Cache Read operation is available only within a block.

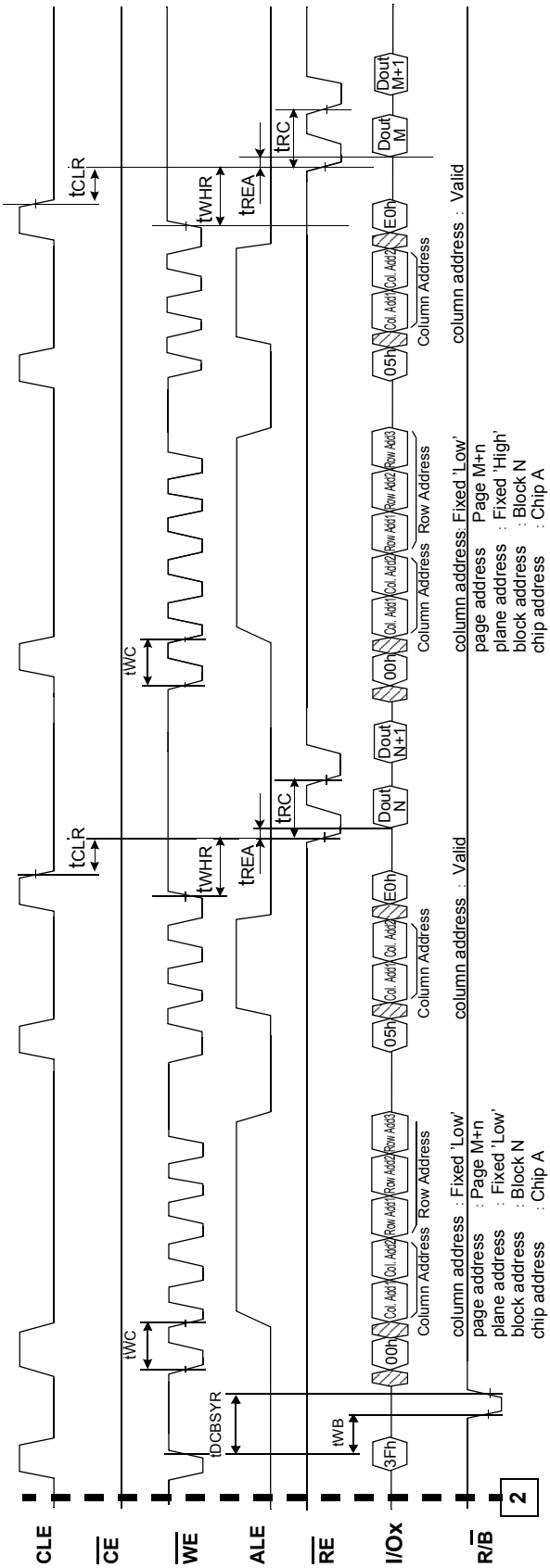
Two-Plane Page Read Operation with Two-Plane Random Data Out



Two-Plane Cache Read Operation with Two-Plane Random Data Out (1/2)

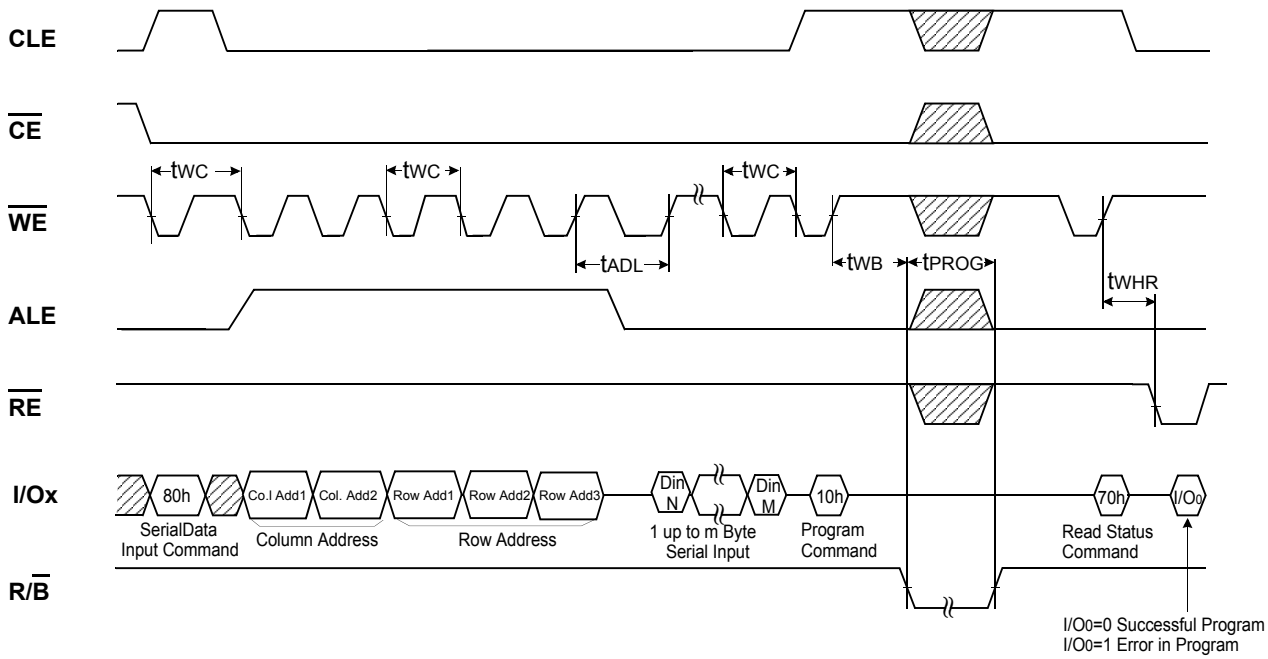


Two-Plane Cache Read Operation with Two-Plane Random Data Out (2/2)



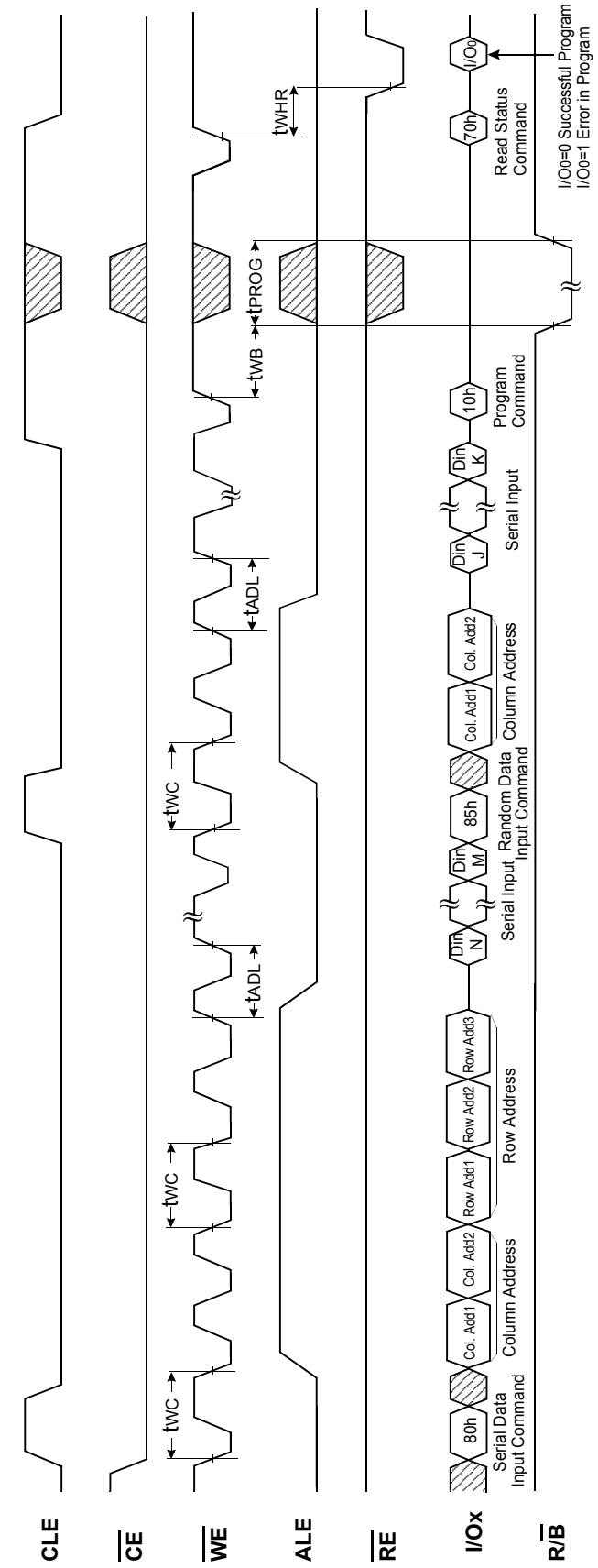
NOTES : 1. The column address will be reset to 0 by the 3Fh command input.
2. Cache Read operation is available only within a block.
3. Make sure to terminate the operation with 3Fh command. If the operation is terminated by 31h command, monitor I/O 6 (Ready/Busy) by issuing Status Read Command (70h) and make sure the previous page read operation is completed. If the page read operation is completed, issue FFh reset before next operation.

Page Program Operation



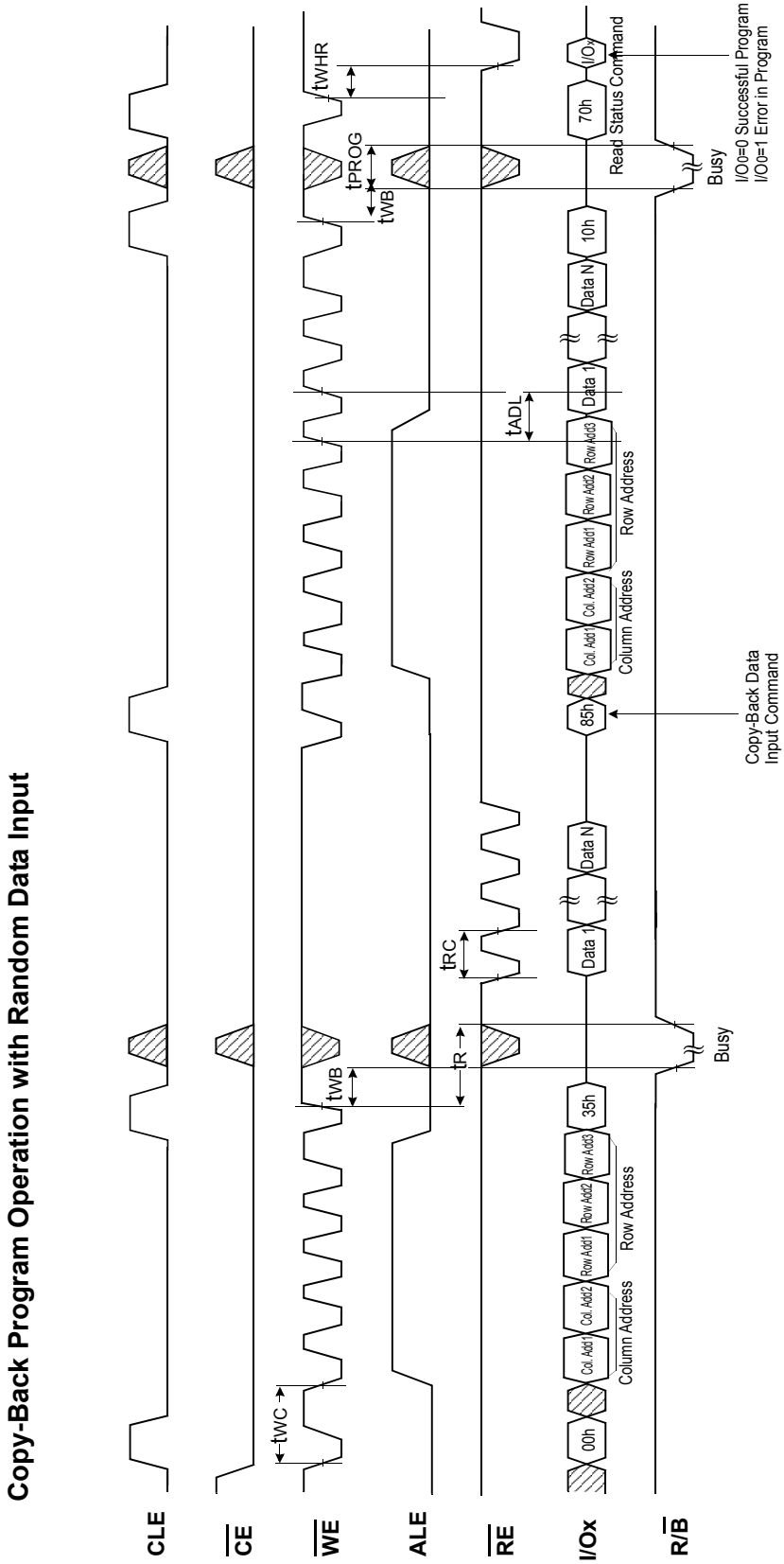
NOTES : tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Page Program Operation with Random Data Input



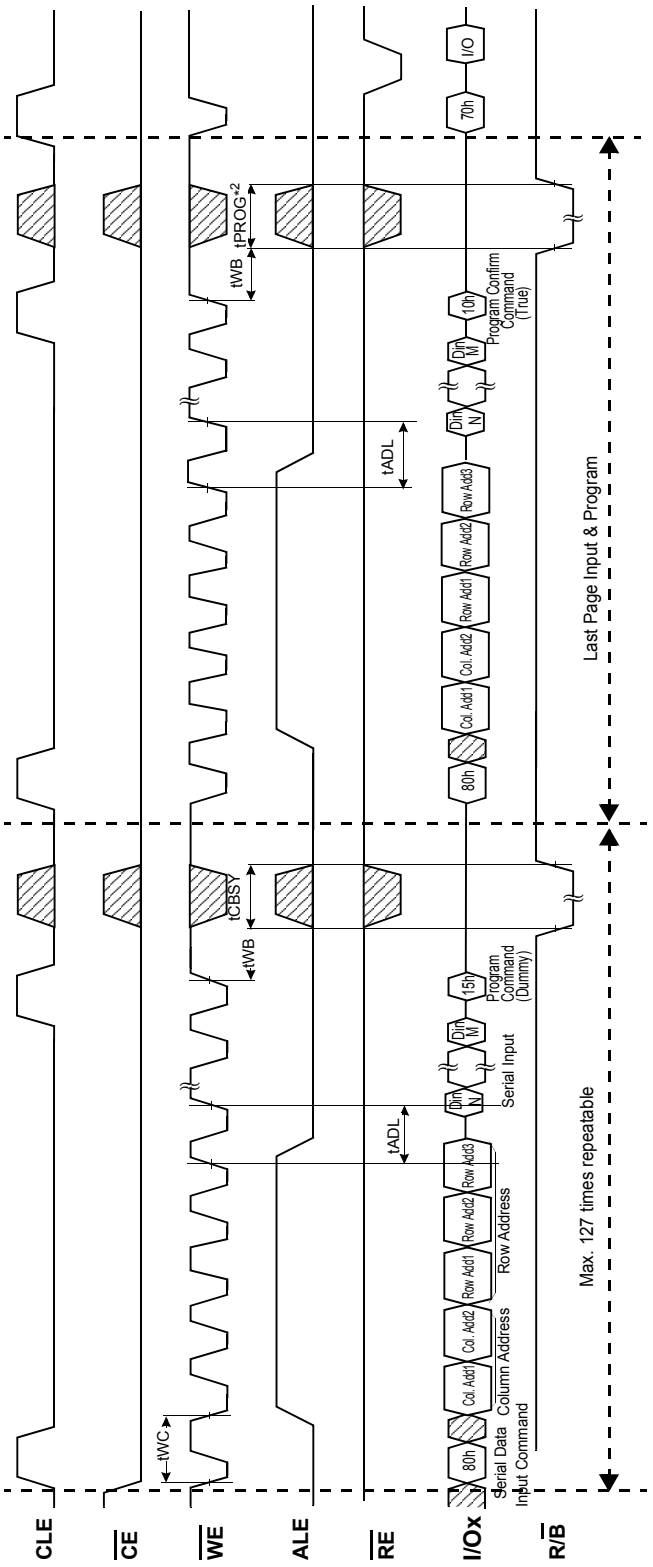
NOTES : 1. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

Copy-Back Program Operation with Random Data Input



NOTES : 1. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.

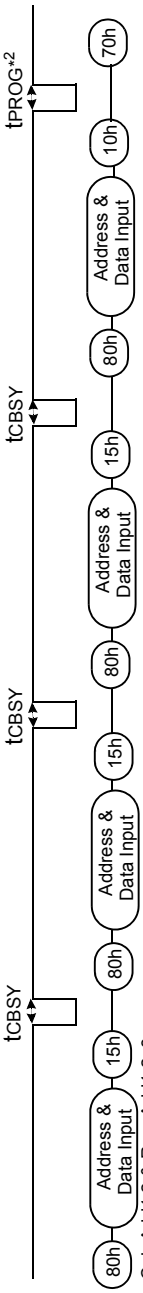
Cache Program Operation(available only within a block)



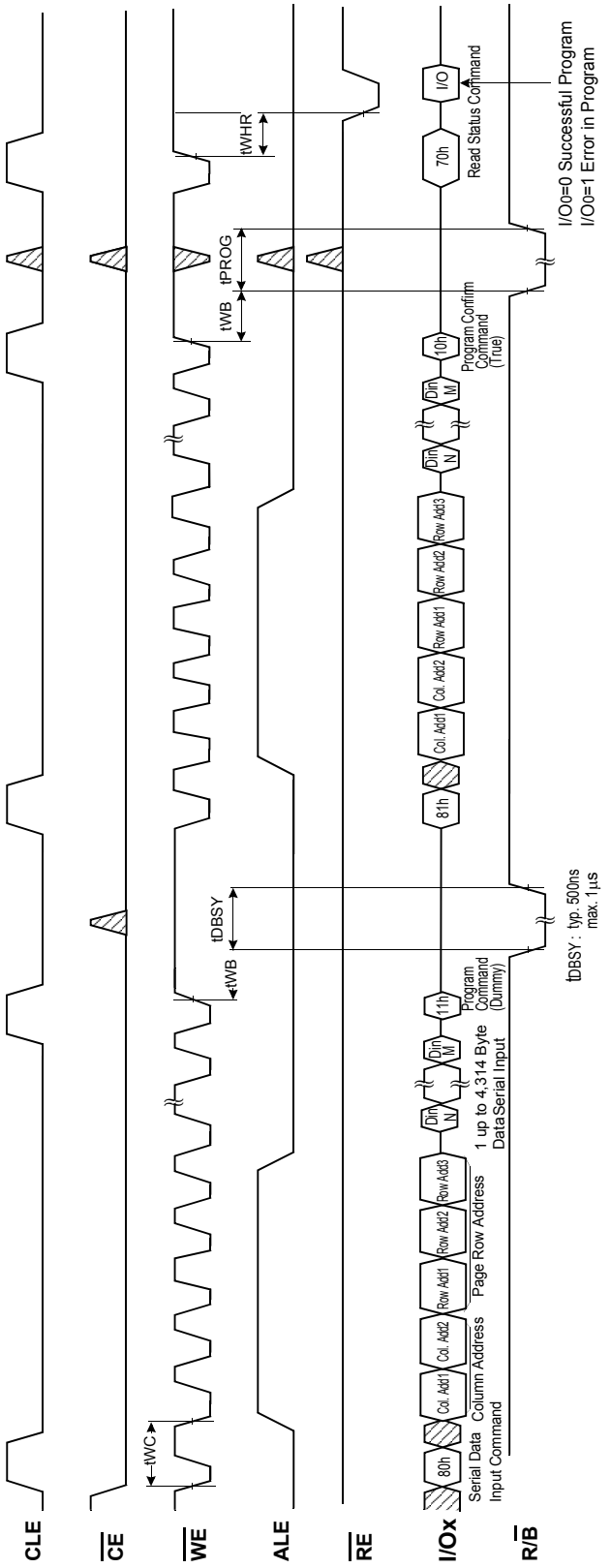
NOTES : 1. tADL is the time from the $\overline{WE}$ rising edge of final address cycle to the $\overline{WE}$ rising edge of first data cycle.
2. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG = Program time for the last page + Program time for the (last -1)th page
- (command input cycle time + address input cycle time + Last page data loading time)

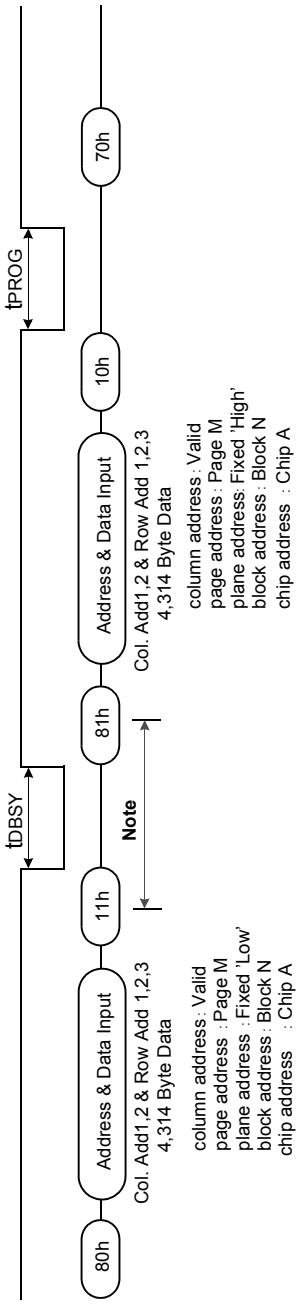
Ex.) Cache Program



Two-Plane Page Program Operation

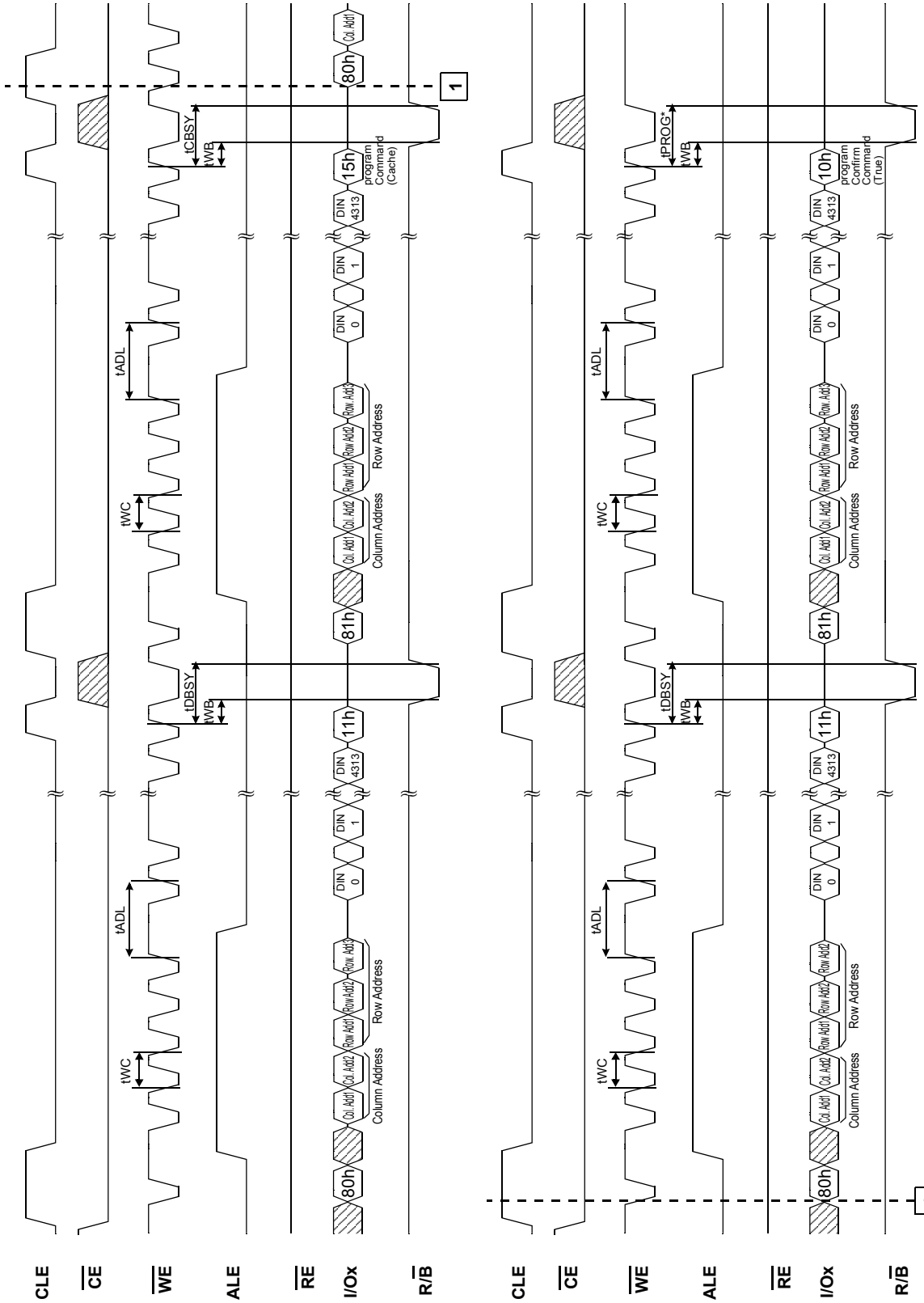


Ex.) Two-Plane Page Program



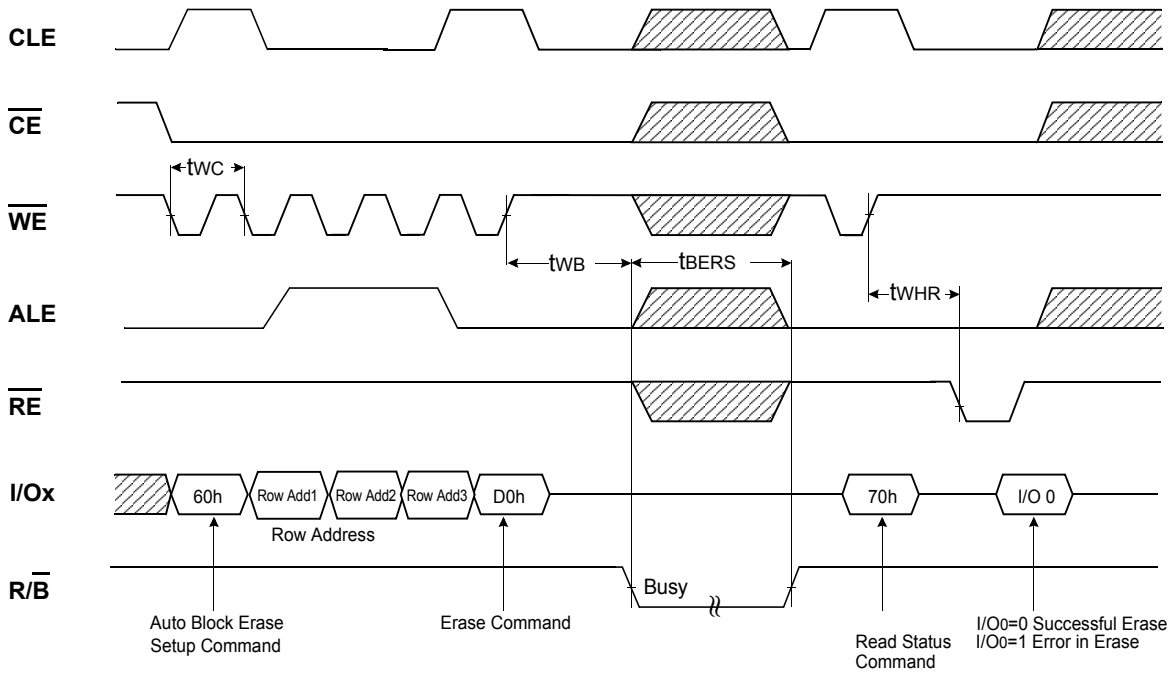
Note: Any command between 11h and 81h is prohibited except 70h/F1hF2h and FFh.

Two-Plane Cache Program Operation

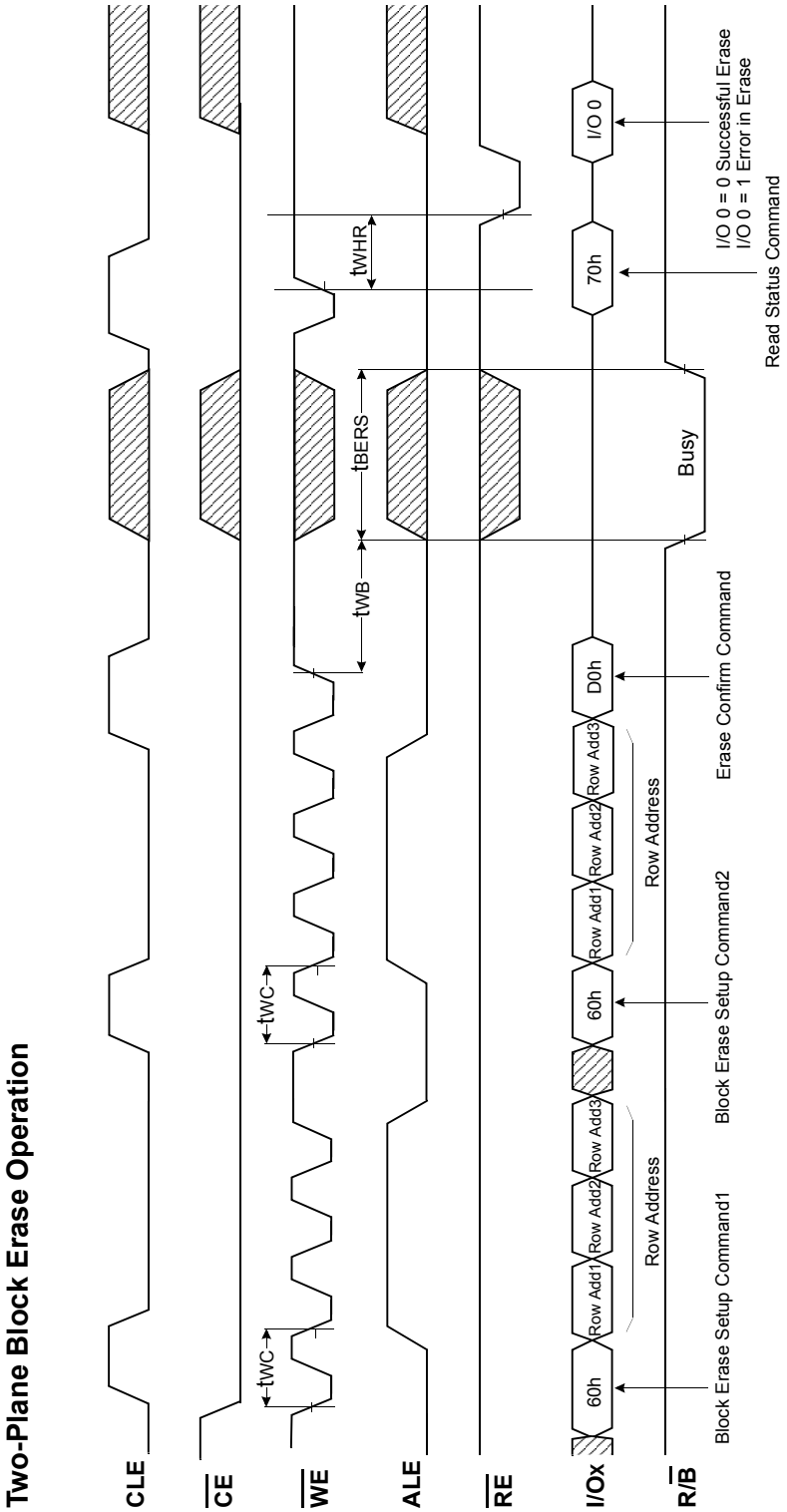


NOTES : 1. tPROG = Program time for the last page + Program time for the (last -1)th page - (command input cycle time + address input cycle time + Last page data loading time)
2. Make sure to terminate the operation with 80h-10h- command sequence. If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready/Busy) by issuing Status Read Command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

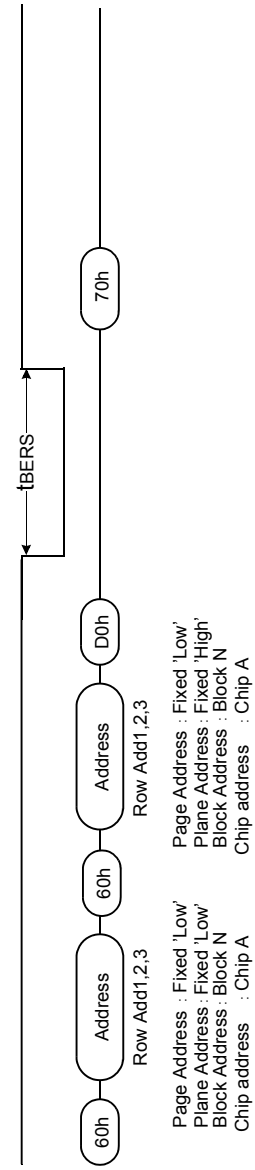
Block Erase Operation



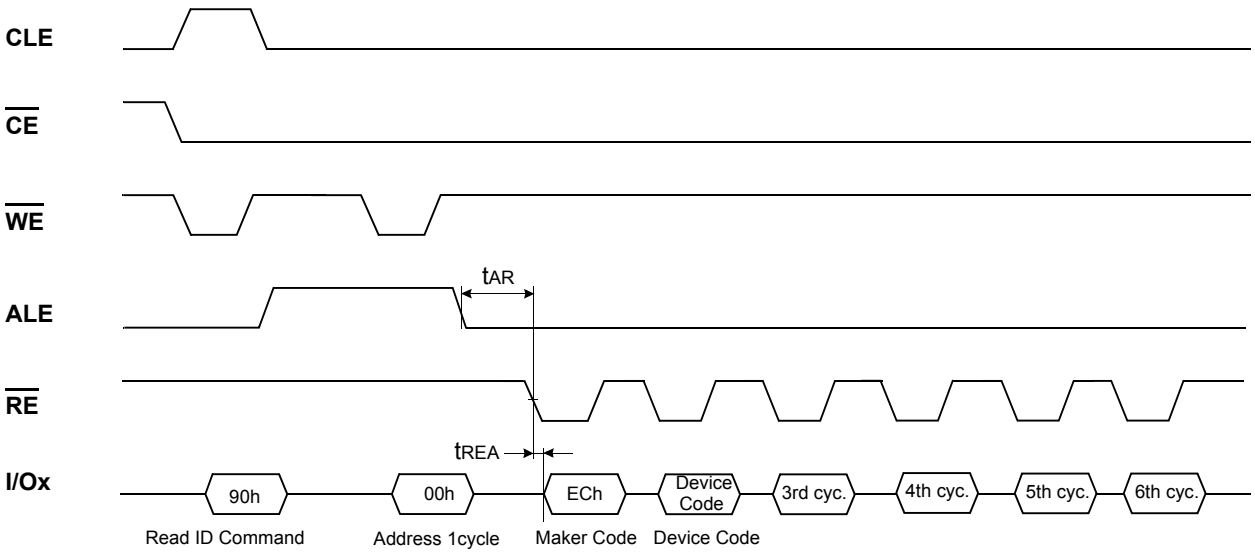
Two-Plane Block Erase Operation



Ex.) Address Restriction for Two-Plane Block Erase Operation



Read ID Operation



Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9LBG08U0D	D7h	D5h	29h	38h	41h
K9HCG08U1D	Same as K9LBG08U0D in it				
K9XDG08U5D					

ID Definition Table

90 ID : Access command = 90H

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc.
4th Byte	Page Size, Block Size,Redundant Area Size.
5th Byte	Plane Number, ECC Level, Organization.
6th Byte	Device Technology, EDO, Interface.

3rd ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3 I/O2	I/O1 I/O0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Support Support		0 1			
Cache Program	Not Support Support	0 1				

4th ID Data

	Description	I/O7	I/O6	I/O5 I/O4	I/O3	I/O2	I/O1 I/O0
Page Size (w/o redundant area)	2KB 4KB 8KB Reserved						0 0 0 1 1 0 1 1
Block Size (w/o redundant area)	128KB 256KB 512KB 1MB Reserved Reserved Reserved Reserved	0 0 0 0 1 1 1 1		0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1			
Redundant Area Size (byte / Page Size)	Reserved 128B 218B Reserved Reserved Reserved Reserved Reserved		0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
ECC Level	1bit / 512B 2bit / 512B 4bit / 512B 8bit / 512B 16bit / 512B Reserved Reserved Reserved		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved		0						0	0

6th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Device Version	50nm 40nm Reserved Reserved Reserved Reserved Reserved Reserved						0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 0
EDO	Not Support Support		0 1						
Interface	SDR DDR	0 1							
Reserved				0	0	0			

Device Operation

PAGE READ

Page read is initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 4,314 bytes of data within the selected page are transferred to the cache registers via data registers in less than 60μs(tR). The system controller can detect the completion of this data transfer(tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the cache registers, they may be read out in 30ns(K9XDG08U5D: 50ns) cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

Figure 6. Read Operation

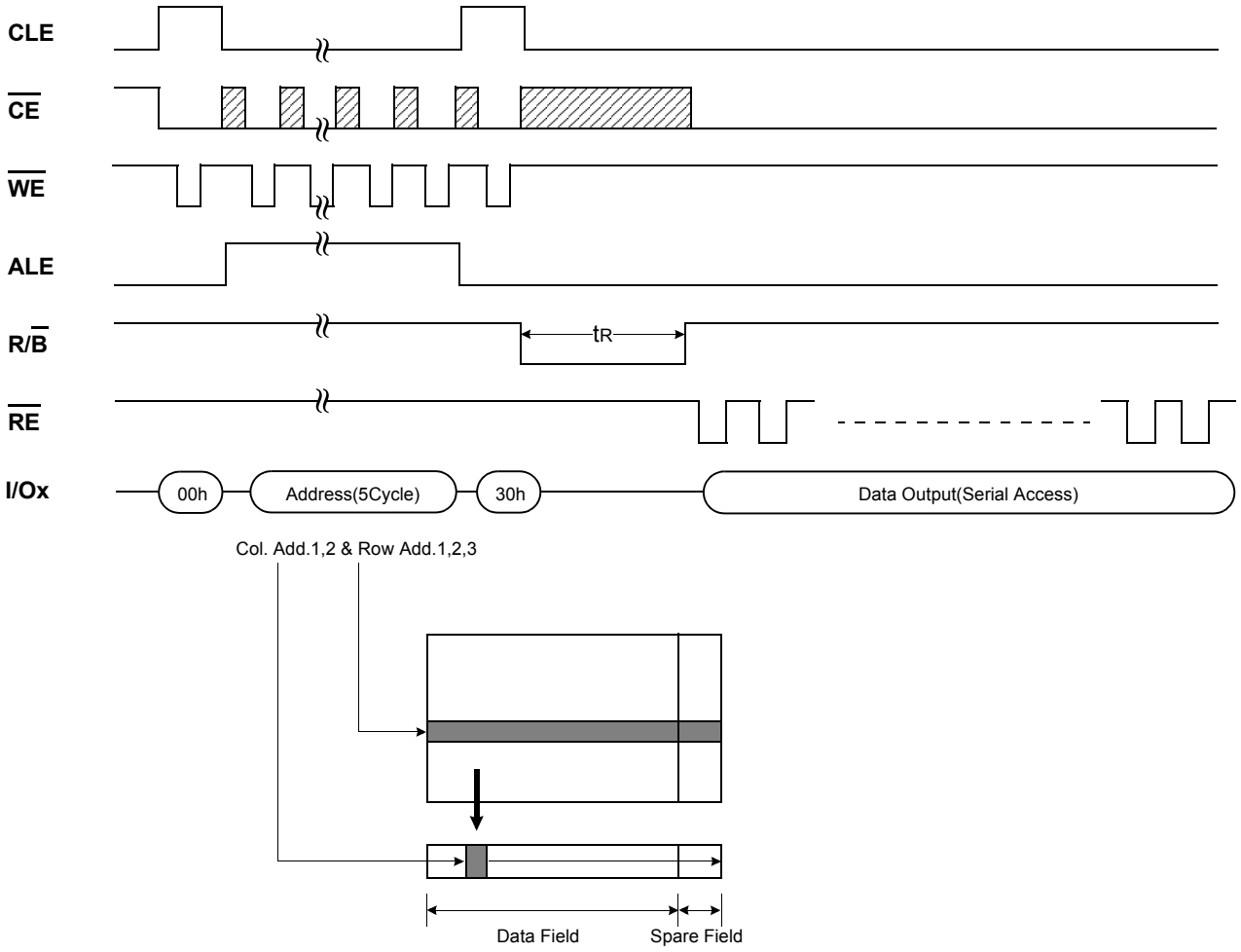
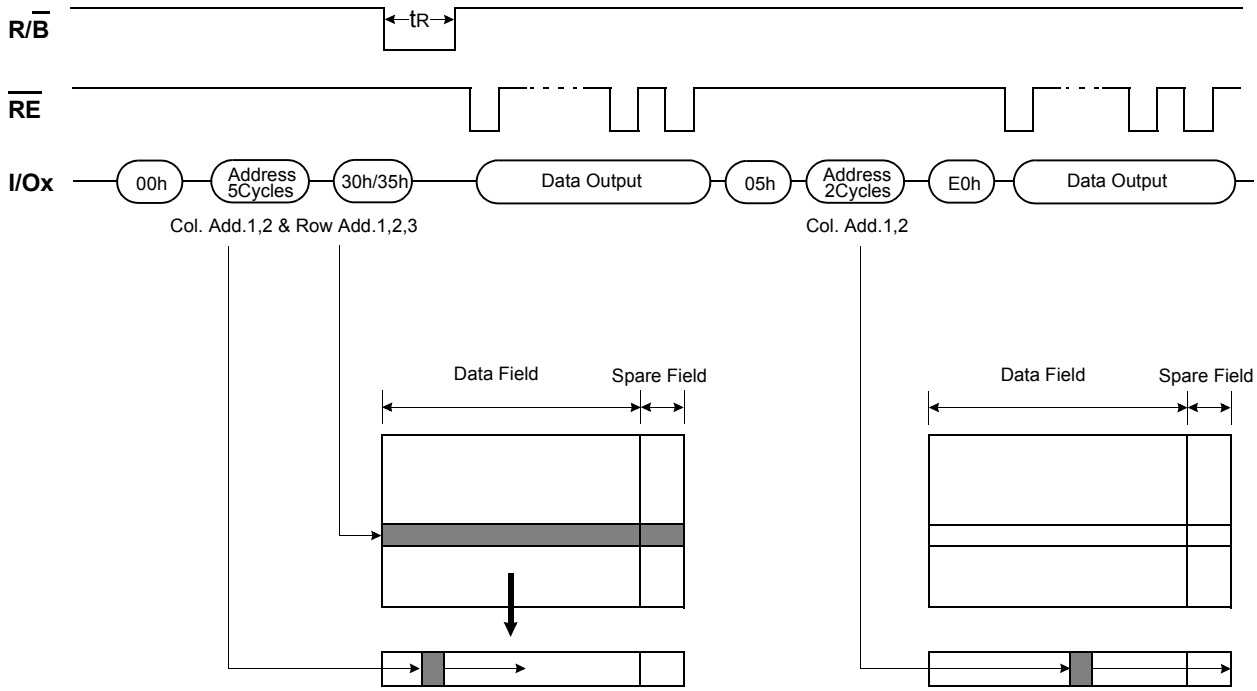


Figure 7. Random Data Output In a Page



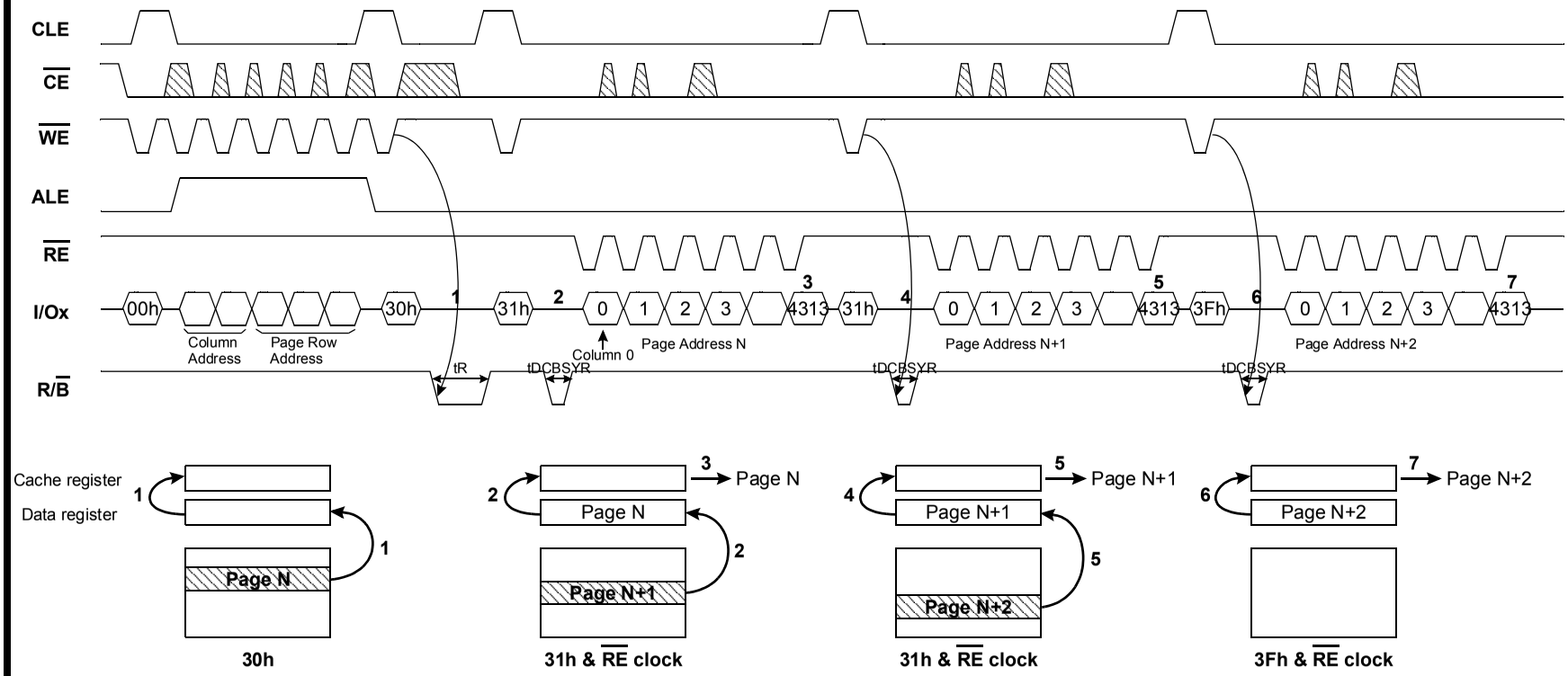
CACHE READ

Cache Read is an extension of Page Read, which is executed with 4,314byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data output may be executed while data in the memory cell is read into cache registers.

Cache read is also initiated by writing 00h-30h to the command register along with five address cycles. After initial power up, 00h command is latched. Therefore only five address cycles and 30h command initiates that operation after initial power up. The 4,314 bytes of data within the selected page are transferred to the cache registers via data registers in less than 60μs(t_R). After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(tDCBSYR). While the data in the cache registers is read out in 30ns cycle time by sequentially pulsing $\overline{RE}$, data of next page is transferred to the data registers. By issuing Last Cache Read command(3Fh), last data is transferred to the cache registers from the data registers after the completion of transfer from memory cell to data registers. Cache Read is available only within a block.

Figure 8. Cache Read

The device has a Read operation with cache registers that enables the high speed read operation shown below. When the block address changes, this sequence has to be started from the beginning.



NOTE

-. If the 31h command is issued to the device, the data content of the next page is transferred to the data registers during serial data out from the cache registers, and therefore the tR (Data transfer from memory cell to data register) will be reduced.

1. Normal read. Data is transferred from Page N to cache registers through data registers. During this time period, the device outputs Busy state for tR max.
2. After the Ready/Busy returns to Ready, 31h command is issued and data is transferred to cache registers from data registers again. This data transfer takes tDCBSYR max and the completion of this time period can be detected by Ready/Busy signal.
3. Data of Page N+1 is transferred to data registers from cell while the data of Page N in cache registers can be read out by $\overline{RE}$ clock simultaneously.
4. The 31h command makes data of Page N+1 transfer to cache registers from data registers after the completion of the transfer from cell to data registers. The device outputs Busy state for tDCBSYR max..This Busy period depends on the combination of the internal data transfer time from cell to data registers and the serial data out time.
5. Data of Page N+2 is transferred to data registers from cell while the data of Page N+1 in cache registers can be read out by $\overline{RE}$ clock simultaneously.
6. The 3Fh command makes the data of Page N+2 transfer to the cache registers from the data registers after the completion of transfer form cell to data registers. The device outputs Busy state for tDCBSYR max.This Busy period depends on the combination of the internal data transfer time from cell to data registers and the transfer from data registers to cache registers.
7. Data of Page N+2 in cache registers can be read out, but since the 3Fh command does not transfer the data from the memory cell to data registers, the device can accept new command input immediately after the completion of serial data out.

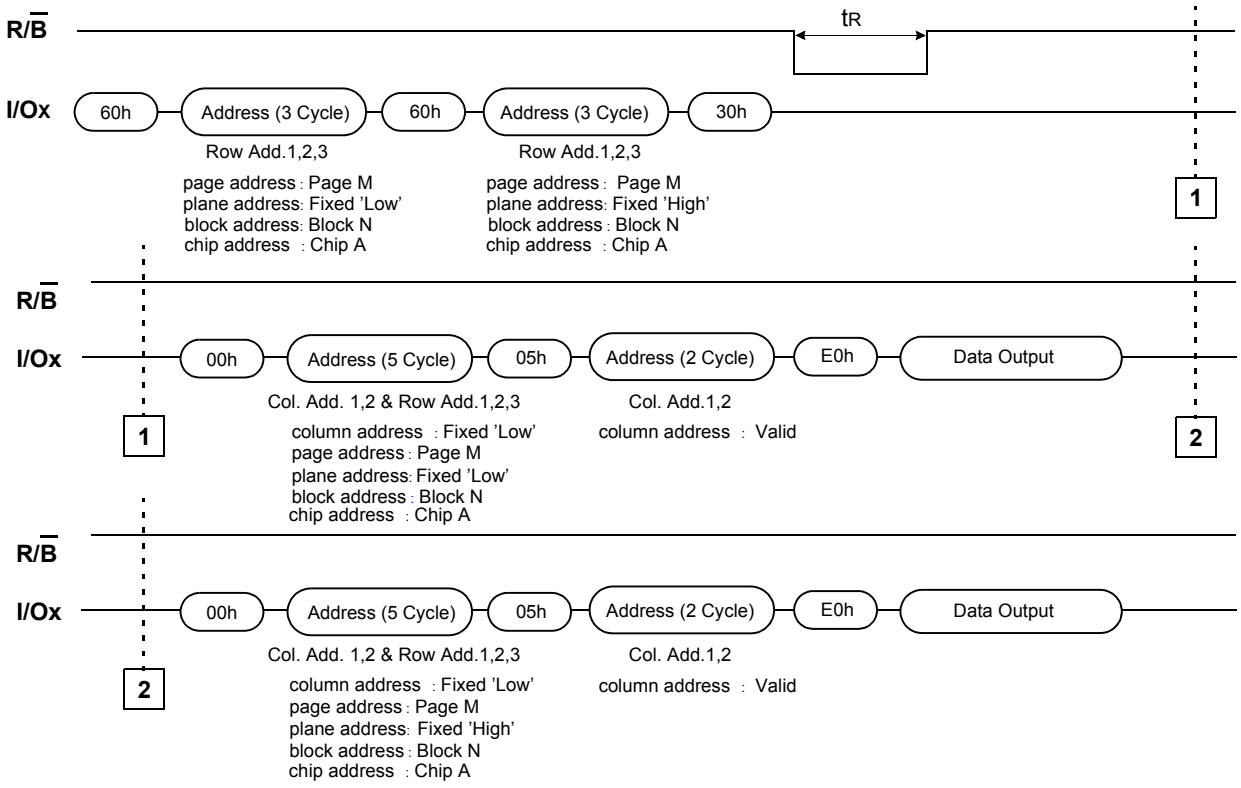
TWO-PLANE PAGE READ

Two-Plane Page Read is an extension of Page Read, for a single plane with 4,314 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 4,314 byte data registers enables a random read of two pages. Two-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. **In this case, only same page of same block can be selected from each plane.**

After Read Confirm command(30h) the 8,628 bytes of data within the selected two page are transferred to the cache registers via data registers in less than 60us(tR). The system controller can detect the completion of data transfer(tR) by monitoring the output of R/B pin.

Once the data is loaded into the cache registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences.

Figure 9. Two-Plane Page Read Operation with Two-Plane Random Data Out



TWO-PLANE CACHE READ

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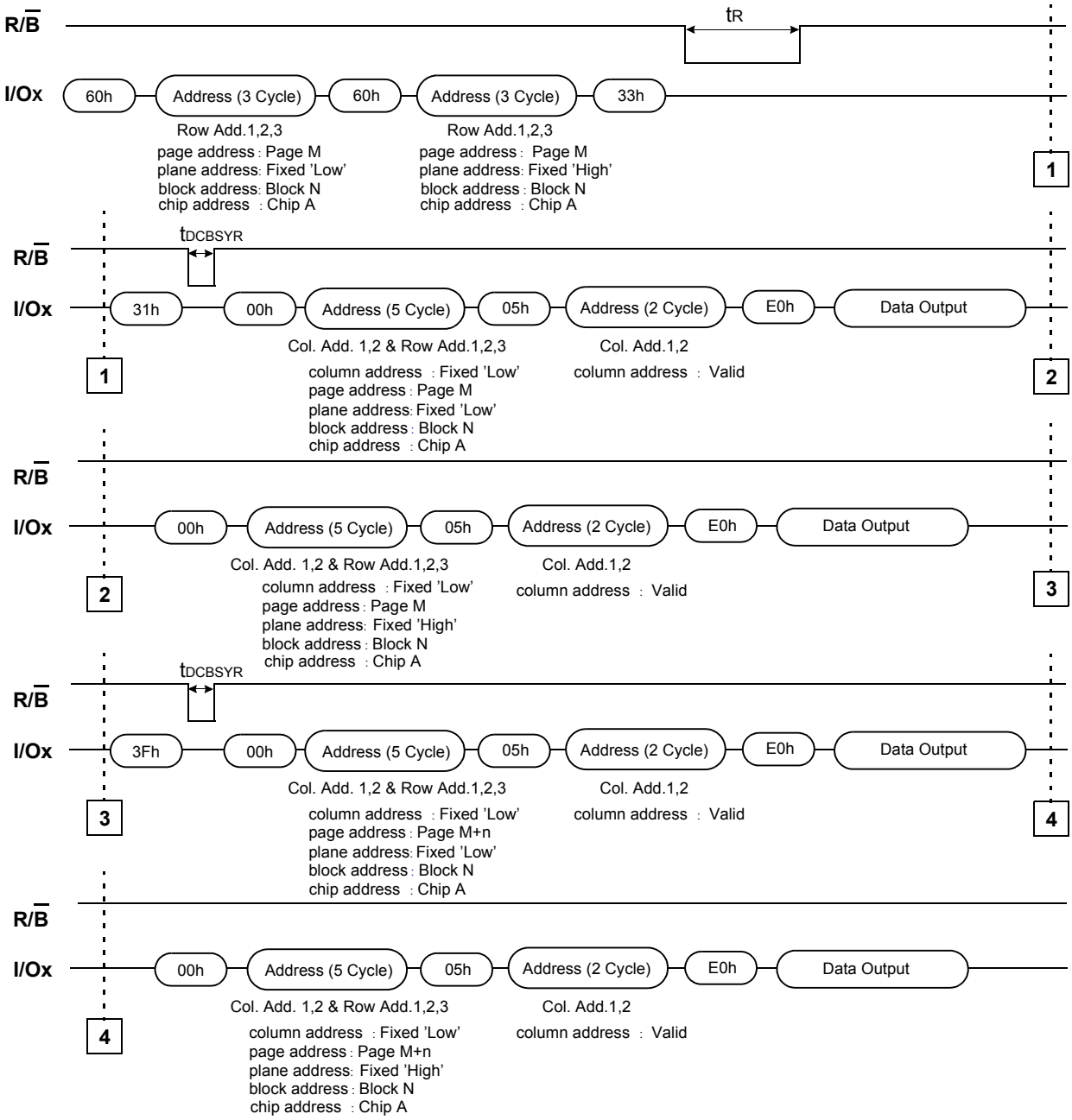
After Read Confirm command(33h) the 8,628 bytes of data within the selected two page are transferred to the cache registers via data registers in less than 60us(tR). After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(tDCBSYR). Once the data is loaded into the cache registers from data registers, the data output of first plane can be read out by issuing command 00h with Five Address Cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences. The detail sequence of Two-Plane Cache Read is shown in Figure 10.

Figure 10. Two-Plane Cache Read Operation with Two-Plane Random Data Out



PAGE PROGRAM

The device is programmed basically on a page basis, and the number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 time for the page. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 4,314bytes of data may be loaded into the data registers via cache registers, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the five cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

Figure 11. Program & Read Status Operation

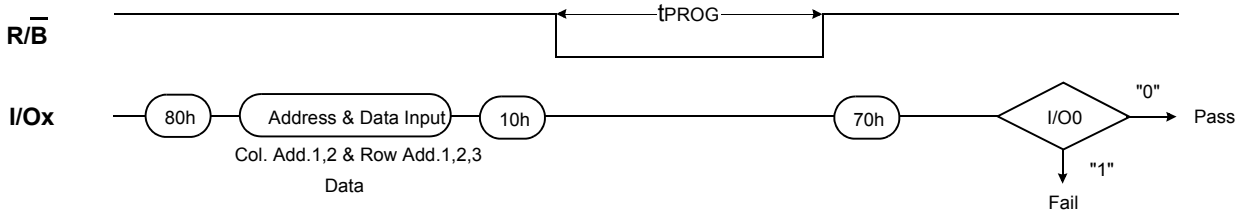
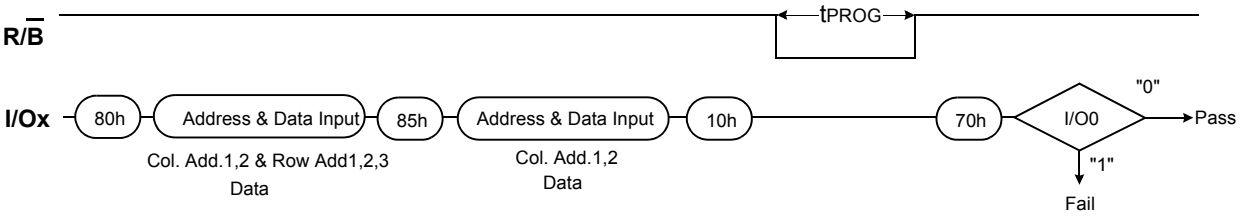


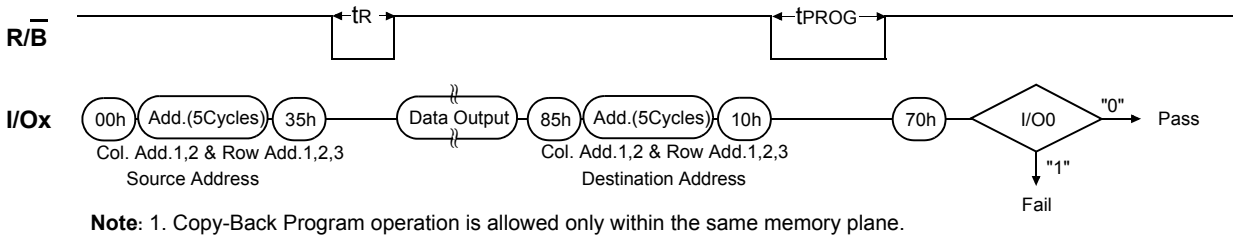
Figure 12. Random Data Input In a Page



COPY-BACK PROGRAM

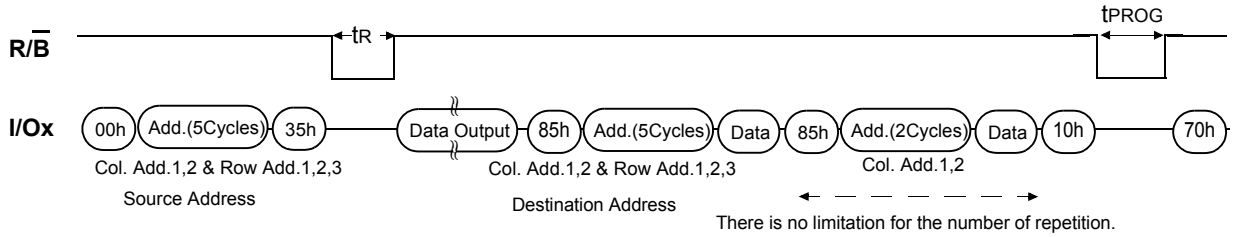
Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data re-loading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 4,314-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 13 & Figure 14). The command register remains in Read Status command mode until another valid command is written to the command register.
During copy-back program, data modification is possible using random data input command (85h) as shown in Figure14.

Figure 13. Page Copy-Back Program Operation



Note: 1. Copy-Back Program operation is allowed only within the same memory plane.

Figure 14. Page Copy-Back Program Operation with Random Data Input

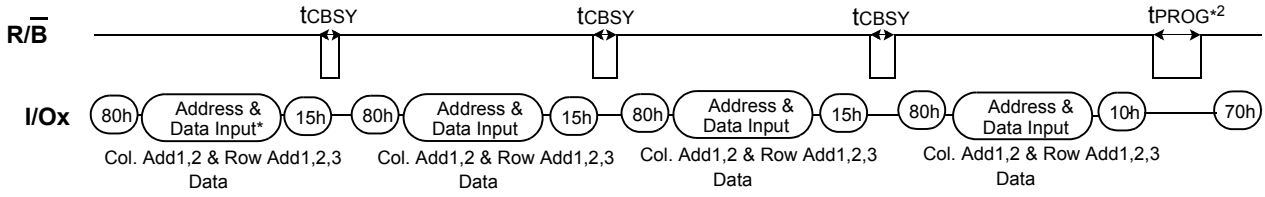


CACHE PROGRAM

Cache Program is an extension of Page Program, which is executed with 4314byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data registers are programmed into memory cell.

After writing the first set of data up to 4314byte into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time(tCBSY) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit(I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit(I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Figure 15. Cache Program(1/2)

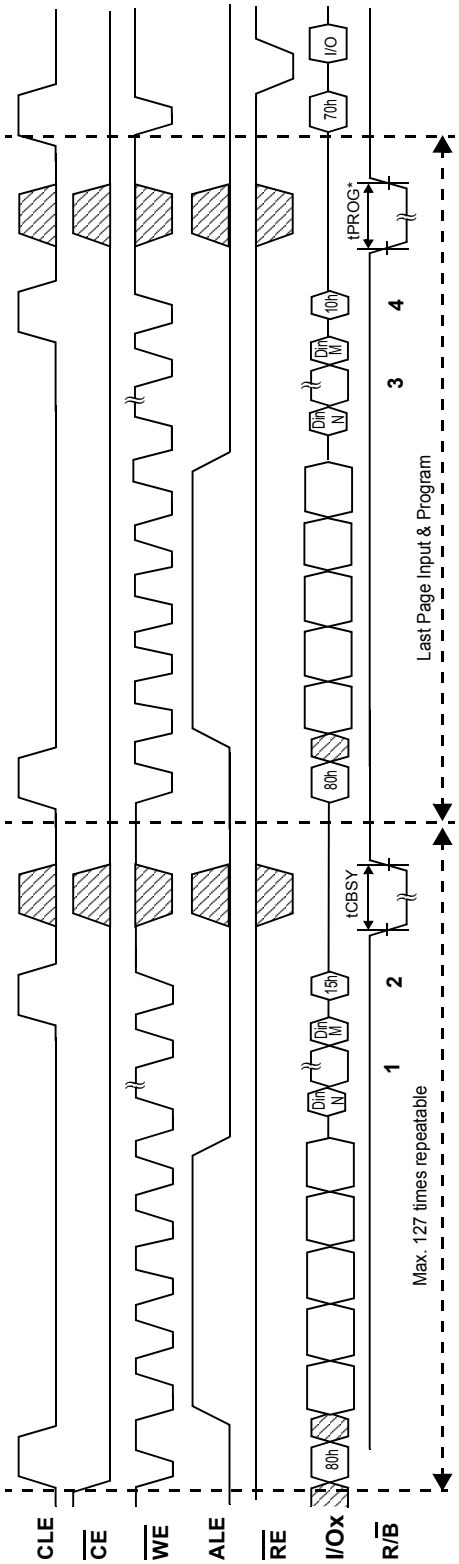


NOTES : 1. Cache Read operation is available only within a block.

2. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG = Program time for the last page + Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

Figure 15. Cache Program(2/2)



NOTE
- Issuing the 15h command to the device after serial data input initiates the program operation with cache registers.
1. Data for Page K is input to cache registers.
2. Data is transferred to the data registers by the 15h command. During the transfer the Ready/Busy outputs Busy State (tCBSY).
3. Data for Page K+1 is input to cache registers while the data of the Page K is being programmed.
4. The programming with cache registers is terminated by the 10h command . When the device becomes Ready, it shows that the internal programming of the Page K+1 is completed.

tPROG* = Program time for the last page + Program time for the (last -1)th page - (command input cycle time + address input cycle time + Last page data loading time)

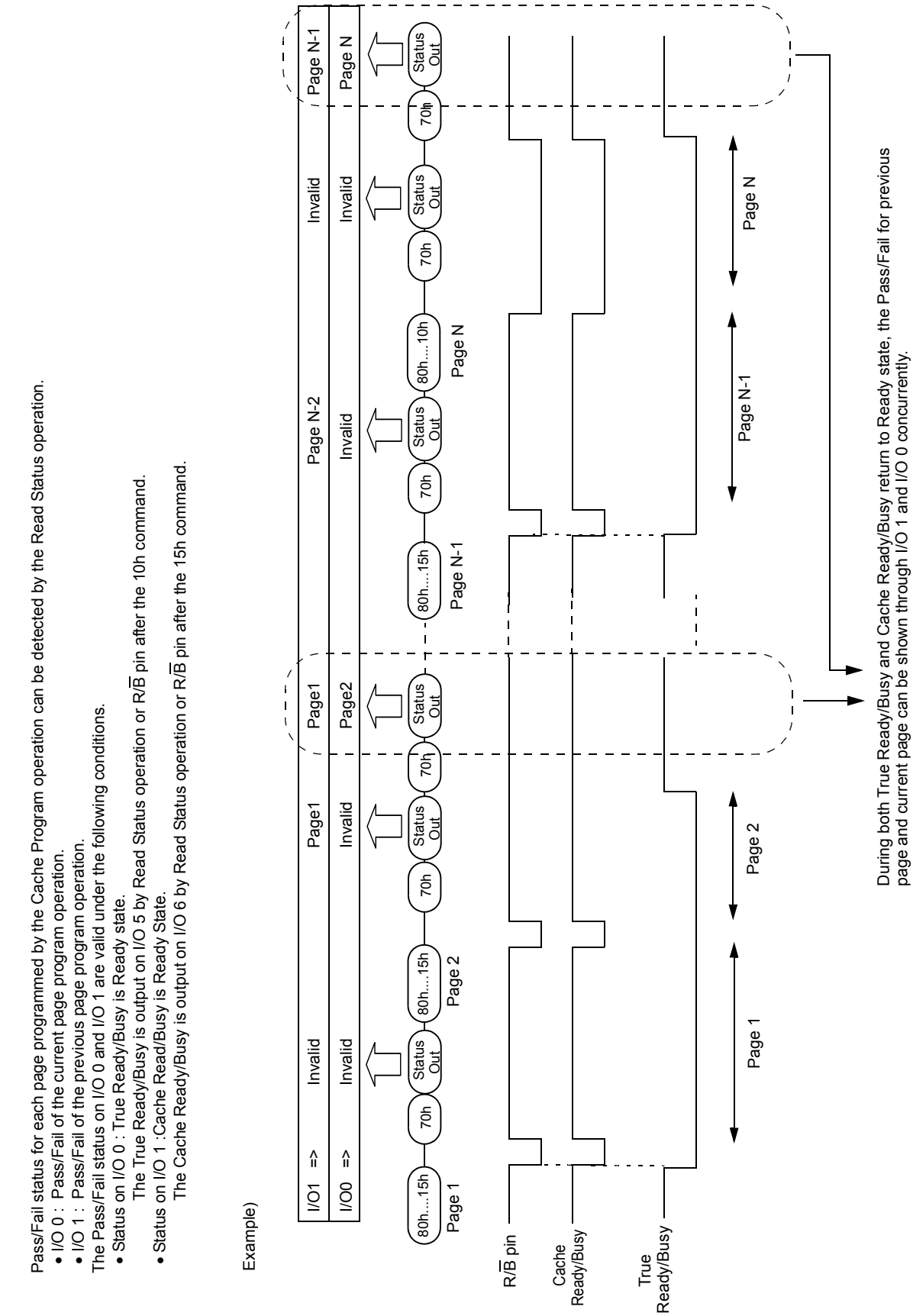
Pass/Fail status for each page programmed by the Cache Program operation can be detected by the Read Status operation.

- I/O 0 : Pass/Fail of the current page program operation.
- I/O 1 : Pass/Fail of the previous page program operation.

The Pass/Fail status on I/O 0 and I/O 1 are valid under the following conditions.

- Status on I/O 0 : True Ready/Busy is Ready state.
  The True Ready/Busy is output on I/O 5 by Read Status operation or R/$\overline{B}$ pin after the 10h command.
- Status on I/O 1 :Cache Read/Busy is Ready State.
  The Cache Ready/Busy is output on I/O 6 by Read Status operation or R/$\overline{B}$ pin after the 15h command.

Example)



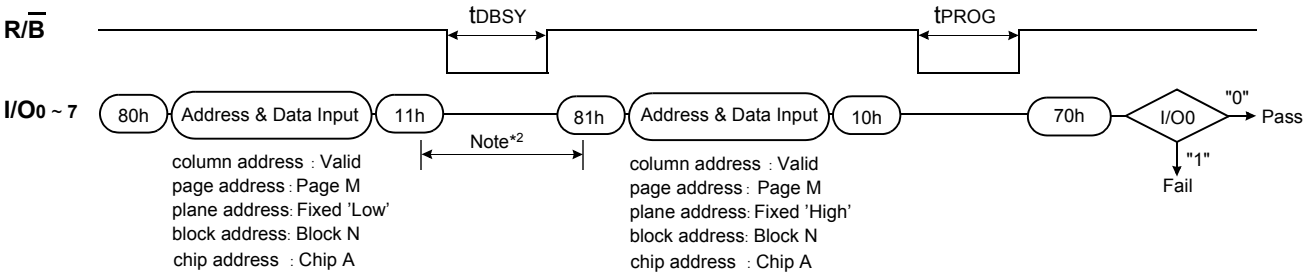
TWO-PLANE PAGE PROGRAM

Two-Plane Page Program is an extension of Page Program, for a single plane with 4,314 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 4,314 byte data registers enables a simultaneous programming of two pages.

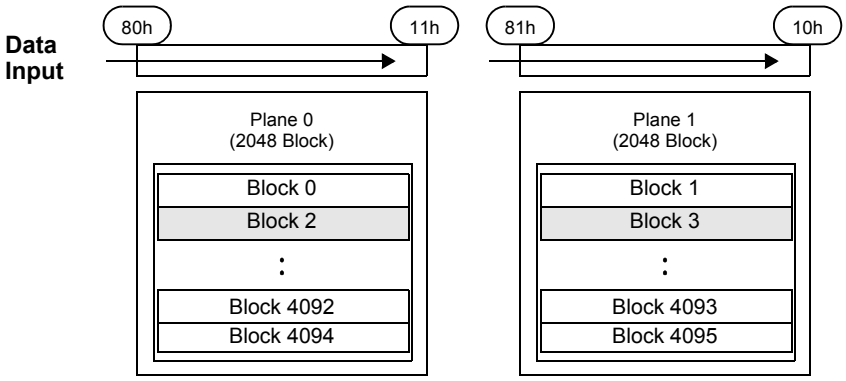
After writing the first set of data up to 4,314 byte into the selected data registers via cache registers, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/$\overline{B}$ remains in Busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to Ready state by polling the Ready/Busy status bit(I/O 6). Then the next set of data for the other plane is inputted after the 81h command and address sequences. After inputting data for the last plane, actual True Page Program(10h) instead of dummy Page Program command (11h) must be followed to start the programming process. The operation of R/$\overline{B}$ and Read Status is the same as that of Page Program. Although two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to "1" when any of the pages fails.

Restriction in addressing with Two-Plane Page Program is shown is Figure16.

Figure 16. Two-Plane Page Program



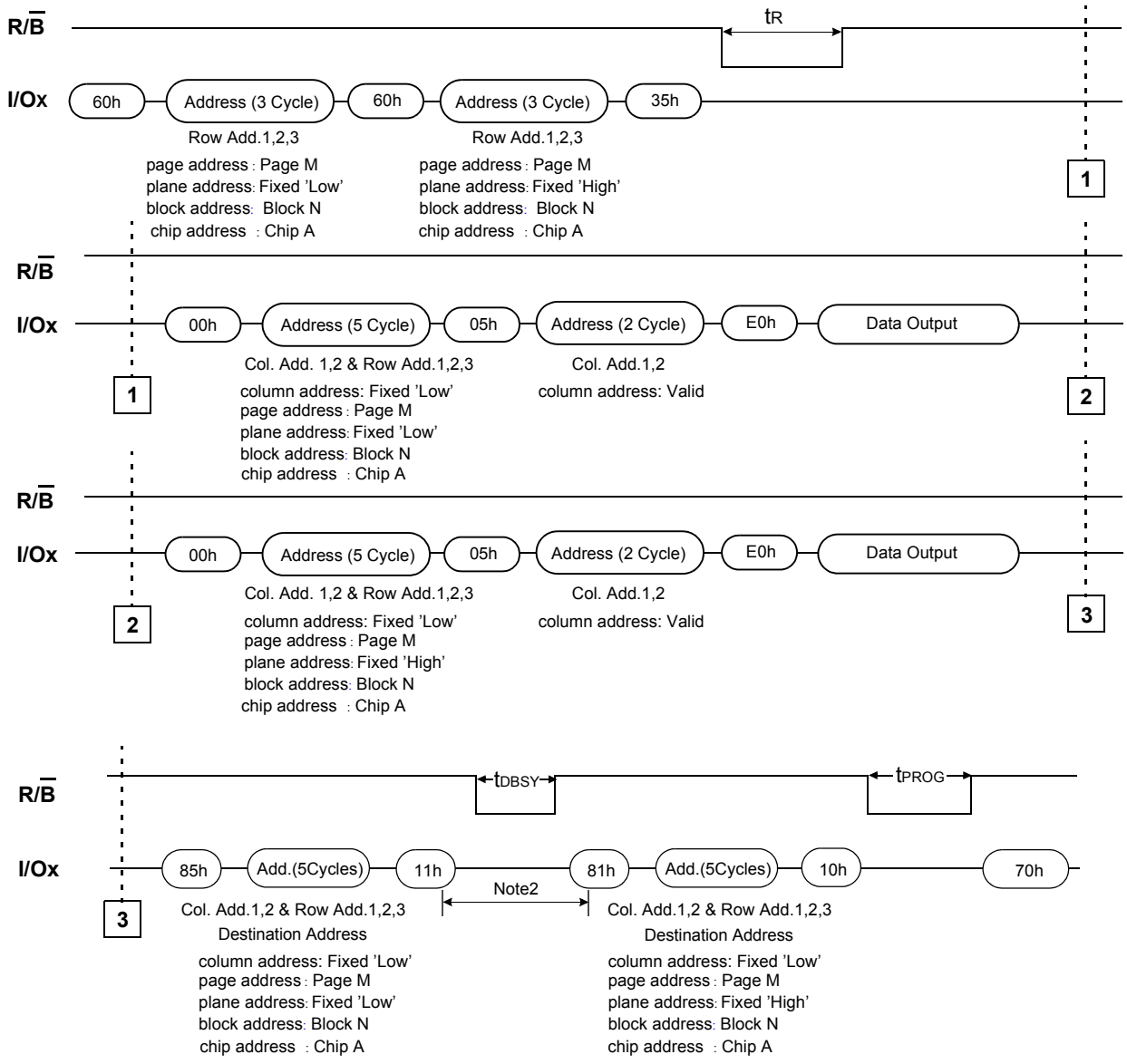
NOTE :1. It is noticeable that same row address except for A_{20} is applied to the two blocks
2. Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

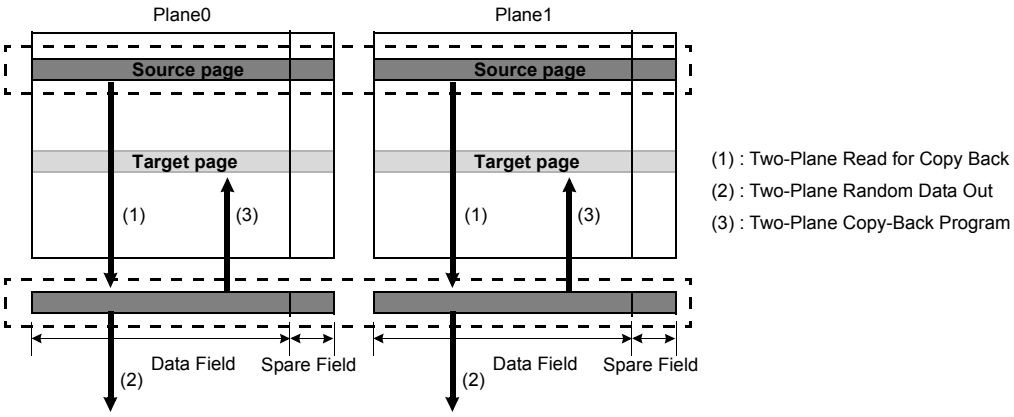


TWO-PLANE COPY-BACK PROGRAM

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 4314 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 4314 byte data registers enables a simultaneous programming of two pages.

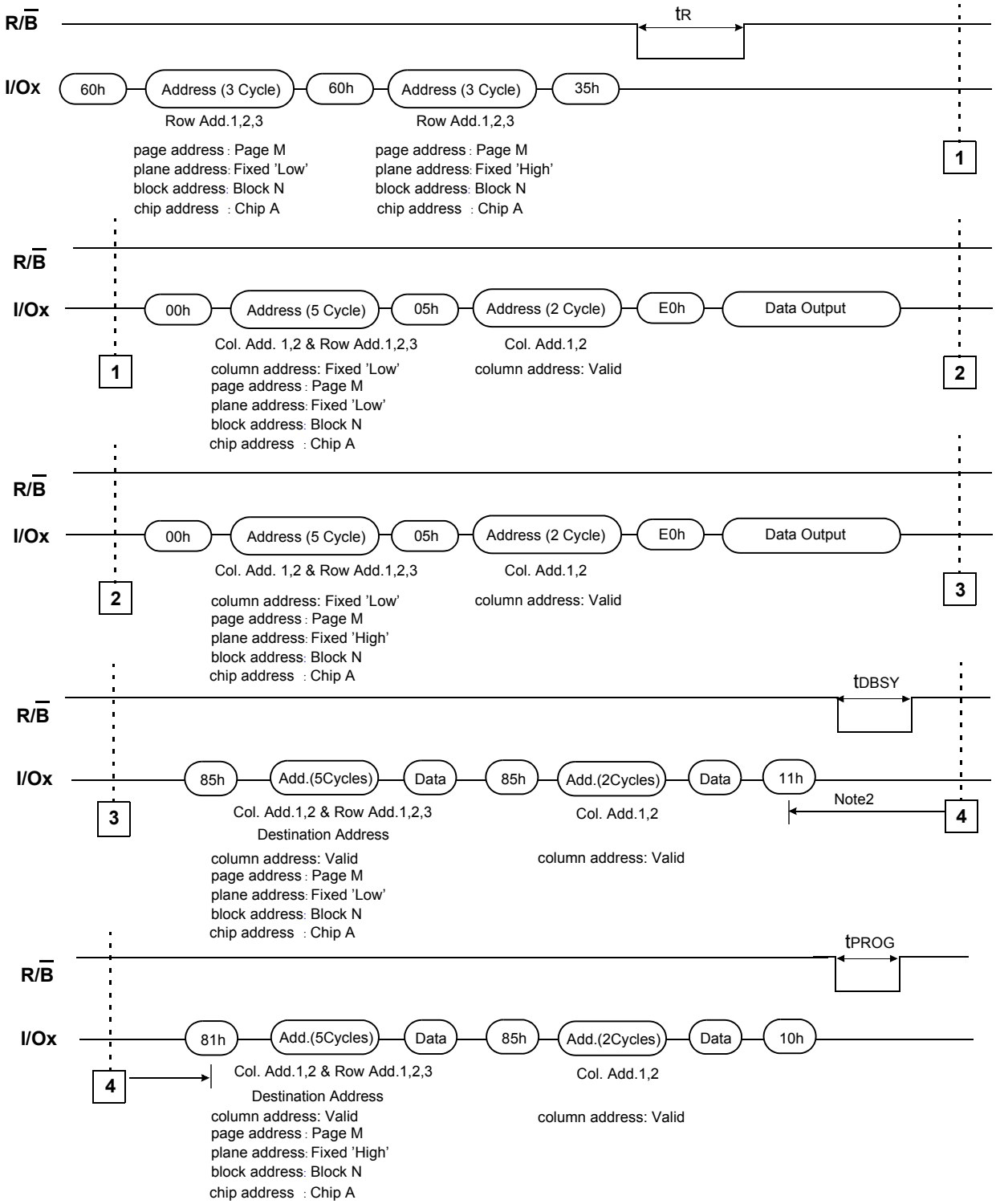
Figure 17. Two-Plane Copy-Back Program Operation





Note: 1. Copy-Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

Figure 18. Two-Plane Copy-Back Program Operation with Random Data Input

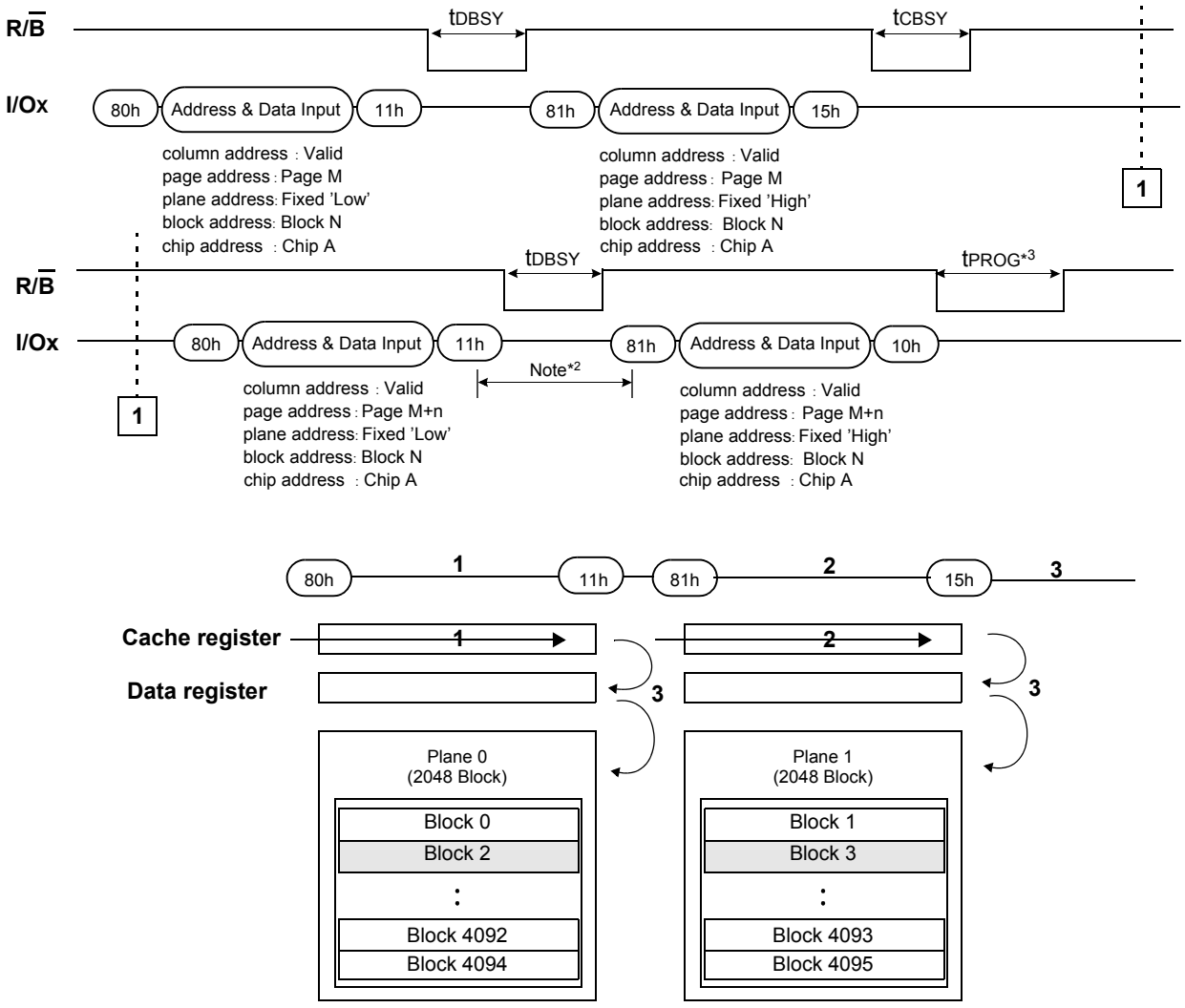


Note: 1. Copy-Back Program operation is allowed only within the same memory plane.
2. Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

TWO-PLANE CACHE PROGRAM

Two-Plane Cache Program is an extension of Cache Program, for a single plane with 4,314 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 4,314 byte data registers enables a simultaneous programming of two pages.

Figure 19. Two-Plane Cache Program Operation



NOTE : **1**. It is noticeable that same row address except for A_{20} is applied to the two blocks

2. Any command between 11h and 81h is prohibited except 70h/F1h/F2h and FFh.

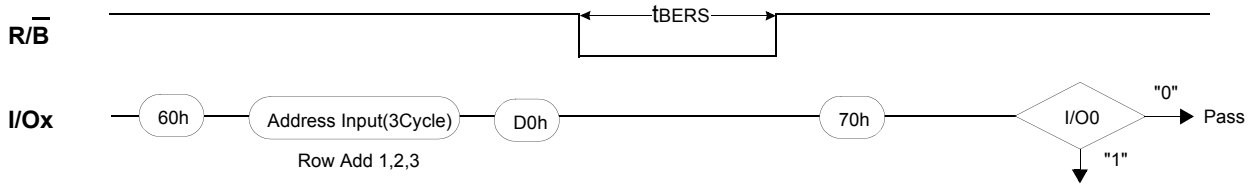
3. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

tPROG = Program time for the last page + Program time for the (last -1)th page
- (Program command cycle time + Last page data loading time)

BLOCK ERASE

The Erase operation is done on a block basis. Block address loading is accomplished in three cycles initiated by an Erase Setup command(60h). Only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 20 details the sequence.

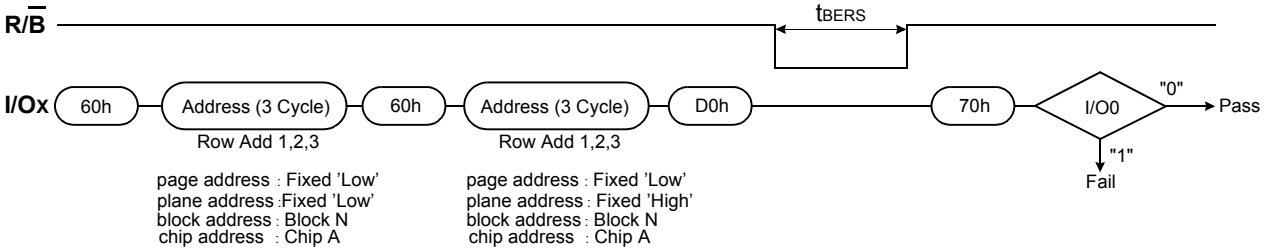
Figure 20. Block Erase Operation



TWO-PLANE BLOCK ERASE

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command(60h) followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command(D0h) initiates the actual erasing process. The completion is detected by monitoring R/$\overline{B}$ pin or Ready/ Busy status bit (I/O 6).

Figure 21. Two-Plane Block Erase Operation



READ STATUS

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h or F1h/F2h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific 70h Status Register definitions and table 3 for specific F1h Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

Table 2. Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 1	Not Use	Not Use	Pass/Fail(N-1)	Not Use	Not Use	Pass : "0" Fail : "1"
I/O 2	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 3	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	True Ready/Busy	Not Use	True Ready/Busy	Busy : "0" Ready : "1"
I/O 6	Ready/Busy	Ready/Busy	Cache Ready/Busy	Ready/Busy	Cache Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.
2. N : current page, N-1: previous page.

Table 3. F1h/F2h Read Status Register Definition

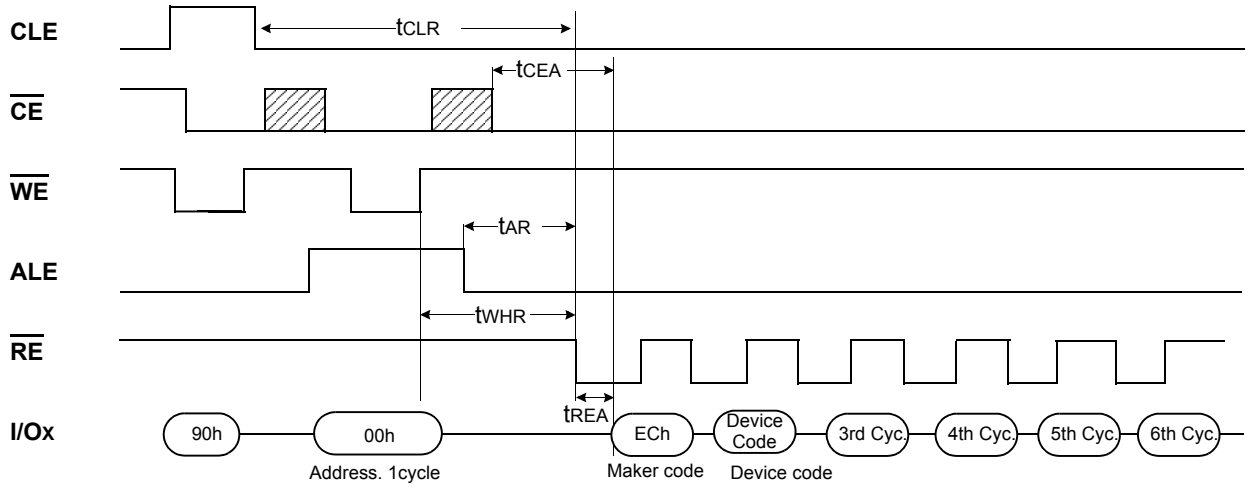
I/O No.	Page Program	Block Erase	Read	Definition
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 3	Not Use	Not Use	Not Use	Don't -cared
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE : 1. I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

READ ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Six read cycles sequentially output the manufacturer code(ECh), the device code, 3rd, 4th, 5th and 6th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence.

Figure 22. Read ID Operation



Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
K9LBG08U0D	D7h	D5h	29h	38h	41h
K9HCG08U1D	Same as K9LBG08U0D in it				
K9XDG08U5D					

RESET

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when $\overline{WP}$ is high. Refer to Table 4 for device status after reset operation. If the device is already in reset state a new reset command will be accepted by the command register. The R/$\overline{B}$ pin changes to low for tRST after the Reset command is written. Refer to Figure 23 below.

Figure 23. RESET Operation

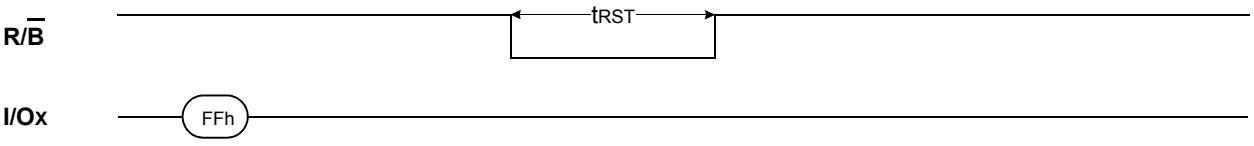


Table 4. Device Status

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

Table 5. Paired Page Address Information

Paired Page Address		Paired Page Address	
00h	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

Note: When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged(Table 5).

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. Because pull-up resistor value is related to tr(R/$\overline{B}$) and current drain during busy(ibusy) , an appropriate value can be obtained with the following reference chart(Fig.24). Its value can be determined by the following guidance.

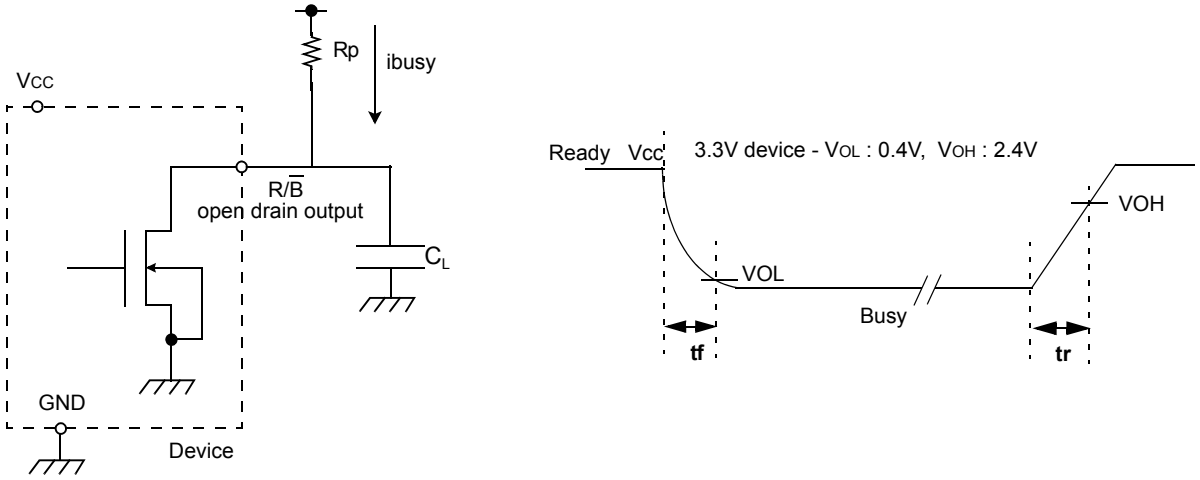
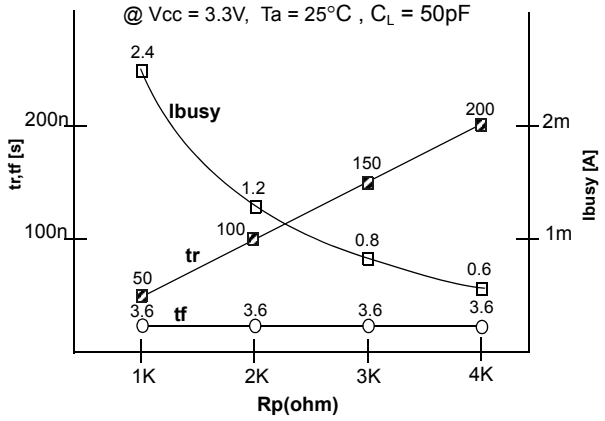


Figure 24. Rp vs tr ,tf & Rp vs ibusy



Rp value guidance

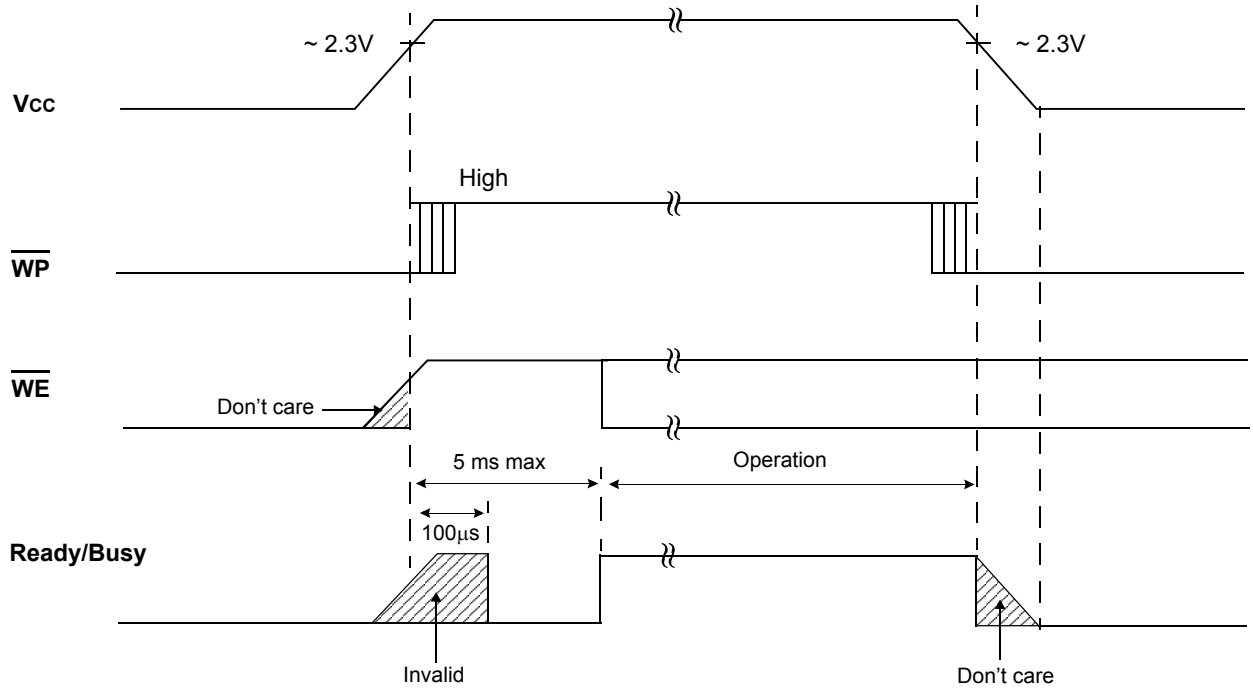
$$Rp(min, 3.3V part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

DATA PROTECTION & POWER UP SEQUENCE

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure 25. In this time period, the acceptable command is 70h(F1h/F2h).
The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2V(3.3V device). $\overline{WP}$ pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. The two step command sequence for program/erase provides additional software protection.

Figure 25. AC Waveforms for Power Transition



Note :During the initialization, the device consumes a maximum current of 30mA ($I_{CC}1$)

$\overline{WP}$ AC Timing guide

Enabling $\overline{WP}$ during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Figure B-1. Program Operation

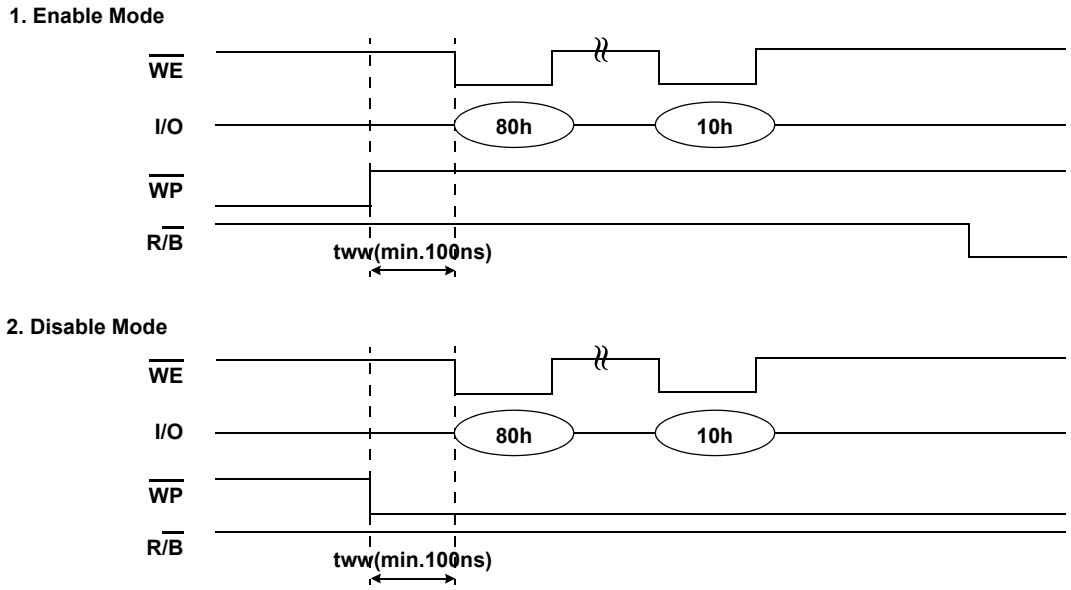


Figure B-2. Erase Operation