

# Kinetis KL27 With Up To 256 KB Flash

## 48 MHz Cortex-M0+ Based Microcontroller

Supports ultra low power ARM based microcontroller with crystal-less USB feature. Ideal solution for smart phone accessories, gaming accessories, sensor hub applications, etc.

The products offers:

- 32KB SRAM for massive data processing
- Ultra low dynamic and static power consumption with smart peripherals for low power applications
- FlexIO for flexible and high performance serial interfaces
- Highly integrated peripherals, including new boot ROM and high accurate internal voltage reference, etc.
- USB FS 2.0 feature without needs of external crystal

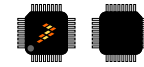
**MKL27Z128Vxx4**  
**MKL27Z256Vxx4**



32 QFN  
5 mm x 5 mm x 0.65 mm  
Pitch 0.5 mm



48 QFN  
7 mm x 7 mm x 0.65 mm  
Pitch 0.5 mm



64 LQFP  
10 mm x 10 mm x 1.4 mm  
Pitch 0.5 mm



64 BGA  
5 mm x 5 mm x 1.23 mm  
Pitch 0.5 mm

### Core

- ARM® Cortex®-M0+ core up to 48 MHz

### Memories

- Up to 256 KB program flash memory
- Up to 32 KB SRAM
- 16 KB ROM with build-in bootloader
- 32 Byte Register File

### System peripherals

- 4-channel DMA controller
- Watchdog
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

### Clocks

- 48 MHz high accuracy internal reference clock
- 32–40 kHz, or 3–32 MHz crystal oscillator
- 1 kHz LPO clock
- 8/2 MHz IRC

### Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

### Human-machine interface

- General-purpose input/output up to 50

### Communication interfaces

- USB full-speed slave controller with on-chip transceiver and 5 V to 3.3 V regulator, supporting crystal-less recovery
- Two 16-bit SPI modules
- One UART module supporting ISO7816
- Two LPUART modules
- Two I2C modules supporting up to 1 Mbit/s
- One I2S (SAI) module
- One FlexIO module

### Analog Modules

- 16-bit, 16-channel SAR ADC with internal voltage reference
- High-speed analog comparator containing a 6-bit DAC and programmable reference input
- One 12-bit DAC
- 1.2 V voltage reference (Vref)

### Timers

- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

### Security and integrity modules

- 80-bit unique identification number per chip

### Ordering Information

Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKL27Z128VFM4	128	32	23
MKL27Z256VFM4	256	32	23
MKL27Z128VFT4	128	32	36
MKL27Z256VFT4	256	32	36
MKL27Z128VMP4	128	32	50
MKL27Z256VMP4	256	32	50
MKL27Z128VLH4	128	32	50
MKL27Z256VLH4	256	32	50

### Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	<a href="#">Solution Advisor</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KLX7PB <sup>1</sup>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL27P64M48SF6RM <sup>1</sup>
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	<sup>1</sup>
Package drawing	Package dimensions are provided in package drawings.	64-LQFP: <sup>1</sup> 64 MAPBGA: <sup>1</sup> 32 QFN: <sup>1</sup> 48 QFN: <sup>1</sup>

1. To find the associated resource, go to <http://www.freescale.com> and perform a search using this term.

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# 1 Ratings

## 1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

Table 4. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	120	mA
$V_{IO}$	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
$V_{USB\_DP}$	USB_DP input voltage	-0.3	3.63	V
$V_{USB\_DM}$	USB_DM input voltage	-0.3	3.63	V
$V_{REGIN}$	USB regulator input	-0.3	6.0	V

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

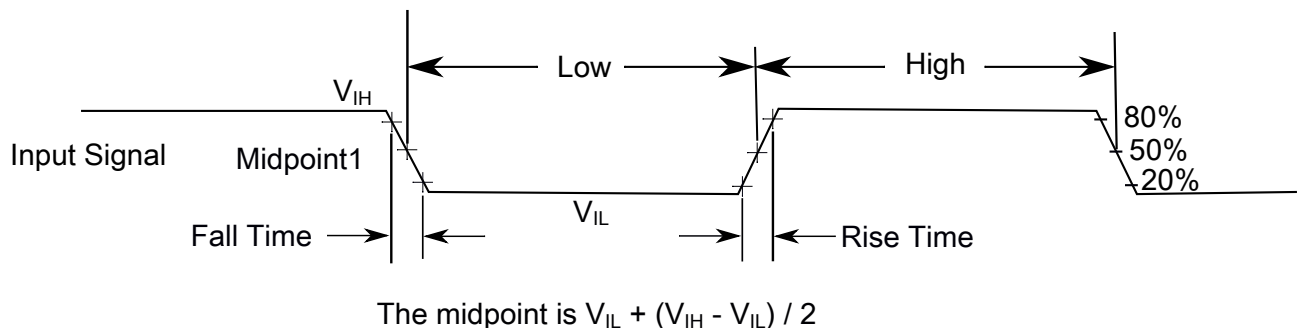


Figure 1. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

## 2.2 Nonswitching electrical specifications

### 2.2.1 Voltage and current operating requirements

Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{IH}$	Input high voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	$0.7 \times V_{DD}$ $0.75 \times V_{DD}$	— —	V V	
$V_{IL}$	Input low voltage <ul style="list-style-type: none"> <li><math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math></li> <li><math>1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math></li> </ul>	— —	$0.35 \times V_{DD}$ $0.3 \times V_{DD}$	V V	
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{ICIO}$	IO pin negative DC injection current — single pin <ul style="list-style-type: none"> <li><math>V_{IN} &lt; V_{SS}-0.3\text{V}</math></li> </ul>	-3	—	mA	1
$I_{ICcont}$	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>Negative current injection</li> </ul>	-25	—	mA	
$V_{ODPU}$	Open drain pullup voltage level	$V_{DD}$	$V_{DD}$	V	2
$V_{RAM}$	$V_{DD}$ voltage required to retain RAM	1.2	—	V	

- All I/O pins are internally clamped to  $V_{SS}$  through a ESD protection diode. There is no diode connection to  $V_{DD}$ . If  $V_{IN}$  greater than  $V_{IO\_MIN}$  ( $= V_{SS}-0.3\text{ V}$ ) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{ICIO}|$ .
- Open drain outputs must be pulled to  $V_{DD}$ .

### 2.2.2 LVD and POR operating requirements

Table 6.  $V_{DD}$  supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{POR}$	Falling $V_{DD}$ POR detect voltage	0.8	1.1	1.5	V	—

Table continues on the next page...

**Table 6. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
V <sub>LVW1H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV = 00)</li> <li>• Level 2 falling (LVWV = 01)</li> <li>• Level 3 falling (LVWV = 10)</li> <li>• Level 4 falling (LVWV = 11)</li> </ul>	2.62	2.70	2.78	V	1
V <sub>LVW2H</sub>		2.72	2.80	2.88	V	
V <sub>LVW3H</sub>		2.82	2.90	2.98	V	
V <sub>LVW4H</sub>		2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV = 00)</li> <li>• Level 2 falling (LVWV = 01)</li> <li>• Level 3 falling (LVWV = 10)</li> <li>• Level 4 falling (LVWV = 11)</li> </ul>	1.74	1.80	1.86	V	1
V <sub>LVW2L</sub>		1.84	1.90	1.96	V	
V <sub>LVW3L</sub>		1.94	2.00	2.06	V	
V <sub>LVW4L</sub>		2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	—
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

1. Rising thresholds are falling threshold + hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 7. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — Normal drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -5 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -1.5 mA</li> </ul>	V <sub>DD</sub> - 0.5	—	V	1
		V <sub>DD</sub> - 0.5	—	V	
V <sub>OH</sub>	Output high voltage — High drive pad <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V, I<sub>OH</sub> = -18 mA</li> <li>• 1.71 V ≤ V<sub>DD</sub> ≤ 2.7 V, I<sub>OH</sub> = -6 mA</li> </ul>	V <sub>DD</sub> - 0.5	—	V	1
		V <sub>DD</sub> - 0.5	—	V	
I <sub>OHT</sub>	Output high current total for all ports	—	100	mA	
V <sub>OL</sub>	Output low voltage — Normal drive pad	—	0.5	V	1

Table continues on the next page...

**Table 7. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 1.5\text{ mA}</math></li> </ul>	—	0.5	V	
$V_{OL}$	Output low voltage — High drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 18\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 6\text{ mA}</math></li> </ul>	—	0.5	V	1
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range	—	1	$\mu\text{A}$	2
$I_{IN}$	Input leakage current (per pin) at 25 °C	—	0.025	$\mu\text{A}$	2
$I_{IN}$	Input leakage current (total all pins) for full temperature range	—		$\mu\text{A}$	2
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	20	50	k $\Omega$	3

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at  $V_{DD} = 3.6\text{ V}$
3. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$

## 2.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $VLLSx \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

**Table 8. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{POR}$	After a POR event, amount of time from the point $V_{DD}$ reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	$\mu\text{s}$	
	<ul style="list-style-type: none"> <li>• <math>VLLS0 \rightarrow \text{RUN}</math></li> </ul>	—	152	166	$\mu\text{s}$	
	<ul style="list-style-type: none"> <li>• <math>VLLS1 \rightarrow \text{RUN}</math></li> </ul>	—	152	166	$\mu\text{s}$	

Table continues on the next page...



**Table 8. Power mode transition operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS3 → RUN	—	93	104	μs	
	• LLS → RUN	—	7.5	8	μs	
	• VLPS → RUN	—	7.5	8	μs	
	• STOP → RUN	—	7.5	8	μs	

## 2.2.5 Power consumption operating behaviors

### NOTE

The while (1) test is executed with flash cache enabled.

**Table 9. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	2
I <sub>DD_RUNCO</sub>	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	—	5.76 6.04	6.40 6.68	mA	3
I <sub>DD_RUNCO</sub>	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	—	3.21 3.49	3.85 4.13	mA	—
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	— —	6.45 6.75	7.09 7.39	mA	3
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>• at 25 °C</li> <li>• at 105 °C</li> </ul>	— —	3.95 4.23	4.59 4.87	mA mA	3,

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.68 2.96	3.32 3.60	mA	3
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock enable 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	8.08 8.39	8.72 9.03	mA	3
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in flash all peripheral clock disable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	3.90 4.21	4.54 4.85	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in Flash all peripheral clock disable, 24 MHz core/12 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.66 2.94	3.30 3.58	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock disable, 12 MHz core/6 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	2.03 2.31	2.67 2.95	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, Running While(1) loop in Flash all peripheral clock enable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	5.52 5.83	6.16 6.47	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock disable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>	—	5.29 5.56	5.93 6.20	mA	
I <sub>DD_RUN</sub>	Run mode current—48M HIRC mode, running While(1) loop in SRAM all peripheral clock enable, 48 MHz core/24 MHz flash, V <sub>DD</sub> = 3.0 V	—	6.91	7.55	mA	

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
	<ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 105 °C</li> </ul>		7.19	7.91		
I <sub>DD_VLPRCO</sub>	Very Low Power Run Core Mark in Flash in Compute Operation mode: Core@4MHz, Flash @1MHz, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	826	907	μA	
I <sub>DD_VLPRCO</sub>	Very-low-power-run While(1) loop in SRAM in compute operation mode— 8 MHz LIRC mode, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	405	486	μA	
I <sub>DD_VLPRCO</sub>	Very-low-power run While(1) loop in SRAM in compute operation mode:—2 MHz LIRC mode, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	154	235	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	108	189	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 2 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	39	120	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock disable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	249	330	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in flash all peripheral clock enable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	337	418	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	416	497	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current— 8 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 4 MHz core / 1 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	494	575	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM in all peripheral clock disable, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V	—	166	247	μA	

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
	<ul style="list-style-type: none"> <li>at 25 °C</li> </ul>					
I <sub>DD_VLPR</sub>	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock disable, 125 kHz core / 31.25 kHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	50	131	μA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V <sub>DD</sub> = 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> </ul>	—	208	289	μA	
I <sub>DD_WAIT</sub>	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V <sub>DD</sub> = 3.0 V	—	1.81	2.12	mA	
I <sub>DD_WAIT</sub>	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V <sub>DD</sub> = 3.0 V	—	1.22	1.84	mA	
I <sub>DD_VLPW</sub>	Very-low-power run wait current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V	—	172	222	μA	
I <sub>DD_VLPW</sub>	Very-low-power run wait current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V	—	69	105	μA	
I <sub>DD_VLPW</sub>	Very-low-power run wait current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V <sub>DD</sub> = 3.0 V	—	36	76	μA	
I <sub>DD_PSTOP2</sub>	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V <sub>DD</sub> = 3.0 V	—	1.81	2.06	mA	
I <sub>DD_PSTOP2</sub>	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V <sub>DD</sub> = 3.0 V	—	1.00	1.25	mA	
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	161.93	181.50	μA	—
		—	181.45	206.95		
		—	236.29	315.62		
		—	390.33	525.63		
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> </ul>	—	3.31	6.32	μA	—
		—	10.43	26.39		
		—	34.14	94.52		

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
	<ul style="list-style-type: none"> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	104.38	219.39		
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	3.21	6.47	μA	—
		—	10.26	26.43		
		—	33.49	93.09		
		—	102.92	216.69		
I <sub>DD_LLS</sub>	Low-leakage stop mode current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	2.06	5.32	μA	—
		—	4.72	9.32		
		—	8.13	14.14		
		—	13.34	25.75		
		—	41.08	59.19		
I <sub>DD_LLS</sub>	Low-leakage stop mode current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	2.46	5.72	μA	
		—	5.12	9.72		
		—	8.53	14.54		
		—	13.74	26.15		
		—	41.48	59.59		
I <sub>DD_LLS</sub>	Low-leakage stop mode current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	2.35	2.99	μA	4
		—	4.91	8.43		
		—	8.32	14.73		
		—	13.44	24.32		
		—	40.47	59.45		
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.45	1.85	μA	—
		—	3.37	4.39		
		—	5.76	10.29		
		—	9.72	16.82		
		—	30.41	41.40		
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> </ul>	—	2.05	2.45	μA	4

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
	<ul style="list-style-type: none"> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	3.97	4.99		
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.96	2.36	μA	4
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	0.66	0.87	nA	—
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.26	1.47	nA	4
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	1.16	1.46	nA	4
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> </ul>	—	352.69	468.91	nA	—
		—	1252.80	1439.94		
		—	2531.05	3241.52		
		—	4400.99	5236.34		

Table continues on the next page...

**Table 9. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max. <sup>1</sup>	Unit	Notes
	<ul style="list-style-type: none"> <li>at 85 °C</li> <li>at 105 °C</li> </ul>		16087.21	21895.19		
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V <ul style="list-style-type: none"> <li>at 25 °C and below</li> <li>at 50 °C</li> <li>at 70 °C</li> <li>at 85 °C</li> <li>at 105 °C</li> </ul>	—	179.60	277.81	nA	—
		—	1086.61	1312.79		
		—	2252.84	2944.26		
		—	4248.16	5096.24		
			15948.78	21726.94		

- The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).
- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- MCG\_Lite configured for HIRC mode. CoreMark benchmark compiled using IAR 7.10 with optimization level high, optimized for balanced.
- RTC uses external 32 kHz crystal as clock source, and the current includes ERCLK32K power consumption.

**Table 10. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IRC8MHz</sub>	8 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 8 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	93	93	93	93	93	93	μA
I <sub>IRC2MHz</sub>	2 MHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 2 MHz IRC enabled, MCG_SC[FCRDIV]=000b, MCG_MC[LIRC_DIV2]=000b.	29	29	29	29	29	29	μA
I <sub>EREFSTEN4MHz</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	224	230	238	245	253	μA
I <sub>EREFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled. <ul style="list-style-type: none"> <li>VLLS1</li> <li>VLLS3</li> <li>LLS</li> <li>VLPS</li> <li>STOP</li> </ul>	440	490	540	560	570	580	nA
		440	490	540	560	570	580	
		490	490	540	560	570	680	
		510	560	560	560	610	680	

Table continues on the next page...

**Table 10. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
		510	560	560	560	610	680	
$I_{LPTMR}$	LPTMR peripheral adder measured by placing the device in VLLS1 mode with LPTMR enabled using LPO.	30	30	30	85	100	200	nA
$I_{CMP}$	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	$\mu$ A
$I_{UART}$	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul>	114 34	114 34	114 34	114 34	114 34	114 34	$\mu$ A
$I_{TPM}$	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. <ul style="list-style-type: none"> <li>• IRC8M (8 MHz internal reference clock)</li> <li>• IRC2M (2 MHz internal reference clock)</li> </ul>	147 42	147 42	147 42	147 42	147 42	147 42	$\mu$ A
$I_{BG}$	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	$\mu$ A
$I_{ADC}$	ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low power	330	330	330	330	330	330	$\mu$ A



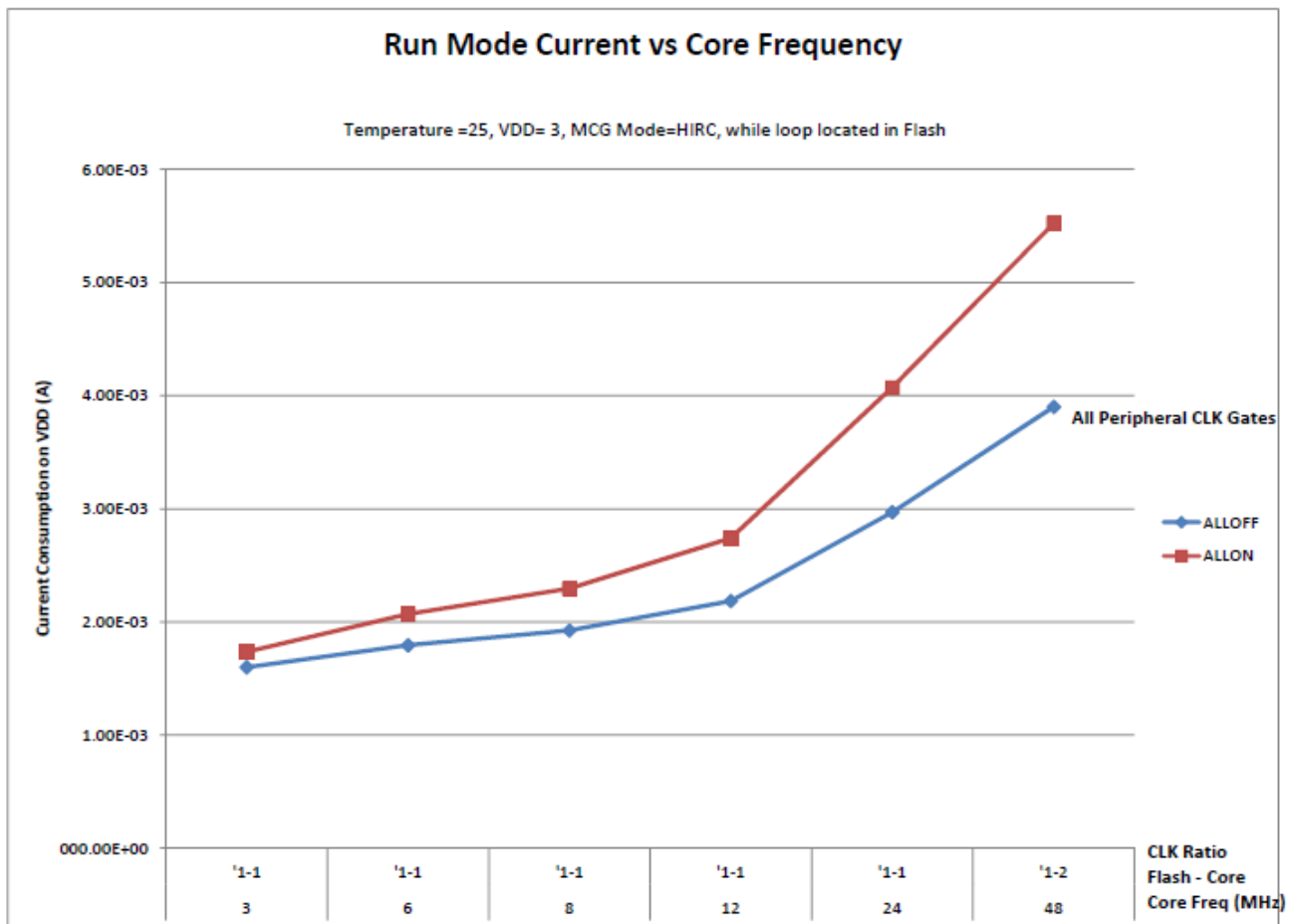
**Table 10. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
	mode using the internal clock and continuous conversions.							

**2.2.5.1 Diagram: Typical IDD\_RUN operating behavior**

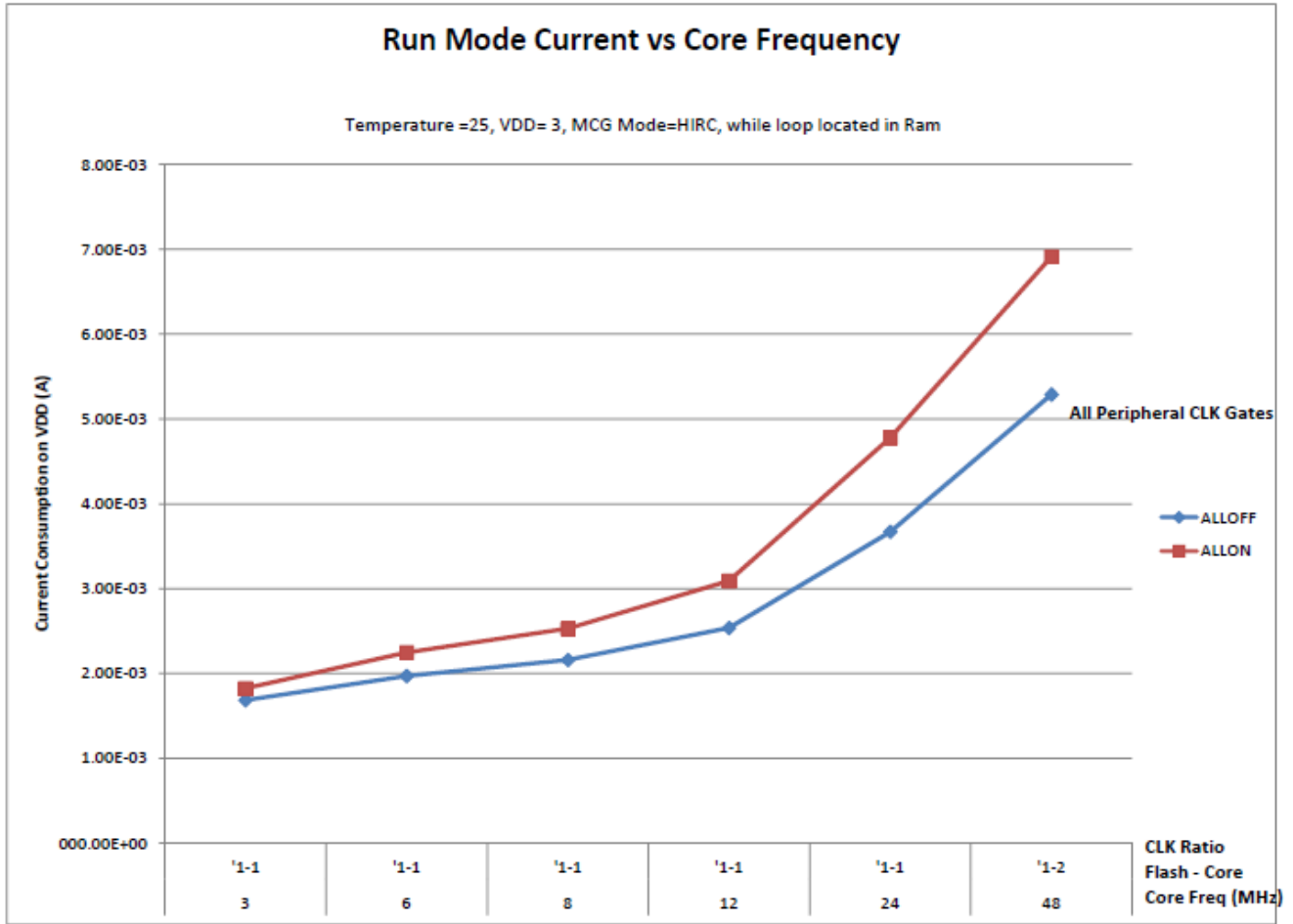
The following data was measured under these conditions:

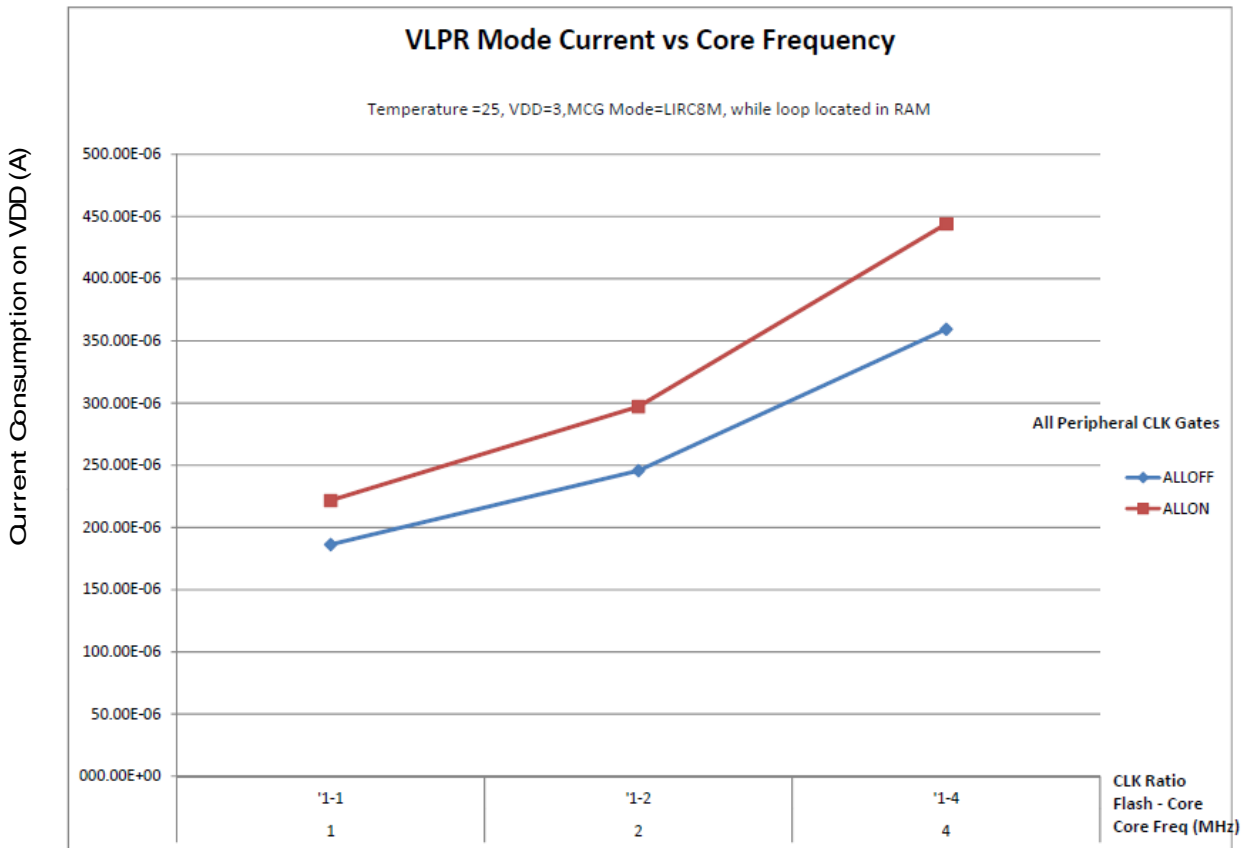
- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 2. Run mode supply current vs. core frequency**

General





**Figure 3. VLPR mode current vs. core frequency**

## 2.2.6 EMC radiated emissions operating behaviors

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

Table 11. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN}$	Input capacitance	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

Table 12. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
$f_{SYS}$	System and core clock	—	48	MHz
$f_{BUS}$	Bus clock	—	24	MHz
$f_{FLASH}$	Flash clock	—	24	MHz
$f_{SYS\_USB}$	System and core clock when Full Speed USB in operation	20	—	MHz
$f_{LPTMR}$	LPTMR clock	—	24	MHz
VLPR and VLPS modes <sup>1</sup>				
$f_{SYS}$	System and core clock	—	4	MHz
$f_{BUS}$	Bus clock	—	1	MHz
$f_{FLASH}$	Flash clock	—	1	MHz
$f_{LPTMR}$	LPTMR clock <sup>2</sup>	—	24	MHz
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
$f_{TPM}$	TPM asynchronous clock	—	8	MHz
$f_{UART0}$	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

### 2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 13. General switching specifications**

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 14. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

### 2.4.2 Thermal attributes

**Table 15. Thermal attributes**

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPBG A	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	°C/W	

Table continues on the next page...

**Table 15. Thermal attributes (continued)**

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPBG A	Unit	Notes
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	°C/W	4
—	$\Psi_{JB}$	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
5. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

## 3 Peripheral operating requirements and behaviors

### 3.1 Core modules

#### 3.1.1 SWD electricals

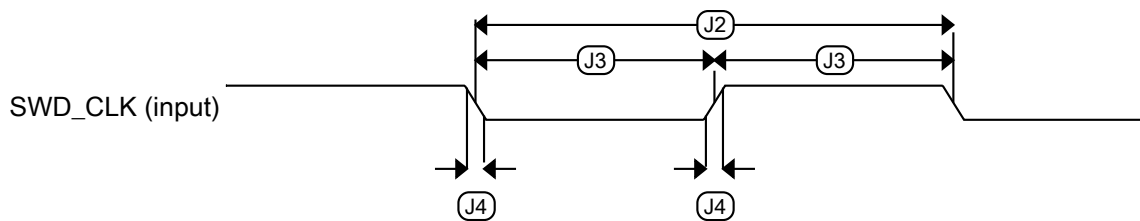
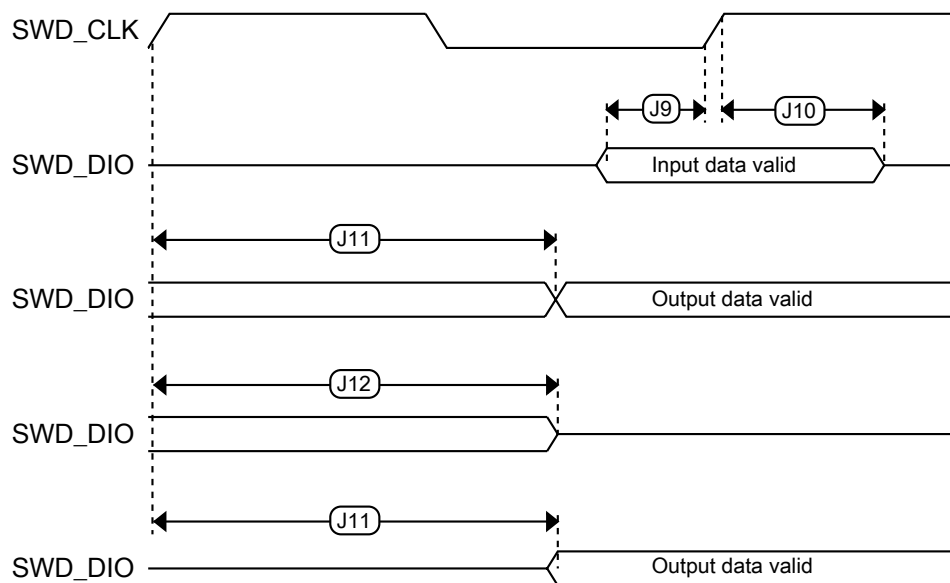
**Table 16. SWD full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>• Serial wire debug</li> </ul>	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns

Table continues on the next page...

**Table 16. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

**Figure 4. Serial wire clock input timing****Figure 5. Serial wire data timing**

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG-Lite specifications

**Table 17. IRC48M specification**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	—
T	Temperature range	-40	—	125	°C	—
$I_{DD}$	Supply current	—	400	500	μA	—
$f_{IRC}$	Output frequency	—	48	—	MHz	—
$f_{IRC\_UT}$	Output frequency range (untrimmed)	—	±10	±25	% $f_{IRC}$	—
$f_{IRC\_T}$	Output frequency range (trimmed)	—	±0.5	±1.0	% $f_{IRC}$	—
$\Delta f_{IRC\_C}$	Coarse trim resolution	±0.5	±0.7	±1	%	—
$\Delta f_{IRC\_F}$	Fine trim resolution	±0.03	±0.04	±0.05	%	—
$T_j$	Period jitter (RMS)	—	35	150	ps	—
$T_{su}$	Startup time	—	2	3	μs	—

**Table 18. IRC8M/2M specification**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.08	—	1.47	V	—
T	Temperature range	-40	—	125	°C	—
$I_{DD\_2M}$	Supply current in 2 MHz mode	—	14	17	μA	—
$I_{DD\_8M}$	Supply current in 8 MHz mode	—	30	35	μA	—
$f_{IRC\_2M}$	Output frequency	—	2	—	MHz	—
$f_{IRC\_8M}$	Output frequency	—	8	—	MHz	—
$f_{IRC\_T\_2M}$	Output frequency range (trimmed)	—	—	±3	% $f_{IRC}$	$V_{DD} \geq 1.89$ V
$f_{IRC\_T\_8M}$	Output frequency range (trimmed)	—	—	±3	% $f_{IRC}$	$V_{DD} \geq 1.89$ V
$T_{su\_2M}$	Startup time	—	—	12.5	μs	—
$T_{su\_8M}$	Startup time	—	—	12.5	μs	—

### 3.3.2 Oscillator electrical specifications



### 3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I <sub>DDOSC</sub>	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	μA	1
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C <sub>x</sub>	EXTAL load capacitance	—	—	—		2, 3
C <sub>y</sub>	XTAL load capacitance	—	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	

Table continues on the next page...

**Table 19. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub>, C<sub>y</sub> can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 3.3.2.2 Oscillator frequency specifications

**Table 20. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	
t <sub>cst</sub>	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 21. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvpgm4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk128k}$	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 3.4.1.2 Flash timing specifications — commands

**Table 22. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk128k}$	Read 1s Block execution time • 128 KB program flash	—	—	1.7	ms	—
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu$ s	1
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	—
$t_{ersblk128k}$	Erase Flash Block execution time • 128 KB program flash	—	88	600	ms	2
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	—
$t_{rdonce}$	Read Once execution time	—	—	25	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	$\mu$ s	—

Table continues on the next page...

**Table 22. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{ersall}$	Erase All Blocks execution time	—	175	1300	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	175	1300	ms	2

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

**Table 23. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DD\_PGM}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{DD\_ERS}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 3.4.1.4 Reliability specifications

**Table 24. NVM reliability specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ .

## 3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 3.6 Analog

### 3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADC<sub>x</sub>\_DP0, ADC<sub>x</sub>\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 3.6.1.1 16-bit ADC operating conditions

**Table 25. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>ADIN</sub>	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	VREFL	—	31/32 * VREFH	V	—
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	—	8	10	pF	—
R <sub>ADIN</sub>	Input series resistance		—	2	5	kΩ	—
R <sub>AS</sub>	Analog source resistance (external)	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	18.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C <sub>rate</sub>	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C <sub>rate</sub>	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V<sub>DDA</sub> = 3.0 V, Temp = 25 °C, f<sub>ADCK</sub> = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.

## Peripheral operating requirements and behaviors

- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 8 \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1$  ns.
- To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
- For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

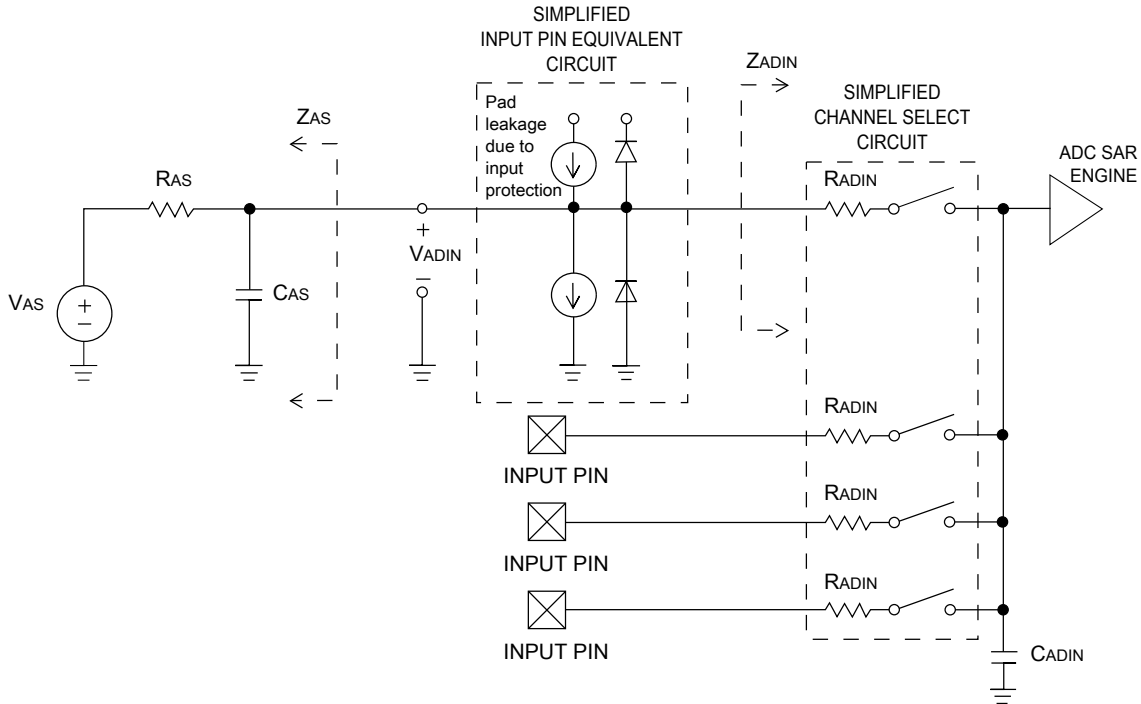


Figure 6. ADC input impedance equivalency diagram

### 3.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					

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**Table 26. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

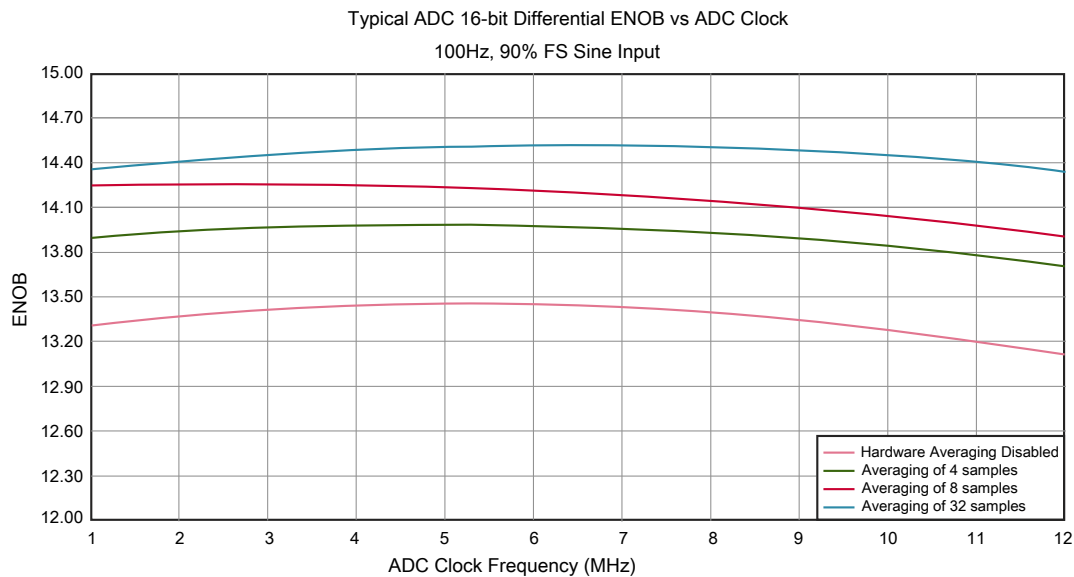
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±4	±6.8	LSB <sup>4</sup>	5
DNL	Differential non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±0.7	-1.1 to +1.9	LSB <sup>4</sup>	5
			—	±0.2	-0.3 to 0.5		
INL	Integral non-linearity	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±1.0	-2.7 to +1.9	LSB <sup>4</sup>	5
			—	±0.5	-0.7 to +0.5		
E <sub>FS</sub>	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	-4	-5.4	LSB <sup>4</sup>	V <sub>ADIN</sub> = V <sub>DDA</sub> <sup>5</sup>
E <sub>Q</sub>	Quantization error	<ul style="list-style-type: none"> <li>16-bit modes</li> <li>≤13-bit modes</li> </ul>	—	-1 to 0	—	LSB <sup>4</sup>	
			—	—	±0.5		
ENOB	Effective number of bits	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> <li>Avg = 4</li> </ul>	12.8 11.9	14.5 13.8	— —	bits bits	6
			12.2 11.4	13.9 13.1	— —	bits bits	
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	—	-94	—	dB	7
			—	-85	—	dB	
SFDR	Spurious free dynamic range	16-bit differential mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul> 16-bit single-ended mode <ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	82 78	95 90	— —	dB dB	7
E <sub>IL</sub>	Input leakage error		I <sub>in</sub> × R <sub>AS</sub>			mV	I <sub>in</sub> = leakage current (refer to the MCU's voltage and

Table continues on the next page...

**Table 26. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

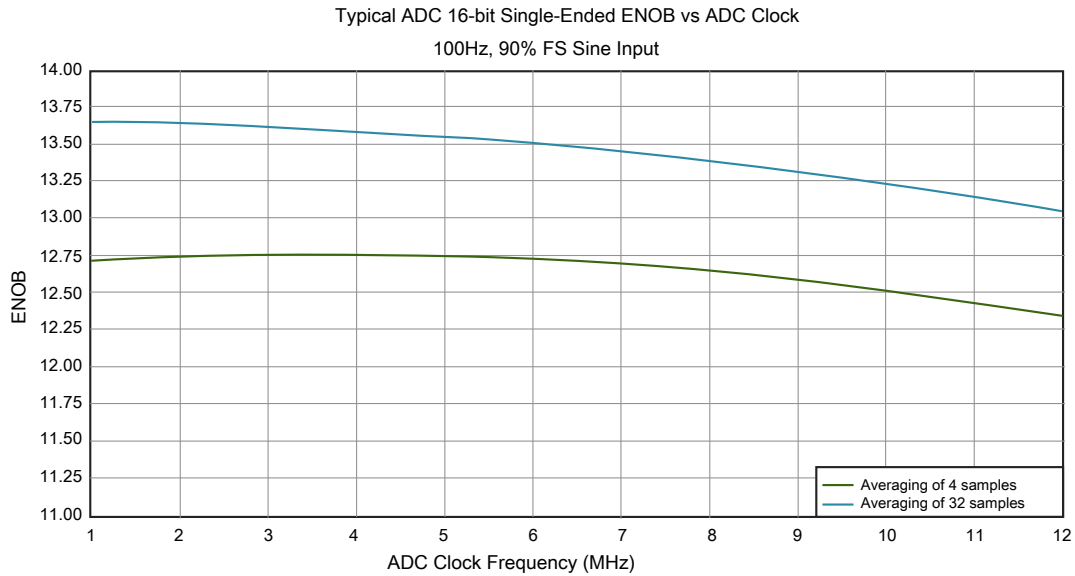
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
							current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
$V_{TEMP25}$	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0\text{ V}$ , Temp = 25 °C,  $f_{ADCK} = 2.0\text{ MHz}$  unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz



**Figure 7. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**





**Figure 8. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

### 3.6.2 Voltage reference electrical specifications

**Table 27. VREF full-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage		3.6	V	—
$T_A$	Temperature	Operating temperature range of the device		°C	—
$C_L$	Output load capacitance	100		nF	1, 2

1.  $C_L$  must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified  $C_L$  value over the operating temperature range of the device.

Table 28 is tested under the condition of setting VREF\_TRM[CHOPEN], VREF\_SC[REGEN] and VREF\_SC[ICOMPEN] bits to 1.

**Table 28. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25°C	1.1915	1.195	1.1977	V	1
$V_{out}$	Voltage reference output — factory trim	1.1584	—	1.2376	V	1
$V_{out}$	Voltage reference output — user trim	1.193	—	1.197	V	1

Table continues on the next page...

**Table 28. VREF full-range operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>step</sub>	Voltage reference trim step	—	0.5	—	mV	1
V <sub>tdrift</sub>	Temperature drift (V <sub>max</sub> -V <sub>min</sub> across the full temperature range: 0 to 70°C)	—	—	50	mV	1
A <sub>c</sub>	Aging coefficient	—	—	400	uV/yr	—
I <sub>bg</sub>	Bandgap only current	—	—	80	μA	1
I <sub>lp</sub>	Low-power buffer current	—	—	360	uA	1
I <sub>hp</sub>	High-power buffer current	—	—	1	mA	1
ΔV <sub>LOAD</sub>	Load regulation • current = ± 1.0 mA	—	200	—	μV	1, 2
T <sub>stup</sub>	Buffer startup time	—	—	100	μs	—
V <sub>vdrift</sub>	Voltage drift (V <sub>max</sub> -V <sub>min</sub> across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 29. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>A</sub>	Temperature	0	50	°C	—

**Table 30. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>out</sub>	Voltage reference output with factory trim	1.173	1.225	V	—

### 3.6.3 CMP and 6-bit DAC electrical specifications

**Table 31. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V
I <sub>DDHS</sub>	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I <sub>DDL</sub>	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V <sub>AIN</sub>	Analog input voltage	V <sub>SS</sub> - 0.3	—	V <sub>DD</sub>	V
V <sub>AIO</sub>	Analog input offset voltage	—	—	20	mV
V <sub>H</sub>	Analog comparator hysteresis <sup>1</sup>				

Table continues on the next page...

**Table 31. Comparator and 6-bit DAC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit
	<ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5	—	mV
		—	10	—	mV
		—	20	—	mV
		—	30	—	mV
V <sub>CMPOh</sub>	Output high	V <sub>DD</sub> - 0.5	—	—	V
V <sub>CMPOl</sub>	Output low	—	—	0.5	V
t <sub>DHS</sub>	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t <sub>DLS</sub>	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	μs
I <sub>DAC6b</sub>	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V<sub>DD</sub>-0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = V<sub>reference</sub>/64

Peripheral operating requirements and behaviors

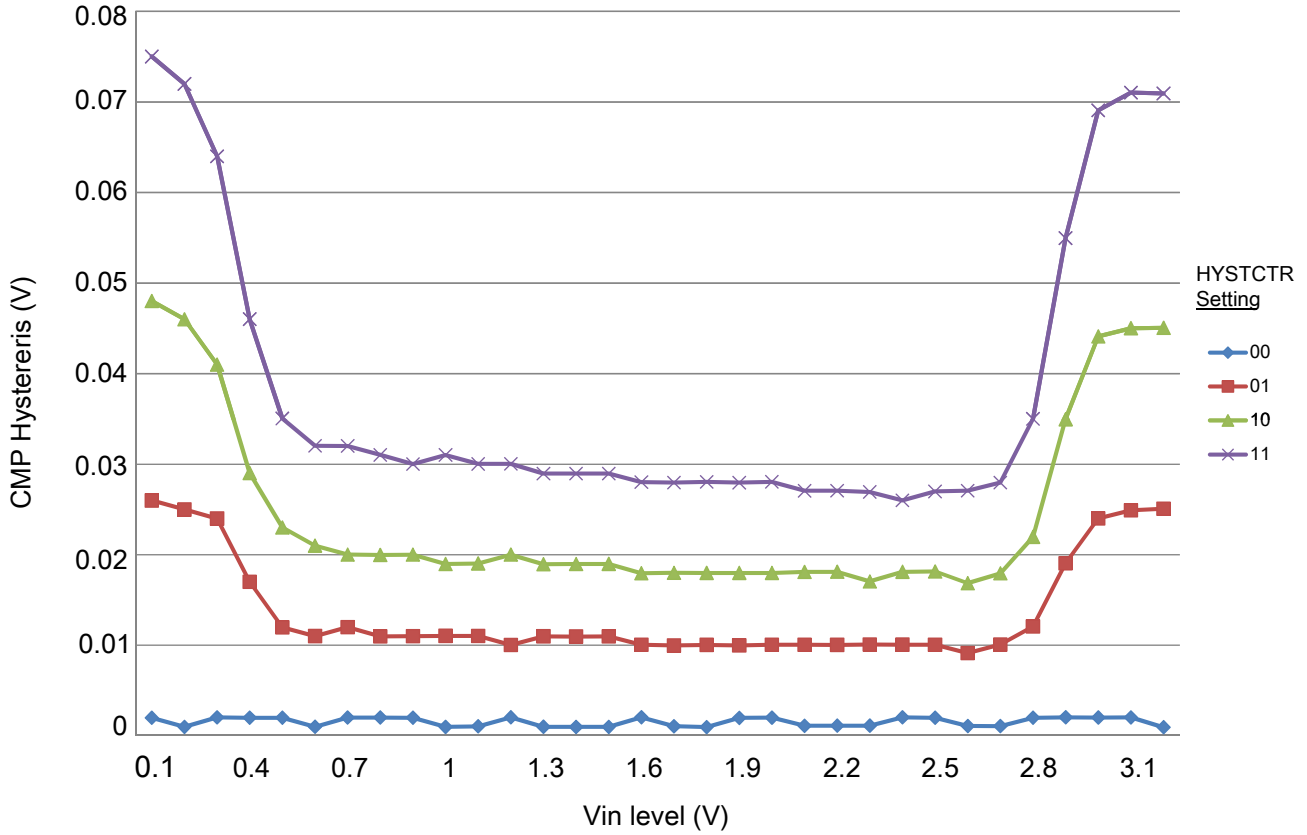


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

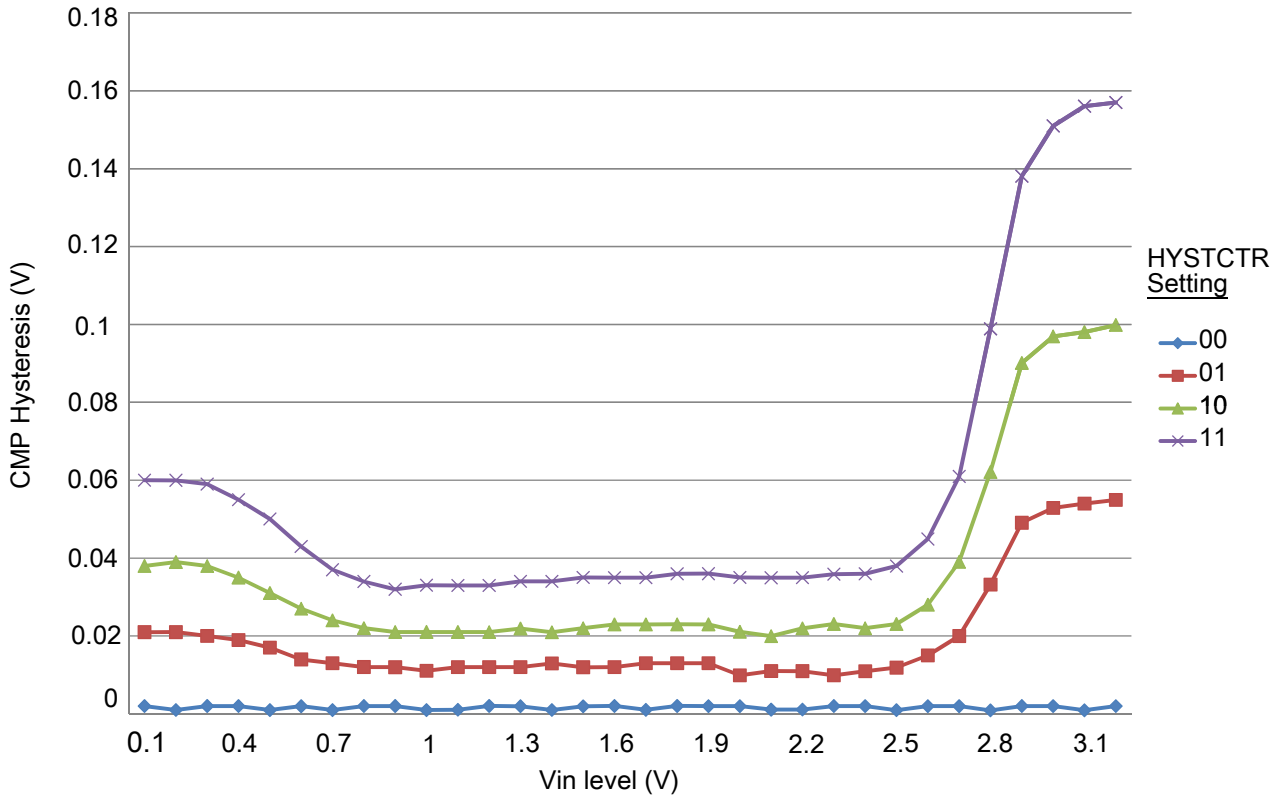


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 3.6.4 12-bit DAC electrical characteristics

#### 3.6.4.1 12-bit DAC operating requirements

Table 32. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage		3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REFH}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

## 3.6.4.2 12-bit DAC operating behaviors

Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	250	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	900	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	$\text{V}/\mu\text{s}$	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  ( $DACx\_CO:DACRFS = 1$ ), high power mode ( $DACx\_CO:LPEN = 0$ ), DAC set to 0x800, temperature range is across the full range of the device

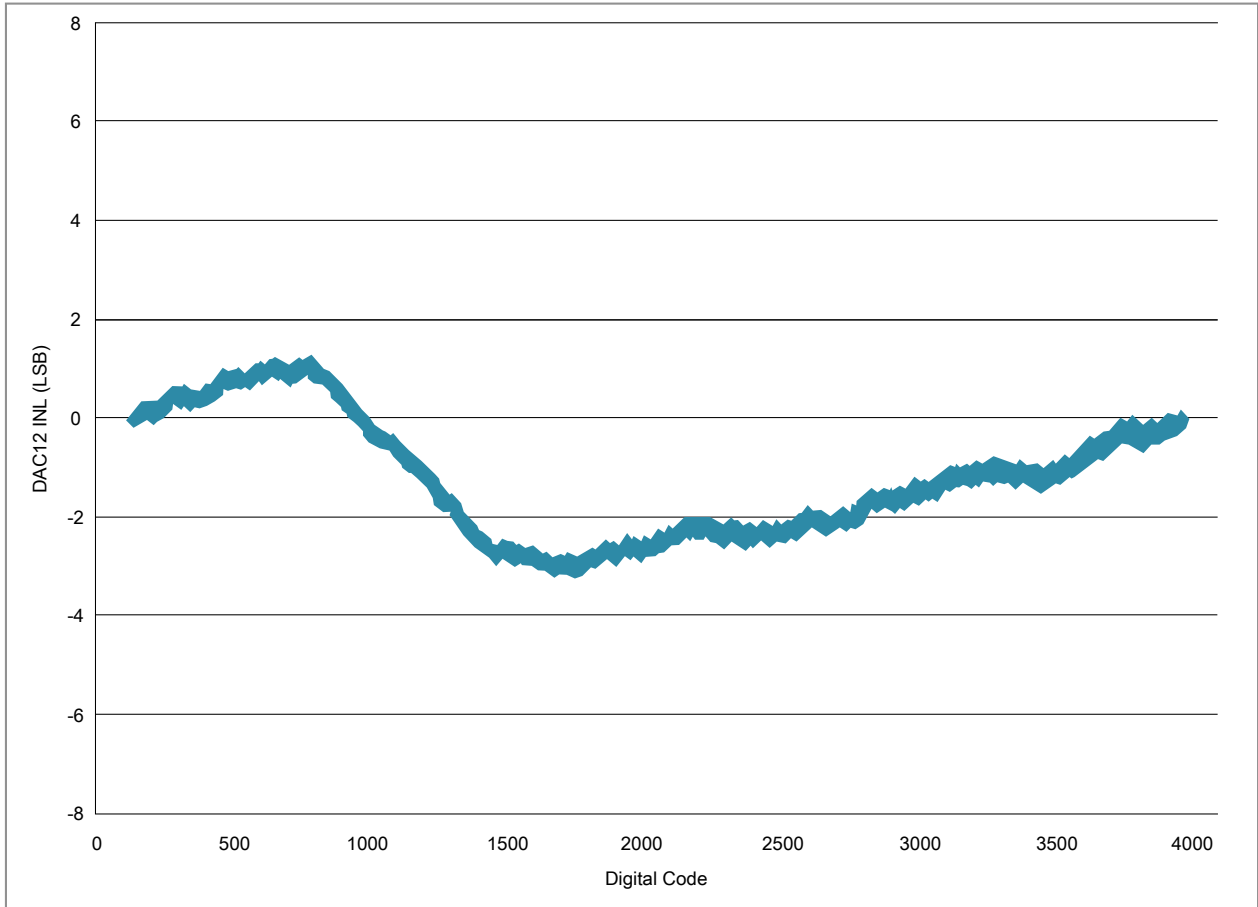


Figure 11. Typical INL error vs. digital code

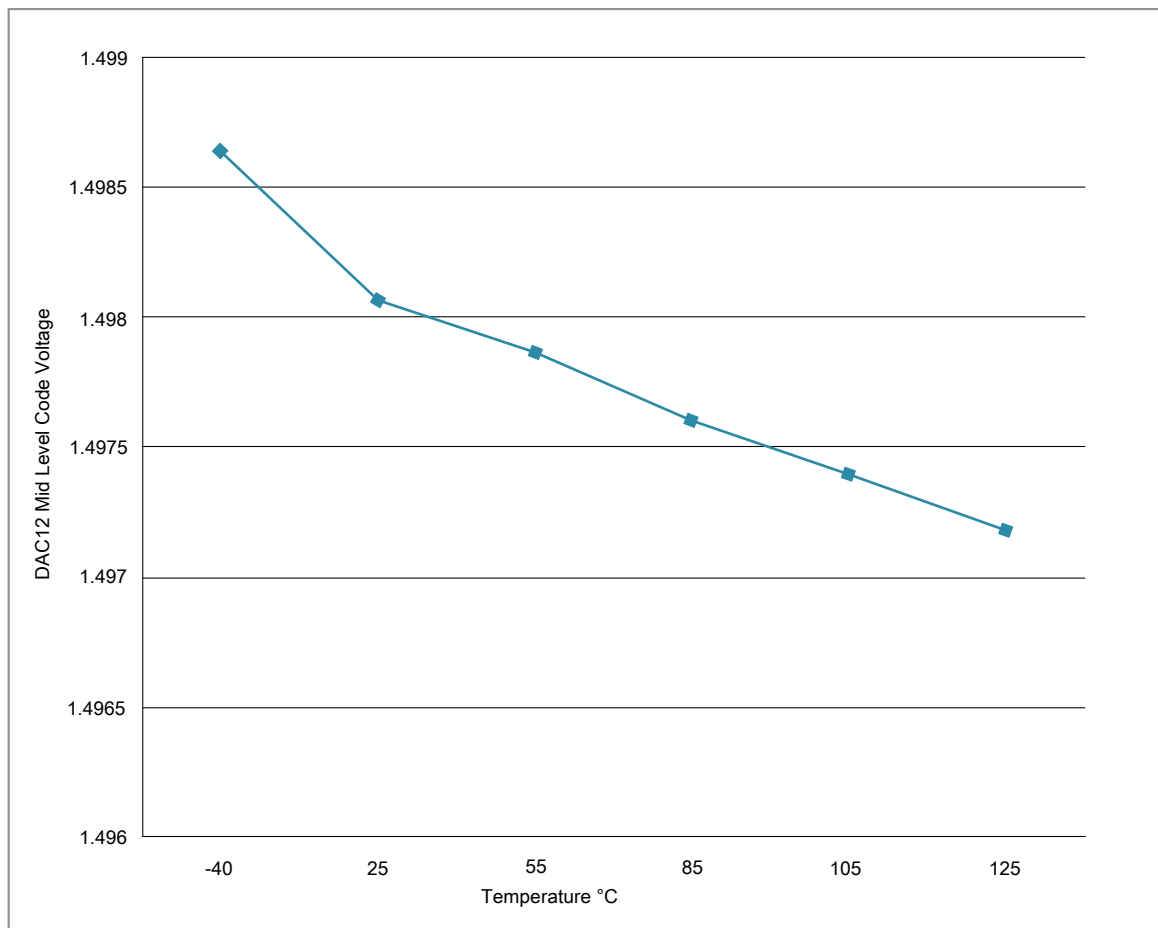


Figure 12. Offset at half scale vs. temperature

### 3.7 Timers

See [General switching specifications](#).

### 3.8 Communication interfaces

#### 3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit [usb.org](http://usb.org).



**NOTE**

The IRC48M do not meet the USB jitter specifications for certification for Host mode operation.

This device does not have the USB\_CLKIN signal available and therefore cannot support Host mode operation.

**3.8.2 USB VREG electrical specifications****Table 34. USB VREG electrical specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I <sub>DDon</sub>	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	μA	
I <sub>DDstby</sub>	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I <sub>DDoff</sub>	Quiescent current — Shutdown mode <ul style="list-style-type: none"> <li>VREGIN = 5.0 V and temperature=25 °C</li> <li>Across operating voltage and temperature</li> </ul>	—	650	—	nA	
		—	—	4	μA	
I <sub>LOADrun</sub>	Maximum load current — Run mode	—	—	120	mA	
I <sub>LOADstby</sub>	Maximum load current — Standby mode	—	—	1	mA	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) > 3.6 V <ul style="list-style-type: none"> <li>Run mode</li> <li>Standby mode</li> </ul>	3	3.3	3.6	V	
		2.1	2.8	3.6	V	
V <sub>Reg33out</sub>	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C <sub>OUT</sub>	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I <sub>LIM</sub>	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I<sub>Load</sub>.

### 3.8.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 35. SPI master mode timing on slew rate disabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	18	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	15	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

- For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
- $t_{periph} = 1/f_{periph}$

**Table 36. SPI master mode timing on slew rate enabled pads**

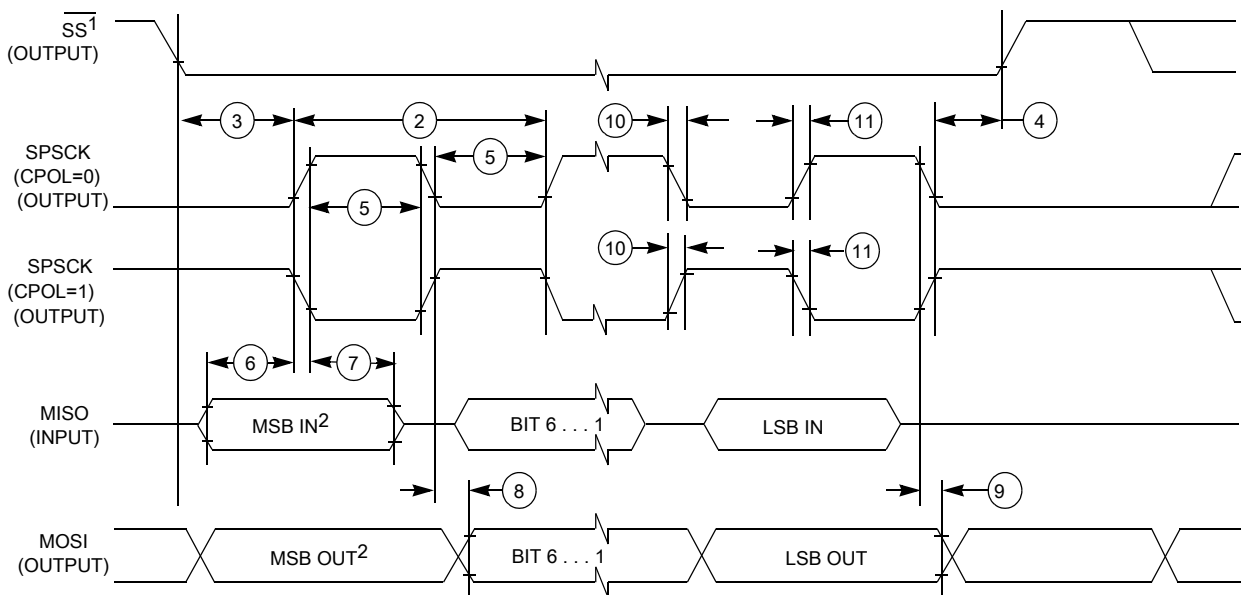
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	96	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—

*Table continues on the next page...*

**Table 36. SPI master mode timing on slew rate enabled pads (continued)**

Num.	Symbol	Description	Min.	Max.	Unit	Note
8	$t_v$	Data valid (after SPSCCK edge)	—	52	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

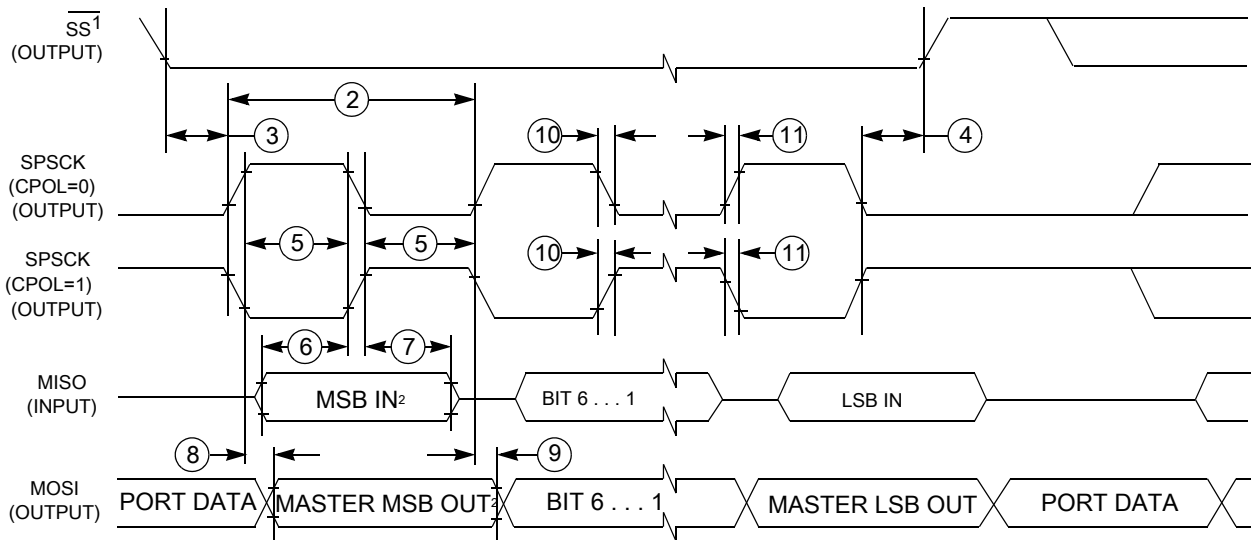
- For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
- $t_{periph} = 1/f_{periph}$



- If configured as an output.
- LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**

## Peripheral operating requirements and behaviors



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

**Table 37. SPI slave mode timing on slew rate disabled pads**

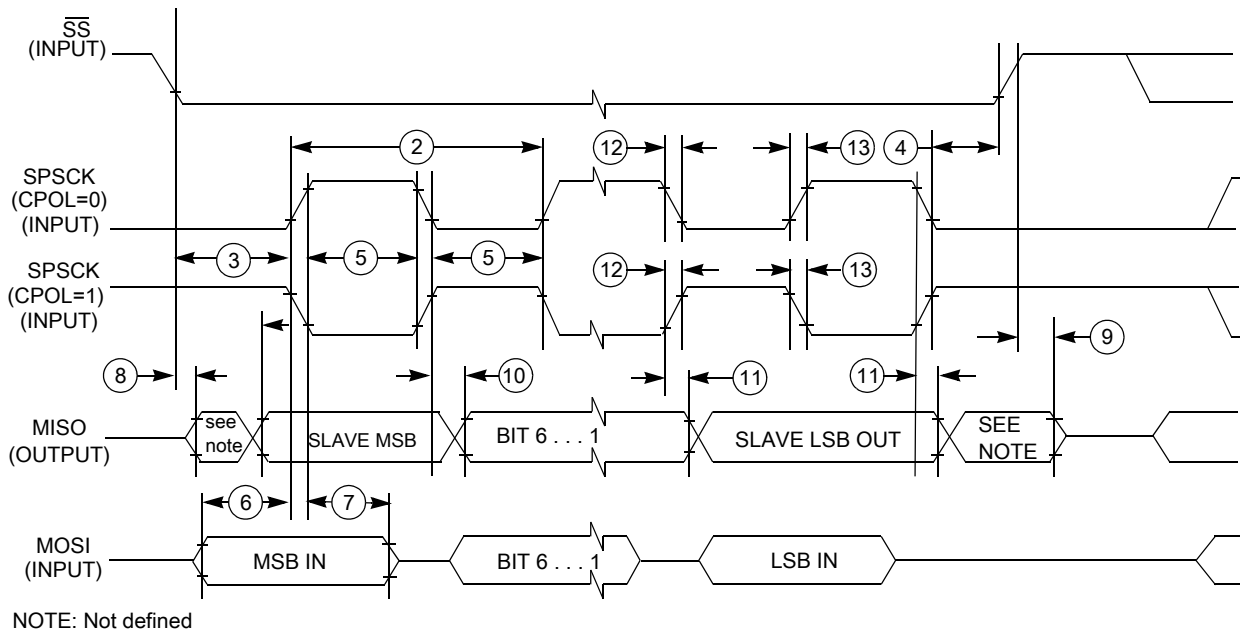
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	2.5	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	3.5	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCK edge)	—	31	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input	—			
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output	—			

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

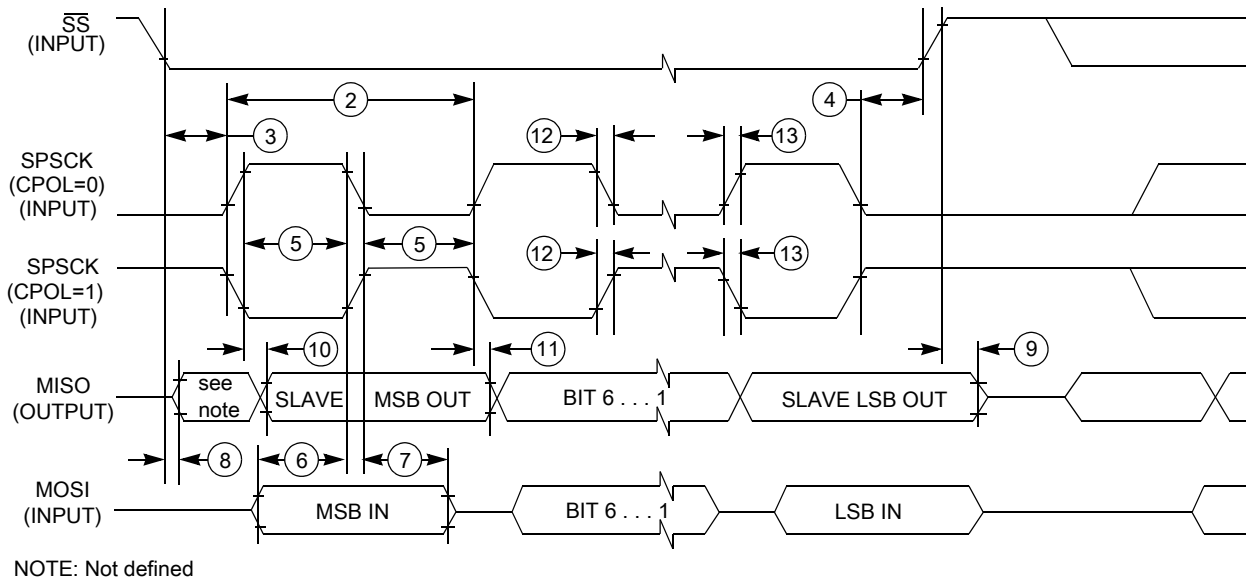
**Table 38. SPI slave mode timing on slew rate enabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSCK edge)	—	122	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Figure 15. SPI slave mode timing (CPHA = 0)**

## Peripheral operating requirements and behaviors



**Figure 16. SPI slave mode timing (CPHA = 1)**

### 3.8.4 I<sup>2</sup>C

See [General switching specifications](#).

### 3.8.5 UART

See [General switching specifications](#).

### 3.8.6 I2S/SAI switching specifications

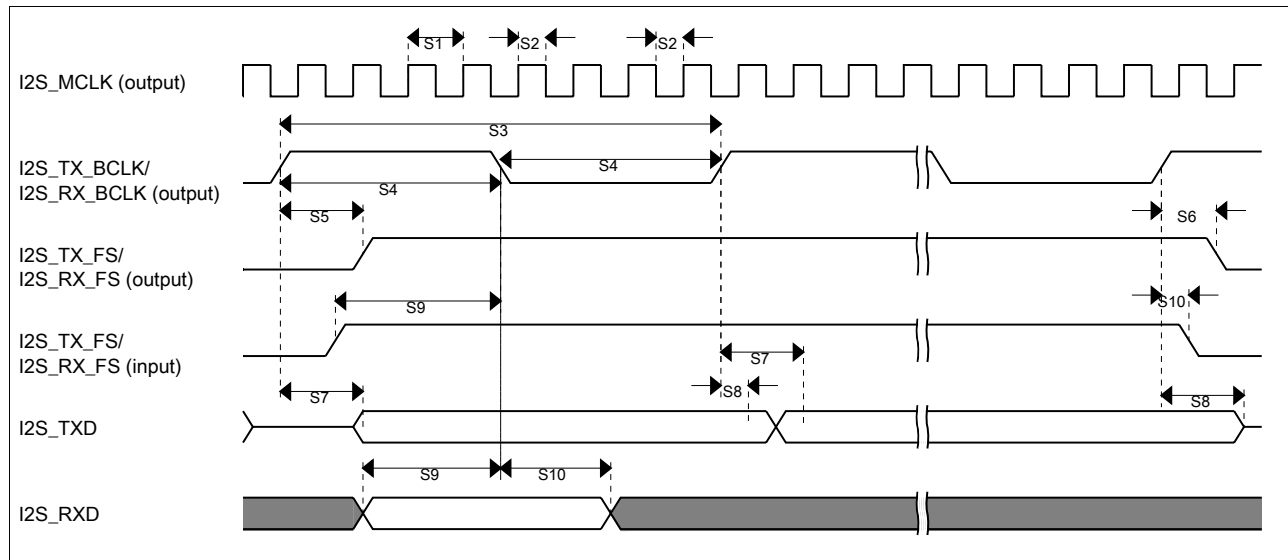
This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

### 3.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 39. I2S/SAI master mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

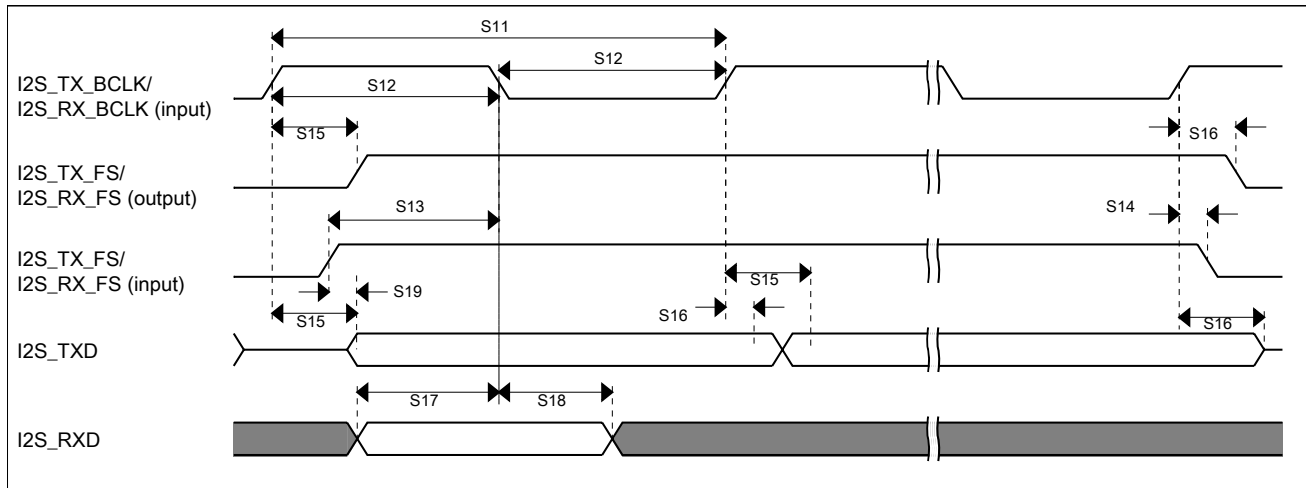


**Figure 17. I2S/SAI timing — master modes**

**Table 40. I2S/SAI slave mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



**Figure 18. I2S/SAI timing — slave modes**

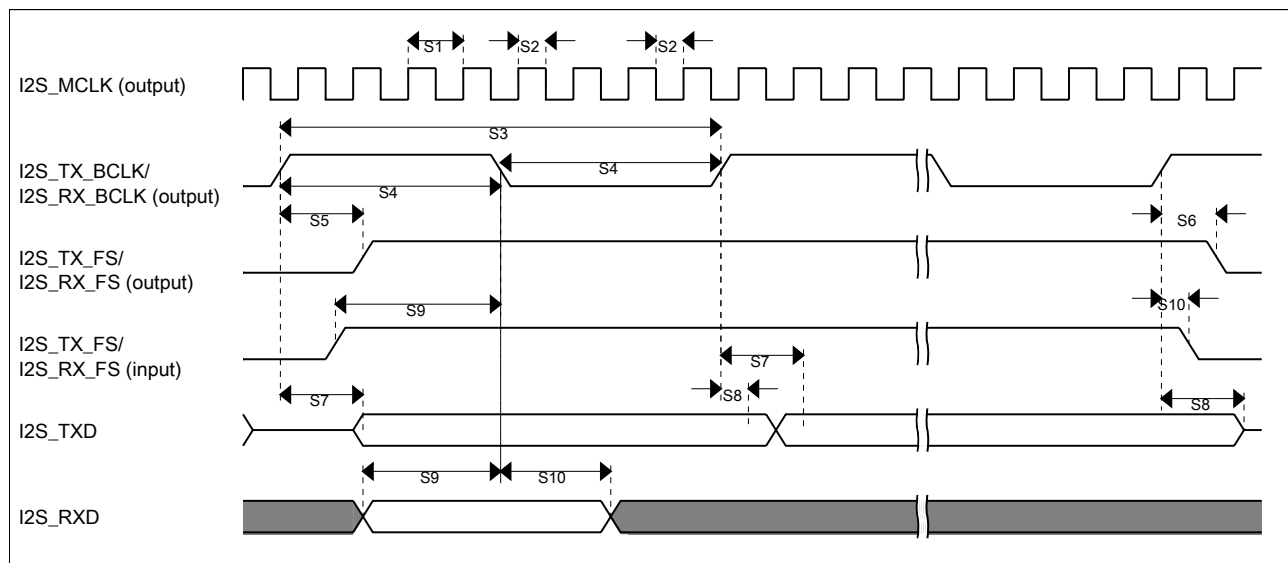
### 3.8.6.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.



**Table 41. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

**Figure 19. I2S/SAI timing — master modes****Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)**

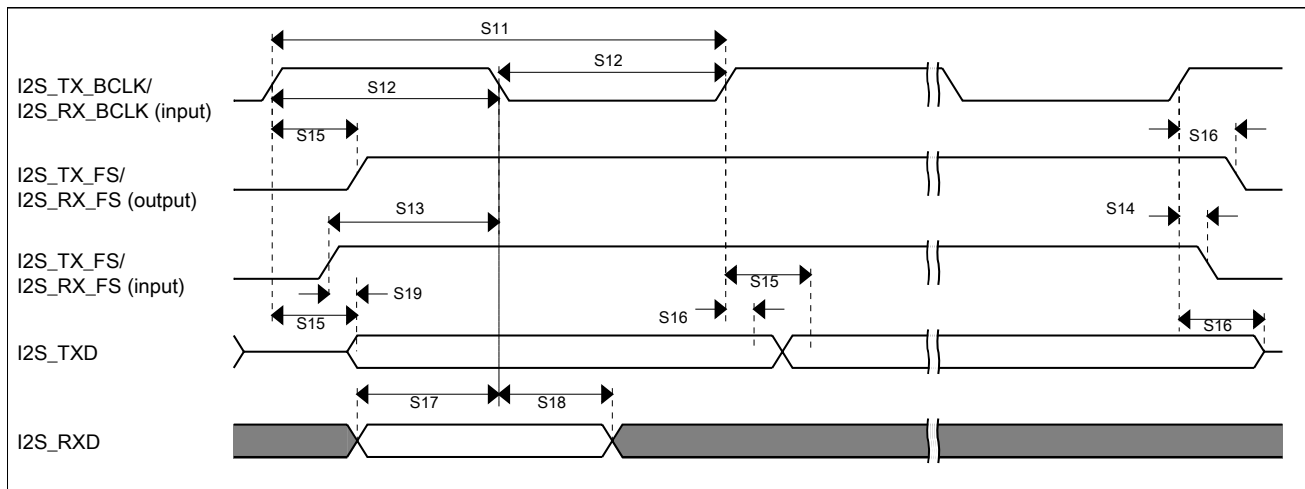
Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns

Table continues on the next page...

**Table 42. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)**

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



**Figure 20. I2S/SAI timing — slave modes**

## 4 Dimensions

### 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00615D
48-pin QFN	98ASA00616D
64-pin LQFP	98ASS23234W
64-pin MAPBGA	98ASA00420D

## 5 Pinouts and Packaging

### 5.1 KL27 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

#### NOTE

VREFH can act as VREF\_OUT when VREFV1 module is enabled.

#### NOTE

It is prohibited to set VREFEN in 32 QFN pin package as 1.2 V on-chip voltage is not available in this package.

32 QFN	48 QFN	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	—	B1	2	PTE1	DISABLED		PTE1	SPI1_MOSI	LPUART1_RX		SPI1_MISO	I2C1_SCL	
—	1	—	3	VDD	VDD	VDD							
—	7	G1	9	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	LPUART0_TX		FXIO0_D4	
—	8	F1	10	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	LPUART0_RX		FXIO0_D5	
—	—	G2	11	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX		FXIO0_D6	
—	—	F2	12	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX		FXIO0_D7	
—	10	G4	14	VREFH	VREFH	VREFH							
—	11	G3	15	VREFL	VREFL	VREFL							
—	13	H1	17	PTE29	CMPO_IN5/ ADC0_SE4b	CMPO_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKINO			
—	—	H3	19	PTE31	DISABLED		PTE31		TPM0_CH4				

## Pinouts and Packaging

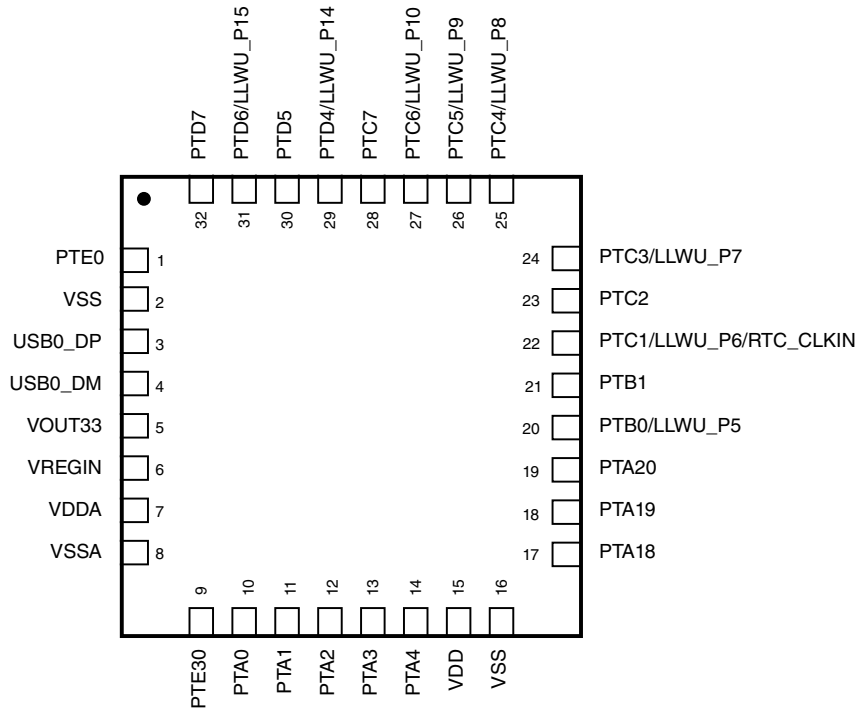
32 QFN	48 QFN	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	15	H4	20	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
—	16	H5	21	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
—	—	F5	27	PTA5	DISABLED		PTA5	USB_CLKIN	TPM0_CH2			I2S0_TX_BCLK	
—	—	H6	28	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	
—	—	G6	29	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
—	29	E7	37	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	TPM2_CH0				
—	30	E8	38	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	TPM2_CH1				
—	31	E6	39	PTB16	DISABLED		PTB16	SPI1_MOSI	LPUART0_RX	TPM_CLKIN0	SPI1_MISO		
—	32	D7	40	PTB17	DISABLED		PTB17	SPI1_MISO	LPUART0_TX	TPM_CLKIN1	SPI1_MOSI		
—	—	D6	41	PTB18	DISABLED		PTB18		TPM2_CH0	I2S0_TX_BCLK			
—	—	C7	42	PTB19	DISABLED		PTB19		TPM2_CH1	I2S0_TX_FS			
—	33	D8	43	PTC0	ADC0_SE14	ADC0_SE14	PTC0		EXTRG_IN	audioUSB_SOF_OUT	CMP0_OUT	I2S0_TXD0	
—	—	E3	47	VSS	VSS	VSS							
—	—	E4	48	VDD	VDD	VDD							
—	—	A6	53	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
—	—	B5	54	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
—	—	B4	55	PTC10	DISABLED		PTC10	I2C1_SCL			I2S0_RX_FS		
—	—	A5	56	PTC11	DISABLED		PTC11	I2C1_SDA			I2S0_RXD0		
—	41	C3	57	PTD0	DISABLED		PTD0	SPI0_SS		TPM0_CH0		FXIO0_D0	
—	42	A4	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1		FXIO0_D1	
—	43	C2	59	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO	FXIO0_D2	
—	44	B3	60	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI	FXIO0_D3	
—	—	C5	—	NC	NC	NC							
1	—	A1	1	PTE0	DISABLED		PTE0/CLKOUT32K	SPI1_MISO	LPUART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	2	C4	4	VSS	VSS	VSS							
3	3	E1	5	USB0_DP	USB0_DP	USB0_DP							
4	4	D1	6	USB0_DM	USB0_DM	USB0_DM							
5	5	E2	7	VOUT33	VOUT33	VOUT33							
6	6	D2	8	VREGIN	VREGIN	VREGIN							
7	9	F4	13	VDDA	VDDA	VDDA							
8	12	F3	16	VSSA	VSSA	VSSA							
9	14	H2	18	PTE30	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	DAC0_OUT/ ADC0_SE23/ CMP0_IN4	PTE30		TPM0_CH3	TPM_CLKIN1	LPUART1_TX	LPTMR0_ALT1	
10	17	D3	22	PTA0	SWD_CLK		PTA0		TPM0_CH5				SWD_CLK

32 QFN	48 QFN	64 MAP BGA	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
11	18	D4	23	PTA1	DISABLED		PTA1	LPUART0_RX	TPM2_CH0				
12	19	E5	24	PTA2	DISABLED		PTA2	LPUART0_TX	TPM2_CH1				
13	20	D5	25	PTA3	SWD_DIO		PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
14	21	G5	26	PTA4	NMI_b		PTA4	I2C1_SDA	TPM0_CH1				NMI_b
15	22	G7	30	VDD	VDD	VDD							
16	23	H7	31	VSS	VSS	VSS							
17	24	H8	32	PTA18	EXTAL0	EXTAL0	PTA18		LPUART1_RX	TPM_CLKIN0			
18	25	G8	33	PTA19	XTAL0	XTAL0	PTA19		LPUART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
19	26	F8	34	PTA20	RESET_b		PTA20						RESET_b
20	27	F7	35	PTB0/LLWU_P5	ADC0_SE8	ADC0_SE8	PTB0/LLWU_P5	I2C0_SCL	TPM1_CH0				
21	28	F6	36	PTB1	ADC0_SE9	ADC0_SE9	PTB1	I2C0_SDA	TPM1_CH1				
22	34	C6	44	PTC1/LLWU_P6/RTC_CLKIN	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6/RTC_CLKIN	I2C1_SCL		TPM0_CH0			I2S0_TXD0
23	35	B7	45	PTC2	ADC0_SE11	ADC0_SE11	PTC2	I2C1_SDA		TPM0_CH1			I2S0_TX_FS
24	36	C8	46	PTC3/LLWU_P7	DISABLED		PTC3/LLWU_P7	SPI1_SCK	LPUART1_RX	TPM0_CH2	CLKOUT		I2S0_TX_BCLK
25	37	B8	49	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_SS	LPUART1_TX	TPM0_CH3	I2S0_MCLK		
26	38	A8	50	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0			CMP0_OUT
27	39	A7	51	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
28	40	B6	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO	audioUSB_SOF_OUT	I2S0_RX_FS	SPI0_MOSI		
29	45	A3	61	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI1_SS	UART2_RX	TPM0_CH4			FXIO0_D4
30	46	C1	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			FXIO0_D5
31	47	B2	63	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI1_MOSI	LPUART0_RX		SPI1_MISO	FXIO0_D6	
32	48	A2	64	PTD7	DISABLED		PTD7	SPI1_MISO	LPUART0_TX		SPI1_MOSI	FXIO0_D7	

## 5.2 KL27 Family Pinouts

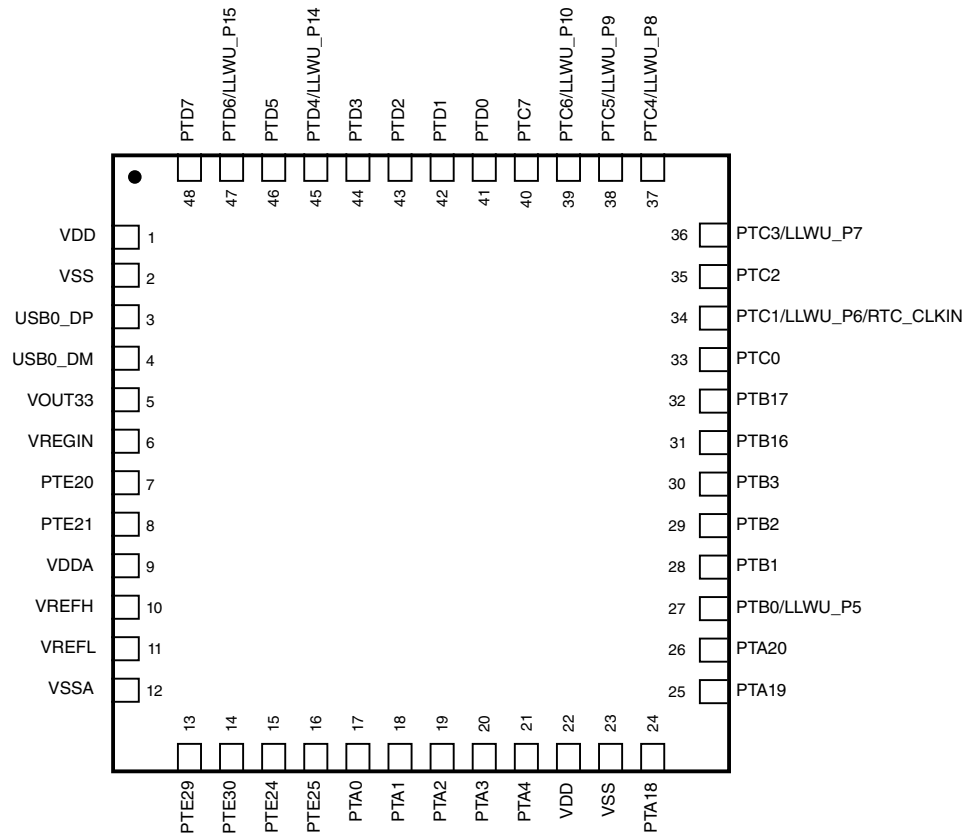
Figure below shows the 32 QFN pinouts:

**Pinouts and Packaging**



**Figure 21. 32 QFN Pinout diagram**

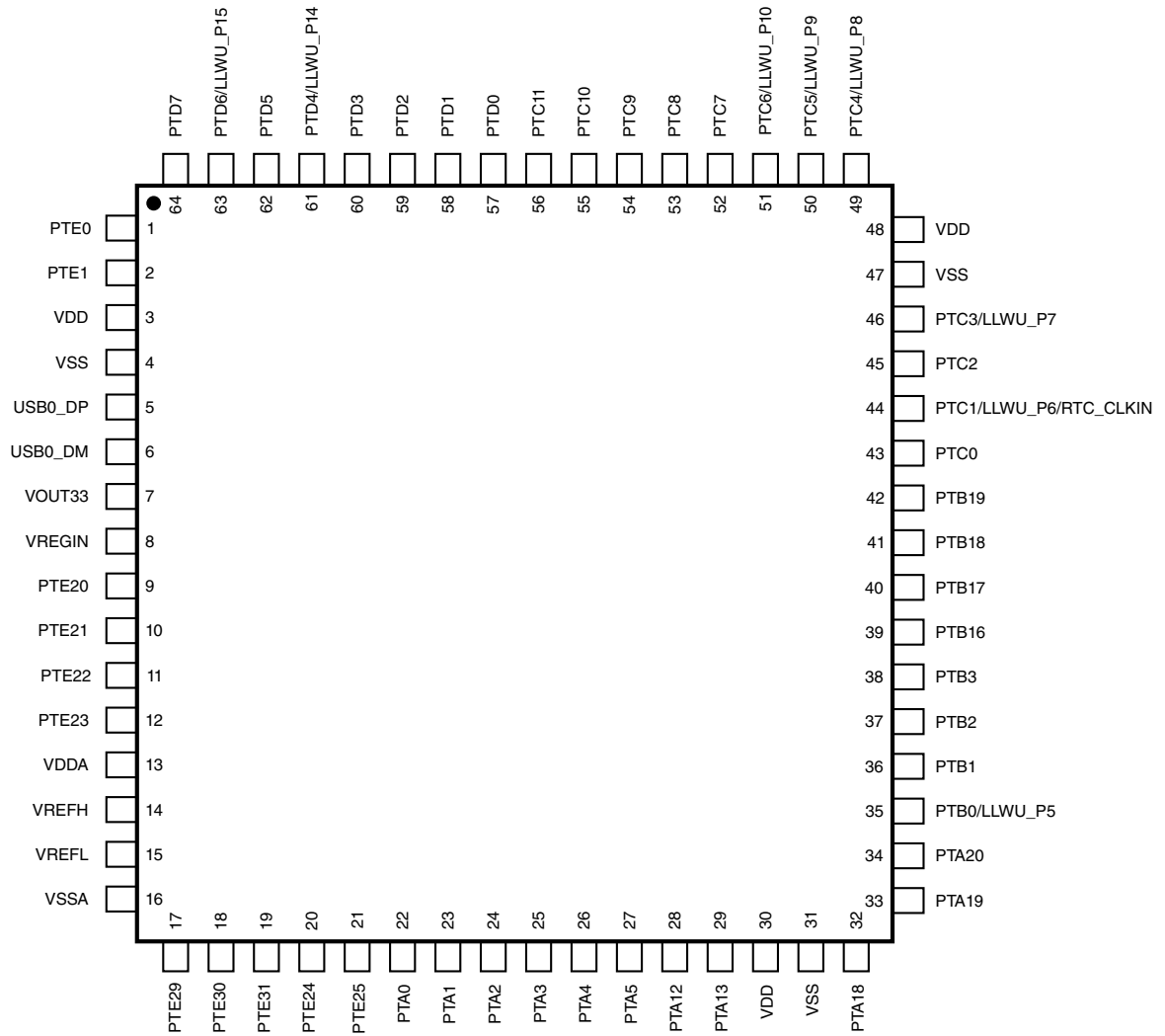
Figure below shows the 48 QFN pinouts:



**Figure 22. 48 QFN Pinout diagram**

Figure below shows the 64 LQFP pinouts:

## Pinouts and Packaging



**Figure 23. 64 LQFP Pinout diagram**

Figure below shows the 64 MAPBGA pinouts:



	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
B	PTE1	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	B
C	PTD5	PTD2	PTD0	VSS	NC	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	C
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
E	USB0_DP	VOOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
H	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	H
	1	2	3	4	5	6	7	8	

Figure 24. 64 MAPBGA Pinout diagram

## 6 Ordering parts

### 6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers:

## 7 Part identification

## 7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 7.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

## 7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

**Table 43. Part number fields descriptions**

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KL##	Kinetis family	<ul style="list-style-type: none"> <li>KL27</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = Cortex-M0+</li> </ul>
FFF	Program flash memory size	
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>FM = 32 QFN (5 mm x 5 mm)</li> <li>FT = 48 QFN (7 mm x 7 mm)</li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> <li>MP = 64 MAPBGA (5 mm x 5 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>4 = 48 MHz</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>R = Tape and reel</li> </ul>

## 7.4 Example

This is an example part number:

MKL27Z256VFT4

## 8 Terminology and guidelines

### 8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

### 8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

#### 8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	130	μA

## 8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

### 8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

## 8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

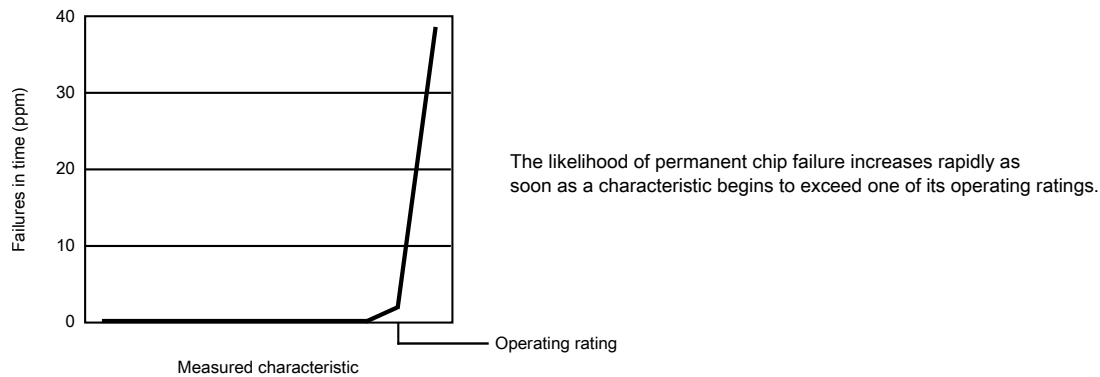
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

### 8.4.1 Example

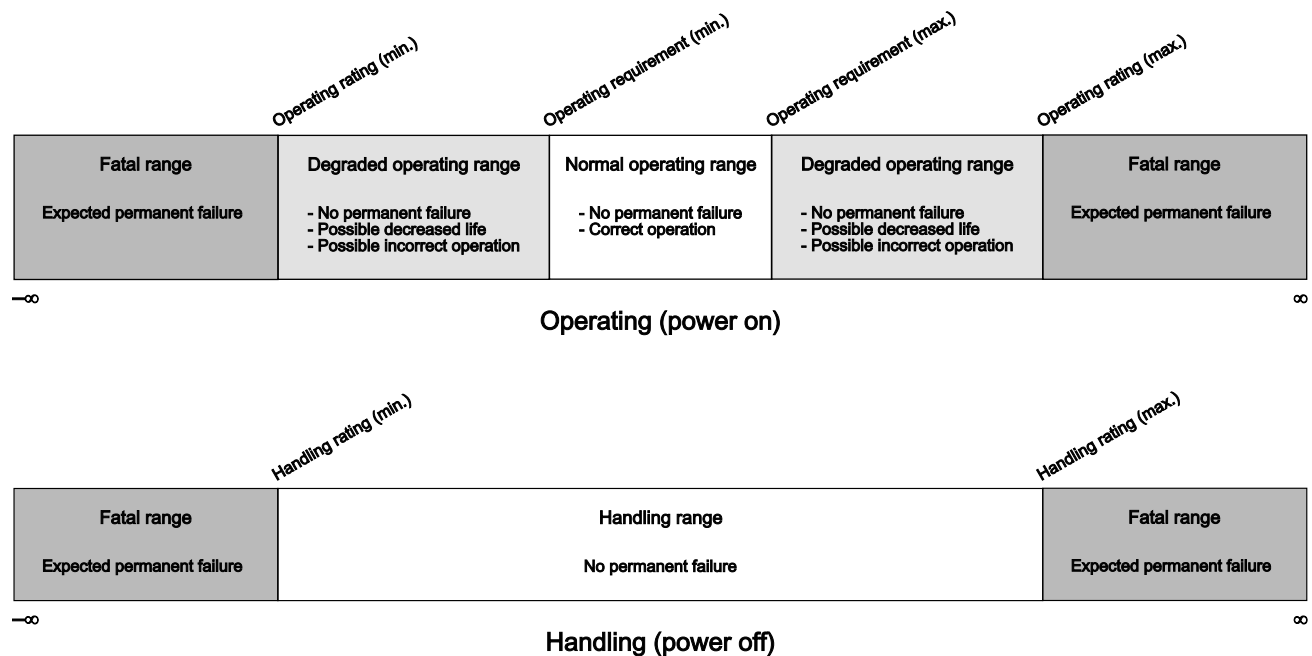
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	−0.3	1.2	V

## 8.5 Result of exceeding a rating



## 8.6 Relationship between ratings and operating requirements



## 8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

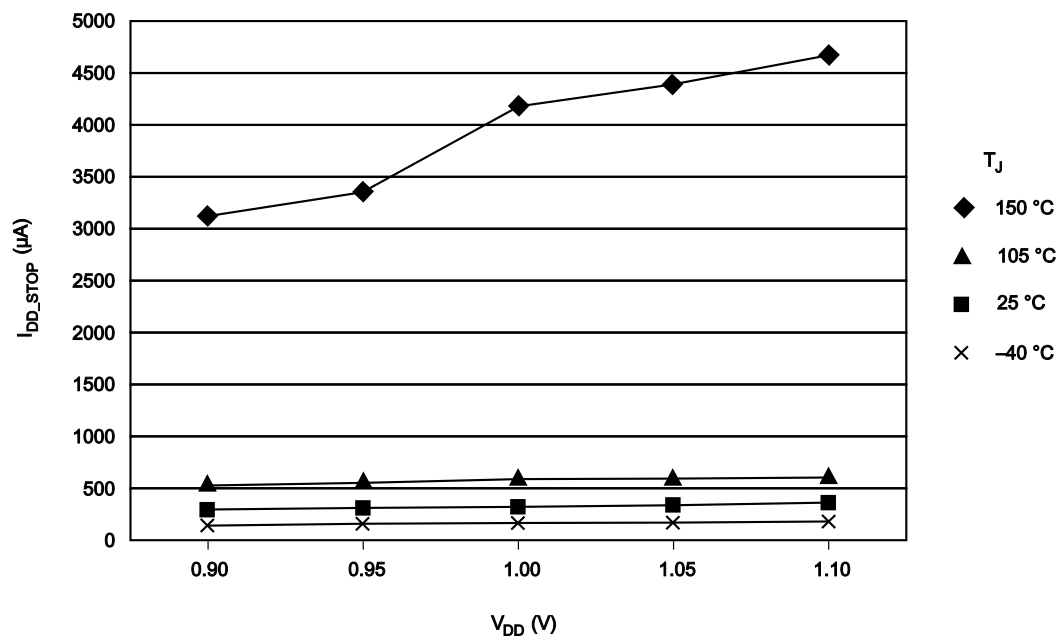
### 8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu A$

### 8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 44. Typical value conditions**

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	3.3 V supply voltage	3.3	V

## 9 Revision History

The following table provides a revision history for this document.

**Table 45. Revision History**

Rev. No.	Date	Substantial Changes
3	09 August 2014	Initial Public release <ul style="list-style-type: none"> <li>Updated Table 9 - Power consumption operating behaviors.</li> <li>Added a note related to 32 QFN pin package in Pinouts topic.</li> </ul>



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