KL5BUDV003

USB2.0 to PCI BUS

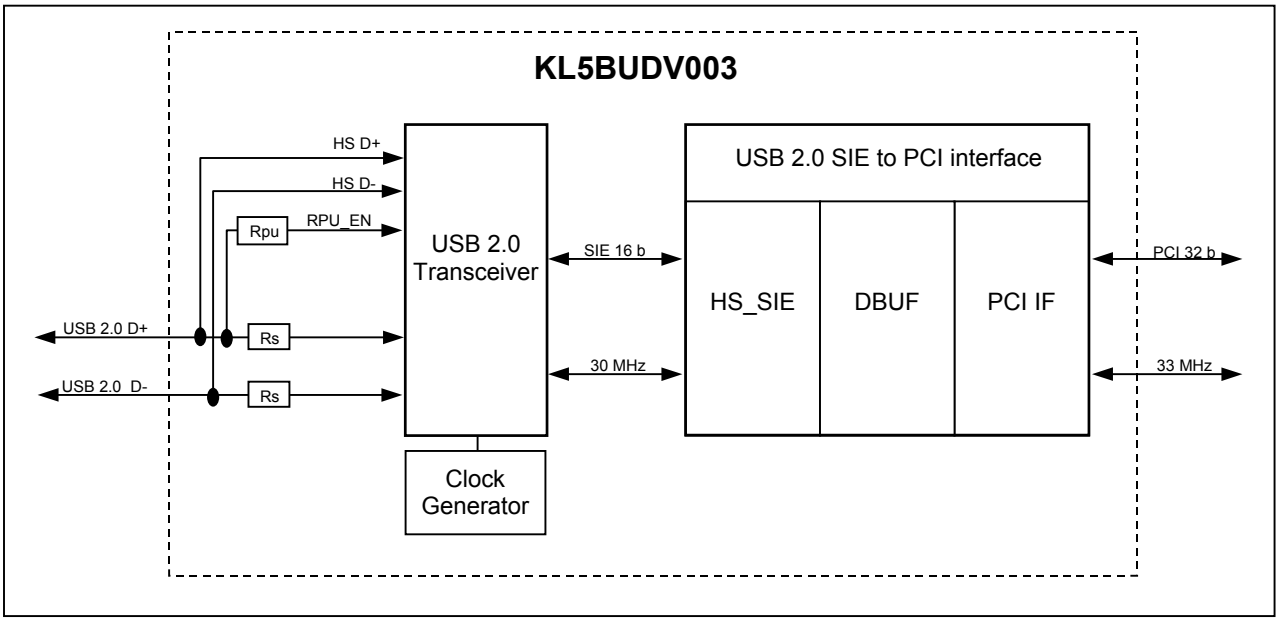
General Description

The Kawasaki KL5KBUDV003 is a high performance device that transfers data between the USB2.0 high-speed BUS and the PCI 33MHz, 32 bit BUS. This 1 chip solution has USB 2.0 transceiver embedded reducing space and cost. The KL5KBUDV003 is an ideal solution to convert a PCI device to a USB2.0 Transceiver, HS_SIE USB2.0 Transceiver interface, 4 sets of high-speed bulk packet size buffers, PCI interface and PCI master 2DMA channel support.

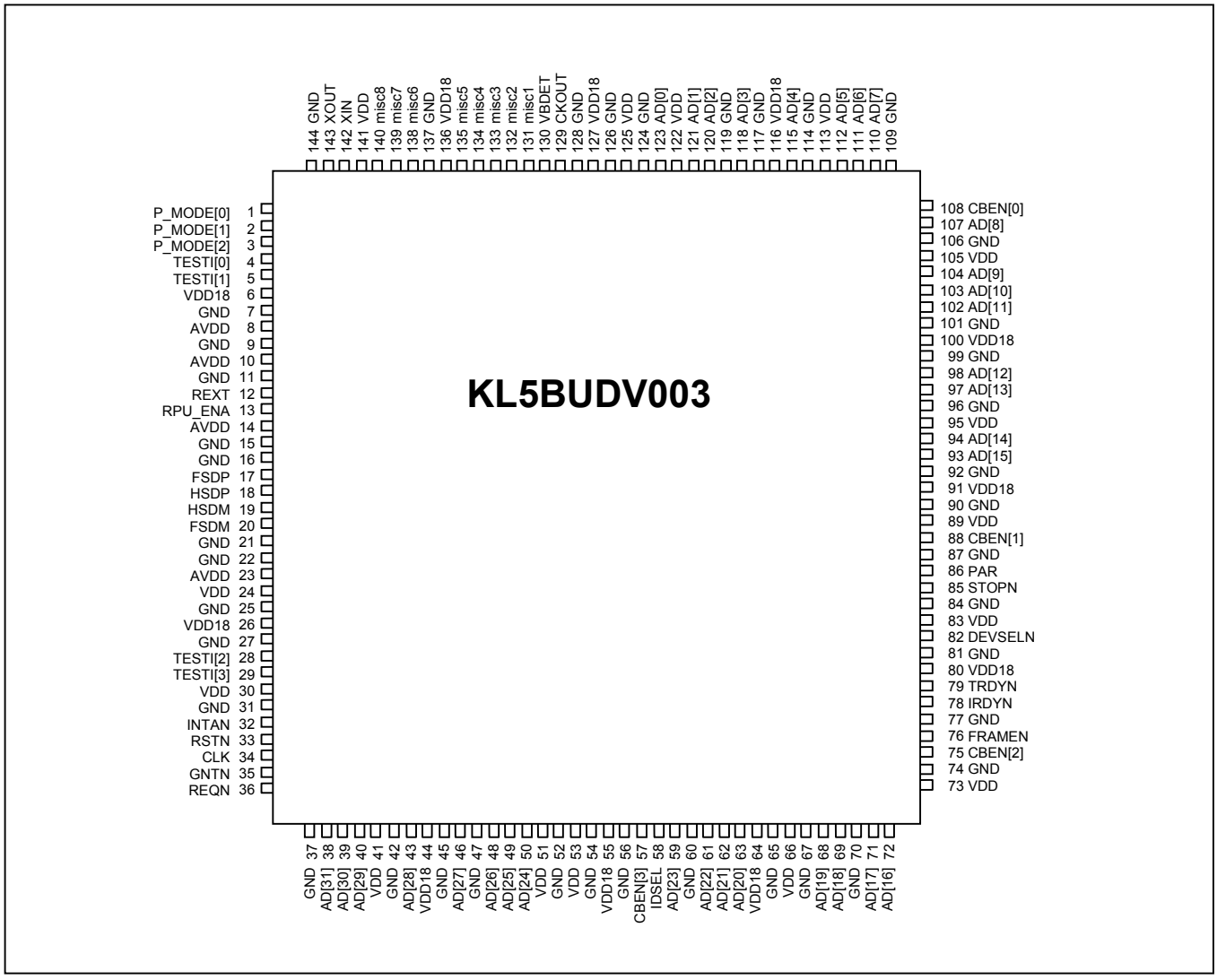
Features

- 33MHz PCI interface
- USB 2.0 standard embedded transceiver.
- 30MHz USB 2.0 SIE BUS for High-Speed SIE operation
- Double packet buffer - 512x2 HS, 64Bx2 FS
- Internal DMA operation between the High-Speed SIE and Double Buffer
- High-Speed chirp protocol
- High-Speed/Full-Speed compatibility
- USB basic operation and transaction control
- Up to 5 endpoints
- PCI interface for Target and Master (2 DMA) modes
- Page and Descriptor DMA Modes
- USB data access by PCI target or DMA
- 0.18u Std cell technology
- V_{dd} = 3.3V, T_a = 0~70°C

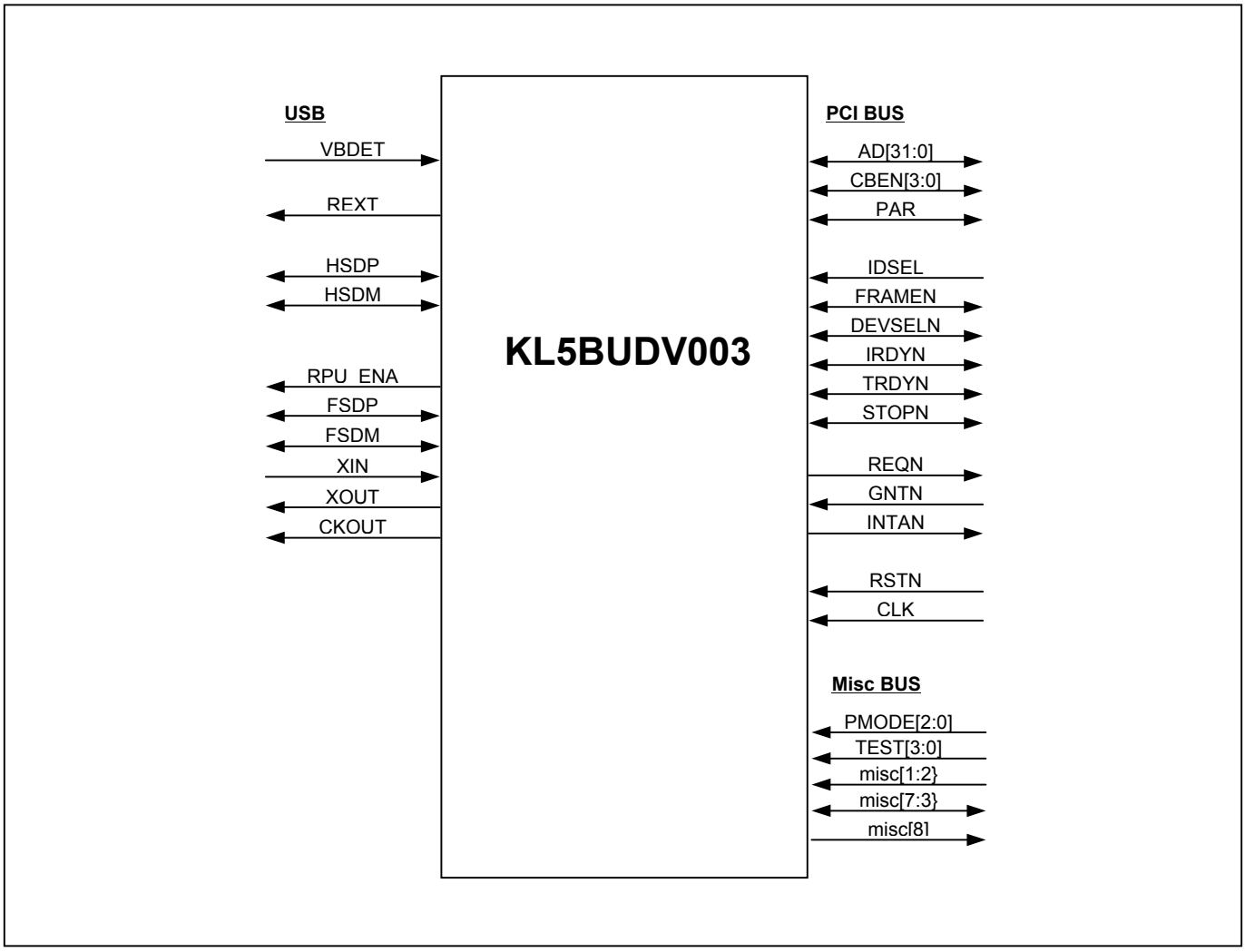
Block Diagram



Pin Diagram 144LQFP



Logical Pin Out



Pin Description (PCI Mode)

Pin # QFP	I/O	Pin Name	Description
1	I	P_MODE[0]	Burst Length select flag
2	I	P_MODE[1]	Burst Length select flag
3	I	P_MODE[2]	Burst Length select flag
4	I	TEST[0]	LSI shipment test input and mode pin
5	I	TEST[1]	LSI shipment test input and mode pin
6	--	VDD18	1.8V power pin
7	--	GND	Ground
8	--	AVDD	3.3V power pin
9	--	GND	Ground
10	--	AVDD	3.3V power pin
11	--	GND	Ground
12	O	REXT	USB100uA fixed reference bias current pin
13	O	RPU_ENA	USB External pull up resistor source drive pin
14	--	AVDD	3.3V power pin
15	--	GND	Ground
16	--	GND	Ground
17	I/O	FSDP	USB FS_XVR DP pin
18	I/O	HSDP	USB HS_XVR DP pin
19	I/O	HSDM	USB HS_XVR DM pin
20	I/O	FSDM	USB FS_XVR DM pin
21	--	GND	Ground
22	--	GND	Ground
23	--	AVDD	3.3V power pin
24	--	VDD	3.3V power pin
25	--	GND	Ground
26	--	VDD18	1.8V power pin
27	--	GND	Ground
28	I	TEST[2]	LSI shipment test input and mode pin
29	I	TEST[3]	LSI shipment test input and mode pin
30	--	VDD	3.3V power pin
31	--	GND	Ground
32	O	INTAN	PCI interrupt signal
33	I	RSTN	PCI bus asynchronous reset input
34	I	CLK	PCI clock input
35	I	GNTN	PCI bus grant signal
36	O	REQN	PCI bus request signal
37	--	GND	Ground
38	I/O	AD[31]	PCI address data bus
39	I/O	AD[30]	PCI address data bus
40	I/O	AD[29]	PCI address data bus
41	--	VDD	3.3V power pin
42	--	GND	Ground
43	I/O	AD[28]	PCI address data bus
44	--	VDD18	1.8V power pin
45	--	GND	Ground
46	I/O	AD[27]	PCI address data bus
47	--	GND	Ground

Pin # QFP	I/O	Pin Name	Description
48	I/O	AD[26]	PCI address data bus
49	I/O	AD[25]	PCI address data bus
50	I/O	AD[24]	PCI address data bus
51	--	VDD	3.3V power pin
52	--	GND	Ground
53	--	VDD	3.3V power pin
54	--	GND	Ground
55	--	VDD18	1.8V power pin
56	--	GND	Ground
57	I/O	CBEN[3]	Bus command byte enable signal
58	I	IDSEL	Device-select signal during configuration
59	I/O	AD[23]	PCI address data bus
60	--	GND	Ground
61	I/O	AD[22]	PCI address data bus
62	I/O	AD[21]	PCI address data bus
63	I/O	AD[20]	PCI address data bus
64	--	VDD18	1.8V power pin
65	--	GND	Ground
66	--	VDD	3.3V power pin
67	--	GND	Ground
68	I/O	AD[19]	PCI address data bus
69	I/O	AD[18]	PCI address data bus
70	--	GND	Ground
71	I/O	AD[17]	PCI address data bus
72	I/O	AD[16]	PCI address data bus
73	--	VDD	3.3V power pin
74	--	GND	Ground
75	I/O	CBEN[2]	Bus command byte enable signal
76	I/O	FRAMEN	Cycle-frame signal
77	--	GND	Ground
78	I/O	IRDYN	Initiator RDY signal
79	I/O	TRDYN	Target RDY signal
80	--	VDD18	1.8V power pin
81	--	GND	Ground
82	I/O	DEVSELN	Device-select signal
83	--	VDD	3.3V power pin
84	--	GND	Ground
85	I/O	STOPN	Target termination signal
86	I/O	PAR	Even parity flag
87	--	GND	3.3V power pin
88	I/O	CBEN[1]	Bus command byte enable signal
89	--	VDD	3.3V power pin
90	--	GND	Ground
91	--	VDD18	1.8V power pin
92	--	GND	Ground
93	I/O	AD[15]	PCI address data bus
94	I/O	AD[14]	PCI address data bus
95	--	VDD	3.3V power pin
96	--	GND	Ground
97	I/O	AD[13]	PCI address data bus
98	I/O	AD[12]	PCI address data bus

Pin # QFP	I/O	Pin Name	Description
99	--	GND	Ground
100	--	VDD18	1.8V power pin
101	--	GND	Ground
102	I/O	AD[11]	PCI address data bus
103	I/O	AD[10]	PCI address data bus
104	I/O	AD[9]	PCI address data bus
105	--	VDD	3.3V power pin
106	--	GND	Ground
107	I/O	AD[8]	PCI address data bus
108	I/O	CBEN[0]	Bus command byte enable signal
109	--	GND	Ground
110	I/O	AD[7]	PCI address data bus
111	I/O	AD[6]	PCI address data bus
112	I/O	AD[5]	PCI address data bus
113	--	VDD	3.3V power pin
114	--	GND	Ground
115	I/O	AD[4]	PCI address data bus
116	--	VDD18	1.8V power pin
117	--	GND	Ground
118	I/O	AD[3]	PCI address data bus
119	--	GND	Ground
120	I/O	AD[2]	PCI address data bus
121	I/O	AD[1]	PCI address data bus
122	--	VDD	3.3V power pin
123	I/O	AD[0]	PCI address data bus
124	--	GND	Ground
125	--	VDD	3.3V power pin
126	--	GND	Ground
127	--	VDD18	1.8V power pin
128	--	GND	Ground
129	O	CKOUT	USB CKOUT pin
130	I	VBDET	USB Vbus level detect pin
131	I	misc1	LSI shipment test pin
132	I	misc2	LSI shipment test pin
133	I/O	misc3	LSI shipment test pin
134	I/O	misc4	LSI shipment test pin
135	I/O	misc5	LSI shipment test pin
136	--	VDD18	1.8V power pin
137	--	GND	Ground
138	I/O	misc6	LSI shipment test pin
139	I/O	misc7	LSI shipment test pin
140	O	misc8	LSI shipment test pin
141	--	VDD	3.3V power pin
142	I	XIN	USB Connect to external crystal oscillator
143	O	XOUT	USB Connect to external crystal oscillator
144	--	GND	Ground