KL5KUSB122

USB Mini Host to 10/100 Ethernet

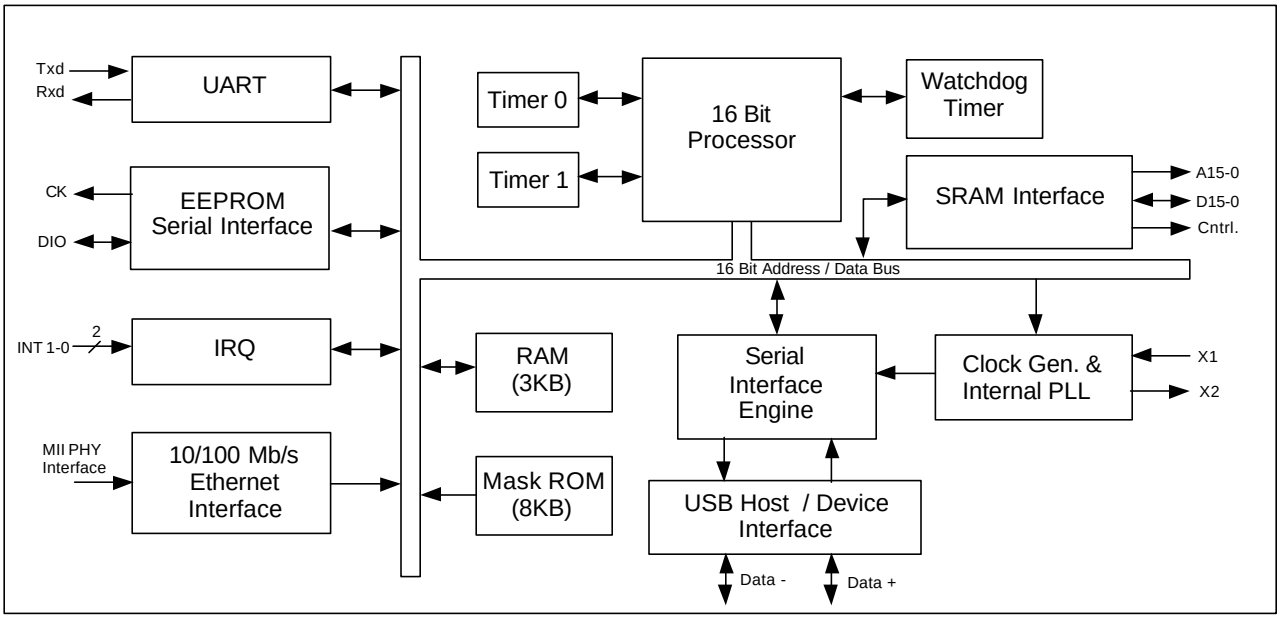
General Description

The Kawasaki KL5KUSB122 Controller is a unique single chip solution that serves as a bridge between USB and Ethernet interfaces. The USB side of the controller supports both USB Host and Device modes. The KL5KUSB122 has been specifically designed to provide Ethernet connectivity to USB devices. This has been accomplished by its highly integrated functionality. The USB controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, External Memory Interface and SPORT Interface. The SIE (Serial Interface Engine) is fully compatible with the USB specification. This USB to Ethernet Mini Host controller is ideal for simple networking of peripherals such as home appliances, cameras, and phones.

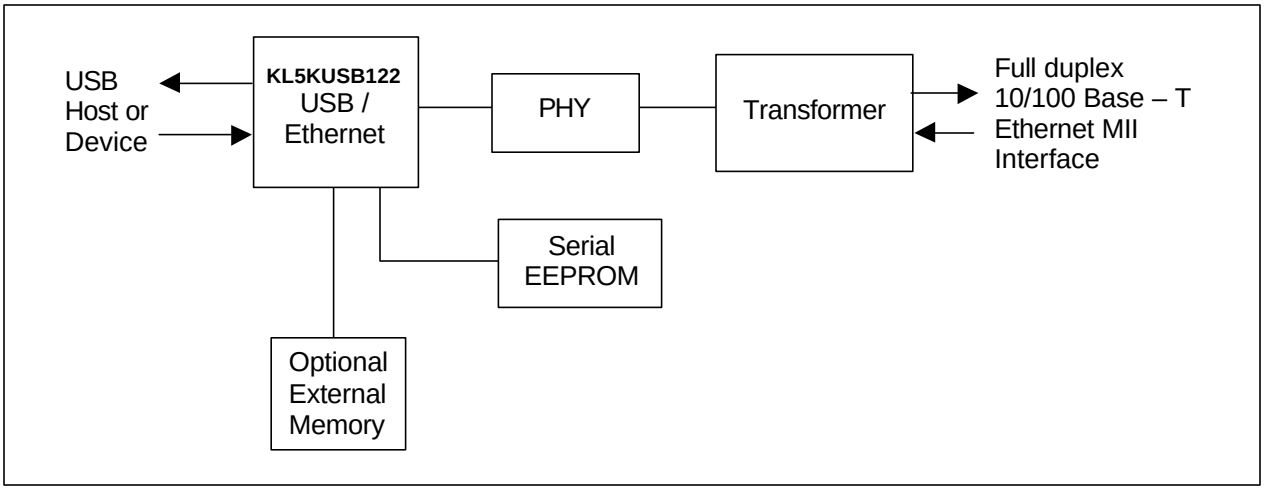
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- 10/100BaseT compatibility
- USB Host or USB Device interface ver. 1.0/1.1 compliant
- Transceivers and SIE (Serial Interface Engine)
- Internal Clock Generation - Utilizes low cost external 12MHz crystal circuitry
- MII Physical Layer interface
- Remote NDIS for faster data transfer.
- Debug UART
- External memory interface
- 100 LQFP package
- Serial Interface for external EEPROM
- 1.5K x 16 Internal RAM buffer

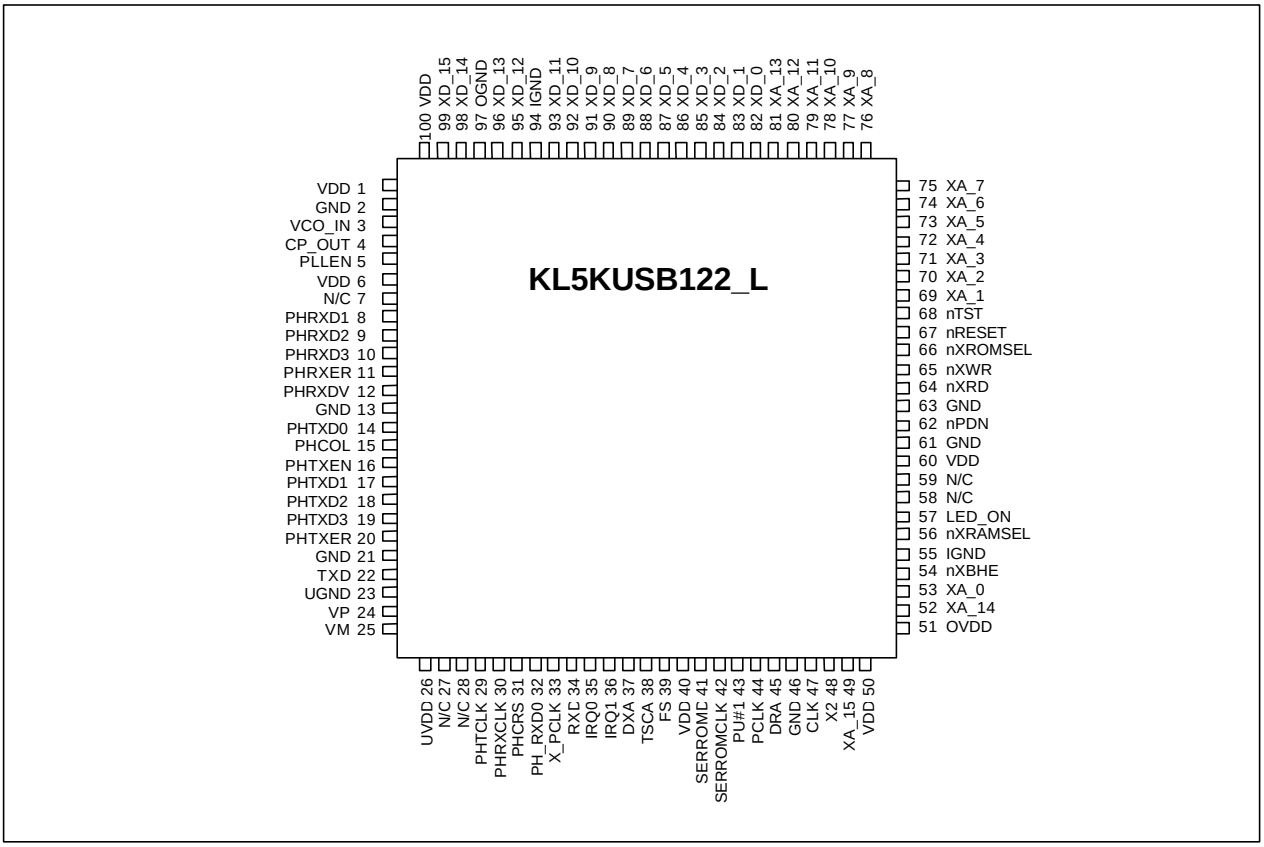
Block Diagram



KL5KUSB122 Application Block Diagram



Pin Diagram 100LQFP



Pin Description

Pin # LQFP	I/O	Pin Name	Description
1	IN	VDD	VDD
2	GND	GND	PLL GND
3	IN	VCO_IN	PLL VCO IN
4	OUT	CP_OUT	PLL VCO OUT
5	IN	PLLEN	PLL Enable
6	IN	VDD	PLL VDD
7	N/C	N/C	*Open connection*
8	IN	PHRXD1	MII PHY Receive Data 1
9	IN	PHRXD2	MII PHY Receive Data 2
10	IN	PHRXD3	MII PHY Receive Data 3
11	IN	PHRXER	MII Receive Data Error from PHY
12	IN	PHRXDV	MII Receive Data Valid from PHY
13	IN	GND	Ground
14	OUT	PHTXD0	MII Transmit data to PHY
15	IN	PHCOL	MII Collision input from PHY
16	OUT	PHTXEN	MII Transmit Enable to PHY
17	OUT	PHTXD1	MII Transmit Data 1 to PHY
18	OUT	PHTXD2	MII Transmit Data 2 to PHY
19	OUT	PHTXD3	MII Transmit Data 3 to PHY
20	OUT	PHTXER	MII Transmit Error to PHY
21	IN	GND	Ground
22	IN/OUT	TXD	UART TXD
23	IN	UGND	USB GND
24	IN/OUT	VP	USB + Pin
25	IN/OUT	VM	USB – Pin
26	IN	UVDD	USB VDD
27	NC	NC	*Open connection*
28	NC	NC	*Open connection*
29	IN	PHTXCLK	MII PHY Transmit Clock
30	IN	PHRXCLK	MII PHY Receive Clock
31	IN	PHCRS	MII PHY Carrier Sense
32	IN	PH_RXD0	MII PHY Serial Receive Data, bit 0
33	IN/OUT	X_PCLK	External PCLK
34	IN/OUT	RXD	UART RXD
35	IN	IRQ0	Edge sens. Interrupt
36	IN	IRQ1	Edge sens. Interrupt
37	OUT	DXA	Sport Mode or GPIO7
38	IN	TSCA	Sport Mode or GPIO8
39	IN/OUT	FS	Sport Mode or GPIO9
40	IN	VDD	*Open connection*
41	IN/OUT	SERROMD	Serial ROM Data
42	OUT	SERROMCLK	Serial ROM Clock
43	IN/OUT	PU#1	Pull up to USB + Pin for High Speed
44	IN	PCLK	Sport Mode or GPIO5
45	IN	DRA	Sport Mode or GPIO6

Pin # LQFP	I/O	Pin Name	Description
46	IN	OGND	GND
47	IN	CLK	12MHz Clock/Crystal Input
48	OUT	X2	12MHz Crystal Output
49	OUT	XA_15	External Address Pin
50	IN	VDD	VDD
51	IN	OVDD	VDD
52	OUT	XA_14	External Address Pin
53	OUT	XA_0	External Address Pin
54	OUT	nXBHE	SRAM Byte High Enable
55	IN	IGND	GND
56	OUT	nXRAMSEL	SRAM Byte Low Enable
57	OUT	LED_ON	Turns on 3.3V to TX LED / MII MDIO
58	N/C	N/C	*Open connection*
59	N/C	N/C	*Open connection*
60	IN	VDD	VDD
61	IN	GND	Ground
62	IN/OUT	nPDN	Active low Powerdown mode signal to Phy
63	IN	GND	GND
64	OUT	nXRD	External Memory Read (Active low)
65	OUT	nXWR	External Memory Write (Active low)
66	N/C	nXROMSEL	External ROM CS, active LO
67	IN	nRESET	Reset Pin
68	IN	nTST	Test Pin, *Disconnect for Normal Operation*
69	OUT	XA_1	External Address Pins
70	OUT	XA_2	External Address Pins
71	OUT	XA_3	External Address Pins
72	OUT	XA_4	External Address Pins
73	OUT	XA_5	External Address Pins
74	OUT	XA_6	External Address Pins
75	OUT	XA_7	External Address Pins
76	OUT	XA_8	External Address Pins
77	OUT	XA_9	External Address Pins
78	OUT	XA_10	External Address Pins
79	OUT	XA_11	External Address Pins
80	OUT	XA_12	External Address Pins
81	OUT	XA_13	External Address Pins
82	IN/OUT	XD_0	External Data Pins
83	IN/OUT	XD_1	External Data Pins
84	IN/OUT	XD_2	External Data Pins
85	IN/OUT	XD_3	External Data Pins
86	IN/OUT	XD_4	External Data Pins
87	IN/OUT	XD_5	External Data Pins
88	IN/OUT	XD_6	External Data Pins
89	IN/OUT	XD_7	External Data Pins
90	IN/OUT	XD_8	External Data Pins
91	IN/OUT	XD_9	External Data Pins
92	IN/OUT	XD_10	External Data Pins
93	IN/OUT	XD_11	External Data Pins
94	IN	IGND	GND
95	IN/OUT	XD_12	External Data Pins

Pin # LQFP	I/O	Pin Name	Description
96	IN/OUT	XD_13	External Data Pins
97	IN	OGND	GND
98	IN/OUT	XD_14	External Data Pins
99	IN/OUT	XD_15	External Data Pins
100	IN	VDD	VDD

Function Description

16 Bit Processor

The integrated 16-bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (8K X 16) in the KL5KUSB122 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor supports prioritized vectored hardware interrupts. Additionally, up to 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

RAM Buffer

The USB controller contains a 3K byte (1.5K X 16) internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16-bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

A 12 MHz external crystal may be used with the KL5KUSB122 Controller. Two pins, X1 and CLK, are provided to connect a lower cost crystal circuit to the device. PLL circuitry is provided to generate the internal 48MHz clock requirements of the device. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit by connecting directly to the CLK input pin.

USB Interface

The KL5KUSB122 Controller has a built in transceiver that meets the Universal Serial Bus (USB) specification v 1.1. The transceiver is capable of transmitting and receiving serial data at the USB full speed, 12 Mbits/sec, data rate. The driver portion of the transceiver is differential, while the Receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE (Serial Interface Engine) logic. Externally, the transceiver connects to the physical layer of the USB. The USB controller may be optionally configured to behave as a USB host or as a USB device.

10Mb, 100Mb/sec Ethernet Interface

The KL5KUSB122 Controller has a built in the Ethernet MAC (Media Access Controller) that is fully compliant with the IEEE 802.3 Ethernet standard. The KL5KUSB122 connects externally to a 10BaseT and/or 100BaseT ENDEC PHY. The KL5KUSB122 Controller 16-bit processor has direct access to the registers of the MAC.

UART Interface

Supports a transfer rate of 7200 to 115.2K baud.

Serial EEPROM Support

The KL5KUSB122 Controller serial interface is used to provide access to external EEPROMs. The interface can support a variety of serial EEPROM formats.

SRAM Interface

A multiplexed address port and 16-bit data port has been provided to interface to an external SRAM. The external SRAM is used to buffer data between USB and Ethernet. The chip will support both 8-bit and 16-bit SRAM.

DC CHARACTERISTICS

U2E is implemented with Kawasaki's 0.5um CMOS CBA and Embedded Memory KZ300EM Technology. The followings are the description of chip electric characteristics.

1. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vdd	–0.3 ~ 4.0	V
Input Voltage	Vin	–0.3 ~ 7.3	V
DC Output Current	Iout	±15	mA
Storage Temperature	Tstg	–55 ~ 125	°C

2. Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	Vdd	3.0	–	3.6	V
Operating ambient temperature	Ta	0	–	70	°C