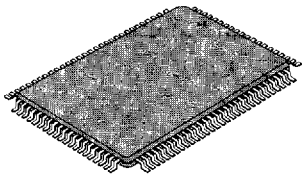
80 CHANNEL SEGMENT DRIVER FOR LCD DOT MATRIX LCD

The KS0104 is a LCD driver LSI which is fabricated by low power CMOS high voltage process technology. This device consists of 80 bit bidirectional shift register, 80 bit data latch and 80 bit driver (refer to fig 1).

100 QFP



FUNCTION

- **Dot matrix LCD segment driver with 80 channel output**
- **Input/Output signal**
  - **— Input: 4 bit parallel display data, control pulse from controller and bias voltage (V_1, V_3, V_4, V_{EE})**
  - **— Output; 80 channel waveform for LCD driving.**
- **Power down function to make power consumption low.**

FEATURES

- **Power supply voltage: +5V±10%**
- **Supply voltage for display: -8~-28V(V_{EE}-V_{DD})**
- **Parallel data processing (4 bit)**
- **Applicable LCD duty: $\frac{1}{64} \sim \frac{1}{256}$**
- **Interface**

driver	
COM	**SEG (cascade)**
KS0083, KS0103	Other KS0104

- **High voltage CMOS process**
- **100 QFP and bare chip available.**

BLOCK DIAGRAM

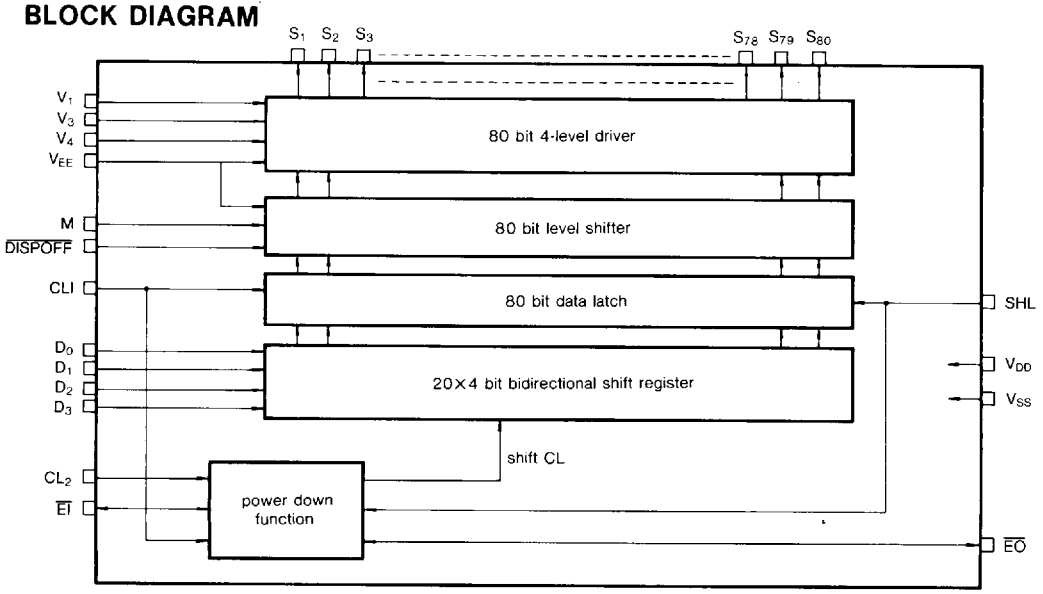


Fig 1. KS0104 Functional block diagram

PIN CONFIGURATION

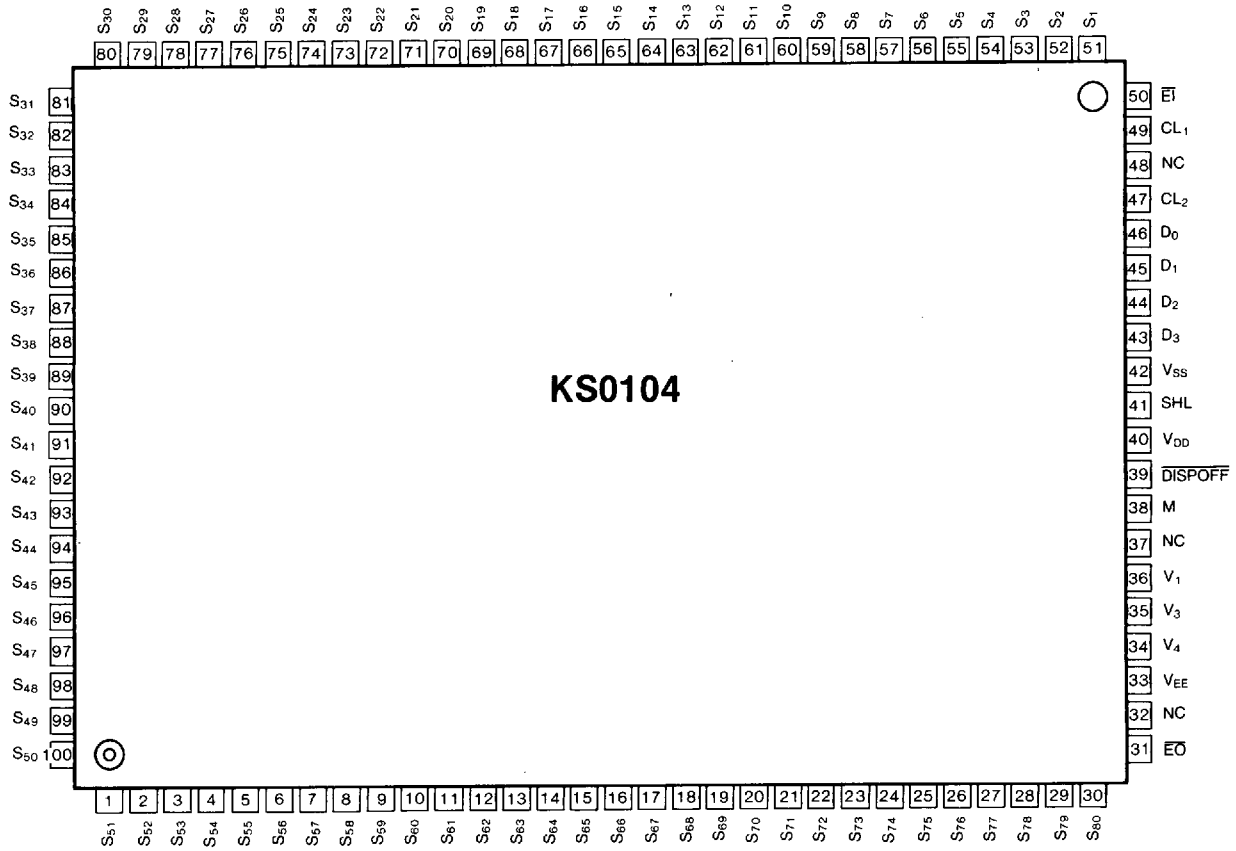
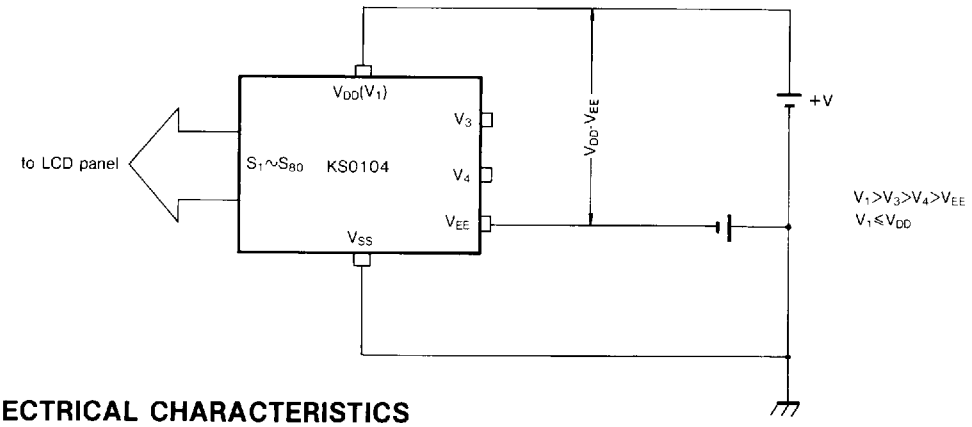


Fig. 2. 100 QFP Top View

MAXIMUM ABSOLUTE LIMIT (Ta=25°C)

Characteristic	Symbol	Value	Unit
Power supply voltage	V_{DD}	−0.3∼6.0	V
Driver supply voltage	V_{LCD}	0∼30	V
Input voltage	V_{IN}	−0.3∼V_{DD}+0.3	V
Operating temperature	T_{opr}	−20∼+85	°C
Storage temperature	T_{stg}	−55∼+150	°C

Voltage greater than above may result in damage to the circuit.



ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD}=5V±10%, V_{SS}=0V, Ta=25°C, C_L=15pF)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
Operating Voltage	V_{DD}	—		4.5	—	5.5	V
	V_{DD}-V_{EE}	—		8	—	28	
Input Voltage (*1)	V_{IH}	—		0.8V_{DD}	—	—	
	V_{IL}	—		—	—	0.2V_{DD}	
Input Current (*1)	I_{IH}	V_{IH}=V_{DD}, V_{DD}=5.5V		—	—	1	μA
	I_{IL}	V_{IH}=0V, V_{DD}=5.5V		—	—	−1	
Output Voltage (*2)	V_{OH}	I_O=−0.2mA, V_{DD}=4.5V		V_{DD}−0.4	—	—	V
	V_{OL}	I_O=0.2mA, V_{DD}=4.5V		—	—	0.4	
On resistance (*3)	R_{ON}	V_{DD}-V_{EE}=23V, V_{DD}=4.5V *4IVn-Vol=0.25V		—	2	4	kΩ
Supply current (*5)	I_{DDSBY}	CL2=1MHz	Display data is not processing	—	—	200	μA
	I_{DDI}	V_{DD}=5.5V	Display data is processing	—	—	3	mA
	IV	V_{DD}-V_{EE}=26V	Current on V_1, V_3, V_4 V_{EE} pins	—	—	±100	μA
Input capacitance	CI	f=1MHz		—	5	—	pF

*1; Applicable pin; CL_1 CL_2, EI, EO, D_0-D_3 SHL, $\overline{DISPOFF}$, M
*2; Applicable pin; EI, EO
*3; Applicable pin; S_1-S_{80}
*4; V_n=V_{DD}-V_{EE}, V_3=13/15 (V_{DD}-V_{EE}), V_4=2/15 (V_{DD}-V_{EE}), V_{DD}=V_1
*5; Display data 1010-M=40Hz.

AC CHARACTERISTICS (V_{DD}=+5±10%, V_{SS}=0V, T_a=+25°C, C_L=15pF)

Caracteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock frequency	f_{CL}	Duty=50%	3.4	—	—	MHz
Clock, pulse width	t_W		100	—	—	ns
Clock rise/fall time	f_{CT}		—	—	50	
Data set-up time	t_{SU}		50	—	—	
Data hold time	t_{DH}		80	—	—	
Clock-CL_1 time	t_{CL}		200	—	—	
CL_1 set-up time	t_{CSU}		90	—	—	
CL_1-clock time	t_{CK}		200	—	—	
Propagation delay time	t_{PHL}	$\overline{EO}$ Output	—	—	224	
		$\overline{EI}$ Output			224	
EO, EI set-up time	t_{PSU}	$\overline{EO}$ Input	70	—	—	
		$\overline{EI}$ Input	70			

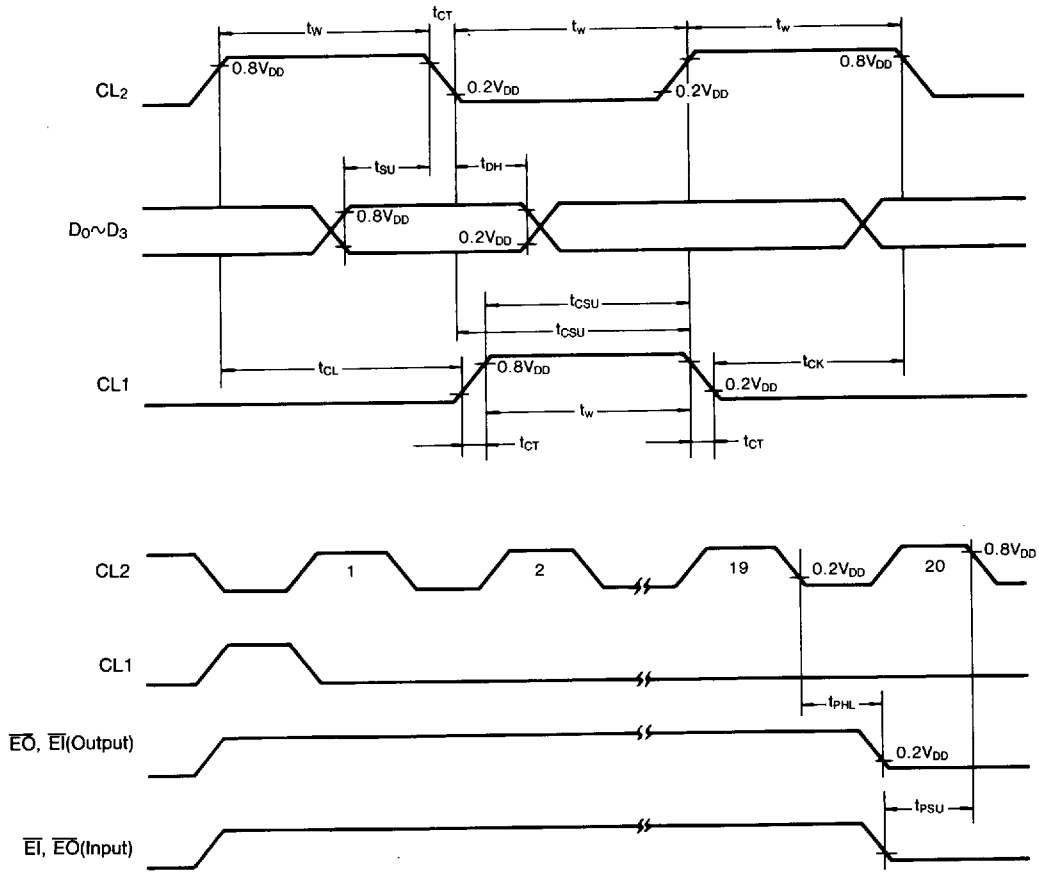


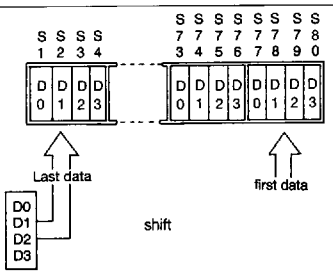
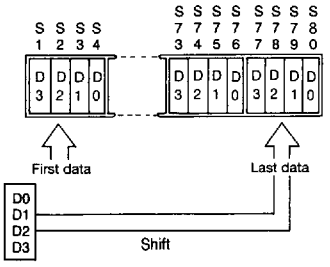
Fig. 3. Timing characteristic

PIN DESCRIPTION

Pin(No)	Input output	name	Function	Interface
V_{DD}(40)		Power supply	For logical circuit (+5V±10%)	Power
V_{SS}(42)			0V (GND)	
V_{EE}(33)			For LCD drive circuit	
V_1,V_3 V_4, (34-36)	Input	LCD driver output voltage level	Bias supply voltage terminals to drive the LCD. Bias voltage divided by the resistance is usually used as supply voltage source. (refer to note I)	Power
S_1~S_{80} (1-30, 51-100)	output	LCD driver output	Display data output pin which corresponds to the respective latch contents. One of V_1,V_3, V_4 and V_{EE} is selected as a display driving voltage source according to the combination of the latched data level and M signal (refer to; note 2)	LCD
CL2 (47)	input	data shift clock	Clock pulse input for the 4 bit parallel shift register. The data is shifted to 80 bit shift register at the falling edge of the clock pulse. The clock pulse, which was input when the ENABLE F/F is not active condition, is invalid.	controller
M (38)	input	alternate signal for LCD driver output	Alternate signal input pin for LCD driving. Normal frame inversion signal is input	controller
CLI (49)	input	data latch clock	The signal for latching the shift register contents is input to this terminal. CL1 pulse "H" level initializes ENABLE F/F.	controller
$\overline{DISPOFF}$ (39)	input	output level control	Control input pin for display data output level (S_1~S_{80}). V_1 level is output from S_1~S_{80} terminal during "L" level input. LCD becomes non-selected by V_1 level output from every output of segment drivers and every output of common drivers.	controller
SHL(41)	Input	Data interface	$\overline{EO}$ and $\overline{EI}$ can be used as either input terminal or output terminal according to the condition of SHL. The shifting direction of each data, D_0~D_3, the I/O condition of $\overline{EO}$ and $\overline{EI}$, and the condition of SHL are described in the table below. (refer to note 3)	
$\overline{EO}$, $\overline{EI}$ (31,50)	Input Output			

pin	I/O	SHL	Display data shift direction	Description
$\overline{EO}$	Input	L	D_0; S_1→S_5→S_{77} D_1; S_2→S_6→S_{78} D_2; S_3→S_7→S_{79} D_3; S_4→S_8→S_{80}	Input terminal to ENABLE F/F of KS0104
$\overline{EI}$	Output			Output terminal of ENABLE F/F. $\overline{EI}$ is connected to next KS0104's $\overline{EO}$ when the KS0104's are connected in series (cascade connection)
$\overline{EI}$	Input	H	D_0; S_{80}→S_{76}→S_4 D_1; S_{79}→S_{75}→S_3 D_2; S_{78}→S_{74}→S_2 D_3; S_{77}→S_{73}→S_1	Input terminal to ENABLE F/F of KS0104
$\overline{EO}$	Output			Output terminal of ENABLE F/F. $\overline{EO}$ is connected to next KS0104's $\overline{EI}$ when the KS0104's are connected in series (cascade connection)

PIN DESCRIPTION (continued)

<table>
<tr><th>Pin(No)</th><th>Input
Output</th><th>name</th><th>Function</th><th>Interface</th></tr>
<tr><td></td><td></td><td>
<table>
<tr><td>PIN</td><td>I/O</td><td>SHL</td><td>Data direction</td></tr>
<tr><td>EO</td><td>Input</td><td rowspan="2">L</td><td rowspan="2"> 
</td></tr>
<tr><td>EI</td><td>Output</td></tr>
<tr><td>EI</td><td>Input</td><td rowspan="2">H</td><td rowspan="2"> 
</td></tr>
<tr><td>EO</td><td>Output</td></tr>
</table>
</td><td></td></tr>
<tr><td>D0~D3
(43-46)</td><td>Input</td><td>Display data
input</td><td>Display data input pins for 4 bit parallel shift register and its is input synchronized with the clock pulse.
The combination of D0~D3 level, M signal, Display data output level and the display on the LCD panel is described on the table below.(DISPOFF=H)
<table>
<tr><th>D0~D3</th><th>M</th><th>Display data output level</th><th>Display on the LCD</th></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>OFF</td></tr>
<tr><td>H</td><td>L</td><td>V1</td><td>ON</td></tr>
<tr><td>L</td><td>H</td><td>V4</td><td>OFF</td></tr>
<tr><td>H</td><td>H</td><td>VEE</td><td>ON</td></tr>
</table>
</td><td>controller</td></tr>
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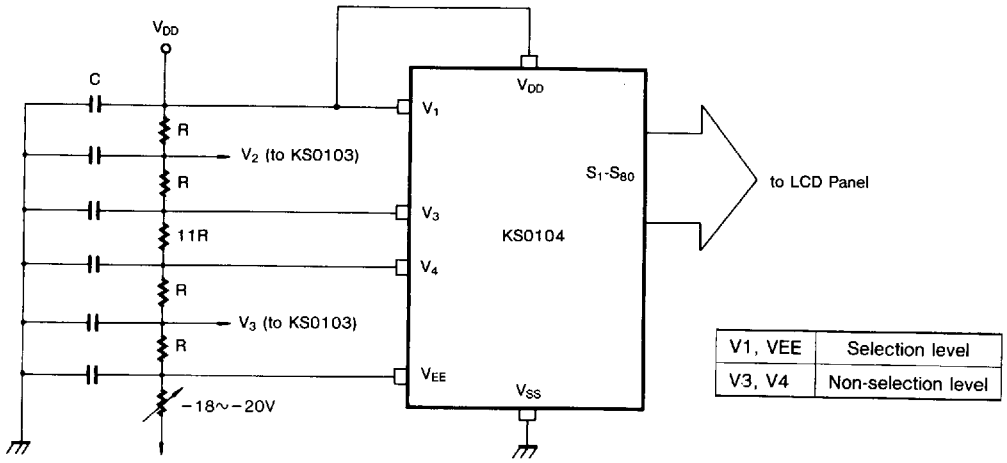
***NOTE 1**
The below figure shows when the bias voltage is divided by the resistor (1/15 Bias, 1/200 Duty)



V1, VEE	Selection level
V3, V4	Non-selection level

***NOTE 2** Truth table

M	Latched data	$\overline{\text{DISPOFF}}$	Output level (S_1-S_{80})
L	L	H	V3
L	H	H	V1
H	L	H	V4
H	H	H	VEE
X	X	L	V1

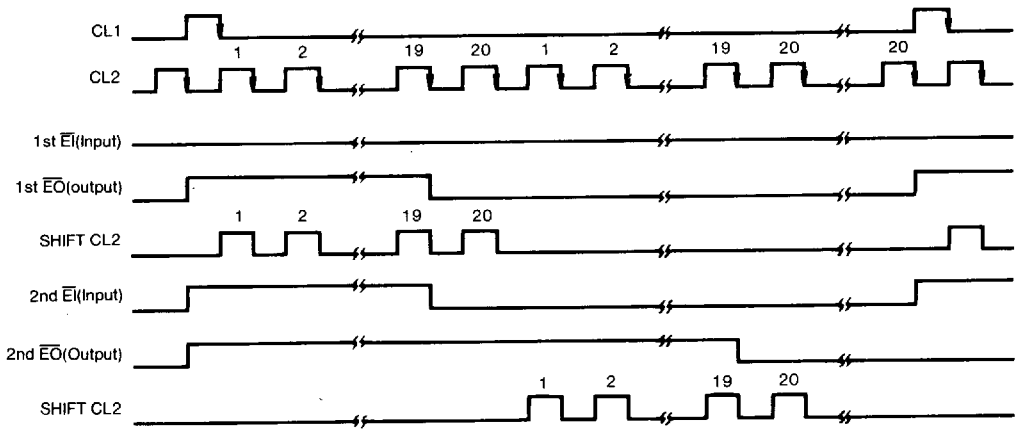
***NOTE 3**

- $\overline{EO}$ and $\overline{EI}$ pins working as input terminals.
  ENABLE F/F stops Display Data In at "H" level input. ENABLE F/F starts Display data In at "L" level input.
- $\overline{EO}$ and $\overline{EI}$ pins working as output terminals.
  These terminals are set to the "H" level immediately after ENABLE F/F is initialized by the load pulse. Upon completion of 80-bit serial/parallel conversion using the shift clock input from the CL2 terminal, these terminals are then set to the "L" level.
  The operation of ENABLE F/F is terminated and held unchanged until the next load pulse is detected.
  (For cascade connection, refer to the application circuit drawing.)

POWER DOWN FUNCTION

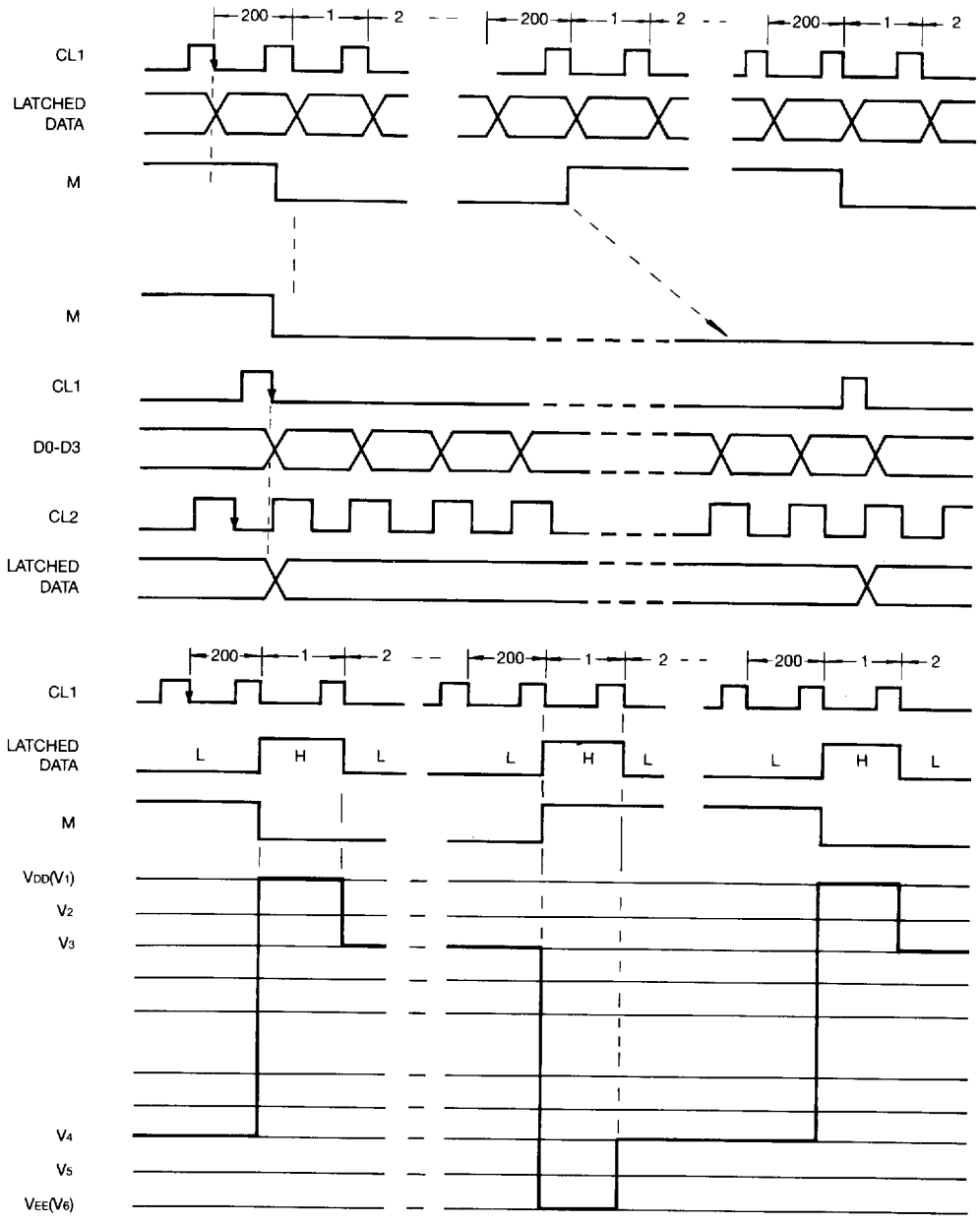
In order to reduce the power consumption, in case of cascade connection, KS0104 has a "power down function".

$\overline{EI}$	Enable input	Enable	L
		Disable	H
$\overline{EO}$	Enable output	$\overline{EO}$ of N th driver is connected to $\overline{EI}$ of (N+1) th driver KS0104	



SHL = "H" ($\overline{EI}$=Input $\overline{EO}$=Output)
First KS0104's $\overline{EO}$ should be connected to second KS0104's $\overline{EI}$.

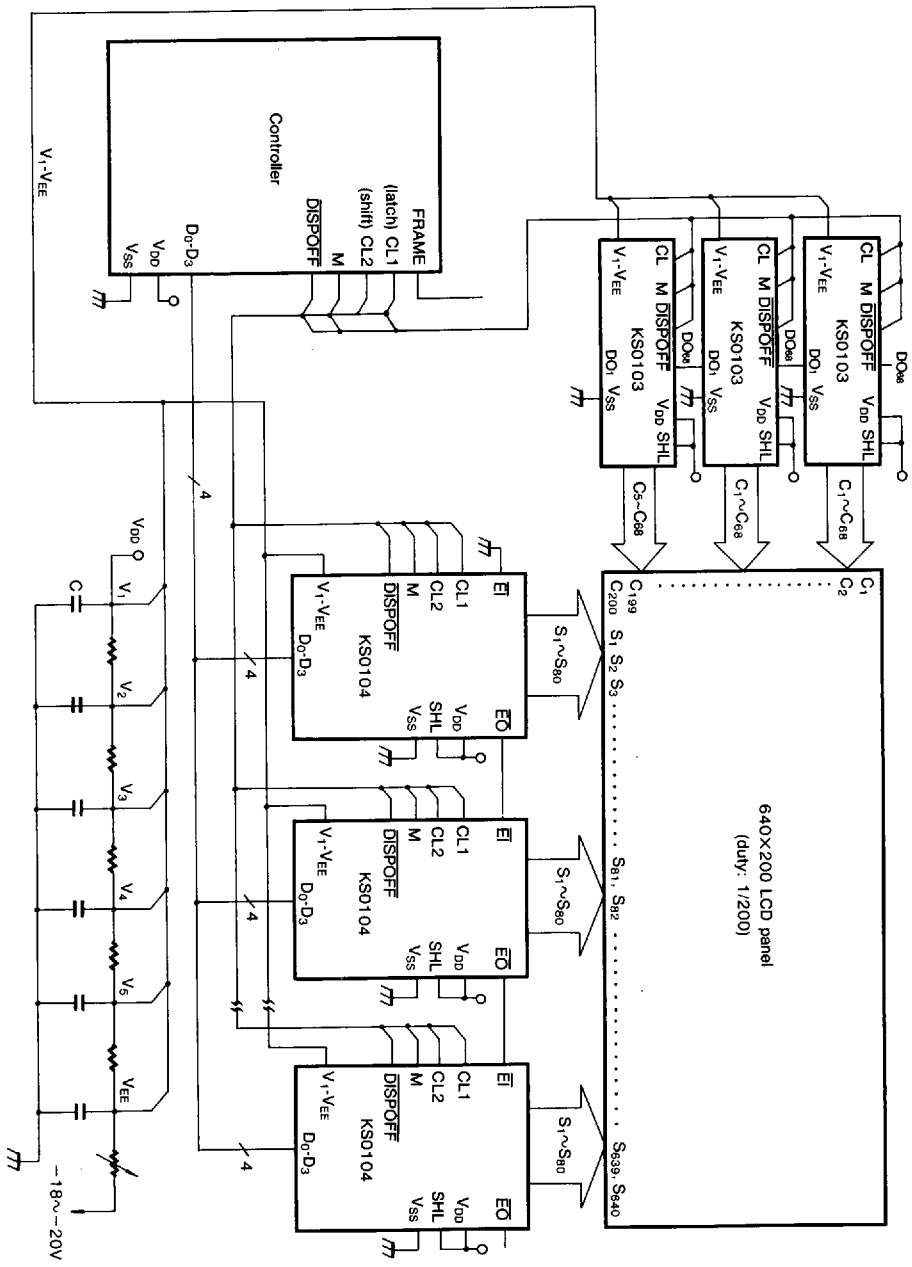
Fig 4. Timing Characteristics. (cascade connection)



V1=VDD
V2=VDD-1/15 VLCD
V3=VDD-2/15 VLCD

V4=VDD-13/15 VLCD
V5=VDD-14/15 VLCD
VLCD=VDD-VEE

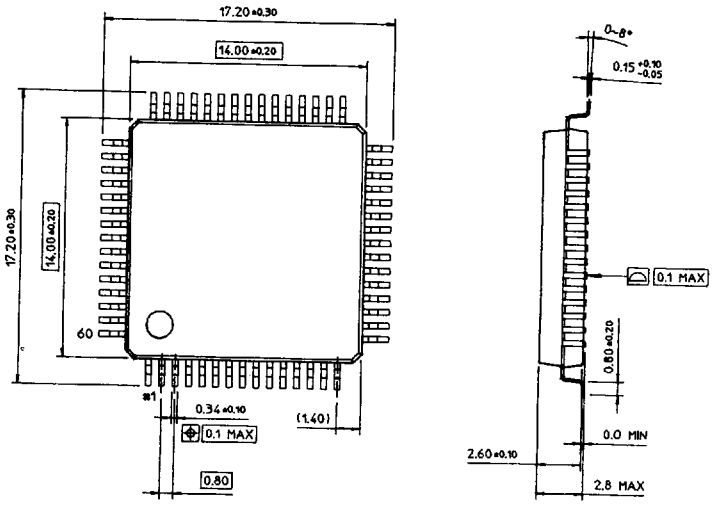
APPLICATION CIRCUIT



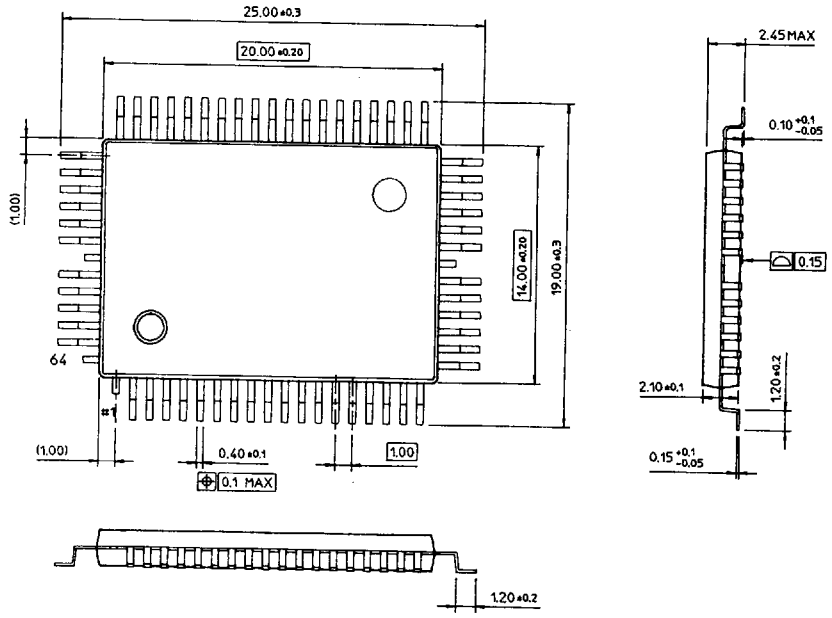
PACKAGE DIMENSIONS

Dimensions in Milimeters

60-QFP-1414A



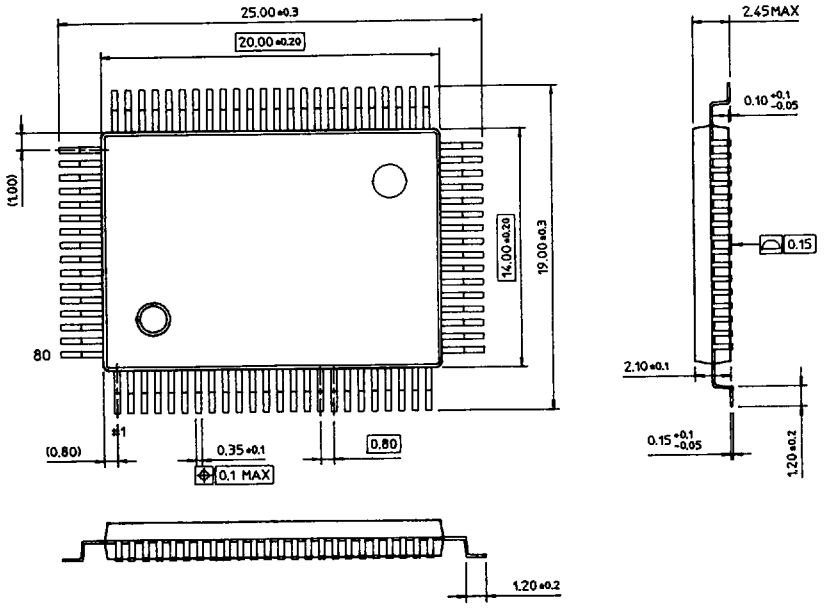
64-QFP-1420D



PACKAGE DIMENSIONS

Dimensions in Milimeters

80-QFP-1420A



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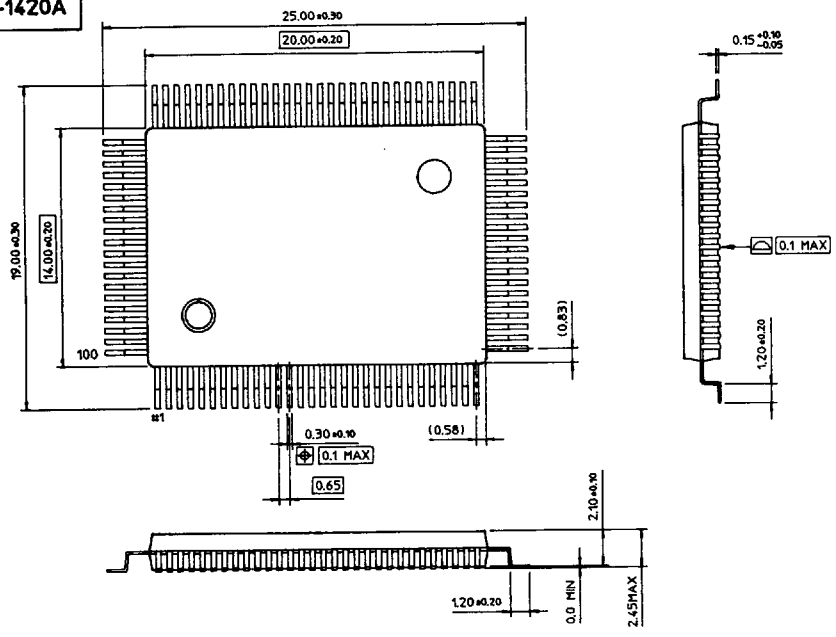

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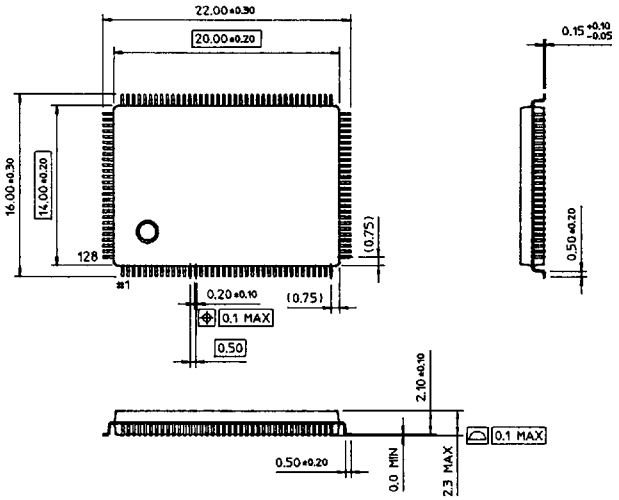
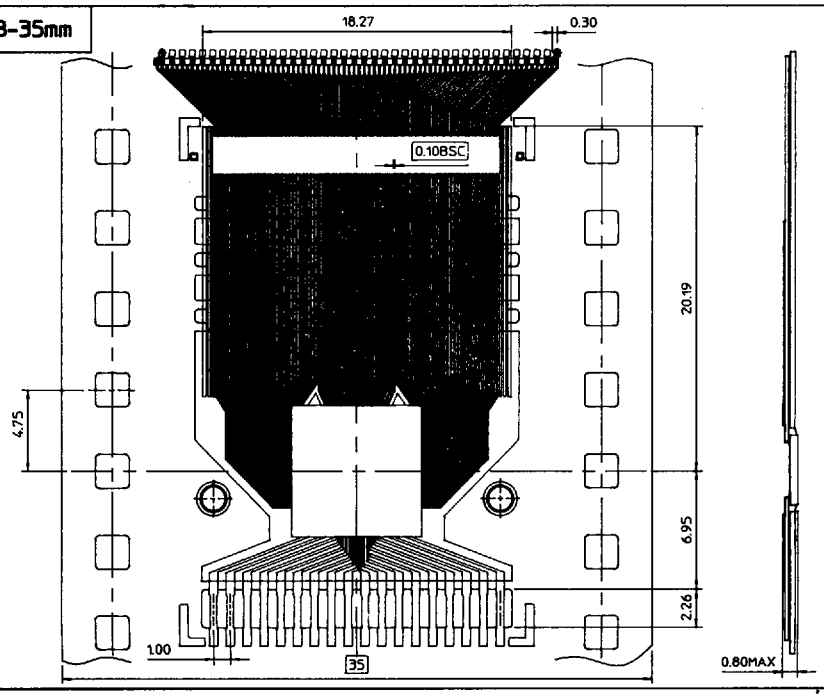
PACKAGE DIMENSIONS

Dimensions in Milimeters

128-QFP-1420



98-TAB-35mm



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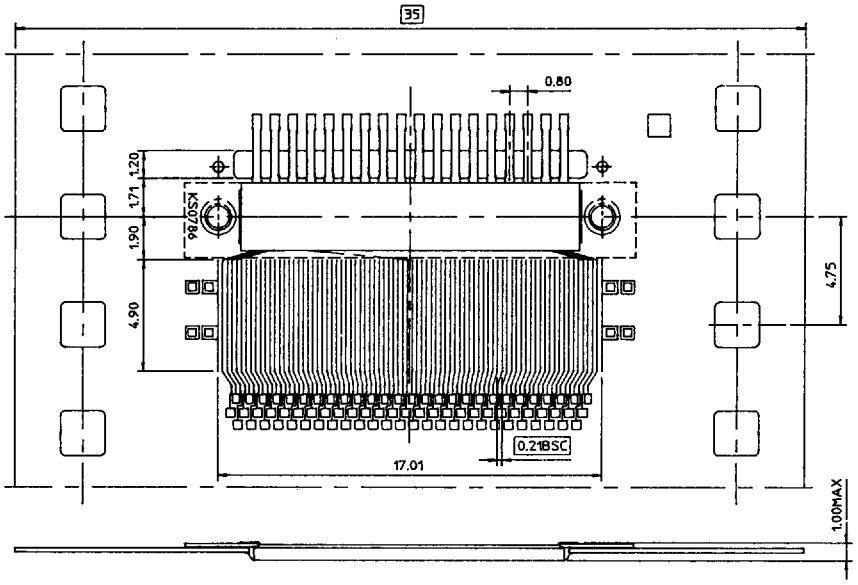
SAMSUNG ELECTRONICS

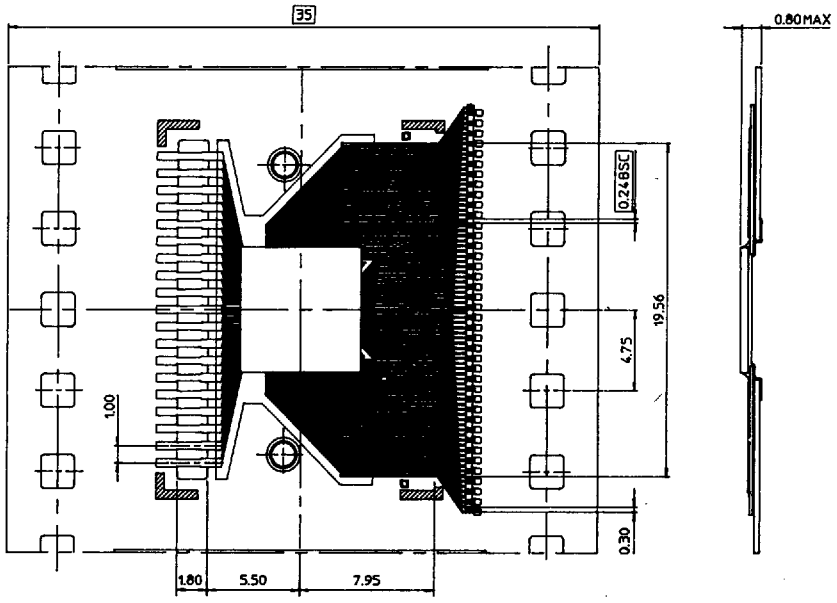
PACKAGE DIMENSIONS

Dimensions in Milimeters

98-STAB-35mm



99-TAB-35mm

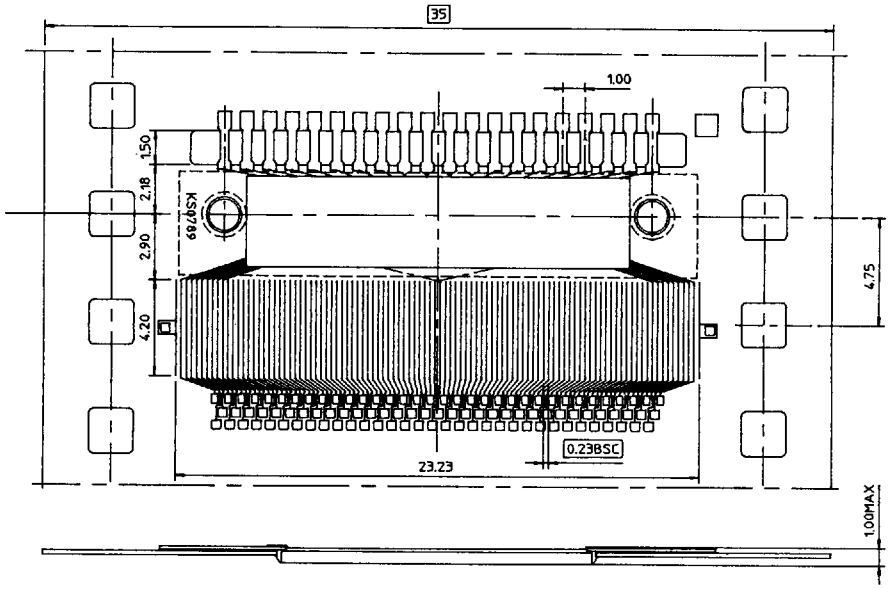


SAMSUNG ELECTRONICS

PACKAGE DIMENSIONS

Dimensions in Milimeters

120-STAB-35mm



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