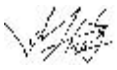
KS0649

256 CHANNEL TFT-LCD GATE DRIVER

November. 1999.

Ver. 0.1

Prepared by:  Jae il Byeon

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KS0649 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Aug.1999
0.1	The contents of page 9 and 10 have been modified	Nov.1999

CONTENTS

INTRODUCTION

The KS0649 is a TFT-LCD gate driver having 256 outputs. It can drive TFT panel gate ON voltage up to 40 V. It can operate within the logic voltage 2.7 to 5.5 V.

FEATURES

- 256 outputs
- Maximum TFT panel gate ON voltage = 40 V
- Bi - directional shift register
- Logic supply voltage = 2.7 to 5.5 V
- TCP

BLOCK DIAGRAM

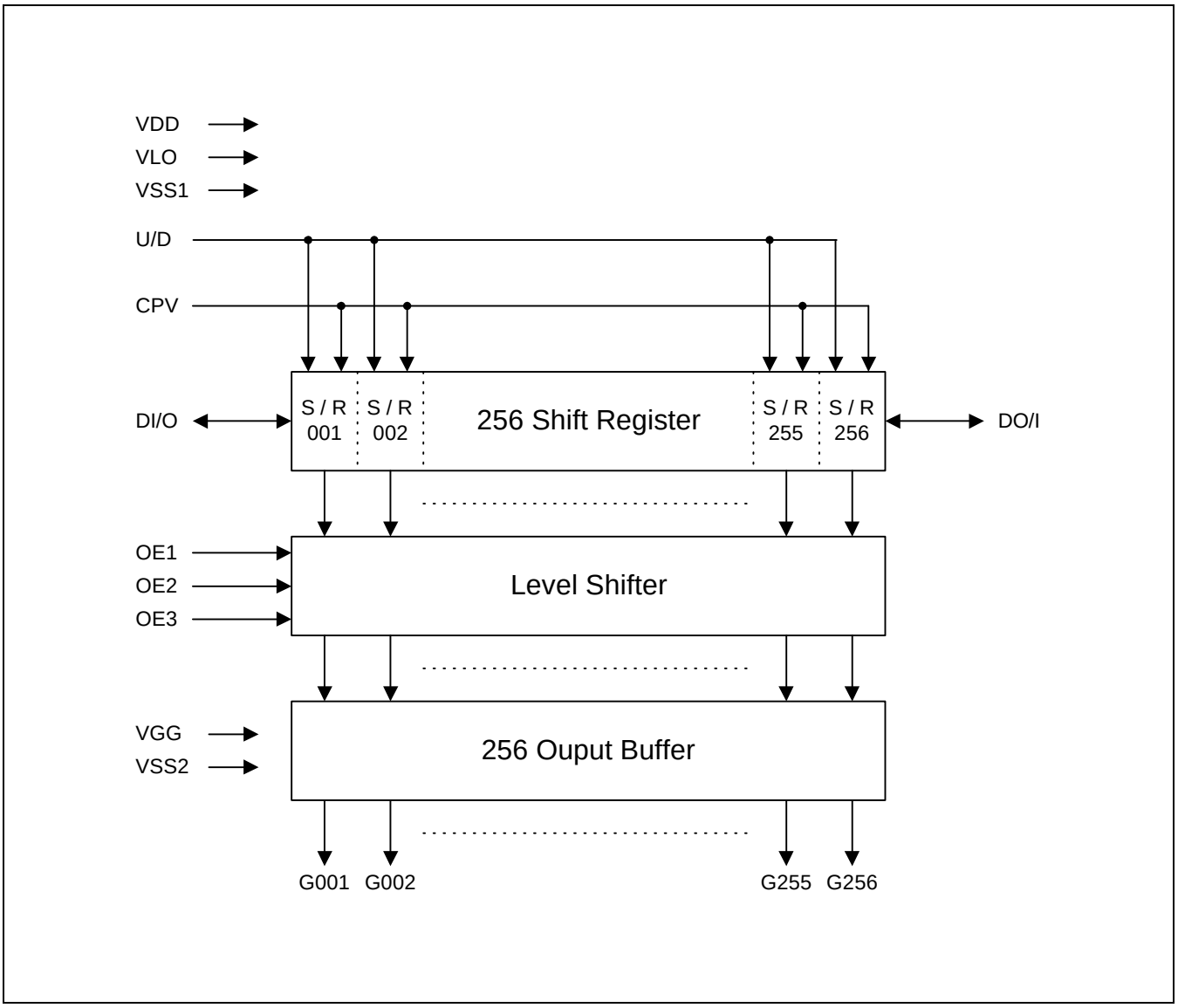

Figure 1. Block Diagram

PIN ASSIGNMENTS

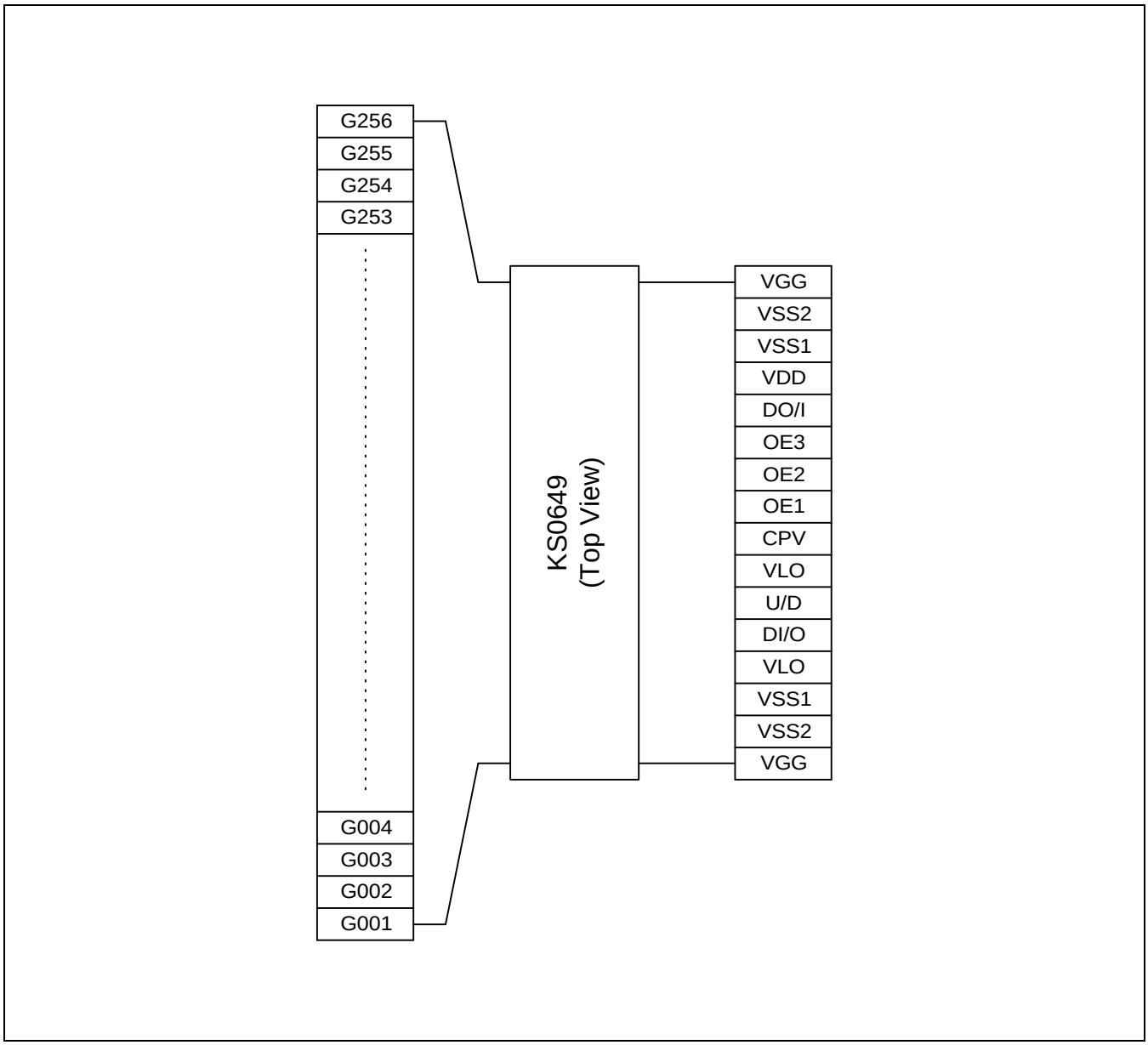

Figure 2. Pin Assignments

PIN DESCRIPTIONS

Symbol	Pin Name	I / O	Description
DI/O DO/I	Start pulse input/output	I / O	When these inputs operate as the input, the start pulse data is read at the rising edge of shift clock, CPV. When these inputs operate as the output, the start pulse output is the next chip's start pulse input. The output pulse is generated at the falling edge of the 256th shift clock, CPV. When U/D = H, the shift register does right shifting operation. (Input = DI/O and output = DO/I) When U/D = L, the shift register does left shifting operation. (Input = DO/I and output = DI/O)
U/D	Shift direction control input	I	When U/D = H, DI/O → G001 →……→ G256 → DO/I When U/D = L, DO/I → G256 →……→ G001 → DI/O
CPV	Shift clock input	I	The shift register operates in synchronization with the rising edge of this input
OE1 OE2 OE3	Output enable input	I	These inputs control the state of the driver outputs. When OE = H, the driver output is fixed to VSS2. When OE = L, the driver output is VGG or VSS2 corresponding to the data.
G001 to G256	Driver output	O	The output signals change in synchronization with the rising edge of shift clock input, CPV. The amplitude of the driver output is VGG - VSS2.
VSS2	Driver negative power supply	I	The input is internally connected to the logic ground, VSS1. The input operates as the TFT panel gate OFF voltage.
VLO	Logic input low voltage	I	Logic input range: VDD - VLO
VGG	Driver positive power supply	I	6 to 35 V The TFT gate ON voltage is VGG - VSS2.
VDD	Logic positive power supply	I	2.7 to 5.5 V
VSS1	Logic negative power supply	I	The logic negative power supply, VSS1, is internally connected to the driver negative power supply, VSS2.

ABSOLUTE MAXIMUM RATINGS (VSS1 = VSS2 = 0 V)

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Logic positive power supply	VDD	- 0.3 to 21.0	V
Driver positive power supply	VGG	- 0.3 to 45.0	V
Logic input low voltage	VLO	- 0.3 to VDD + 0.3	V
Input voltage	VIN	- 0.3 to VDD + 0.3	V
Operation temperature	Top	- 20 to 75	°C
Storage temperature	Tstg	- 55 to 150	°C

CAUTIONS

If the absolute maximum rating is exceeded momentarily, the quality of this product may be degraded.
It is desirable to use this product within the range of the absolute maximum ratings.
The power supplying order is as follows.
ON: VLO → VDD → VSS1, VSS2 → Control Input → VGG
OFF: VGG → Control Input → VSS1, VSS2 → VDD → VLO

RECOMMENDED OPERATION RATINGS (VLO = 0 V)

Table 2. Recommended Operation Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic positive power supply	VDD	2.7	-	5.5	V
Driver positive power supply	VGG	6	-	35	V
Logic negative power supply	VSS1	- 15	-	- 5	V
Driver negative power supply	VSS2	- 15	-	- 5	V
Power supply voltage	VGG - VSS2	21	-	40	V
Operation frequency	fCPV	-	100	200	kHz
Output load	CL	-	-	500	pF

DC CHARACTERISTICS (VLO = 0V)

Table 3. DC Characteristics (Ta = - 20 to 75 °C, VGG - VSS2 = 21 to 40 V, VLO - VSS1 = 15 to 5 V, VDD - VLO = 2.7 to 5.5 V, fCPV=100KHz)

Parameter	Symbol	Condition	Min.	Max.	Unit	Pin used
High input voltage	VIH	VX = VDD - VLO	VLO + 0.9VX	VDD	V	(1)
Low input voltage	VIL		VSS1	VLO + 0.1VX	V	
High output voltage	VOH	IOH = - 40 μA	VDD - 0.4	VDD	V	(2)
Low output voltage	VOL	IOL = 40 μA	VSS1	VSS1 + 0.4	V	
LCD driver output ON resistance	ROH	VOUT = VGG - 0.5 V, VGG = 40 V, VSS2 = 0 V	-	500	Ω	G001 to G256
	ROL	VOUT = 0.5 V, VGG = 40 V, VSS2 = 0 V	-	500	Ω	G001 to G256
High output current	IGG	Without output load	-	400	μA	VGG
Low output current	IDD	VDD - VSS1 = 3.3 V	-	400	μA	(1)
		VDD - VSS1 = 19 V	-	1000	μA	(3)
Input leak current	ILK	-	- 5	5	μA	(1)

NOTES:

1. DI/O, DO/I, CPV, OE1, OE2, OE3, U/D used.
2. When U/D = H, DO/I used, and when U/D = L, DI/O used.
3. Input swing voltage = VDD to VDD - 2.7 V

AC CHARACTERISTICS (VLO = 0 V)

Table 4. AC Characteristics (Ta = - 20 to 75 °C, VGG - VSS2 = 21 to 40 V, VLO - VSS1 = 15 to 5 V, VDD - VLO = 2.7 to 5.5 V, fCPV=100KHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Operation frequency	fCPV	-		200	kHz
Clock pulse width	tCPVH, tCPVL	Duty = 50 %	2	-	µs
Output enable input width	twOE	-	1	-	
Data setup time	tsDI	-	800	-	ns
Data hold time	thDI	-	800	-	
Output delay time (1)	tpdDO	CL = 30 pF	-	800	
Output delay time (2)	tpdG	CL = 300 pF	-	800	
Output delay time (3)	tpdOE		-	800	

AC TIMING DIAGRAM

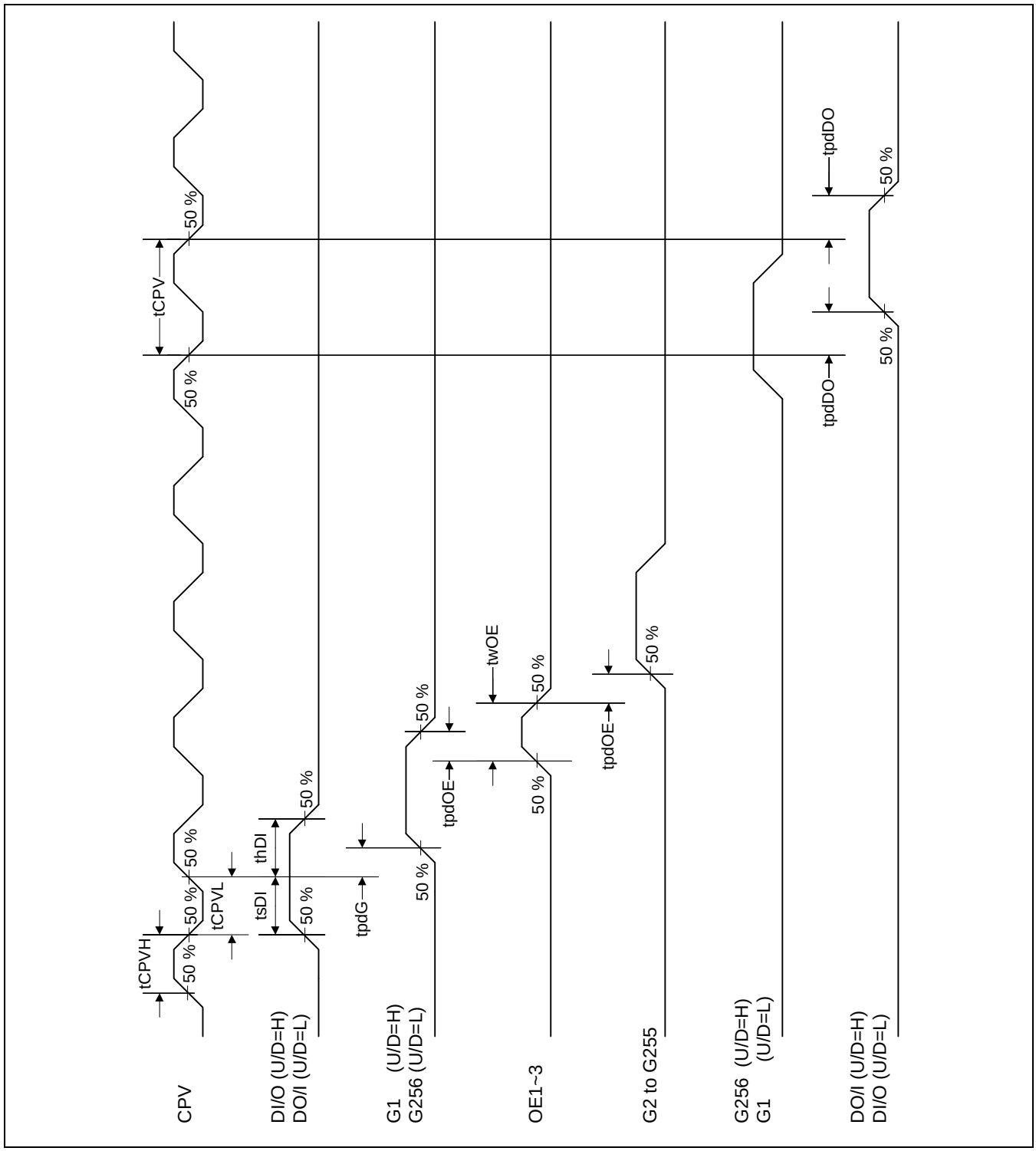

Figure 3. AC Timing Diagram

OPERATION DESCRIPTION

OPERATION METHOD

The start pulse input, DI/O (when U/D is “H”) or DO/I (when U/D = “L”), is synchronized with the rising edge of CPV and stored in the first shift register.
While stored pulse is transferred to the next register at the next rising edge of CPV, a new pulse is stored simultaneously.
Output pin (G1 to G256) supplies VGG voltage or VSS2 voltage to the TFT-LCD panel depending on the pulse of the shift register.

The start pulse output, DO/I (when U/D is “H”) or DI/O (when U/D = “L”), is synchronized with the falling edge of CPV and the pulse of the last register (G1 or G256) is transferred to the next IC.
The voltage level of the start pulse output is VDD with “H” data, VSS1 with “L” data

The relationship between U/D and shift data inout pin is as follows:

Table 5. The relationship between U/D and the start pulse input / output

U/D Pin	Start pulse input / output		Data shift direction
	Input	Output	
“H” (VDD)	DI/O	DO/I	G1 → G2 → G3 → G4 → G5 →……→ G256
“L” (VSS1 - VLO)	DO/I	DI/O	G256 → G255 → G254 → G253 →……→ G1

OUTPUT PIN (G1 TO G256)

If the data of the shift register to an output drive pin is “H”, the voltage level of the output is VGG and if the data is “L”, the level of the output is VSS2.
But, when OE is “H”, the voltage level of the output is VSS2 irrespective of the data of the shift register.

Table 6. The voltage level of the output

Condition		Control pin to LCD panel	
Pin	State	Controlled output pin by OE signal	Output level
OE1	“H”	G1, G4, G7, …… , G250, G253, G256	VSS2
OE2		G2, G5, G8, …… , G251, G254	
OE3		G3, G6, G9, …… , G252, G255	
OE1	“L”	G1, G4, G7, …… , G250, G253, G256	Normal output (VGG or VSS2)
OE2		G2, G5, G8, …… , G251, G254	
OE3		G3, G6, G9, …… , G252, G255	

VOLTAGE BIASING

The driver negative power supply, VSS2, can be any value between VLO - 5V and VLO - 15V.
And VSS2 is internally connected to the logic negative power supply, VSS1.

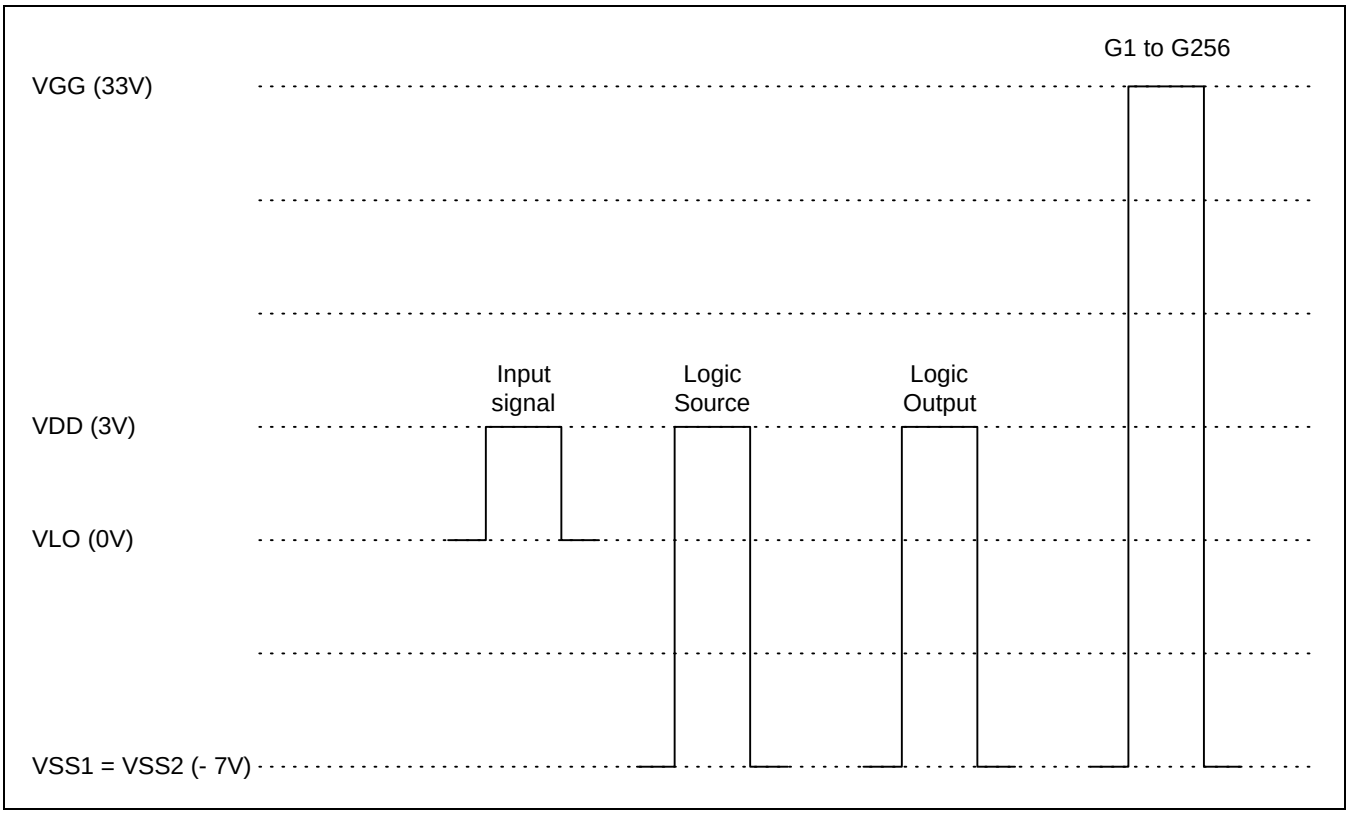

Figure 4. Example of Voltage Biasing

RECOMMENDED TIMING

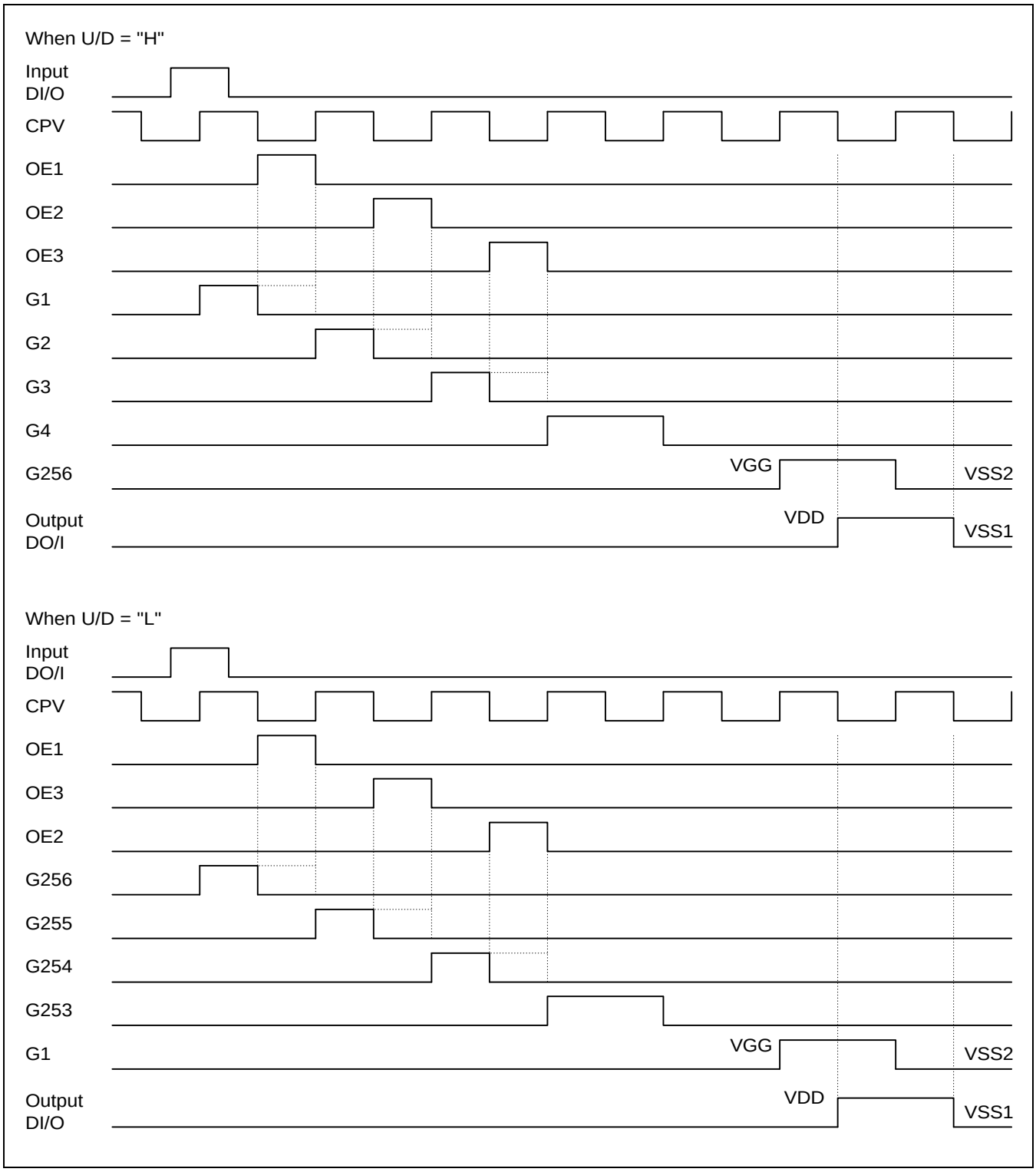

Figure 5. Recommended Timing

NOTES