

# KS0668

## 6 BIT 384 CHANNEL TFT-LCD SOURCE DRIVER

November. 1999.

Ver. 0.1

Prepared by  Dae-Young, Ahn

Mail: [jesus9@samsung.co.kr](mailto:jesus9@samsung.co.kr)

Contents in this document are subject to change without notice. No part of this document may be reproduced or transmitted in any form or by any means, electronic or mechanical, for any purpose, without the express written permission of LCD Driver IC Team.

<b>KS0668 Specification Revision History</b>		
<b>Version</b>	<b>Content</b>	<b>Date</b>
0.0	Original	Aug.1999
0.1	The contents of page 16, 17 and 18 have been modified	Nov.1999

# CONTENTS

INTRODUCTION .....	4
FEATURES .....	4
BLOCK DIAGRAM .....	5
PIN ASSIGNMENTS.....	6
PIN DESCRIPTIONS.....	7
OPERATION DESCRIPTION .....	8
DISPLAY DATA TRANSFER.....	8
EXTENSION OF OUTPUT .....	8
RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE.....	8
ABSOLUTE MAXIMUM RATINGS .....	15
RECOMMENDED OPERATION CONDITIONS .....	15
DC CHARACTERISTICS.....	16
AC CHARACTERISTICS.....	17
WAVEFORMS .....	18
RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD.....	19

## INTRODUCTION

The KS0668 is a 384 channel output, TFT-LCD source driver for an 64 gray-scale LCD panel. Data input is based on digital input consisting of 6 bits by 6 dots, which can realize a full-color display of 260,000 colors by output of 64 values gamma-corrected.

This device has an internal D/A (digital-to-analog) converter for each output and 10 (5-by-2) reference voltages. Because the output dynamic range is as large as 4.8 - 7.8 Vp-p, it is unnecessary to operate level inversion of the LCD's common electrode. Besides, to be able to deal with dot-line inversion when mounted on a single-side, output gray-scale voltages with different polarity can be output to the odd number output pins and the even output pins.

KS0668 can be adopted to larger panel, and SHL (shift direction selection) pin makes the use of the LCD panel connection conveniently. Maximum operation clock frequency is 55 MHz at 2.7 V logic operation, single edge and it can be applied to the TFT-LCD panel of XGA to SXGA standard.

## FEATURES

- TFT active matrix LCD source driver LSI
- 64 gray-scale is possible through 10 (5-by-2) reference voltages and D/A converter
- Both dot inversion display and N-line inversion display are possible
- CMOS level input
- Compatible with gamma-correction
- Input data inversion function (DATPOL)
- Logic supply voltage: 2.7 - 3.6 V
- LCD driver supply voltage: 5.0 - 8.0 V
- Output dynamic range: 4.8 - 7.8 Vp-p
- Maximum operating frequency:  $f_{MAX} = 55$  MHz (internal data transmission rate at 2.7 V operation)
- Output: 384 outputs
- TCP

# BLOCK DIAGRAM

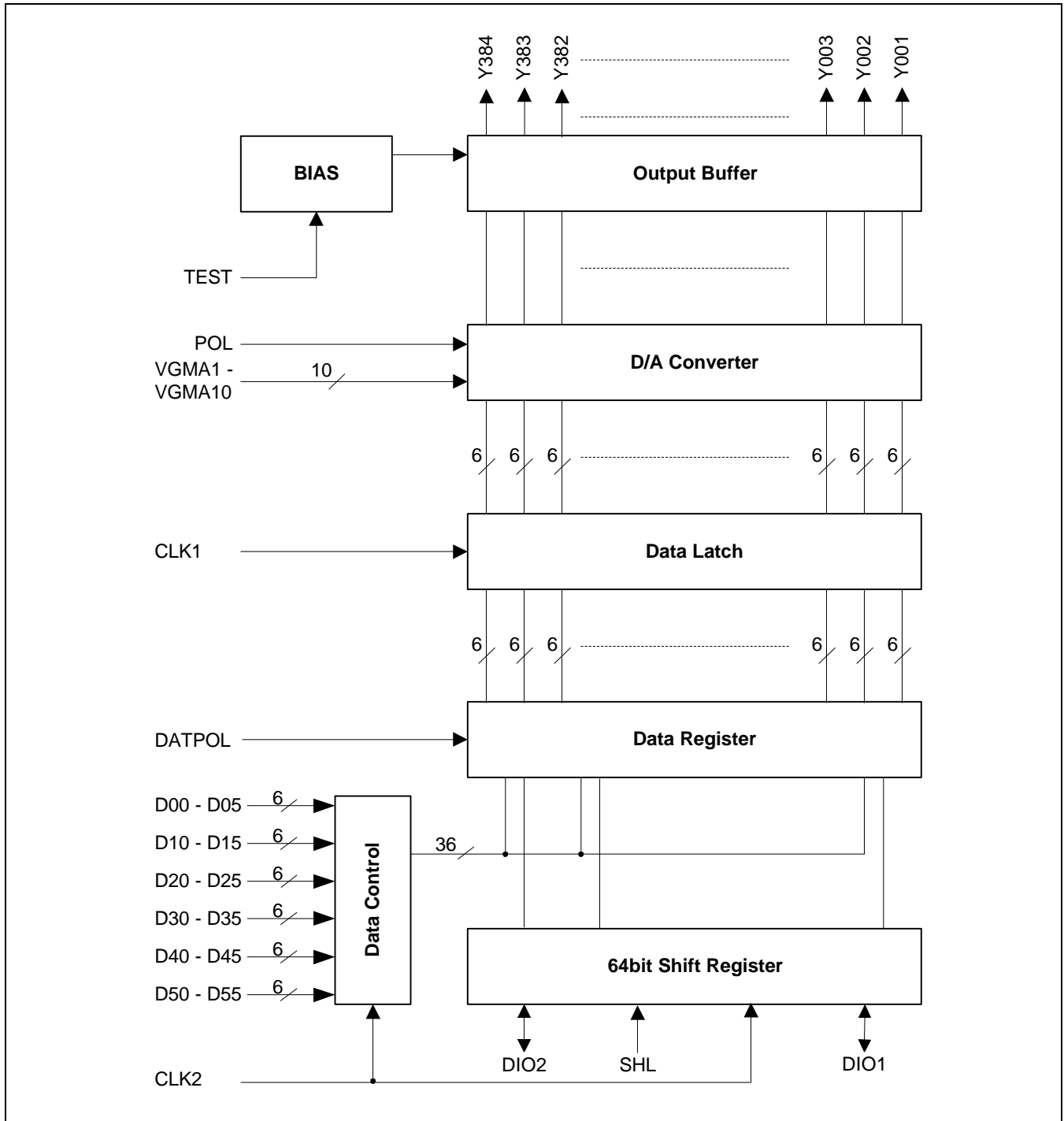


Figure 1. KS0668 Block Diagram

# PIN ASSIGNMENTS

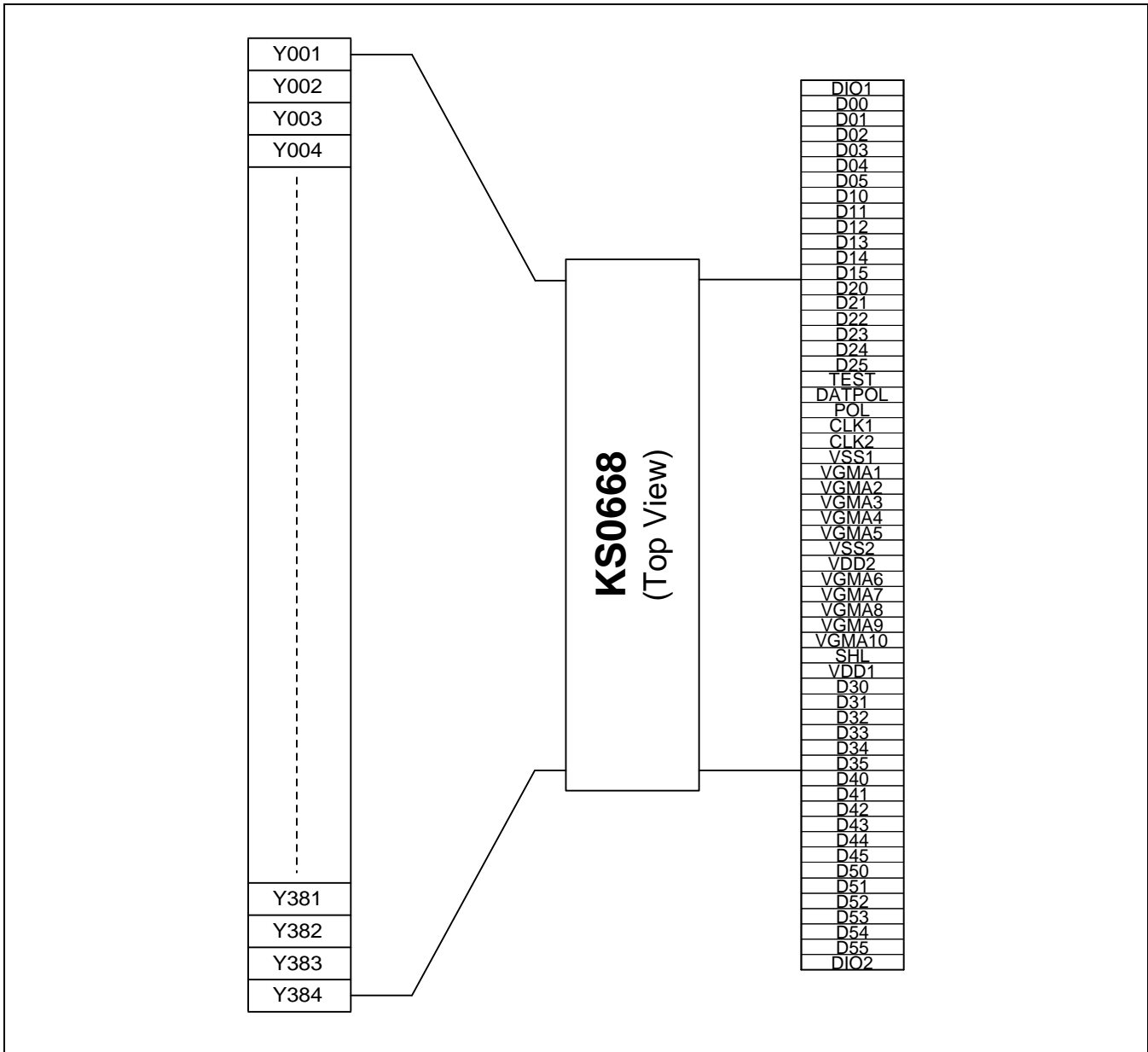


Figure 2. KS0668 Pin Assignments

## PIN DESCRIPTIONS

Symbol	Pin Name	Description
VDD1	Logic power supply	2.7 - 3.6 V
VDD2	Driver power supply	5.0 - 8.0 V
VSS1	Logic ground	Ground (0 V)
VSS2	Driver ground	Ground (0 V)
Y1 - Y384	Driver outputs	The D/A converted 64 gray-scale analog voltage is output.
D0<0:5> - D5<0:5>	Display data input	The display data is input with a width of 36 bits, gray-scale data (6 bits) by 6 dots (R,G,B) DX0: LSB, DX5: MSB
SHL	Shift direction control input	This pin controls the direction of shift register in cascade connection. The shift direction of the shift registers is as follows. SHL = H: DIO1 input, Y1 → Y384, DIO2 output SHL = L: DIO2 input, Y384 → Y1, DIO1 output
DIO1	Start pulse input / output	SHL = H: Used as the start pulse input pin SHL = L: Used as the start pulse output pin
DIO2	Start pulse input / output	SHL = H: Used as the start pulse output pin SHL = L: Used as the start pulse input pin
DATPOL	Data inversion input	DATPOL = H: Display data is inverted DATPOL = L: Display data is not inverted Detects H or L at rising edge of every CLK2.
POL	Polarity input	POL = H: The reference voltage for odd number outputs are VGMA1 – VGMA5 and those for even number outputs are VGMA6 – VGMA10 POL = L: The reference voltage for odd number outputs are VGMA6 – VGMA10 and those for even number outputs are VGMA1 – VGMA5
CLK2	Shift clock input	Refer to the shift register's shift clock input. The display data is loaded to the data register at the rising edge of CLK2.
CLK1	Latch input	Latches the contents of the data register at rising edge and transfers them to the D/A converter. Also, after CLK1 input, clears the internal shift register contents. After 1 pulse input on start, operates normally. CLK1 input timing refers to the "Relationships between CLK1 start pulse (DIO1, DIO2) and blanking period" of the switching characteristic waveform. Outputs the gray-scale data at falling edge.
VGMA1 – VGMA10	Gamma corrected power supplies	Input the gamma corrected power supplies from external source. VDD2 > VGMA1 > VGMA2 > ..... > VGMA9 > VGMA10 > VSS2 Keep gray-scale power supply unchanged during the gray-scale voltage output.
TEST	Test input	TEST = L: Normal operation mode TEST = H: Test mode (OP AMP CUT-OFF, Rpd = 15kΩ)

## OPERATION DESCRIPTION

### DISPLAY DATA TRANSFER

When DIO1 (or DIO2) pulse is loaded into internal latch on the rising edge of CLK2, DIO1 (or DIO2) pulse enables the data transfer operation, so display data is valid on the next rising edge of CLK2. Once all the data of 384 channels are loaded into internal latch, it goes into stand-by state automatically, and any new data is not accepted even though CLK2 is provided until next DIO1 (or DIO2) input. When next DIO1 (or DIO2) is provided, new display data is valid on the 2nd rising edge of CLK2 after the rising edge of DIO1 (or DIO2).

### EXTENSION OF OUTPUT

Output pin can be adjusted to an extended screen by cascade connection.

- (1) SHL = "L"  
Connect DIO1 pin of previous stage to the DIO2 pin of next stage and all the input pins except DIO1 and DIO2 are connected together in each device
- (2) SHL = "H"  
Connect DIO2 pin of previous stage to the DIO1 pin of next stage and all the input pins except DIO2 and DIO1 are connected together in each device.

### RELATIONSHIP BETWEEN INPUT DATA VALUE AND OUTPUT VOLTAGE

The LCD drive output voltages are determined by the input data and 10 (5-by-2) gamma corrected power supplies (VGMA1 - VGMA10). Besides, to be able to deal with dot-line inversion when mounted on a single-side, gradation voltages with different polarity can be output to the odd number output pins and the even number output pins. Among 5-by-2 gamma corrected voltages, input gray-scale voltages of the same polarity with respect to the common voltage, for the respective 5 gamma corrected voltages of VGMA1 - VGMA5 and VGMA6 - VGMA10.

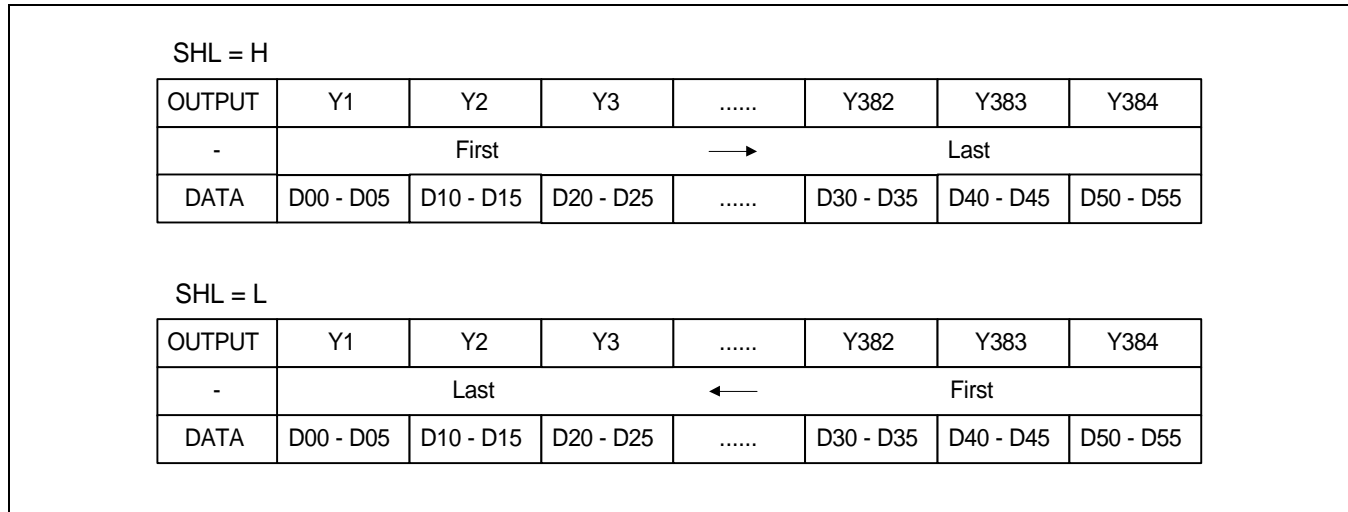


Figure 3. Relationship between Shift Direction and Output Data



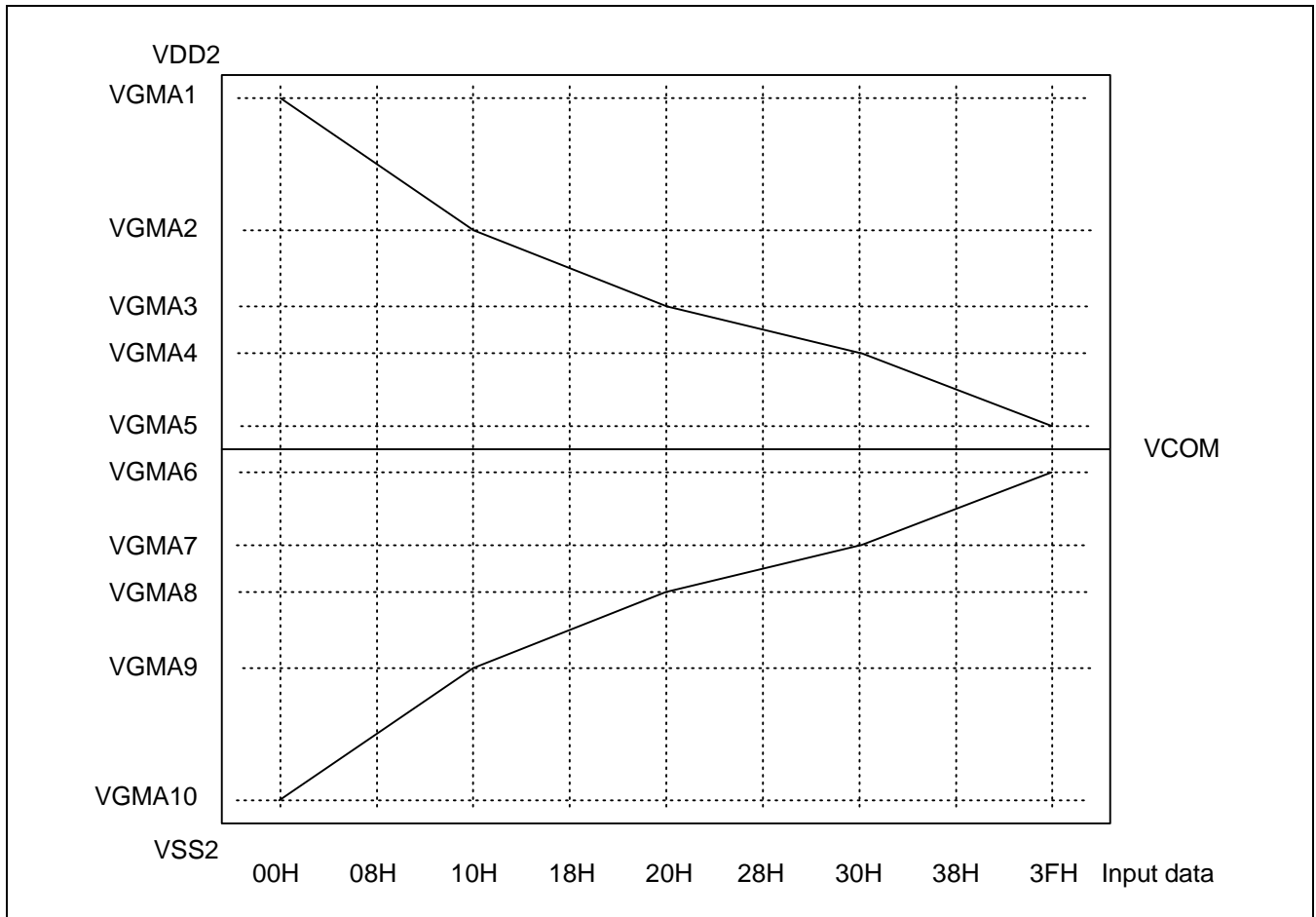


Figure 4. Gamma Correction Curve

Table 1. Resistor Strings (R0 - R62, unit:  $\Omega$ )

Name	Value	Name	Value	Name	Value	Name	Value
R0	500	R16	330	R32	175	R48	210
R1	500	R17	330	R33	175	R49	220
R2	500	R18	330	R34	170	R50	230
R3	500	R19	320	R35	170	R51	240
R4	500	R20	300	R36	165	R52	250
R5	500	R21	280	R37	165	R53	260
R6	500	R22	270	R38	165	R54	270
R7	500	R23	260	R39	165	R55	290
R8	500	R24	250	R40	170	R56	300
R9	500	R25	240	R41	170	R57	310
R10	500	R26	230	R42	170	R58	320
R11	500	R27	220	R43	175	R59	340
R12	450	R28	210	R44	175	R60	340
R13	450	R29	200	R45	175	R61	340
R14	400	R30	190	R46	180	R62	340
R15	370	R31	180	R47	200		

Table 2. Relationship between Input Data and Output Voltage Value

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VH0	VGMA1
01H	0	0	0	0	0	1	VH1	$VGMA1 + (VGMA2 - VGMA1) \times 500 / 7670$
02H	0	0	0	0	1	0	VH2	$VGMA1 + (VGMA2 - VGMA1) \times 1000 / 7670$
03H	0	0	0	0	1	1	VH3	$VGMA1 + (VGMA2 - VGMA1) \times 1500 / 7670$
04H	0	0	0	1	0	0	VH4	$VGMA1 + (VGMA2 - VGMA1) \times 2000 / 7670$
05H	0	0	0	1	0	1	VH5	$VGMA1 + (VGMA2 - VGMA1) \times 2500 / 7670$
06H	0	0	0	1	1	0	VH6	$VGMA1 + (VGMA2 - VGMA1) \times 3000 / 7670$
07H	0	0	0	1	1	1	VH7	$VGMA1 + (VGMA2 - VGMA1) \times 3500 / 7670$
08H	0	0	1	0	0	0	VH8	$VGMA1 + (VGMA2 - VGMA1) \times 4000 / 7670$
09H	0	0	1	0	0	1	VH9	$VGMA1 + (VGMA2 - VGMA1) \times 4500 / 7670$
0AH	0	0	1	0	1	0	VH10	$VGMA1 + (VGMA2 - VGMA1) \times 5000 / 7670$
0BH	0	0	1	0	1	1	VH11	$VGMA1 + (VGMA2 - VGMA1) \times 5500 / 7670$
0CH	0	0	1	1	0	0	VH12	$VGMA1 + (VGMA2 - VGMA1) \times 6000 / 7670$
0DH	0	0	1	1	0	1	VH13	$VGMA1 + (VGMA2 - VGMA1) \times 6450 / 7670$
0EH	0	0	1	1	1	0	VH14	$VGMA1 + (VGMA2 - VGMA1) \times 6900 / 7670$
0FH	0	0	1	1	1	1	VH15	$VGMA1 + (VGMA2 - VGMA1) \times 7300 / 7670$
10H	0	1	0	0	0	0	VH16	VGMA2
11H	0	1	0	0	0	1	VH17	$VGMA2 + (VGMA3 - VGMA2) \times 330 / 4140$
12H	0	1	0	0	1	0	VH18	$VGMA2 + (VGMA3 - VGMA2) \times 660 / 4140$
13H	0	1	0	0	1	1	VH19	$VGMA2 + (VGMA3 - VGMA2) \times 990 / 4140$
14H	0	1	0	1	0	0	VH20	$VGMA2 + (VGMA3 - VGMA2) \times 1310 / 4140$
15H	0	1	0	1	0	1	VH21	$VGMA2 + (VGMA3 - VGMA2) \times 1610 / 4140$
16H	0	1	0	1	1	0	VH22	$VGMA2 + (VGMA3 - VGMA2) \times 1890 / 4140$
17H	0	1	0	1	1	1	VH23	$VGMA2 + (VGMA3 - VGMA2) \times 2160 / 4140$
18H	0	1	1	0	0	0	VH24	$VGMA2 + (VGMA3 - VGMA2) \times 2420 / 4140$
19H	0	1	1	0	0	1	VH25	$VGMA2 + (VGMA3 - VGMA2) \times 2670 / 4140$
1AH	0	1	1	0	1	0	VH26	$VGMA2 + (VGMA3 - VGMA2) \times 2910 / 4140$
1BH	0	1	1	0	1	1	VH27	$VGMA2 + (VGMA3 - VGMA2) \times 3140 / 4140$
1CH	0	1	1	1	0	0	VH28	$VGMA2 + (VGMA3 - VGMA2) \times 3360 / 4140$
1DH	0	1	1	1	0	1	VH29	$VGMA2 + (VGMA3 - VGMA2) \times 3570 / 4140$
1EH	0	1	1	1	1	0	VH30	$VGMA2 + (VGMA3 - VGMA2) \times 3770 / 4140$
1FH	0	1	1	1	1	1	VH31	$VGMA2 + (VGMA3 - VGMA2) \times 3960 / 4140$

NOTE: VDD2&gt;VGMA1&gt;VGMA2&gt;VGMA3&gt;VGMA4&gt;VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VH32	VGMA3
21H	1	0	0	0	0	1	VH33	$VGMA3 + (VGMA4 - VGMA3) \times 175 / 2765$
22H	1	0	0	0	1	0	VH34	$VGMA3 + (VGMA4 - VGMA3) \times 350 / 2765$
23H	1	0	0	0	1	1	VH35	$VGMA3 + (VGMA4 - VGMA3) \times 520 / 2765$
24H	1	0	0	1	0	0	VH36	$VGMA3 + (VGMA4 - VGMA3) \times 690 / 2765$
25H	1	0	0	1	0	1	VH37	$VGMA3 + (VGMA4 - VGMA3) \times 855 / 2765$
26H	1	0	0	1	1	0	VH38	$VGMA3 + (VGMA4 - VGMA3) \times 1020 / 2765$
27H	1	0	0	1	1	1	VH39	$VGMA3 + (VGMA4 - VGMA3) \times 1185 / 2765$
28H	1	0	1	0	0	0	VH40	$VGMA3 + (VGMA4 - VGMA3) \times 1350 / 2765$
29H	1	0	1	0	0	1	VH41	$VGMA3 + (VGMA4 - VGMA3) \times 1520 / 2765$
2AH	1	0	1	0	1	0	VH42	$VGMA3 + (VGMA4 - VGMA3) \times 1690 / 2765$
2BH	1	0	1	0	1	1	VH43	$VGMA3 + (VGMA4 - VGMA3) \times 1860 / 2765$
2CH	1	0	1	1	0	0	VH44	$VGMA3 + (VGMA4 - VGMA3) \times 2035 / 2765$
2DH	1	0	1	1	0	1	VH45	$VGMA3 + (VGMA4 - VGMA3) \times 2210 / 2765$
2EH	1	0	1	1	1	0	VH46	$VGMA3 + (VGMA4 - VGMA3) \times 2385 / 2765$
2FH	1	0	1	1	1	1	VH47	$VGMA3 + (VGMA4 - VGMA3) \times 2565 / 2765$
30H	1	1	0	0	0	0	VH48	VGMA4
31H	1	1	0	0	0	1	VH49	$VGMA4 + (VGMA5 - VGMA4) \times 210 / 4260$
32H	1	1	0	0	1	0	VH50	$VGMA4 + (VGMA5 - VGMA4) \times 430 / 4260$
33H	1	1	0	0	1	1	VH51	$VGMA4 + (VGMA5 - VGMA4) \times 660 / 4260$
34H	1	1	0	1	0	0	VH52	$VGMA4 + (VGMA5 - VGMA4) \times 900 / 4260$
35H	1	1	0	1	0	1	VH53	$VGMA4 + (VGMA5 - VGMA4) \times 1150 / 4260$
36H	1	1	0	1	1	0	VH54	$VGMA4 + (VGMA5 - VGMA4) \times 1410 / 4260$
37H	1	1	0	1	1	1	VH55	$VGMA4 + (VGMA5 - VGMA4) \times 1680 / 4260$
38H	1	1	1	0	0	0	VH56	$VGMA4 + (VGMA5 - VGMA4) \times 1970 / 4260$
39H	1	1	1	0	0	1	VH57	$VGMA4 + (VGMA5 - VGMA4) \times 2270 / 4260$
3AH	1	1	1	0	1	0	VH58	$VGMA4 + (VGMA5 - VGMA4) \times 2580 / 4260$
3BH	1	1	1	0	1	1	VH59	$VGMA4 + (VGMA5 - VGMA4) \times 2900 / 4260$
3CH	1	1	1	1	0	0	VH60	$VGMA4 + (VGMA5 - VGMA4) \times 3240 / 4260$
3DH	1	1	1	1	0	1	VH61	$VGMA4 + (VGMA5 - VGMA4) \times 3580 / 4260$
3EH	1	1	1	1	1	0	VH62	$VGMA4 + (VGMA5 - VGMA4) \times 3920 / 4260$
3FH	1	1	1	1	1	1	VH63	VGMA5

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
00H	0	0	0	0	0	0	VL0	VGMA10
01H	0	0	0	0	0	1	VL1	$VGMA10 + (VGMA9 - VGMA10) \times 500 / 7670$
02H	0	0	0	0	1	0	VL2	$VGMA10 + (VGMA9 - VGMA10) \times 1000 / 7670$
03H	0	0	0	0	1	1	VL3	$VGMA10 + (VGMA9 - VGMA10) \times 1500 / 7670$
04H	0	0	0	1	0	0	VL4	$VGMA10 + (VGMA9 - VGMA10) \times 2000 / 7670$
05H	0	0	0	1	0	1	VL5	$VGMA10 + (VGMA9 - VGMA10) \times 2500 / 7670$
06H	0	0	0	1	1	0	VL6	$VGMA10 + (VGMA9 - VGMA10) \times 3000 / 7670$
07H	0	0	0	1	1	1	VL7	$VGMA10 + (VGMA9 - VGMA10) \times 3500 / 7670$
08H	0	0	1	0	0	0	VL8	$VGMA10 + (VGMA9 - VGMA10) \times 4000 / 7670$
09H	0	0	1	0	0	1	VL9	$VGMA10 + (VGMA9 - VGMA10) \times 4500 / 7670$
0AH	0	0	1	0	1	0	VL10	$VGMA10 + (VGMA9 - VGMA10) \times 5000 / 7670$
0BH	0	0	1	0	1	1	VL11	$VGMA10 + (VGMA9 - VGMA10) \times 5500 / 7670$
0CH	0	0	1	1	0	0	VL12	$VGMA10 + (VGMA9 - VGMA10) \times 6000 / 7670$
0DH	0	0	1	1	0	1	VL13	$VGMA10 + (VGMA9 - VGMA10) \times 6450 / 7670$
0EH	0	0	1	1	1	0	VL14	$VGMA10 + (VGMA9 - VGMA10) \times 6900 / 7670$
0FH	0	0	1	1	1	1	VL15	$VGMA10 + (VGMA9 - VGMA10) \times 7300 / 7670$
10H	0	1	0	0	0	0	VL16	VGMA9
11H	0	1	0	0	0	1	VL17	$VGMA9 + (VGMA8 - VGMA9) \times 330 / 4140$
12H	0	1	0	0	1	0	VL18	$VGMA9 + (VGMA8 - VGMA9) \times 660 / 4140$
13H	0	1	0	0	1	1	VL19	$VGMA9 + (VGMA8 - VGMA9) \times 990 / 4140$
14H	0	1	0	1	0	0	VL20	$VGMA9 + (VGMA8 - VGMA9) \times 1310 / 4140$
15H	0	1	0	1	0	1	VL21	$VGMA9 + (VGMA8 - VGMA9) \times 1610 / 4140$
16H	0	1	0	1	1	0	VL22	$VGMA9 + (VGMA8 - VGMA9) \times 1890 / 4140$
17H	0	1	0	1	1	1	VL23	$VGMA9 + (VGMA8 - VGMA9) \times 2160 / 4140$
18H	0	1	1	0	0	0	VL24	$VGMA9 + (VGMA8 - VGMA9) \times 2420 / 4140$
19H	0	1	1	0	0	1	VL25	$VGMA9 + (VGMA8 - VGMA9) \times 2670 / 4140$
1AH	0	1	1	0	1	0	VL26	$VGMA9 + (VGMA8 - VGMA9) \times 2910 / 4140$
1BH	0	1	1	0	1	1	VL27	$VGMA9 + (VGMA8 - VGMA9) \times 3140 / 4140$
1CH	0	1	1	1	0	0	VL28	$VGMA9 + (VGMA8 - VGMA9) \times 3360 / 4140$
1DH	0	1	1	1	0	1	VL29	$VGMA9 + (VGMA8 - VGMA9) \times 3570 / 4140$
1EH	0	1	1	1	1	0	VL30	$VGMA9 + (VGMA8 - VGMA9) \times 3770 / 4140$
1FH	0	1	1	1	1	1	VL31	$VGMA9 + (VGMA8 - VGMA9) \times 3960 / 4140$

NOTE: VGMA6&gt;VGMA7&gt;VGMA8&gt;VGMA9&gt;VGMA10&gt;VSS2

Table 2. Relationship between Input Data and Output Voltage Value (Continued)

Input data	DX5	DX4	DX3	DX2	DX1	DX0	G/S	Output voltage
20H	1	0	0	0	0	0	VL32	VGMA8
21H	1	0	0	0	0	1	VL33	$VGMA8 + (VGMA7 - VGMA8) \times 175 / 2765$
22H	1	0	0	0	1	0	VL34	$VGMA8 + (VGMA7 - VGMA8) \times 350 / 2765$
23H	1	0	0	0	1	1	VL35	$VGMA8 + (VGMA7 - VGMA8) \times 520 / 2765$
24H	1	0	0	1	0	0	VL36	$VGMA8 + (VGMA7 - VGMA8) \times 690 / 2765$
25H	1	0	0	1	0	1	VL37	$VGMA8 + (VGMA7 - VGMA8) \times 855 / 2765$
26H	1	0	0	1	1	0	VL38	$VGMA8 + (VGMA7 - VGMA8) \times 1020 / 2765$
27H	1	0	0	1	1	1	VL39	$VGMA8 + (VGMA7 - VGMA8) \times 1185 / 2765$
28H	1	0	1	0	0	0	VL40	$VGMA8 + (VGMA7 - VGMA8) \times 1350 / 2765$
29H	1	0	1	0	0	1	VL41	$VGMA8 + (VGMA7 - VGMA8) \times 1520 / 2765$
2AH	1	0	1	0	1	0	VL42	$VGMA8 + (VGMA7 - VGMA8) \times 1690 / 2765$
2BH	1	0	1	0	1	1	VL43	$VGMA8 + (VGMA7 - VGMA8) \times 1860 / 2765$
2CH	1	0	1	1	0	0	VL44	$VGMA8 + (VGMA7 - VGMA8) \times 2035 / 2765$
2DH	1	0	1	1	0	1	VL45	$VGMA8 + (VGMA7 - VGMA8) \times 2210 / 2765$
2EH	1	0	1	1	1	0	VL46	$VGMA8 + (VGMA7 - VGMA8) \times 2385 / 2765$
2FH	1	0	1	1	1	1	VL47	$VGMA8 + (VGMA7 - VGMA8) \times 2565 / 2765$
30H	1	1	0	0	0	0	VL48	VGMA7
31H	1	1	0	0	0	1	VL49	$VGMA7 + (VGMA6 - VGMA7) \times 210 / 4260$
32H	1	1	0	0	1	0	VL50	$VGMA7 + (VGMA6 - VGMA7) \times 430 / 4260$
33H	1	1	0	0	1	1	VL51	$VGMA7 + (VGMA6 - VGMA7) \times 660 / 4260$
34H	1	1	0	1	0	0	VL52	$VGMA7 + (VGMA6 - VGMA7) \times 900 / 4260$
35H	1	1	0	1	0	1	VL53	$VGMA7 + (VGMA6 - VGMA7) \times 1150 / 4260$
36H	1	1	0	1	1	0	VL54	$VGMA7 + (VGMA6 - VGMA7) \times 1410 / 4260$
37H	1	1	0	1	1	1	VL55	$VGMA7 + (VGMA6 - VGMA7) \times 1680 / 4260$
38H	1	1	1	0	0	0	VL56	$VGMA7 + (VGMA6 - VGMA7) \times 1970 / 4260$
39H	1	1	1	0	0	1	VL57	$VGMA7 + (VGMA6 - VGMA7) \times 2270 / 4260$
3AH	1	1	1	0	1	0	VL58	$VGMA7 + (VGMA6 - VGMA7) \times 2580 / 4260$
3BH	1	1	1	0	1	1	VL59	$VGMA7 + (VGMA6 - VGMA7) \times 2900 / 4260$
3CH	1	1	1	1	0	0	VL60	$VGMA7 + (VGMA6 - VGMA7) \times 3240 / 4260$
3DH	1	1	1	1	0	1	VL61	$VGMA7 + (VGMA6 - VGMA7) \times 3580 / 4260$
3EH	1	1	1	1	1	0	VL62	$VGMA7 + (VGMA6 - VGMA7) \times 3920 / 4260$
3FH	1	1	1	1	1	1	VL63	VGMA6

## ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings (VSS1 = VSS2 = 0 V)

Parameter	Symbol	Ratings	Unit
Logic supply voltage	VDD1	-0.3 to 5.5	V
Driver supply voltage	VDD2	-0.3 to 9.0	V
Input voltage	VGMA1 - 10	-0.3 to VDD2 + 0.3	V
	Others	-0.3 to VDD1 + 0.3	
Output voltage	DIO1, 2	-0.3 to VDD1 + 0.3	V
	Y1 - Y384	-0.3 to VDD2 + 0.3	
Operating power dissipation	Pd	200 <sup>(1)</sup>	mW
Operation temperature	Top	-20 to 75	°C
Storage temperature	Tstg	-55 to 125	°C

**NOTE:** 1. Relationship between TFT-LCD panel and Pd ( $Pd \propto CL * (VDD2)^2 * fCLK1$ )

### CAUTIONS:

If LSIs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Turn on power order: VDD1 → control signal input → VDD2 → VGMA1 - VGMA10

Turn off power order: VGMA1 - VGMA10 → VDD2 → control signal input → VDD1

## RECOMMENDED OPERATION CONDITIONS

Table 4. Recommended Operation Conditions (Ta = -20 to 75 °C, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Logic supply voltage	VDD1	2.7	3.0	3.6	V
Driver supply voltage	VDD2 <sup>(1)</sup>	5.0	7.0	8.0	V
Gamma corrected voltage	VGMA1 - VGMA5	0.5VDD2	-	VDD2 - 0.1	V
	VGMA6 - VGMA10	VSS2 + 0.1	-	0.5VDD2	V
Driver part output voltage	Vyo	VSS2 + 0.1	-	VDD2 - 0.1	V
Maximum clock frequency	fmax	VDD1 = 2.7 V		55	MHz
Output load capacitance	CL <sup>(1)</sup>	-	-	200	pF / PIN

**NOTE:** 1. Relationship between TFT-LCD panel and Pd ( $Pd \propto CL * (VDD2)^2 * fCLK1$ )

## DC CHARACTERISTICS

Table 5. DC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 5.0 to 8.0 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage	VIH	SHL, CLK2, D00 - D55, CLK1, DATPOL, POL, DIO1 (DIO2)	0.6VDD1	-	VDD1	V
Low level input voltage	VIL		0	-	0.3VDD1	
Input leakage current	IL		-1	-	1	μA
High level output voltage	VOH	DIO1 (DIO2), IO = -1.0 mA	VDD1 - 0.5	-	-	V
Low level output voltage	VOL	DIO1 (DIO2), IO = +1.0 mA	-	-	0.5	
Resistor	R0 - R62	Refer to Table 1. Resistor Strings	Rn × 0.7	-	Rn × 1.3	Ω
Driver output current	I <sub>VOH</sub>	VDD2 = 7.0 V, Vx = 2.5 V, Vyo = 6.5 V <sup>(1)</sup>	-	-1.0	-0.5	mA
	I <sub>VOL</sub>	VDD2 = 7.0 V, Vx = 4.5 V, Vyo = 0.5 V <sup>(1)</sup>	0.5	1.0	-	mA
Output voltage deviation	ΔVO	VSS2 + 0.1 V - VDD2 - 1.4 V	-	±10	±20	mV
		VDD2 - 1.4 V - VDD2 - 0.1 V	-	±20	-	
Output RMS voltage deviation	dVrms <sup>(2)</sup>	VSS2 + 1.4 V - VDD2 - 1.4 V	-	±5	±10	
		VSS2 + 0.1 V - VSS2 + 1.4 V VDD2 - 1.4 V - VDD2 - 0.1 V	-	±20	±30	
Output voltage range	Vyo	Input data: 00H to 3FH	VSS2 + 0.1	-	VDD2 - 0.1	V
Logic part dynamic current	IDD1	VDD1 = 3.0 V <sup>(3)</sup>	-	4.0	5.5	mA
Driver part dynamic current	IDD2	VDD1 = 3.0 V, VDD2 = 7.0 V <sup>(3)(4)(5)</sup>	-	4.0	10.0	

### NOTES:

- Vyo is the output voltage of analog output pins Y1 to Y384. Vx is the voltage applied to analog output pins Y1 to Y384.
- dVrms is a maximum deviation value from ideal difference between high output and low output at the same gray-scale.
- CLK1 period is defined to be 20 μs at fCLK2 = 33 MHz, data pattern = 101010(checkerboard pattern), Ta = 25 °C.
- The current consumption per a driver when XGA single-sided mounting (8 drivers) is connected in cascade
- No Load



## AC CHARACTERISTICS

Table 6. AC Characteristics (Ta = -20 to 75 °C, VDD1 = 2.7 to 3.6 V, VDD2 = 5.0 to 8.0 V, VSS1 = VSS2 = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock pulse width	PWCLK	-	18	-	-	ns
Clock pulse low period	PWCLK (L)	-	5	-	-	
Clock pulse high period	PWCLK (H)	-	5	-	-	
Data setup time	tSETUP1	(1)	4 / 6	-	-	
Data hold time	tHOLD1	(1)	0 / 2	-	-	
Start pulse setup time	tSETUP2	(1)	4 / 6	-	-	
Start pulse hold time	tHOLD2	(1)	0 / 2	-	-	
DATPOL-CLK2 setup time	tSETUP4	(1)	4 / 6	-	-	
DATPOL-CLK2 hold time	tHOLD4	(1)	0 / 2	-	-	
Start pulse delay time	tPLH1	CL = 20pF	-	-	12	
CLK1 setup time	tSETUP3	-	2	-	-	CLK2 period
Driver output delay time1	tPHL1	(2), (4)	-	-	5	μs
Driver output delay time2	tPHL2	(3), (4)	-	-	10	
CLK1 pulse high period	PWCLK1	-	0.2	-	2	
Data invalid period	tINV	DIO1 (2) ↑ → CLK2↑	1			CLK2 period
Last data timing	tLDT	-	1	-	-	
CLK1 - CLK2 time	tCLK1 - CLK2	CLK1↑ → CLK2↑	6	-	-	ns
POL - CLK1 time	tPOL -CLK1	POL↑or↓ → CLK1↑	5	-	-	ns

### NOTES:

1. Input condition (VIH = 0.6VDD1, VIL = 0.3VDD1 / VIH = 0.5VDD1, VIL = 0.5VDD1)
2. The value is specified when the drive voltage value reaches the target output voltage level of 90%
3. The value is specified when the drive voltage value reaches the target output voltage level of 6-bit accuracy.
4. Yout Load Condition

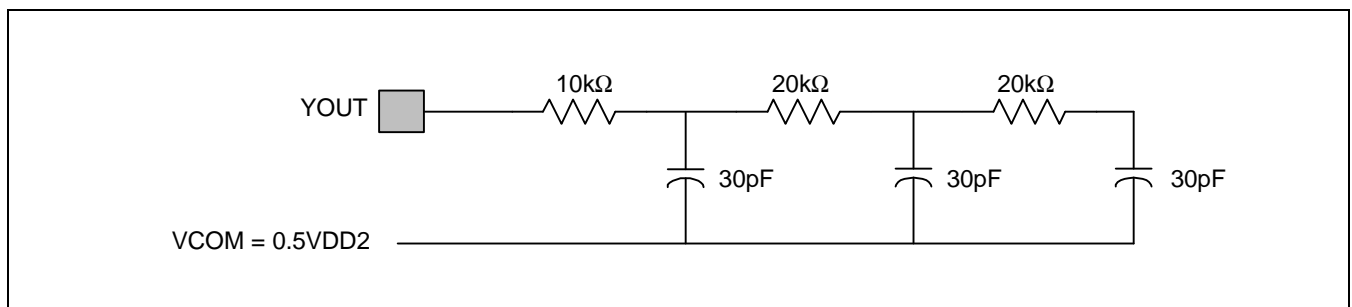


Figure 5. Yout Load Condition

WAVEFORMS

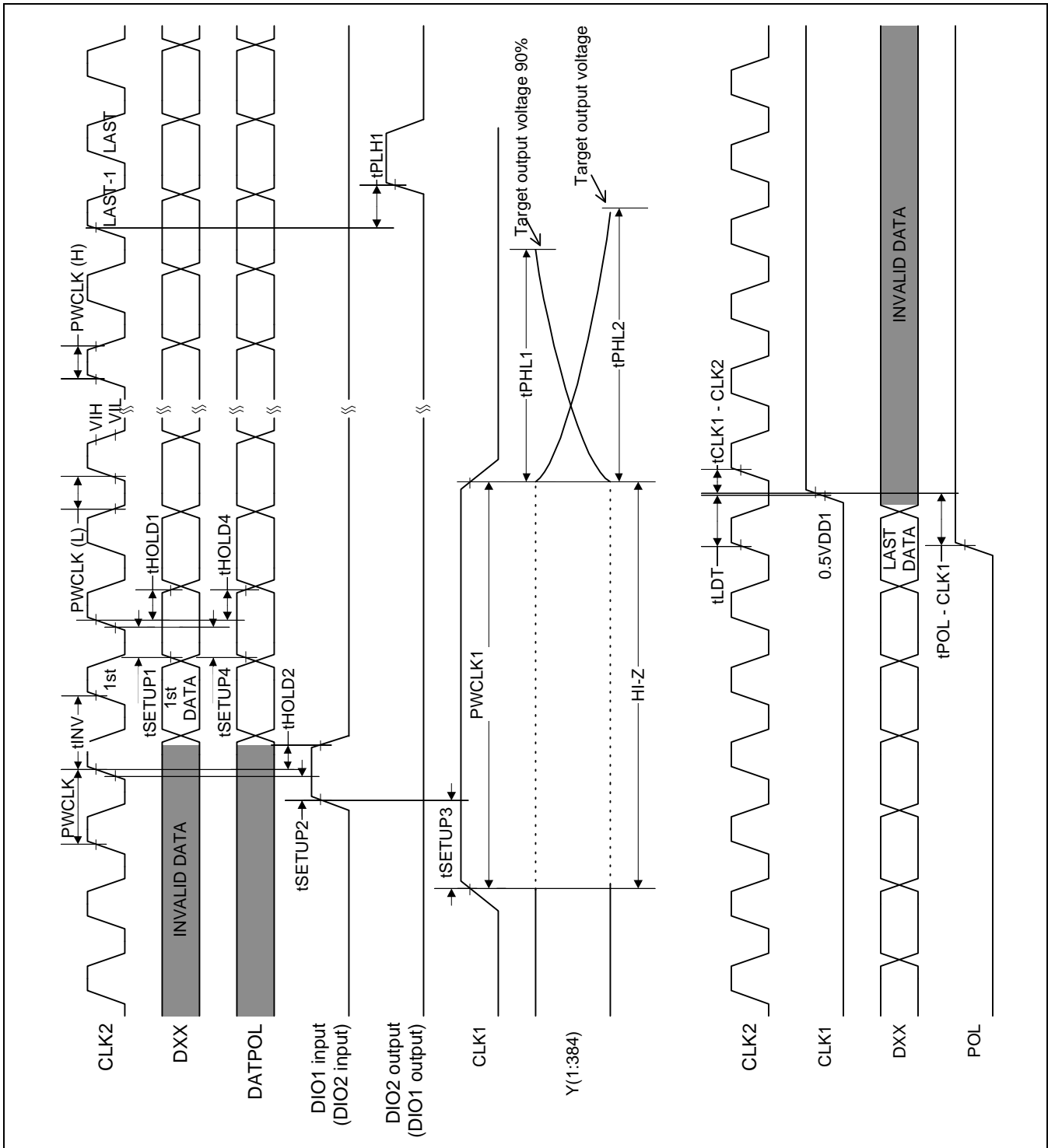


Figure 6. Waveforms

### RELATIONSHIPS BETWEEN CLK1, START PULSE (DIO1, DIO2) AND BLANKING PERIOD

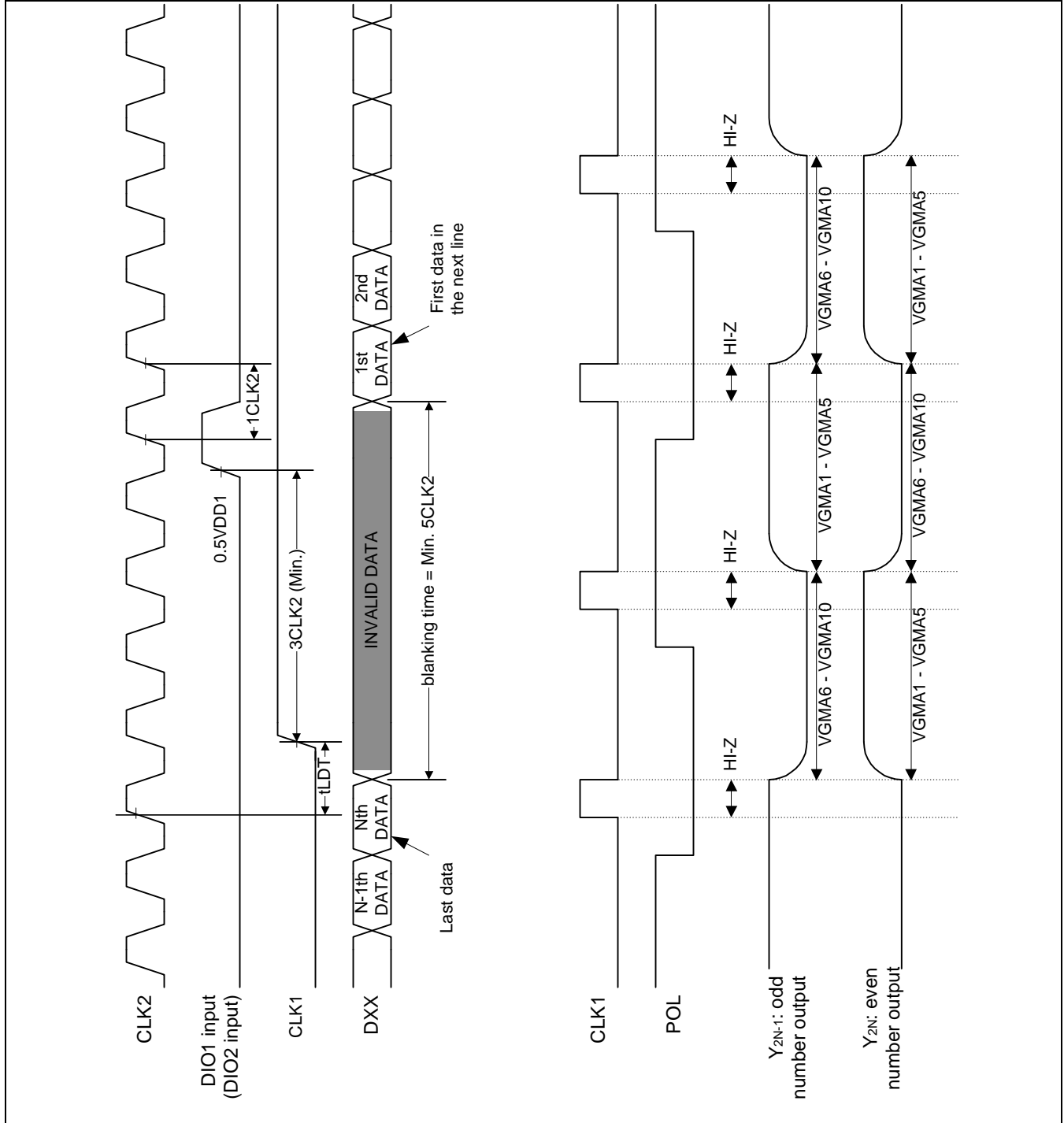


Figure 7. Waveforms