# KSZ9031RNX

## Gigabit Ethernet Transceiver with RGMII Support

**Revision 2.2**

## General Description

The KSZ9031RNX is a completely integrated triple-speed (10Base-T/100Base-TX/1000Base-T) Ethernet physical-layer transceiver for transmission and reception of data on standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ9031RNX provides the reduced gigabit media independent interface (RGMII) for direct connection to RGMII MACs in gigabit Ethernet processors and switches for data transfer at 10/100/1000Mbps.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

The KSZ9031RNX offers diagnostic features to facilitate system bring-up and debugging in production testing and in product deployment. Parametric NAND tree support enables fault detection between KSZ9031 I/Os and the board. The LinkMD® TDR-based cable diagnostic identifies faulty copper cabling. Remote and local loopback functions verify analog and digital data paths.

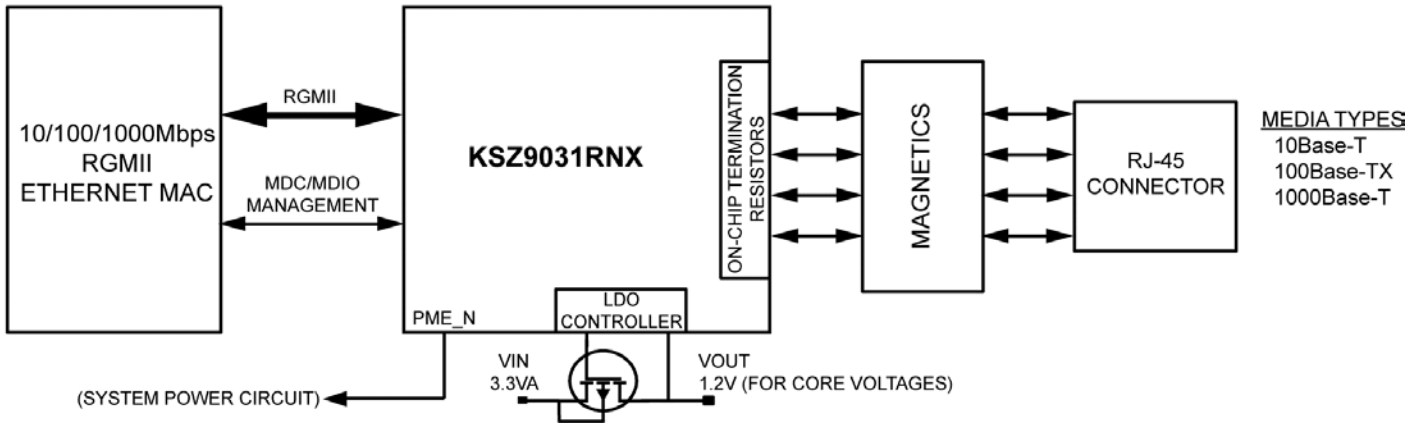
The standard KSZ9031RNX is available in the 48-pin, lead-free QFN package, and the AEC-Q100 automotive qualified parts, KSZ9031RNXUA and KSZ9031RNXVA, are available in the 48-pin lead-free WQFN package (see *Ordering Information*).

Data sheets and support documentation are available on Micrel's web site at: www.micrel.com.

## Features

- Single-chip 10/100/1000Mbps IEEE 802.3-compliant Ethernet transceiver
- RGMII timing supports on-chip delay according to RGMII Version 2.0, with programming options for external delay and making adjustments and corrections to TX and RX timing paths
- RGMII with 3.3V/2.5V/1.8V tolerant I/Os
- Auto-negotiation to automatically select the highest link-up speed (10/100/1000Mbps) and duplex (half/full)
- On-chip termination resistors for the differential pairs
- On-chip LDO controller to support single 3.3V supply operation – requires only one external FET to generate 1.2V for the core
- Jumbo frame support up to 16KB
- 125MHz reference clock output
- Energy detect power-down mode for reduced power consumption when the cable is not attached
- Energy Efficient Ethernet (EEE) support with low-power idle (LPI) mode and clock stoppage for 100Base-TX/1000Base-T and transmit amplitude reduction with 10Base-Te option
- Wake-On-LAN (WOL) support with robust custom-packet detection
- AEC-Q100 qualified for automotive applications (KSZ9031RNXUA, KSZ9031RNXVA)

## Functional Diagram

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## Features (Continued)

- Programmable LED outputs for link, activity, and speed
- Baseline wander correction
- LinkMD TDR-based cable diagnostic to identify faulty copper cabling
- Parametric NAND tree support to detect faults between chip I/Os and board
- Loopback modes for diagnostics
- Automatic MDI/MDI-X crossover to detect and correct pair swap at all speeds of operation
- Automatic detection and correction of pair swaps, pair skew, and pair polarity
- MDC/MDIO management interface for PHY register configuration
- Interrupt pin option
- Power-down and power-saving modes
- Operating voltages
  - Core (DVDDL, AVDDL, AVDDL_PLL):
    1.2V (external FET or regulator)
  - VDD I/O (DVDDH):
    3.3V, 2.5V, or 1.8V
  - Transceiver (AVDDH):
    3.3V or 2.5V (commercial temp)
- Available in a 48-pin QFN (7mm × 7mm) package

## Applications

- Laser/network printer
- Network attached storage (NAS)
- Network server
- Gigabit LAN on motherboard (GLOM)
- Broadband gateway
- Gigabit SOHO/SMB router
- IPTV
- IP set-top box
- Game console
- Triple-play (data, voice, video) media center
- Media converter

## Ordering Information

| Part Number | Temperature Range | Package | Lead Finish | Wire Bonding | Description |
|---|---|---|---|---|---|
| KSZ9031RNXCA | 0°C to 70°C | 48-Pin QFN | Pb-Free | Gold | RGMII, Commercial Temperature, Gold Wire Bonding |
| KSZ9031RNXCC(1) | 0°C to 70°C | 48-Pin QFN | Pb-Free | Copper | RGMII, Commercial Temperature, Copper Wire Bonding |
| KSZ9031RNXIA(1) | –40°C to 85°C | 48-Pin QFN | Pb-Free | Gold | RGMII, Industrial Temperature, Gold Wire Bonding |
| KSZ9031RNXIC(1) | –40°C to 85°C | 48-Pin QFN | Pb-Free | Copper | RGMII, Industrial Temperature, Copper Wire Bonding |
| KSZ9031RNXUA(1) | –40°C to 85°C | 48-Pin WQFN | Pb-Free | Gold | RGMII, AEC-Q100 Automotive Qualified to 85°C, Gold Wire Bonding |
| KSZ9031RNXVA(1) | –40°C to 105°C | 48-Pin WQFN | Pb-Free | Gold | RGMII, AEC-Q100 Automotive Qualified to 105°C, Gold Wire Bonding |
| KSZ9031RNX-EVAL | 0°C to 70°C | 48-Pin QFN | Pb-Free | | KSZ9031RNX Evaluation Board (Mounted with KSZ9031RNX device in commercial temperature) |

**Note:**

1. Contact factory for availability.

## Revision History

| Revision | Date | Summary of Changes |
|---|---|---|
| 1.0 | 10/31/12 | Data sheet created |
| 2.0 | 07/31/13 | • Updated *Functional Diagram* with "PME_N" signal.<br>• Indicated pin type is not an open-drain for PME_N1 (Pin 17) and INT_N/PME_N2 (Pin 38).<br>• Deleted TSLP package height from *Package Information*(11) and Recommended Land Pattern.<br>• Added typical series resistance and load capacitance for crystal selection criteria.<br>• Added setup/hold timings for integrated delays per the RGMII v2.0 Specification.<br>• Added note that RGMII data-to-clock skews for 10/100Mbps speeds are looser than for 1000Mbps speed.<br>• Corrected register definition for override strap-in for LED_MODE in MMD Address 2h, Register 0h.<br>• Clarified register description for software power-down bit (Register 0h, Bit [11]). |
| 2.1 | 11/18/14 | • Clarified power cycling specification to have all supply voltages to the KSZ9031RNX reach less than 0.4V before the next power-up cycle.<br>• Added AEC-Q100 automotive qualified part numbers, KSZ9031RNXUA and KSZ9031RNXVA, to *General Description*, *Features*, *Ordering Information* and *Electrical Characteristics*(10) sections.<br>• Added Package Information(11) and Recommended Land Pattern for 48-pin (7mm x 7mm) WQFN for the automotive qualified part numbers.<br>• Corrected *Package Information(11) and Recommended* Land Pattern for 48-pin (7mm x 7mm) QFN. This is a datasheet correction. There is no change to the 48-pin (7mm x 7mm) QFN package.<br>• Added note that internal pull-up values are measured with pin input voltage level at 1/2 DVDDH in *Electrical Characteristics*(10) section. |
| 2.2 | 5/14/15 | • Corrected datasheet revision 2.1 formatting errors for Standard Register 13h.<br>• Added more details for XI (25MHz reference clock) input specification to *Reference Clock – Connection and Selection* section.<br>• Added note in Standard Register 0h, Bit [12] to indicate when Auto-Negotiation is disabled, Auto MDI-X is also automatically disabled.<br>• Added note in *10Base-T Receive* section that all 7 bytes of preamble are removed.<br>• Added instruction in Register 9h, Bits [15:13] to enable 1000Base-T Test Mode.<br>• Added description in *Auto-Negotiation Timing* section to change FLP timing from 8ms to 16ms.<br>• Added MMD Address 0h, Registers 3h and 4h for FLP timing.<br>• Specified maximum frequency (minimum clock period) for MDC clock.<br>• Updated input leakage current for the digital input pins in *Electrical Characteristics*(10) section.<br>• Added minimum output currents for the digital output pins in *Electrical Characteristics*(10) section.<br>• Corrected output drive current for LED1 and LED2 pins in *Electrical Characteristics*(10) section.<br>• Updated *Reset Circuit* section and added reset circuit with MIC826 Voltage Supervisor.<br>• Clarified LED indication support for 1.8V DVDDH requires voltage level shifters.<br>• Added *10/100 Speeds Only* section.<br>• Added section for MOSFET selection for optional on-chip LDO controller.<br>• Clarified RGMII timing and added Original RGMII (v1.3) timing with external delay for reference. |

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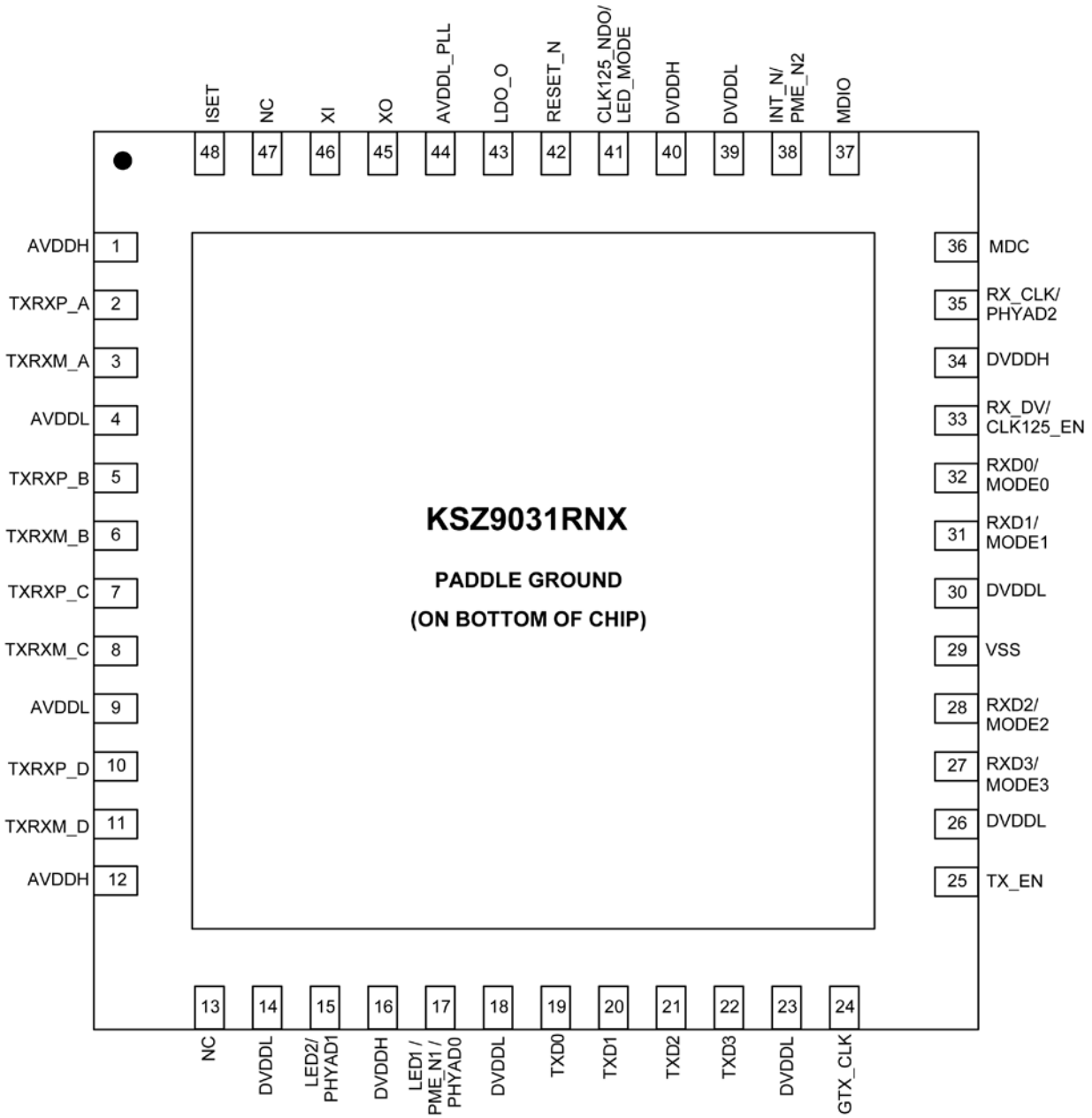
## Pin Configuration




**48-Pin QFN**
**(Top View)**

## Pin Description

| Pin Number | Pin Name | Type[2] | Pin Function |
|---|---|---|---|
| 1 | AVDDH | P | 3.3V/2.5V (commercial temp only) analog $V_{DD}$ |
| 2 | TXRXP_A | I/O | Media Dependent Interface[0], positive signal of differential pair<br>1000Base-T mode:<br>TXRXP_A corresponds to BI_DA+ for MDI configuration and BI_DB+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXP_A is the positive transmit signal (TX+) for MDI configuration and the positive receive signal (RX+) for MDI-X configuration, respectively. |
| 3 | TXRXM_A | I/O | Media Dependent Interface[0], negative signal of differential pair<br>1000Base-T mode:<br>TXRXM_A corresponds to BI_DA– for MDI configuration and BI_DB– for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXM_A is the negative transmit signal (TX–) for MDI configuration and the negative receive signal (RX–) for MDI-X configuration, respectively. |
| 4 | AVDDL | P | 1.2V analog $V_{DD}$ |
| 5 | TXRXP_B | I/O | Media Dependent Interface[1], positive signal of differential pair<br>1000Base-T mode:<br>TXRXP_B corresponds to BI_DB+ for MDI configuration and BI_DA+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXP_B is the positive receive signal (RX+) for MDI configuration and the positive transmit signal (TX+) for MDI-X configuration, respectively. |
| 6 | TXRXM_B | I/O | Media Dependent Interface[1], negative signal of differential pair<br>1000Base-T mode:<br>TXRXM_B corresponds to BI_DB– for MDI configuration and BI_DA– for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXM_B is the negative receive signal (RX–) for MDI configuration and the negative transmit signal (TX–) for MDI-X configuration, respectively. |
| 7 | TXRXP_C | I/O | Media Dependent Interface[2], positive signal of differential pair<br>1000Base-T mode:<br>TXRXP_C corresponds to BI_DC+ for MDI configuration and BI_DD+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXP_C is not used. |

**Note:**

2. P = Power supply.
   GND = Ground.
   I = Input.
   O = Output.
   I/O = Bi-directional.
   Ipu = Input with internal pull-up (see *Electrical Characteristics* for value).
   Ipu/O = Input with internal pull-up (see *Electrical Characteristics* for value)/Output.

## Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[2]</th><th>Pin Function</th></tr>
<tr><td>8</td><td>TXRXM_C</td><td>I/O</td><td>Media Dependent Interface[2], negative signal of differential pair<br>1000Base-T mode:<br>TXRXM_C corresponds to BI_DC– for MDI configuration and BI_DD– for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXM_C is not used.</td></tr>
<tr><td>9</td><td>AVDDL</td><td>P</td><td>1.2V analog $V_{DD}$</td></tr>
<tr><td>10</td><td>TXRXP_D</td><td>I/O</td><td>Media Dependent Interface[3], positive signal of differential pair<br>1000Base-T mode:<br>TXRXP_D corresponds to BI_DD+ for MDI configuration and BI_DC+ for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXP_D is not used.</td></tr>
<tr><td>11</td><td>TXRXM_D</td><td>I/O</td><td>Media Dependent Interface[3], negative signal of differential pair<br>1000Base-T mode:<br>TXRXM_D corresponds to BI_DD– for MDI configuration and BI_DC– for MDI-X configuration, respectively.<br>10Base-T/100Base-TX mode:<br>TXRXM_D is not used.</td></tr>
<tr><td>12</td><td>AVDDH</td><td>P</td><td>3.3V/2.5V (commercial temp only) analog $V_{DD}$</td></tr>
<tr><td>13</td><td>NC</td><td>–</td><td>No connect. This pin is not bonded and can be connected to digital ground for footprint compatibility with the Micrel KSZ9021RN Gigabit PHY.</td></tr>
<tr><td>14</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>15</td><td>LED2/<br>PHYAD1</td><td>I/O</td><td>LED output: Programmable LED2 output<br>Config mode: The pull-up/pull-down value is latched as PHYAD[1] during power-up/reset. See the Strapping Options section for details.<br>The LED2 pin is programmed by the LED_MODE strapping option (Pin 41), and is defined as follows:<br>Single-LED Mode
<table>
<tr><th>Link</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>Link off</td><td>H</td><td>OFF</td></tr>
<tr><td>Link on (any speed)</td><td>L</td><td>ON</td></tr>
</table>
Tri-Color Dual-LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For tri-color dual-LED mode, LED2 works in conjunction with LED1 (Pin 17) to indicate 10Mbps link and activity.</td></tr>
</table>

## Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[2]</th><th>Pin Function</th></tr>
<tr><td>16</td><td>DVDDH</td><td>P</td><td>3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$</td></tr>
<tr><td>17</td><td>LED1/<br>PHYAD0/<br><br>PME_N1</td><td>I/O</td><td>
LED1 output: Programmable LED1 output<br>
Config mode: The voltage on this pin is sampled and latched during the power-up/reset process to determine the value of PHYAD[0]. See the Strapping Options section for details.<br>
PME_N output: Programmable PME_N output (pin option 1). This pin function requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0kΩ to 4.7kΩ. When asserted low, this pin signals that a WOL event has occurred.<br><br>
This pin is not an open-drain for all operating modes.<br>
The LED1 pin is programmed by the LED_MODE strapping option (Pin 41), and is defined as follows.<br>
Single-LED Mode
<table>
<tr><th>Activity</th><th>Pin State</th><th>LED Definition</th></tr>
<tr><td>No activity</td><td>H</td><td>OFF</td></tr>
<tr><td>Activity (RX, TX)</td><td>Toggle</td><td>Blinking</td></tr>
</table>
Tri-Color Dual-LED Mode
<table>
<tr><th rowspan="2">Link/Activity</th><th colspan="2">Pin State</th><th colspan="2">LED Definition</th></tr>
<tr><th>LED2</th><th>LED1</th><th>LED2</th><th>LED1</th></tr>
<tr><td>Link off</td><td>H</td><td>H</td><td>OFF</td><td>OFF</td></tr>
<tr><td>1000 Link / No activity</td><td>L</td><td>H</td><td>ON</td><td>OFF</td></tr>
<tr><td>1000 Link / Activity (RX, TX)</td><td>Toggle</td><td>H</td><td>Blinking</td><td>OFF</td></tr>
<tr><td>100 Link / No activity</td><td>H</td><td>L</td><td>OFF</td><td>ON</td></tr>
<tr><td>100 Link / Activity (RX, TX)</td><td>H</td><td>Toggle</td><td>OFF</td><td>Blinking</td></tr>
<tr><td>10 Link / No activity</td><td>L</td><td>L</td><td>ON</td><td>ON</td></tr>
<tr><td>10 Link / Activity (RX, TX)</td><td>Toggle</td><td>Toggle</td><td>Blinking</td><td>Blinking</td></tr>
</table>
For tri-color dual-LED mode, LED1 works in conjunction with LED2 (Pin 15) to indicate 10Mbps link and activity.
</td></tr>
<tr><td>18</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>19</td><td>TXD0</td><td>I</td><td>RGMII mode: RGMII TD0 (Transmit Data 0) input</td></tr>
<tr><td>20</td><td>TXD1</td><td>I</td><td>RGMII mode: RGMII TD1 (Transmit Data 1) input</td></tr>
<tr><td>21</td><td>TXD2</td><td>I</td><td>RGMII mode: RGMII TD2 (Transmit Data 2) input</td></tr>
<tr><td>22</td><td>TXD3</td><td>I</td><td>RGMII mode: RGMII TD3 (Transmit Data 3) input</td></tr>
<tr><td>23</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>24</td><td>GTX_CLK</td><td>I</td><td>RGMII mode:RGMII TXC (Transmit Reference Clock) input</td></tr>
<tr><td>25</td><td>TX_EN</td><td>I</td><td>RGMII mode:RGMII TX_CTL (Transmit Control) input</td></tr>
<tr><td>26</td><td>DVDDL</td><td>P</td><td>1.2V digital $V_{DD}$</td></tr>
<tr><td>27</td><td>RXD3/<br>MODE3</td><td>I/O</td><td>RGMII mode: RGMII RD3 (Receive Data 3) output<br>Config mode: The pull-up/pull-down value is latched as MODE3 during power-up/reset. See the Strapping Options section for details.</td></tr>
<tr><td>28</td><td>RXD2/<br>MODE2</td><td>I/O</td><td>RGMII mode: RGMII RD2 (Receive Data 2) output<br>Config mode: The pull-up/pull-down value is latched as MODE2 during power-up/reset. See the Strapping Options section for details.</td></tr>
</table>

## Pin Description (Continued)

| Pin Number | Pin Name | Type[2] | Pin Function |
|---|---|---|---|
| 29 | VSS | GND | Digital ground |
| 30 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 31 | RXD1/<br>MODE1 | I/O | RGMII mode: RGMII RD1 (Receive Data 1) output<br>Config mode: The pull-up/pull-down value is latched as MODE1 during power-up/reset. See the *Strapping Options* section for details. |
| 32 | RXD0/<br>MODE0 | I/O | RGMII mode: RGMII RD0 (Receive Data 0) output<br>Config mode: The pull-up/pull-down value is latched as MODE0 during power-up/reset. See the *Strapping Options* section for details. |
| 33 | RX_DV/<br>CLK125_EN | I/O | RGMII mode: RGMII RX_CTL (Receive Control) output<br>Config mode: Latched as CLK125_NDO Output Enable during power-up/reset. See the *Strapping Options* section for details. |
| 34 | DVDDH | P | 3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$ |
| 35 | RX_CLK/<br>PHYAD2 | I/O | RGMII mode: RGMII RXC (Receive Reference Clock) output<br>Config mode: The pull-up/pull-down value is latched as PHYAD[2] during power-up/reset. See the *Strapping Options* section for details. |
| 36 | MDC | Ipu | Management data clock input<br>This pin is the input reference clock for MDIO (Pin 37). |
| 37 | MDIO | Ipu/O | Management data input/output<br>This pin is synchronous to MDC (Pin 36) and requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0kΩ to 4.7kΩ. |
| 38 | INT_N/<br><br>PME_N2 | O | Interrupt output: Programmable interrupt output, with Register 1Bh as the Interrupt Control/Status register, for programming the interrupt conditions and reading the interrupt status. Register 1Fh, Bit [14] sets the interrupt output to active low (default) or active high.<br>PME_N output: Programmable PME_N output (pin option 2). When asserted low, this pin signals that a WOL event has occurred.<br>For Interrupt (when active low) and PME functions, this pin requires an external pull-up resistor to DVDDH (digital $V_{DD\_I/O}$) in a range from 1.0kΩ to 4.7kΩ.<br>This pin is not an open-drain for all operating modes. |
| 39 | DVDDL | P | 1.2V digital $V_{DD}$ |
| 40 | DVDDH | P | 3.3V, 2.5V, or 1.8V digital $V_{DD\_I/O}$ |
| 41 | CLK125_NDO/<br><br>LED_MODE | I/O | 125MHz clock output<br>This pin provides a 125MHz reference clock output option for use by the MAC.<br>Config mode: The pull-up/pull-down value is latched as LED_MODE during power-up/reset. See the *Strapping Options* section for details. |
| 42 | RESET_N | Ipu | Chip reset (active low)<br>Hardware pin configurations are strapped-in at the de-assertion (rising edge) of RESET_N. See the *Strapping Options* section for more details. |
| 43 | LDO_O | O | On-chip 1.2V LDO controller output<br>This pin drives the input gate of a P-channel MOSFET to generate 1.2V for the chip's core voltages. If the system provides 1.2V and this pin is not used, it can be left floating. |
| 44 | AVDDL_PLL | P | 1.2V analog $V_{DD}$ for PLL |
| 45 | XO | O | 25MHz crystal feedback<br>This pin is a no connect if an oscillator or external clock source is used. |

## Pin Description (Continued)

| Pin Number | Pin Name | Type[2] | Pin Function |
|---|---|---|---|
| 46 | XI | I | Crystal / Oscillator/ External Clock input<br>25MHz ±50ppm tolerance |
| 47 | NC | – | No connect<br>This pin is not bonded and can be connected to AVDDH power for footprint compatibility with the Micrel KSZ9021RN Gigabit PHY. |
| 48 | ISET | I/O | Set the transmit output level<br>Connect a 12.1kΩ 1% resistor to ground on this pin. |
| PADDLE | P_GND | GND | Exposed paddle on bottom of chip<br>Connect P_GND to ground. |

## Strapping Options

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type[3]</th><th>Pin Function</th></tr>
<tr><td>35<br>15<br>17</td><td>PHYAD2<br>PHYAD1<br>PHYAD0</td><td>I/O<br>I/O<br>I/O</td><td>The PHY address, PHYAD[2:0], is sampled and latched at power-up/reset and is configurable to any value from 0 to 7. Each PHY address bit is configured as follows:<br>Pull-up = 1<br>Pull-down = 0<br>PHY Address Bits [4:3] are always set to ‘00’.</td></tr>
<tr><td>27<br>28<br>31<br>32</td><td>MODE3<br>MODE2<br>MODE1<br>MODE0</td><td>I/O<br>I/O<br>I/O<br>I/O</td><td>The MODE[3:0] strap-in pins are sampled and latched at power-up/reset as follows:
<table>
<tr><th>MODE[3:0]</th><th>Mode</th></tr>
<tr><td>0000</td><td>Reserved – not used</td></tr>
<tr><td>0001</td><td>Reserved – not used</td></tr>
<tr><td>0010</td><td>Reserved – not used</td></tr>
<tr><td>0011</td><td>Reserved – not used</td></tr>
<tr><td>0100</td><td>NAND tree mode</td></tr>
<tr><td>0101</td><td>Reserved – not used</td></tr>
<tr><td>0110</td><td>Reserved – not used</td></tr>
<tr><td>0111</td><td>Chip power-down mode</td></tr>
<tr><td>1000</td><td>Reserved – not used</td></tr>
<tr><td>1001</td><td>Reserved – not used</td></tr>
<tr><td>1010</td><td>Reserved – not used</td></tr>
<tr><td>1011</td><td>Reserved – not used</td></tr>
<tr><td>1100</td><td>RGMII mode – advertise 1000Base-T full-duplex only</td></tr>
<tr><td>1101</td><td>RGMII mode – advertise 1000Base-T full- and half-duplex only</td></tr>
<tr><td>1110</td><td>RGMII mode – advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000Base-T half-duplex</td></tr>
<tr><td>1111</td><td>RGMII mode – advertise all capabilities (10/100/1000 speed half-/full-duplex)</td></tr>
</table></td></tr>
<tr><td>33</td><td>CLK125_EN</td><td>I/O</td><td>CLK125_EN is sampled and latched at power-up/reset and is defined as follows:<br>Pull-up = Enable 125MHz clock output<br>Pull-down = Disable 125MHz clock output<br>Pin 41 (CLK125_NDO) provides the 125MHz reference clock output option for use by the MAC.</td></tr>
<tr><td>41</td><td>LED_MODE</td><td>I/O</td><td>LED_MODE is latched at power-up/reset and is defined as follows:<br>Pull-up = Single-LED mode<br>Pull-down = Tri-color dual-LED mode</td></tr>
</table>

**Note:**

3. I/O = Bi-directional.

Pin strap-ins are latched during power-up or reset. In some systems, the MAC receive input pins may be driven during power-up or reset, and consequently cause the PHY strap-in pins on the RGMII signals to be latched to an incorrect configuration. In this case, Micrel recommends adding external pull-ups/pull-downs on the PHY strap-in pins to ensure the PHY is configured to the correct pin strap-in mode.

## Functional Overview

The KSZ9031RNX is a completely integrated triple-speed (10Base-T/100Base-TX/1000Base-T) Ethernet physical layer transceiver solution for transmission and reception of data over a standard CAT-5 unshielded twisted pair (UTP) cable. Its on-chip proprietary 1000Base-T transceiver and Manchester/MLT-3 signaling-based 10Base-T/100Base-TX transceivers are all IEEE 802.3 compliant.

The KSZ9031RNX reduces board cost and simplifies board layout by using on-chip termination resistors for the four differential pairs and by integrating an LDO controller to drive a low-cost MOSFET to supply the 1.2V core.

On the copper media interface, the KSZ9031RNX can automatically detect and correct for differential pair misplacements and polarity reversals, and correct propagation delays and re-sync timing between the four differential pairs, as specified in the IEEE 802.3 standard for 1000Base-T operation.

The KSZ9031RNX provides the RGMII interface for direct and seamless connection to RGMII MACs in Gigabit Ethernet processors and switches for data transfer at 10/100/1000Mbps.

Figure 1 shows a high-level block diagram of the KSZ9031RNX.

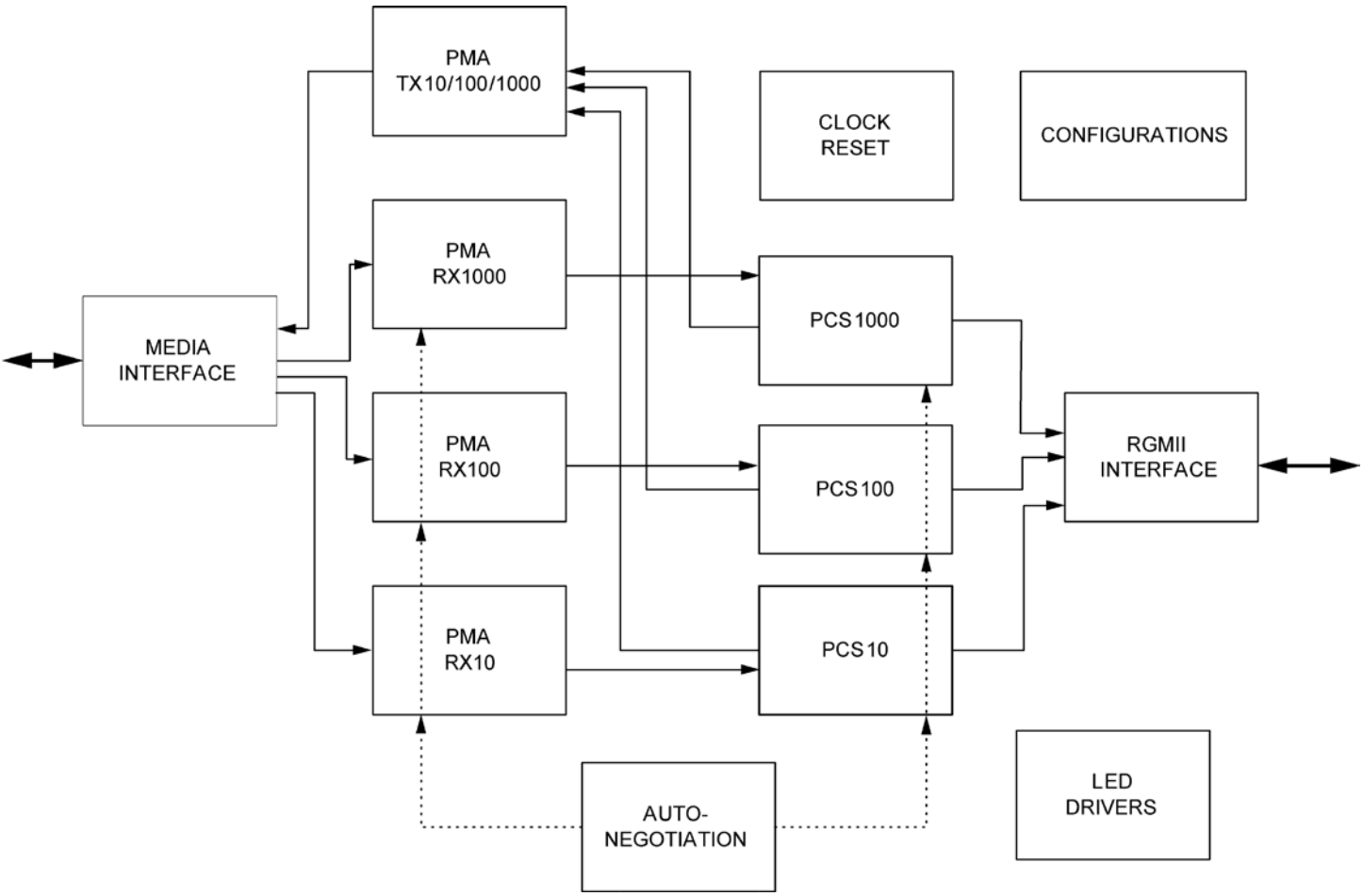



**Figure 1. KSZ9031RNX Block Diagram**

# Functional Description: 10Base-T/100Base-TX Transceiver

### 100Base-TX Transmit

The 100Base-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, and MLT-3 encoding and transmission.

The circuitry starts with a parallel-to-serial conversion, which converts the RGMII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding, followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format then transmitted in MLT-3 current output. The output current is set by an external 12.1kΩ 1% resistor for the 1:1 transformer ratio.

The output signal has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10Base-T output is also incorporated into the 100Base-TX transmitter.

### 100Base-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT-3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, de-scrambling, 4B/5B decoding, and serial-to-parallel conversion.

The receiving side starts with the equalization filter to compensate for inter-symbol interference (ISI) over the twisted pair cable. Because the amplitude loss and phase distortion are a function of the cable length, the equalizer must adjust its characteristics to optimize performance. In this design, the variable equalizer makes an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and self-adjusts against environmental changes such as temperature variations.

Next, the equalized signal goes through a DC-restoration and data-conversion block. The DC-restoration circuit compensates for the effect of baseline wander and improves the dynamic range. The differential data-conversion circuit converts the MLT-3 format back to NRZI. The slicing threshold is also adaptive.

The clock-recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. This signal is sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the RGMII format and provided as the input data to the MAC.

### Scrambler/De-Scrambler (100Base-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal to reduce electromagnetic interference (EMI) and baseline wander. Transmitted data is scrambled using an 11-bit wide linear feedback shift register (LFSR). The scrambler generates a 2047-bit non-repetitive sequence, then the receiver de-scrambles the incoming data stream using the same sequence as at the transmitter.

### 10Base-T Transmit

The 10Base-T output drivers are incorporated into the 100Base-TX drivers to allow for transmission with the same magnetic. The drivers perform internal wave-shaping and pre-emphasis, and output signals with a typical amplitude of 2.5V peak for standard 10Base-T mode and 1.75V peak for energy-efficient 10Base-Te mode. The 10Base-T/10Base-Te signals have harmonic contents that are at least 31dB below the fundamental frequency when driven by an all-ones Manchester-encoded signal.

### 10Base-T Receive

On the receive side, input buffer and level-detecting squelch circuits are used. A differential input receiver circuit and a phase-locked loop (PLL) perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 300mV or with short pulse widths to prevent noises at the receive inputs from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ9031RNX decodes a data frame. The receiver clock is maintained active during idle periods between receiving data frames.

The KSZ9031RNX removes all 7 bytes of the preamble and presents the received frame starting with the SFD (start of frame delimiter) to the MAC.

Auto-polarity correction is provided for the receive differential pair to automatically swap and fix the incorrect +/– polarity wiring in the cabling.

## Functional Description: 1000Base-T Transceiver

The 1000Base-T transceiver is based-on a mixed-signal/digital-signal processing (DSP) architecture, which includes the analog front-end, digital channel equalizers, trellis encoders/decoders, echo cancellers, cross-talk cancellers, precision clock recovery scheme, and power-efficient line drivers.

Figure 2 shows a high-level block diagram of a single channel of the 1000Base-T transceiver for one of the four differential pairs.

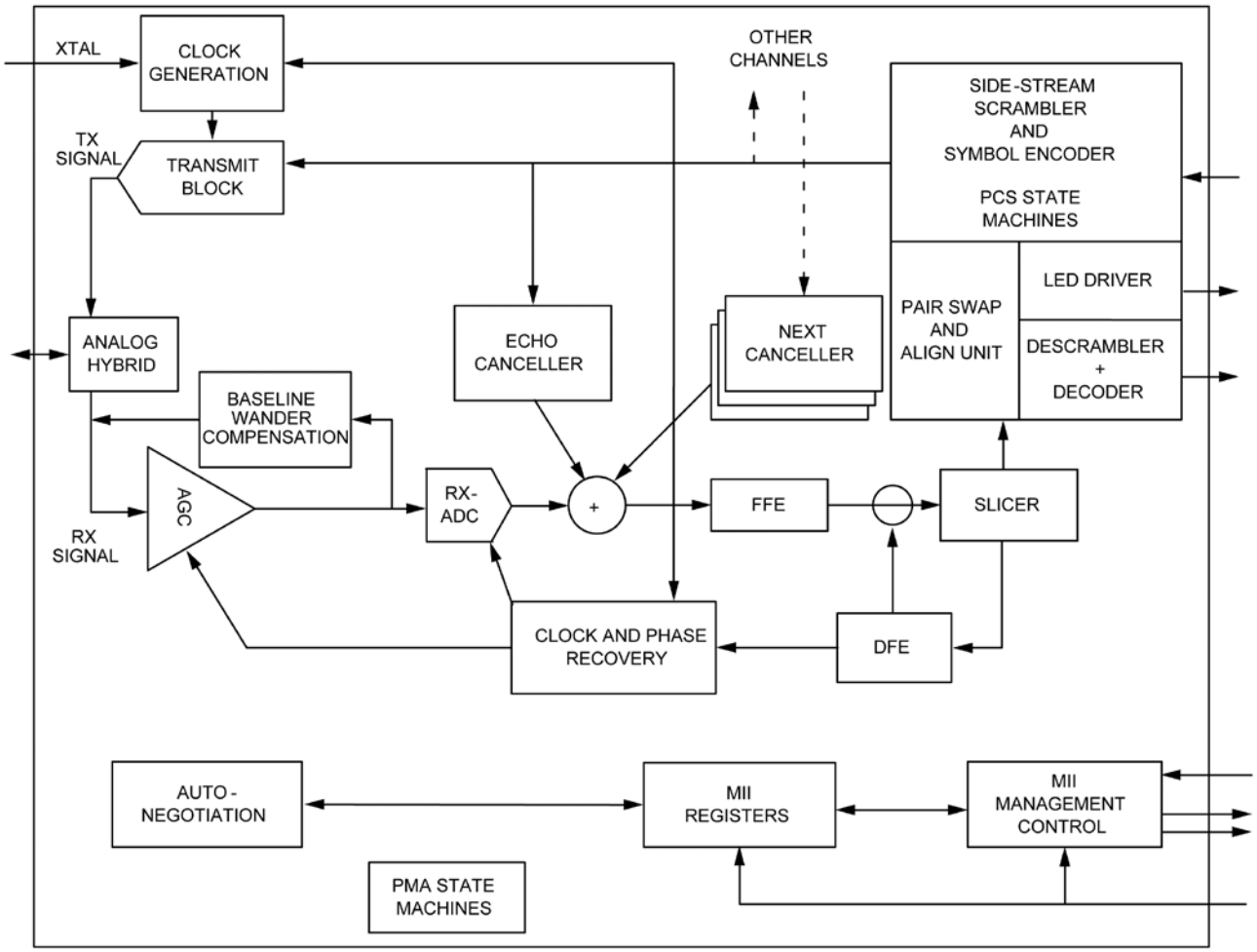



**Figure 2. KSZ9031RNX 1000Base-T Transceiver Block Diagram – Single Channel**

### Analog Echo-Cancellation Circuit

In 1000Base-T mode, the analog echo-cancellation circuit helps to reduce the near-end echo. This analog hybrid circuit relieves the burden of the ADC and the adaptive equalizer.

This circuit is disabled in 10Base-T/100Base-TX mode.

### Automatic Gain Control (AGC)

In 1000Base-T mode, the automatic gain control (AGC) circuit provides initial gain adjustment to boost up the signal level. This pre-conditioning circuit is used to improve the signal-to-noise ratio of the receive signal.

### Analog-to-Digital Converter (ADC)

In 1000Base-T mode, the analog-to-digital converter (ADC) digitizes the incoming signal. ADC performance is essential to the overall performance of the transceiver.

This circuit is disabled in 10Base-T/100Base-TX mode.

### Timing Recovery Circuit

In 1000Base-T mode, the mixed-signal clock recovery circuit together with the digital phase-locked loop is used to recover and track the incoming timing information from the received data. The digital phase-locked loop has very low long-term jitter to maximize the signal-to-noise ratio of the receive signal.

The 1000Base-T slave PHY must transmit the exact receive clock frequency recovered from the received data back to the 1000Base-T master PHY. Otherwise, the master and slave will not be synchronized after long transmission. This also helps to facilitate echo cancellation and NEXT removal.

### Adaptive Equalizer

In 1000Base-T mode, the adaptive equalizer provides the following functions:

- Detection for partial response signaling
- Removal of NEXT and ECHO noise
- Channel equalization

Signal quality is degraded by residual echo that is not removed by the analog hybrid because of impedance mismatch. The KSZ9031RNX uses a digital echo canceller to further reduce echo components on the receive signal.

In 1000Base-T mode, data transmission and reception occurs simultaneously on all four pairs of wires (four channels). This results in high-frequency cross-talk coming from adjacent wires. The KSZ9031RNX uses three NEXT cancellers on each receive channel to minimize the cross-talk induced by the other three channels.

In 10Base-T/100Base-TX mode, the adaptive equalizer needs only to remove the inter-symbol interference and recover the channel loss from the incoming data.

### Trellis Encoder and Decoder

In 1000Base-T mode, the transmitted 8-bit data is scrambled into 9-bit symbols and further encoded into 4D-PAM5 symbols. The initial scrambler seed is determined by the specific PHY address to reduce EMI when more than one KSZ9031RNX is used on the same board. On the receiving side, the idle stream is examined first. The scrambler seed, pair skew, pair order, and polarity must be resolved through the logic. The incoming 4D-PAM5 data is then converted into 9-bit symbols and de-scrambled into 8-bit data.

# Functional Description: 10/100/1000 Transceiver Features

### Auto MDI/MDI-X

The Automatic MDI/MDI-X feature eliminates the need to determine whether to use a straight cable or a crossover cable between the KSZ9031RNX and its link partner. This auto-sense function detects the MDI/MDI-X pair mapping from the link partner, and assigns the MDI/MDI-X pair mapping of the KSZ9031RNX accordingly.

Table 1 shows the KSZ9031RNX 10/100/1000 pin configuration assignments for MDI/MDI-X pin mapping.

**Table 1. MDI/MDI-X Pin Mapping**

| Pin (RJ-45 pair) | MDI | | | MDI-X | | |
|---|---|---|---|---|---|---|
| | 1000Base-T | 100Base-TX | 10Base-T | 1000Base-T | 100Base-TX | 10Base-T |
| TXRXP/M_A (1,2) | A+/– | TX+/– | TX+/– | B+/– | RX+/– | RX+/– |
| TXRXP/M_B (3,6) | B+/– | RX+/– | RX+/– | A+/– | TX+/– | TX+/– |
| TXRXP/M_C (4,5) | C+/– | Not used | Not used | D+/– | Not used | Not used |
| TXRXP/M_D (7,8) | D+/– | Not used | Not used | C+/– | Not used | Not used |

Auto MDI/MDI-X is enabled by default. It is disabled by writing a one to Register 1Ch, Bit [6]. MDI and MDI-X mode is set by Register 1Ch, Bit [7] if Auto MDI/MDI-X is disabled.

An isolation transformer with symmetrical transmit and receive data paths is recommended to support Auto MDI/MDI-X.

### Pair-Swap, Alignment, and Polarity Check

In 1000Base-T mode, the KSZ9031RNX

- Detects incorrect channel order and automatically restores the pair order for the A, B, C, D pairs (four channels)
- Supports 50±10ns difference in propagation delay between pairs of channels in accordance with the IEEE 802.3 standard, and automatically corrects the data skew so the corrected four pairs of data symbols are synchronized

Incorrect pair polarities of the differential signals are automatically corrected for all speeds.

### Wave Shaping, Slew-Rate Control, and Partial Response

In communication systems, signal transmission encoding methods are used to provide the noise-shaping feature and to minimize distortion and error in the transmission channel.

- For 1000Base-T, a special partial-response signaling method is used to provide the band-limiting feature for the transmission path.
- For 100Base-TX, a simple slew-rate control method is used to minimize EMI.
- For 10Base-T, pre-emphasis is used to extend the signal quality through the cable.

### PLL Clock Synthesizer

The KSZ9031RNX generates 125MHz, 25MHz, and 10MHz clocks for system timing. Internal clocks are generated from the external 25MHz crystal or reference clock.

## Auto-Negotiation

The KSZ9031RNX conforms to the auto-negotiation protocol, defined in Clause 28 of the IEEE 802.3 Specification.

Auto-negotiation allows UTP (unshielded twisted pair) link partners to select the highest common mode-of-operation.

During auto-negotiation, link partners advertise capabilities across the UTP link to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the operating mode.

The following list shows the speed and duplex operation mode from highest-to-lowest.

- Priority 1: 1000Base-T, full-duplex
- Priority 2: 1000Base-T, half-duplex
- Priority 3: 100Base-TX, full-duplex
- Priority 4: 100Base-TX, half-duplex
- Priority 5: 10Base-T, full-duplex
- Priority 6: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ9031RNX link partner is forced to bypass auto-negotiation for 10Base-T and 100Base-TX modes, the KSZ9031RNX sets its operating mode by observing the input signal at its receiver. This is known as parallel detection, and allows the KSZ9031RNX to establish a link by listening for a fixed signal protocol in the absence of the auto-negotiation advertisement protocol.

The auto-negotiation link-up process is shown in Figure 3.

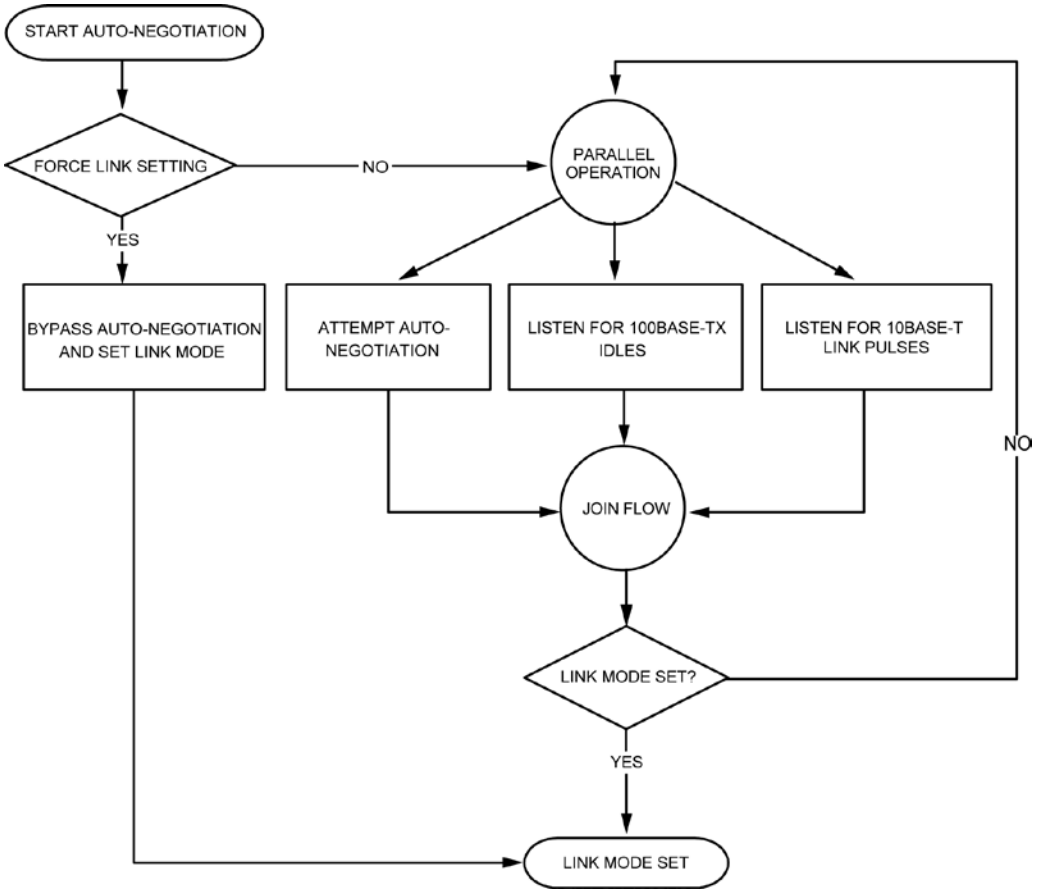



**Figure 3. Auto-Negotiation Flow Chart**

For 1000Base-T mode, auto-negotiation is always required to establish a link. During 1000Base-T auto-negotiation, the master and slave configuration is first resolved between link partners. Then the link is established with the highest common capabilities between link partners.

Auto-negotiation is enabled by default after power-up or hardware reset. After that, auto-negotiation can be enabled or disabled through Register 0h, Bit [12]. If auto-negotiation is disabled, the speed is set by Register 0h, Bits [6, 13] and the duplex is set by Register 0h, Bit [8].

If the speed is changed on the fly, the link goes down and auto-negotiation and parallel detection initiate until a common speed between KSZ9031RNX and its link partner is re-established for a link.

If the link is already established and there is no change of speed on the fly, the changes (for example, duplex and pause capabilities) will not take effect unless either auto-negotiation is restarted through Register 0h, Bit [9], or a link-down to link-up transition occurs (that is, disconnecting and reconnecting the cable).

After auto-negotiation is completed, the link status is updated in Register 1h, Bit [2], and the link partner capabilities are updated in Registers 5h, 6h, 8h, and Ah.

The auto-negotiation finite state machines use interval timers to manage the auto-negotiation process. The duration of these timers under normal operating conditions is summarized in Table 2.

**Table 2. Auto-Negotiation Timers**

| Auto-Negotiation Interval Timers | Time Duration |
|---|---|
| Transmit burst interval | 16ms |
| Transmit pulse interval | 68µs |
| FLP detect minimum time | 17.2µs |
| FLP detect maximum time | 185µs |
| Receive minimum burst interval | 6.8ms |
| Receive maximum burst interval | 112ms |
| Data detect minimum interval | 35.4µs |
| Data detect maximum interval | 95µs |
| NLP test minimum interval | 4.5ms |
| NLP test maximum interval | 30ms |
| Link loss time | 52ms |
| Break link time | 1480ms |
| Parallel detection wait time | 830ms |
| Link enable wait time | 1000ms |

## 10/100 Speeds Only

Some applications require link-up to be limited to 10/100Mbps speeds only.

After power-up/reset, the KSZ9031RNX can be restricted to auto-negotiate and link-up to 10/100Mbps speeds only by programming the following register settings:

1. Set Register 0h, Bit [6] = ‘0’ to remove 1000Mbps speed.
2. Set Register 9h, Bits [9:8] = ‘00’ to remove Auto-Negotiation Advertisements for 1000Mbps full/half duplex.
3. Write a ‘1’ to Register 0h, Bit [9], a self-clearing bit, to force a restart of Auto-Negotiation.

Auto-Negotiation and 10Base-T/100Base-TX speeds use only differential pairs A (pins 2, 3) and B (pins 5, 6). Differential pairs C (pins 7, 8) and D (pins 10, 11) can be left as no connects.

## RGMII Interface

The Reduced Gigabit Media Independent Interface (RGMII) supports on-chip data-to-clock delay timing according to the RGMII Version 2.0 Specification, with programming options for external delay timing and to adjust and correct TX and RX timing paths.

RGMII provides a common interface between RGMII PHYs and MACs, and has the following key characteristics:

- Pin count is reduced from 24 pins for the IEEE Gigabit Media Independent Interface (GMII) to 12 pins for RGMII.
- All speeds (10Mbps, 100Mbps, and 1000Mbps) are supported at both half- and full-duplex.
- Data transmission and reception are independent and belong to separate signal groups.
- Transmit data and receive data are each four bits wide, a nibble.

In RGMII operation, the RGMII pins function as follows:

- The MAC sources the transmit reference clock, TXC, at 125MHz for 1000Mbps, 25MHz for 100Mbps, and 2.5MHz for 10Mbps.
- The PHY recovers and sources the receive reference clock, RXC, at 125MHz for 1000Mbps, 25MHz for 100Mbps, and 2.5MHz for 10Mbps.
- For 1000Base-T, the transmit data, TXD[3:0], is presented on both edges of TXC, and the received data, RXD[3:0], is clocked out on both edges of the recovered 125MHz clock, RXC.
- For 10Base-T/100Base-TX, the MAC holds TX_CTL low until both PHY and MAC operate at the same speed. During the speed transition, the receive clock is stretched on either a positive or negative pulse to ensure that no clock glitch is presented to the MAC.
- TX_ER and RX_ER are combined with TX_EN and RX_DV, respectively, to form TX_CTL and RX_CTL. These two RGMII control signals are valid at the falling clock edge.

After power-up or reset, the KSZ9031RNX is configured to RGMII mode if the MODE[3:0] strap-in pins are set to one of the RGMII mode capability options. See the *Strapping Options* section for available options.

The KSZ9031RNX has the option to output a 125MHz reference clock on the CLK125_NDO pin. This clock provides a lower-cost reference clock alternative for RGMII MACs that require a 125MHz crystal or oscillator. The 125MHz clock output is enabled after power-up or reset if the CLK125_EN strap-in pin is pulled high.

### RGMII Signal Definition

Table 3 describes the RGMII signals. Refer to the RGMII Version 2.0 Specification for more detailed information.

**Table 3. RGMII Signal Definition**

| RGMII Signal Name (per spec) | RGMII Signal Name (per KSZ9031RNX) | Pin Type (with respect to PHY) | Pin Type (with respect to MAC) | Description |
|---|---|---|---|---|
| TXC | GTX_CLK | Input | Output | Transmit Reference Clock<br>(125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps) |
| TX_CTL | TX_EN | Input | Output | Transmit Control |
| TXD[3:0] | TXD[3:0] | Input | Output | Transmit Data[3:0] |
| RXC | RX_CLK | Output | Input | Receive Reference Clock<br>(125MHz for 1000Mbps, 25MHz for 100Mbps, 2.5MHz for 10Mbps) |
| RX_CTL | RX_DV | Output | Input | Receive Control |
| RXD[3:0] | RXD[3:0] | Output | Input | Receive Data[3:0] |

### RGMII Signal Diagram

The KSZ9031RNX RGMII pin connections to the MAC are shown in Figure 4.

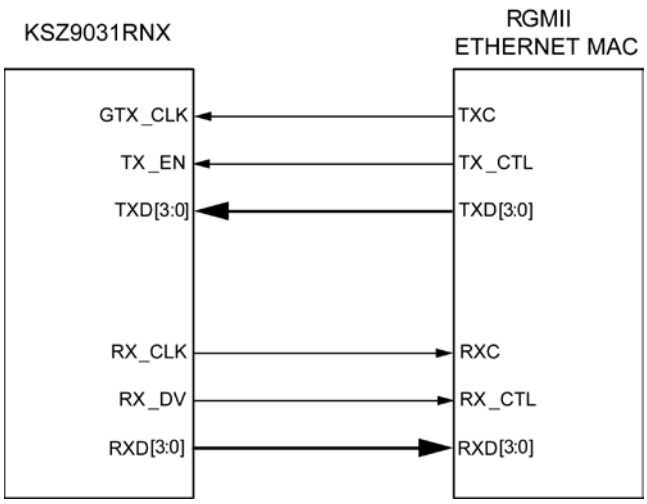



**Figure 4. KSZ9031RNX RGMII Interface**

### RGMII Pad Skew Registers

Pad skew registers are available for all RGMII pins (clocks, control signals, and data bits) to provide programming options to adjust or correct the timing relationship for each RGMII pin. Because RGMII is a source-synchronous bus interface, the timing relationship needs to be maintained only within the RGMII pin's respective timing group.

- RGMII transmit timing group pins: GTX_CLK, TX_EN, TXD[3:0]
- RGMII receive timing group pins: RX_CLK, RX_DV, RXD[3:0]

Table 4 details the four registers located at MMD Address 2h that are provided for pad skew programming.

**Table 4. RGMII Pad Skew Registers**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 4h – RGMII Control Signal Pad Skew** | | | | |
| 2.4.15:8 | Reserved | Reserved | RW | 0000_0000 |
| 2.4.7:4 | RX_DV Pad Skew | RGMII RX_CTL output pad skew control (0.06ns/step) | RW | 0111 |
| 2.4.3:0 | TX_EN Pad Skew | RGMII TX_CTL input pad skew control (0.06ns/step) | RW | 0111 |
| **MMD Address 2h, Register 5h – RGMII RX Data Pad Skew** | | | | |
| 2.5.15:12 | RXD3 Pad Skew | RGMII RXD3 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.11:8 | RXD2 Pad Skew | RGMII RXD2 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.7:4 | RXD1 Pad Skew | RGMII RXD1 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.3:0 | RXD0 Pad Skew | RGMII RXD0 output pad skew control (0.06ns/step) | RW | 0111 |
| **MMD Address 2h, Register 6h – RGMII TX Data Pad Skew** | | | | |
| 2.6.15:12 | TXD3 Pad Skew | RGMII TXD3 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.11:8 | TXD2 Pad Skew | RGMII TXD2 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.7:4 | TXD1 Pad Skew | RGMII TXD1 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.3:0 | TXD0 Pad Skew | RGMII TXD0 input pad skew control (0.06ns/step) | RW | 0111 |
| **MMD Address 2h, Register 8h – RGMII Clock Pad Skew** | | | | |
| 2.8.15:10 | Reserved | Reserved | RW | 0000_00 |
| 2.8.9:5 | GTX_CLK Pad Skew | RGMII GTX_CLK input pad skew control (0.06ns/step) | RW | 01_111 |
| 2.8.4:0 | RX_CLK Pad Skew | RGMII RX_CLK output pad skew control (0.06ns/step) | RW | 0_1111 |

The RGMII control signals and data bits have 4-bit skew settings, while the RGMII clocks have 5-bit skew settings.

Each register bit is approximately a 0.06ns step change. A single-bit decrement decreases the delay by approximately 0.06ns, while a single-bit increment increases the delay by approximately 0.06ns.

Table 5 and Table 6 list the approximate absolute delay for each pad skew (value) setting.

**Table 5. Absolute Delay for 5-Bit Pad Skew Setting**

| Pad Skew (value) | Delay (ns) |
|---|---|
| 0_0000 | –0.90 |
| 0_0001 | –0.84 |
| 0_0010 | –0.78 |
| 0_0011 | –0.72 |
| 0_0100 | –0.66 |
| 0_0101 | –0.60 |
| 0_0110 | –0.54 |
| 0_0111 | –0.48 |
| 0_1000 | –0.42 |
| 0_1001 | –0.36 |
| 0_1010 | –0.30 |
| 0_1011 | –0.24 |
| 0_1100 | –0.18 |
| 0_1101 | –0.12 |
| 0_1110 | –0.06 |
| 0_1111 | No delay adjustment (default value) |
| 1_0000 | +0.06 |
| 1_0001 | +0.12 |
| 1_0010 | +0.18 |
| 1_0011 | +0.24 |
| 1_0100 | +0.30 |
| 1_0101 | +0.36 |
| 1_0110 | +0.42 |
| 1_0111 | +0.48 |
| 1_1000 | +0.54 |
| 1_1001 | +0.60 |
| 1_1010 | +0.66 |
| 1_1011 | +0.72 |
| 1_1100 | +0.78 |
| 1_1101 | +0.84 |
| 1_1110 | +0.90 |
| 1_1111 | +0.96 |

**Table 6. Absolute Delay for 4-Bit Pad Skew Setting**

| Pad Skew (value) | Delay (ns) |
|---|---|
| 0000 | –0.42 |
| 0001 | –0.36 |
| 0010 | –0.30 |
| 0011 | –0.24 |
| 0100 | –0.18 |
| 0101 | –0.12 |
| 0110 | –0.06 |
| 0111 | No delay adjustment (default value) |
| 1000 | +0.06 |
| 1001 | +0.12 |
| 1010 | +0.18 |
| 1011 | +0.24 |
| 1100 | +0.30 |
| 1101 | +0.36 |
| 1110 | +0.42 |
| 1111 | +0.48 |

When computing the RGMII timing relationships, delays along the entire data path must be aggregated to determine the total delay to be used for comparison between RGMII pins within their respective timing group. For the transmit data path, total delay includes MAC output delay, MAC-to-PHY PCB routing delay, and PHY (KSZ9031RNX) input delay and skew setting (if any). For the receive data path, the total delay includes PHY (KSZ9031RNX) output delay, PHY-to-MAC PCB routing delay, and MAC input delay and skew setting (if any).

As the default, after power-up or reset, the KSZ9031RNX RGMII timing conforms to the timing requirements in the RGMII Version 2.0 Specification for internal PHY chip delay.

For the transmit path (MAC to KSZ9031RNX), the KSZ9031RNX does not add any delay locally at its GTX_CLK, TX_EN and TXD[3:0] input pins, and expects the GTX_CLK delay to be provided on-chip by the MAC. If MAC does not provide any delay or insufficient delay for the GTX_CLK, the KSZ9031RNX has pad skew registers that can provide up to 1.38ns on-chip delay.

For the receive path (KSZ9031RNX to MAC), the KSZ9031RNX adds 1.2ns typical delay to the RX_CLK output pin with respect to RX_DV and RXD[3:0] output pins. If necessary, the KSZ9031RNX has pad skew registers that can adjust the RX_CLK on-chip delay up to 2.58ns from the 1.2ns default delay.

The above default RGMII timings imply:

- RX_CLK clock skew is set by the KSZ9031RNX default register settings.
- GTX_CLK clock skew is provided by the MAC.
- No PCB delay is required for GTX_CLK and RX_CLK clocks.

The following examples show how to read/write to MMD Address 2h, Register 8h for the RGMII GTX_CLK and RX_CLK skew settings. MMD register access is through the direct portal Registers Dh and Eh. For more programming details, refer to the *MMD Registers – Descriptions* section.

- Read back value of MMD Address 2h, Register 8h.
  - Write Register 0xD = 0x0002 // Select MMD Device Address 2h
  - Write Register 0xE = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write Register 0xD = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Read Register 0xE // Read value of MMD Device Address 2h, Register 8h

- Write value 0x03FF (delay GTX_CLK and RX_CLK pad skews to their maximum values) to MMD Address 2h, Register 8h
  - Write Register 0xD = 0x0002 // Select MMD Device Address 2h
  - Write Register 0xE = 0x0008 // Select Register 8h of MMD Device Address 2h
  - Write Register 0xD = 0x4002 // Select register data for MMD Device Address 2h, Register 8h
  - Write Register 0xE = 0x03FF // Write value 0x03FF to MMD Device Address 2h, Register 8h

**RGMII In-Band Status**

The KSZ9031RNX provides in-band status to the MAC during the inter-frame gap when RX_DV is de-asserted. RGMII in-band status is always enabled after power-up.

The in-band status is sent to the MAC using the RXD[3:0] data pins, and is described in Table 7.

**Table 7. RGMII In-Band Status**

| RX_DV | RXD3 | RXD[2:1] | RXD0 |
|---|---|---|---|
| 0<br>(valid only when RX_DV is low) | Duplex Status<br>0 = Half-duplex<br>1 = Full-duplex | RX_CLK clock speed<br>00 = 2.5MHz (10Mbps)<br>01 = 25MHz (100Mbps)<br>10 = 125MHz (1000Mbps)<br>11 = Reserved | Link Status<br>0 = Link down<br>1 = Link up |

## MII Management (MIIM) Interface

The KSZ9031RNX supports the IEEE 802.3 MII Management interface, also known as the Management Data Input/ Output (MDIO) interface. This interface allows upper-layer devices to monitor and control the state of the KSZ9031RNX. An external device with MIIM capability is used to read the PHY status and/or configure the PHY settings. More details about the MIIM interface can be found in Clause 22.2.4 of the IEEE 802.3 Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the clock line (MDC) and the data line (MDIO).
- A specific protocol that operates across the physical connection mentioned earlier, which allows an external controller to communicate with one or more KSZ9031RNX devices. Each KSZ9031RNX device is assigned a unique PHY address between 0h and 7h by the PHYAD[2:0] strapping pins.
- A 32-register address space for direct access to IEEE-defined registers and vendor-specific registers, and for indirect access to MMD addresses and registers. See the *Register Map* section.

PHY Address 0h is supported as the unique PHY address only; it is not supported as the broadcast PHY address, which allows for a single write command to simultaneously program an identical PHY register for two or more PHY devices (for example, using PHY Address 0h to set Register 0h to a value of 0x1940 to set Bit [11] to a value of one to enable software power-down). Instead, separate write commands are used to program each PHY device.

Table 8 shows the MII Management frame format for the KSZ9031RNX.

**Table 8. MII Management Frame Format for the KSZ9031RNX**

| | Preamble | Start of Frame | Read/Write OP Code | PHY Address Bits [4:0] | REG Address Bits [4:0] | TA | Data Bits [15:0] | Idle |
|---|---|---|---|---|---|---|---|---|
| **Read** | 32 1's | 01 | 10 | 00AAA | RRRRR | Z0 | DDDDDDDD_DDDDDDDD | Z |
| **Write** | 32 1's | 01 | 01 | 00AAA | RRRRR | 10 | DDDDDDDD_DDDDDDDD | Z |

## Interrupt (INT_N)

The INT_N pin is an optional interrupt signal that is used to inform the external controller that there has been a status update in the KSZ9031RNX PHY Register. Bits [15:8] of Register 1Bh are the interrupt control bits that enable and disable the conditions for asserting the INT_N signal. Bits [7:0] of Register 1Bh are the interrupt status bits that indicate which interrupt conditions have occurred. The interrupt status bits are cleared after reading Register 1Bh.

Bit [14] of Register 1Fh sets the interrupt level to active high or active low. The default is active low.

The MII Management bus option gives the MAC processor complete access to the KSZ9031RNX control and status registers. Additionally, an interrupt pin eliminates the need for the processor to poll the PHY for status change.

## LED Mode

The KSZ9031RNX provides two programmable LED output pins, LED2 and LED1, which are configurable to support two LED modes. The LED mode is configured by the LED_MODE strap-in (Pin 41). It is latched at power-up/reset and is defined as follows:

- Pull-up: Single-LED mode
- Pull-down: Tri-color dual-LED mode

### Single-LED Mode

In single-LED mode, the LED2 pin indicates the link status while the LED1 pin indicates the activity status, as shown in Table 9.

**Table 9. Single-LED Mode – Pin Definition**

| LED Pin | Pin State | LED Definition | Link/Activity |
|---|---|---|---|
| **LED2** | H | OFF | Link off |
| | L | ON | Link on (any speed) |
| **LED1** | H | OFF | No activity |
| | Toggle | Blinking | Activity (RX, TX) |

### Tri-color Dual-LED Mode

In tri-color dual-LED mode, the link and activity status are indicated by the LED2 pin for 1000Base-T; by the LED1 pin for 100Base-TX; and by both LED2 and LED1 pins, working in conjunction, for 10Base-T. This is summarized in Table 10.

**Table 10. Tri-color Dual-LED Mode – Pin Definition**

| LED Pin (State) | | LED Pin (Definition) | | Link/Activity |
|---|---|---|---|---|
| **LED2** | **LED1** | **LED2** | **LED1** | |
| H | H | OFF | OFF | Link off |
| L | H | ON | OFF | 1000 Link / No activity |
| Toggle | H | Blinking | OFF | 1000 Link / Activity (RX, TX) |
| H | L | OFF | ON | 100 Link / No activity |
| H | Toggle | OFF | Blinking | 100 Link / Activity (RX, TX) |
| L | L | ON | ON | 10 Link / No activity |
| Toggle | Toggle | Blinking | Blinking | 10 Link / Activity (RX, TX) |

Each LED output pin can directly drive an LED with a series resistor (typically 220Ω to 470Ω).

## Loopback Mode

The KSZ9031RNX supports the following loopback operations to verify analog and/or digital data paths.

- Local (digital) loopback
- Remote (analog) loopback

### Local (Digital) Loopback

This loopback mode checks the RGMII transmit and receive data paths between KSZ9031RNX and external MAC, and is supported for all three speeds (10/100/1000Mbps) at full-duplex.

The loopback data path is shown in Figure 5.

- RGMII MAC transmits frames to KSZ9031RNX.
- Frames are wrapped around inside KSZ9031RNX.
- KSZ9031RNX transmits frames back to RGMII MAC.

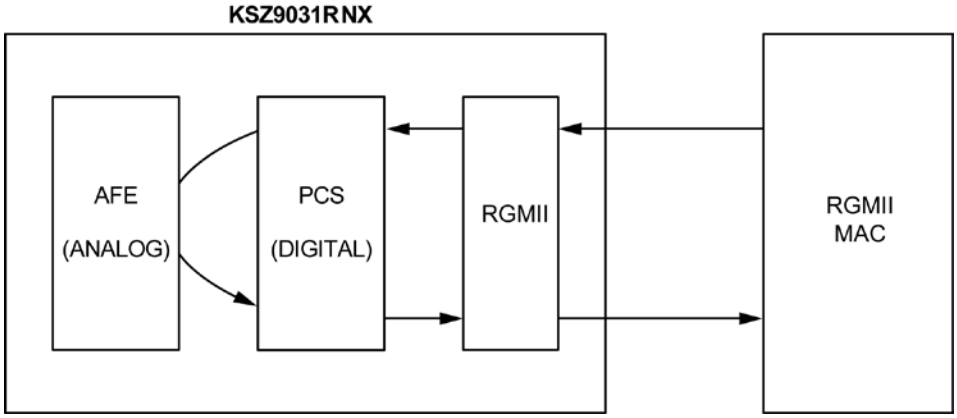



**Figure 5. Local (Digital) Loopback**

The following programming steps and register settings are used for local loopback mode.

For 1000Mbps loopback,

- Set Register 0h,
  - Bit [14] = 1 // Enable local loopback mode
  - Bits [6, 13] = 10 // Select 1000Mbps speed
  - Bit [12] = 0 // Disable auto-negotiation
  - Bit [8] = 1 // Select full-duplex mode
- Set Register 9h,
  - Bit [12] = 1 // Enable master-slave manual configuration
  - Bit [11] = 0 // Select slave configuration (required for loopback mode)

For 10/100Mbps loopback,

- Set Register 0h,
  - Bit [14] = 1 // Enable local loopback mode
  - Bits [6, 13] = 00 / 01 // Select 10Mbps/100Mbps speed
  - Bit [12] = 0 // Disable auto-negotiation
  - Bit [8] = 1 // Select full-duplex mode

**Remote (Analog) Loopback**

This loopback mode checks the line (differential pairs, transformer, RJ-45 connector, Ethernet cable) transmit and receive data paths between KSZ9031RNX and its link partner, and is supported for 1000Base-T full-duplex mode only.

The loopback data path is shown in Figure 6.

- The Gigabit PHY link partner transmits frames to KSZ9031RNX.
- Frames are wrapped around inside KSZ9031RNX.
- KSZ9031RNX transmits frames back to the Gigabit PHY link partner.

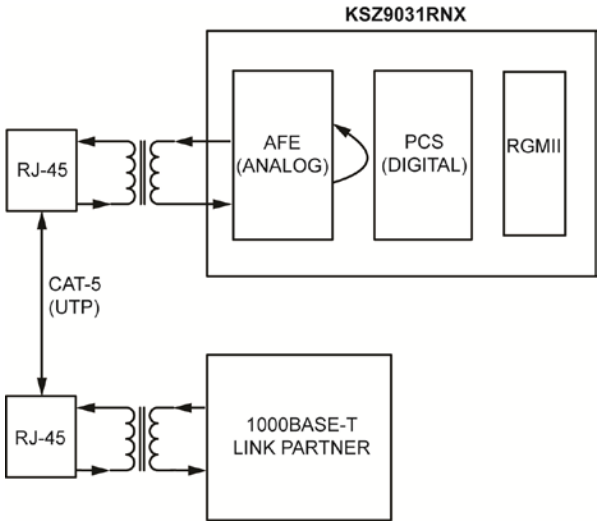



**Figure 6. Remote (Analog) Loopback**

The following programming steps and register settings are used for remote loopback mode.

- Set Register 0h,
  - Bits [6, 13] = 10 // Select 1000Mbps speed
  - Bit [12] = 0 // Disable auto-negotiation
  - Bit [8] = 1 // Select full-duplex mode

Or just auto-negotiate and link up at 1000Base-T full-duplex mode with link partner.

- Set Register 11h,
  - Bit [8] = 1 // Enable remote loopback mode

## LinkMD® Cable Diagnostic

The LinkMD function uses time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems, such as open circuits, short circuits, and impedance mismatches.

LinkMD operates by sending a pulse of known amplitude and duration down the selected differential pair, then analyzing the polarity and shape of the reflected signal to determine the type of fault: open circuit for a positive/non-inverted amplitude reflection and short circuit for a negative/inverted amplitude reflection. The time duration for the reflected signal to return provides the approximate distance to the cabling fault. The LinkMD function processes this TDR information and presents it as a numerical value that can be translated to a cable distance.

LinkMD is initiated by accessing Register 12h, the LinkMD – Cable Diagnostic register, in conjunction with Register 1Ch, the Auto MDI/MDI-X register. The latter register is needed to disable the Auto MDI/MDI-X function before running the LinkMD test. Additionally, a software reset (Reg. 0h, Bit [15] = 1) should be performed before and after running the LinkMD test. The reset helps to ensure the KSZ9031RNX is in the normal operating state before and after the test.

## NAND Tree Support

The KSZ9031RNX provides parametric NAND tree support for fault detection between chip I/Os and board. NAND tree mode is enabled at power-up/reset with the MODE[3:0] strap-in pins set to ‘0100’. Table 11 lists the NAND tree pin order.

**Table 11. NAND Tree Test Pin Order for KSZ9031RNX**

| Pin | Description |
|---|---|
| LED2 | Input |
| LED1/PME_N1 | Input |
| TXD0 | Input |
| TXD1 | Input |
| TXD2 | Input |
| TXD3 | Input |
| GTX_CLK | Input |
| TX_EN | Input |
| RX_DV | Input |
| RX_CLK | Input |
| INT_N/PME_N2 | Input |
| MDC | Input |
| MDIO | Input |
| CLK125_NDO | Output |

## Power Management

The KSZ9031RNX incorporates a number of power-management modes and features that provide methods to consume less energy. These are discussed in the following sections.

### Energy-Detect Power-Down Mode

Energy-detect power-down (EDPD) mode is used to further reduce the transceiver power consumption when the cable is unplugged. It is enabled by writing a one to MMD Address 1Ch, Register 23h, Bit [0], and is in effect when auto-negotiation mode is enabled and the cable is disconnected (no link).

In EDPD Mode, the KSZ9031RNX shuts down all transceiver blocks, except for the transmitter and energy detect circuits. Power can be reduced further by extending the time interval between the transmissions of link pulses to check for the presence of a link partner. The periodic transmission of link pulses is needed to ensure the KSZ9031RNX and its link partner, when operating in the same low-power state and with Auto MDI/MDI-X disabled, can wake up when the cable is connected between them. By default, EDPD mode is disabled after power-up.

### Software Power-Down Mode

This mode is used to power down the KSZ9031RNX device when it is not in use after power-up. Software power-down (SPD) mode is enabled by writing a one to Register 0h, Bit [11]. In the SPD state, the KSZ9031RNX disables all internal functions, except for the MII management interface. The KSZ9031RNX exits the SPD state after a zero is written to Register 0h, Bit [11].

### Chip Power-Down Mode

This mode provides the lowest power state for the KSZ9031RNX device when it is mounted on the board but not in use. Chip power-down (CPD) mode is enabled after power-up/reset with the MODE[3:0] strap-in pins set to ‘0111’. The KSZ9031RNX exits CPD mode after a hardware reset is applied to the RESET_N pin (Pin 42) with the MODE[3:0] strap-in pins set to an operating mode other than CPD.

## Energy Efficient Ethernet (EEE)

The KSZ9031RNX implements Energy Efficient Ethernet (EEE) as described in IEEE Standard 802.3az for line signaling by the four differential pairs (analog side) and according to the multisource agreement (MSA) of collaborating Gigabit Ethernet chip vendors for the RGMII (digital side). This agreement is based on the IEEE Standard's EEE implementation for GMII (1000Mbps) and MII (100Mbps). The specification is defined around an EEE-compliant MAC on the host side and an EEE-compliant link partner on the line side that support the special signaling associated with EEE. EEE saves power by keeping the AC signal on the copper Ethernet cable at approximately 0V peak-to-peak as often as possible during periods of no traffic activity, while maintaining the link-up status. This is referred to as low-power idle (LPI) mode or state.

During LPI mode, the copper link responds automatically when it receives traffic and resumes normal PHY operation immediately, without blockage of traffic or loss of packet. This involves exiting LPI mode and returning to normal 100/1000Mbps operating mode. Wake-up times are <16µs for 1000Base-T and <30µs for 100Base-TX.The LPI state is controlled independently for transmit and receive paths, allowing the LPI state to be active (enabled) for:

- Transmit cable path only
- Receive cable path only
- Both transmit and receive cable paths

The KSZ9031RNX has the EEE function disabled as the power-up default setting. The EEE function is enabled by setting the following EEE advertisement bits at MMD Address 7h, Register 3Ch, followed by restarting auto-negotiation (writing a '1' to Register 0h, Bit [9]):

- Bit [2] = 1 // Enable 1000Mbps EEE mode
- Bit [1] = 1 // Enable 100Mbps EEE mode

For standard (non-EEE) 10Base-T mode, normal link pulses (NLPs) with long periods of no AC signal transmission are used to maintain the link during the idle period when there is no traffic activity. To save more power, the KSZ9031RNX provides the option to enable 10Base-Te mode, which saves additional power by reducing the transmitted signal amplitude from 2.5V to 1.75V. To enable 10Base-Te mode, write a '1' to MMD Address 1Ch, Register 4h, Bit [10].

During LPI mode, refresh transmissions are used to maintain the link; power savings occur in quiet periods. Approximately every 20 to 22 milliseconds, a refresh transmission of 200 to 220 microseconds is sent to the link partner. The refresh transmissions and quiet periods are shown in Figure 7.

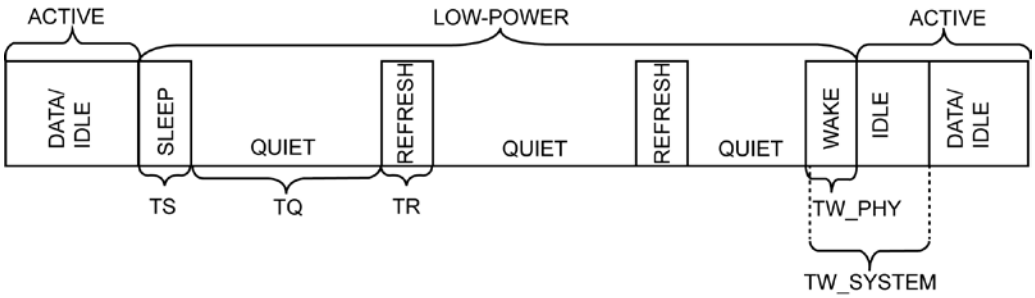



**Figure 7. LPI Mode (Refresh Transmissions and Quiet Periods)**

**Transmit Direction Control (MAC-to-PHY)**

RGMII 1000Mbps transmission from MAC-to-PHY uses both rising and falling edges of the GTX_CLK clock. The KSZ9031RNX uses the TX_EN pin as the RGMII transmit control signal (TX_CTL) to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge. It also uses the TXD[3:0] pins to clock in the TX data low nibble bits [3:0] on the rising edge and the TX data high nibble Bits [7:4] on the falling edge.

The KSZ9031RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the TX_EN signal (the TX_CTL pin outputs low on the rising edge), asserts the TX_ER signal (the TX_CTL pin outputs high on the falling edge), and sets TX data Bits [7:0] to 0000_0001 (TXD[3:0] pins output 0001 on the rising edge and 0000 on the falling edge). The KSZ9031RNX remains in the 1000Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9031RNX exits the LPI transmit state.

To save more power, the MAC can stop the GTX_CLK clock after the RGMII signals for the LPI state have been asserted for 10 or more GTX_CLK clock cycles.

Figure 8 shows the LPI transition for RGMII transmit in 1000Mbps mode.

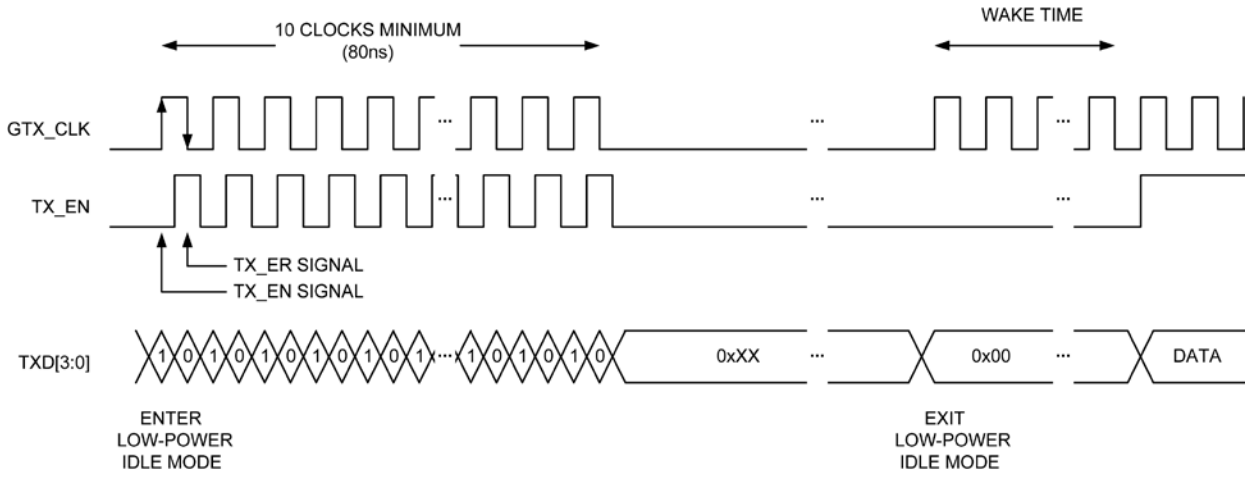



**Figure 8. LPI Transition – RGMII (1000Mbps) Transmit**

RGMII 100Mbps transmission from MAC-to-PHY uses both rising and falling edges of the GTX_CLK clock. The KSZ9031RNX uses the TX_EN pin as the RGMII transmit control signal (TX_CTL) to clock in the TX_EN signal on the rising edge and the TX_ER signal on the falling edge. It also uses the TXD[3:0] pins to clock in the TX data Bits [3:0] on the rising edge.

The KSZ9031RNX enters LPI mode for the transmit direction when its attached EEE-compliant MAC de-asserts the TX_EN signal (the TX_CTL pin outputs low on the rising edge), asserts the TX_ER signal (the TX_CTL pin outputs high on the falling edge), and sets TX data Bits [3:0] to 0001 (the TXD[3:0] pins output 0001). The KSZ9031RNX remains in the 100Mbps transmit LPI state while the MAC maintains the states of these signals. When the MAC changes any of the TX_EN, TX_ER, or TX data signals from their LPI state values, the KSZ9031RNX exits the LPI transmit state.

To save more power, the MAC can stop the GTX_CLK clock after the RGMII signals for the LPI state have been asserted for 10 or more GTX_CLK clock cycles.

Figure 9 shows the LPI transition for RGMII transmit in 100Mbps mode.

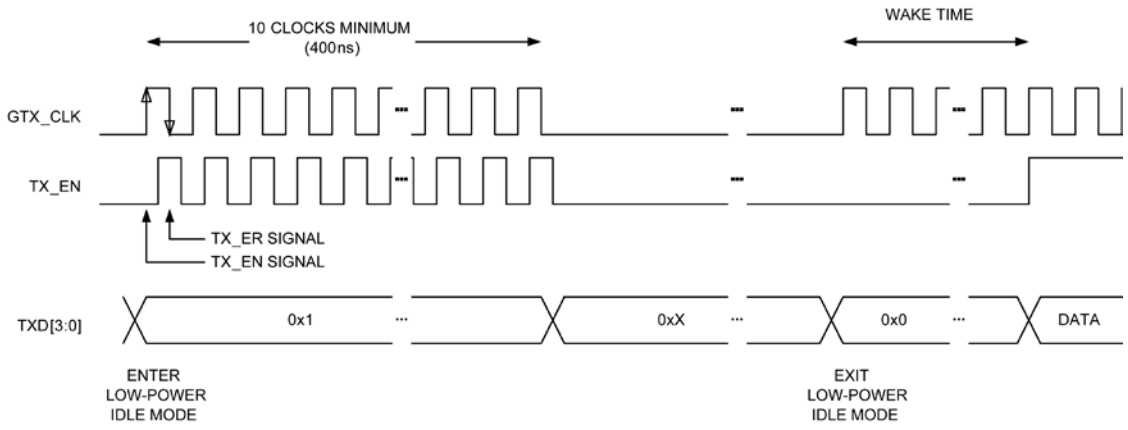



**Figure 9. LPI Transition – RGMII (100Mbps) Transmit**

### Receive Direction Control (PHY-to-MAC)

RGMII 1000Mbps transmission from PHY-to-MAC uses both rising and falling edges of the RX_CLK clock. The KSZ9031RNX uses the RX_DV pin as the RGMII receive control signal (RX_CTL) to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge It also uses the RXD[3:0] pins to clock out the RX data low nibble Bits [3:0] on the rising edge and the RX data high nibble Bits [7:4] on the falling edge.

The KSZ9031RNX enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the RX_DV pin low on the rising clock edge and high on the falling clock edge to de-assert the RX_DV signal and assert the RX_ER signal, respectively, to the MAC. Also, the RXD[3:0] pins are driven to 0001 on the rising clock edge and 0000 on the falling clock edge to set the RX data Bits [7:0] to 0000_0001. The KSZ9031RNX remains in the 1000Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9031RNX receives a non /P/ code bit pattern (non-Refresh), it exits the receive LPI state and sets the RX_DV and RXD[3:0] output pins accordingly for a normal frame or normal idle.

To save more power, the KSZ9031RNX stops the RX_CLK clock output to the MAC after 10 or more RX_CLK clock cycles have occurred in the receive LPI state.

Figure 10 shows the LPI transition for RGMII receive in 1000Mbps mode.

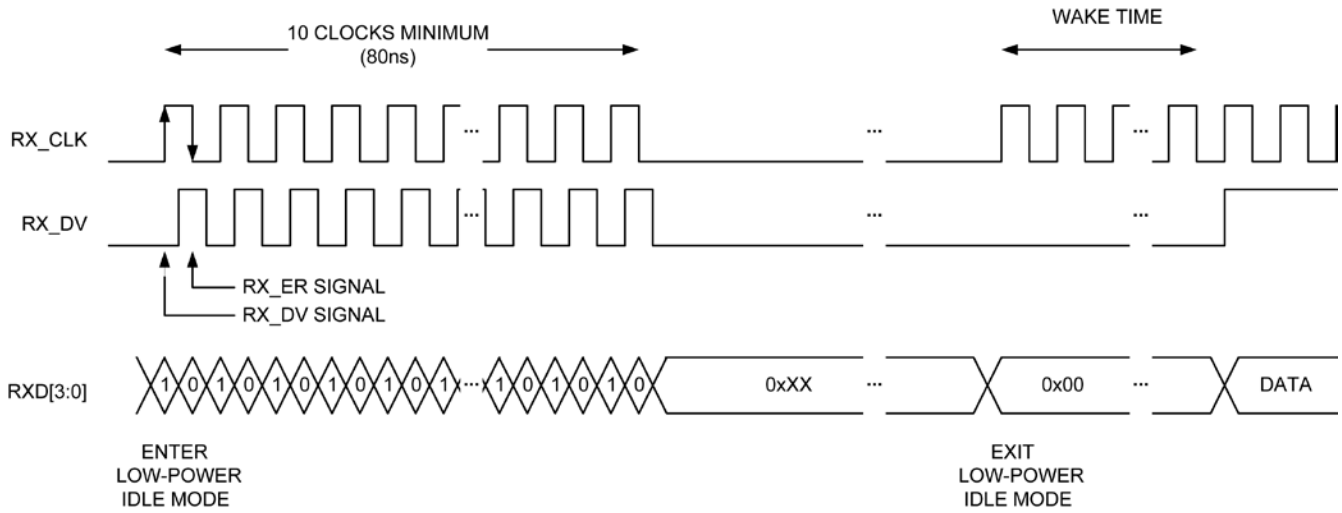



**Figure 10. LPI Transition – RGMII (1000Mbps) Receive**

RGMII 100Mbps transmission from PHY-to-MAC uses both rising and falling edges of the RX_CLK clock. The KSZ9031RNX uses the RX_DV pin as the RGMII receive control signal (RX_CTL) to clock out the RX_DV signal on the rising edge and the RX_ER signal on the falling edge. It also uses the RXD[3:0] pins to clock out the RX data Bits [3:0] on the rising edge.

The KSZ9031RNX enters LPI mode for the receive direction when it receives the /P/ code bit pattern (sleep/refresh) from its EEE-compliant link partner. It then drives the RX_DV pin low on the rising clock edge and high on the falling clock edge to de-assert the RX_DV signal and assert the RX_ER signal, respectively, to the MAC. Also, the RXD[3:0] pins are driven to 0001. The KSZ9031RNX remains in the 100Mbps receive LPI state while it continues to receive the refresh from its link partner, so it will continue to maintain and drive the LPI output states for the RGMII receive output pins to inform the attached EEE-compliant MAC that it is in the receive LPI state. When the KSZ9031RNX receives a non /P/ code bit pattern (non-refresh), it exits the receive LPI state and sets the RX_DV and RXD[3:0] output pins accordingly for a normal frame or normal idle.

The KSZ9031RNX stops the RX_CLK clock output to the MAC after 10 or more RX_CLK clock cycles have occurred in the receive LPI state to save more power.

Figure 11 shows the LPI transition for RGMII receive in 100Mbps mode.

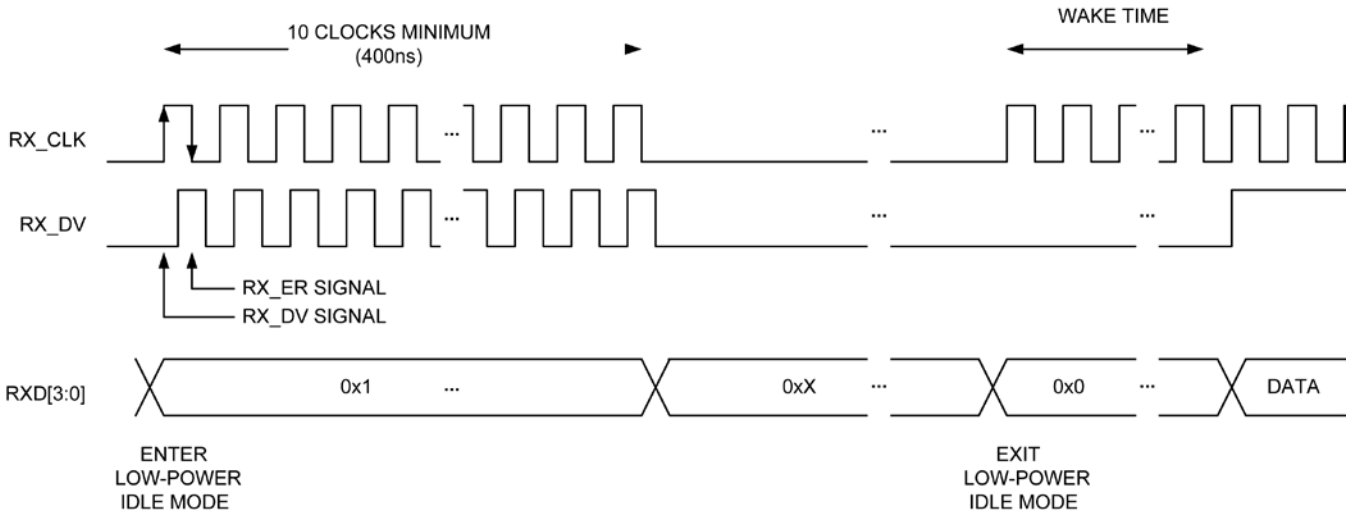



**Figure 11. LPI Transition – RGMII (100Mbps) Receive**

### Registers Associated with EEE

The following MMD registers are provided for EEE configuration and management:

- MMD Address 3h, Register 0h - PCS EEE – Control register
- MMD Address 3h, Register 1h - PCS EEE – Status register
- MMD Address 7h, Register 3Ch - EEE Advertisement register
- MMD Address 7h, Register 3Dh - EEE Link Partner Advertisement register

## Wake-On-LAN

Wake-On-LAN (WOL) is normally a MAC-based function to wake up a host system (for example, an Ethernet end device, such as a PC) that is in standby power mode. Wake-up is triggered by receiving and detecting a special packet (commonly referred to as the “magic packet”) that is sent by the remote link partner. The KSZ9031RNX can perform the same WOL function if the MAC address of its associated MAC device is entered into the KSZ9031RNX PHY registers for magic-packet detection. When the KSZ9031RNX detects the magic packet, it wakes up the host by driving its power management event (PME) output pin low.

By default, the WOL function is disabled. It is enabled by setting the enabling bit and configuring the associated registers for the selected PME wake-up detection method.

The KSZ9031RNX provides three methods to trigger a PME wake-up:

- Magic-packet detection
- Customized-packet detection
- Link status change detection

### Magic-Packet Detection

The magic packet’s frame format starts with 6 bytes of 0xFFh and is followed by 16 repetitions of the MAC address of its associated MAC device (local MAC device).

When the magic packet is detected from its link partner, the KSZ9031RNX asserts its PME output pin low.

The following MMD Address 2h registers are provided for magic-packet detection:

- Magic-packet detection is enabled by writing a ‘1’ to MMD Address 2h, Register 10h, Bit [6]
- The MAC address (for the local MAC device) is written to and stored in MMD Address 2h, Registers 11h – 13h

The KSZ9031RNX does not generate the magic packet. The magic packet must be provided by the external system.

### Customized-Packet Detection

The customized packet has associated register/bit masks to select which byte, or bytes, of the first 64 bytes of the packet to use in the CRC calculation. After the KSZ9031RNX receives the packet from its link partner, the selected bytes for the received packet are used to calculate the CRC. The calculated CRC is compared to the expected CRC value that was previously written to and stored in the KSZ9031RNX PHY registers. If there is a match, the KSZ9031RNX asserts its PME output pin low.

Four customized packets are provided to support four types of wake-up scenarios. A dedicated set of registers is used to configure and enable each customized packet.

The following MMD registers are provided for customized-packet detection:

- Each of the four customized packets is enabled via MMD Address 2h, Register 10h,
  - Bit [2] // For customized packets, type 0
  - Bit [3] // For customized packets, type 1
  - Bit [4] // For customized packets, type 2
  - Bit [5] // For customized packets, type 3
- 32-bit expected CRCs are written to and stored in:
  - MMD Address 2h, Registers 14h – 15h // For customized packets, type 0
  - MMD Address 2h, Registers 16h – 17h // For customized packets, type 1
  - MMD Address 2h, Registers 18h – 19h // For customized packets, type 2
  - MMD Address 2h, Registers 1Ah – 1Bh // For customized packets, type 3
- Masks to indicate which of the first 64-bytes to use in the CRC calculation are set in:
  - MMD Address 2h, Registers 1Ch – 1Fh // For customized packets, type 0
  - MMD Address 2h, Registers 20h – 23h // For customized packets, type 1
  - MMD Address 2h, Registers 24h – 27h // For customized packets, type 2
  - MMD Address 2h, Registers 28h – 2Bh // For customized packets, type 3

**Link Status Change Detection**

If link status change detection is enabled, the KSZ9031RNX asserts its PME output pin low whenever there is a link status change, using the following MMD Address 2h register bits and their enabled (1) or disabled (0) settings:

- MMD Address 2h, Register 10h, Bit [0] // For link-up detection
- MMD Address 2h, Register 10h, Bit [1] // For link-down detection

The PME output signal is available on either LED1/PME_N1 (Pin 17) or INT_N/PME_N2 (Pin 38), and is selected and enabled using MMD Address 2h, Register 2h, Bits [8] and [10], respectively. Additionally, MMD Address 2h, Register 10h, Bits [15:14] defines the output functions for Pins 17 and 38.

The PME output is active low and requires a 1kΩ pull-up to the VDDIO supply. When asserted, the PME output is cleared by disabling the register bit that enabled the PME trigger source (magic packet, customized packet, link status change).

## Typical Current/Power Consumption

Table 12 through Table 15 show the typical current consumption by the core (DVDDL, AVDDL, AVDDL_PLL), transceiver (AVDDH) and digital I/O (DVDDH) supply pins, and the total typical power for the entire KSZ9031RNX device for various nominal operating voltage combinations.

**Table 12. Typical Current/Power Consumption – Transceiver (3.3V), Digital I/Os (3.3V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 3.3V Transceiver (AVDDH) | 3.3V Digital I/Os (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| | mA | mA | mA | mW |
| 1000Base-T link-up (no traffic) | 210 | 67.4 | 19.5 | 538 |
| 1000Base-T full-duplex @ 100% utilization | 221 | 66.3 | 41.5 | 621 |
| 100Base-TX link-up (no traffic) | 63.6 | 28.7 | 13.9 | 217 |
| 100Base-TX full-duplex @ 100% utilization | 63.8 | 28.6 | 17.2 | 228 |
| 10Base-T link-up (no traffic) | 7.1 | 15.9 | 11.5 | 99 |
| 10Base-T full-duplex @ 100% utilization | 7.7 | 28.6 | 13.7 | 149 |
| EEE Mode – 1000Mbps | 43.5 | 5.7 | 30.6 | 172 |
| EEE Mode – 100Mbps (TX and RX in LPI) | 25.6 | 5.3 | 18.1 | 108 |
| Software power-down mode (Reg. 0h.11 = 1) | 1.0 | 4.2 | 9.3 | 46 |

**Table 13. Typical Current/Power Consumption – Transceiver (3.3V), Digital I/Os (1.8V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 3.3V Transceiver (AVDDH) | 1.8V Digital I/Os (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| | mA | mA | mA | mW |
| 1000Base-T link-up (no traffic) | 210 | 67.4 | 11.2 | 494 |
| 1000Base-T full-duplex @ 100% utilization | 221 | 66.3 | 23.6 | 526 |
| 100Base-TX link-up (no traffic) | 63.6 | 28.7 | 8.4 | 186 |
| 100Base-TX full-duplex @ 100% utilization | 63.8 | 28.6 | 9.8 | 189 |
| 10Base-T link-up (no traffic) | 7.1 | 15.9 | 3.6 | 67 |
| 10Base-T full-duplex @ 100% utilization | 7.7 | 28.6 | 5.6 | 114 |
| EEE Mode – 1000Mbps | 43.5 | 5.7 | 15.9 | 100 |
| EEE Mode – 100Mbps (TX and RX in LPI) | 25.6 | 5.3 | 9.1 | 65 |
| Software power-down mode (Reg. 0h.11 = 1) | 1.0 | 4.2 | 5.5 | 25 |

**Table 14. Typical Current/Power Consumption – Transceiver (2.5V), Digital I/Os (2.5V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 2.5V Transceiver[4] (AVDDH – Commercial Temperature Only) | 2.5V Digital I/Os (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| | mA | mA | mA | mW |
| 1000Base-T link-up (no traffic) | 210 | 58.8 | 14.7 | 435 |
| 1000Base-T full-duplex @ 100% utilization | 221 | 57.9 | 31.5 | 488 |
| 100Base-TX link-up (no traffic) | 63.6 | 24.9 | 10.5 | 165 |
| 100Base-TX full-duplex @ 100% utilization | 63.8 | 24.9 | 13.0 | 171 |
| 10Base-T link-up (no traffic) | 7.1 | 11.5 | 6.3 | 53 |
| 10Base-T full-duplex @ 100% utilization | 7.7 | 25.3 | 9.0 | 95 |
| EEE Mode – 1000Mbps | 43.5 | 4.5 | 23.6 | 122 |
| EEE Mode – 100Mbps (TX and RX in LPI) | 25.6 | 4.1 | 13.8 | 75 |
| Software power-down mode (Reg. 0h.11 = 1) | 1.0 | 3.1 | 6.7 | 26 |

**Note:**

4. 2.5V AVDDH is recommended for commercial temperature range (0°C to +70°C) operation only.

**Table 15. Typical Current/Power Consumption – Transceiver (2.5V), Digital I/Os (1.8V)**

| Condition | 1.2V Core (DVDDL, AVDDL, AVDDL_PLL) | 2.5V Transceiver[4] (AVDDH – Commercial Temperature Only) | 1.8V Digital I/Os (DVDDH) | Total Chip Power |
|---|---|---|---|---|
| | mA | mA | mA | mW |
| 1000Base-T link-up (no traffic) | 210 | 58.8 | 11.2 | 419 |
| 1000Base-T full-duplex @ 100% utilization | 221 | 57.9 | 23.6 | 452 |
| 100Base-TX link-up (no traffic) | 63.6 | 24.9 | 8.4 | 154 |
| 100Base-TX full-duplex @ 100% utilization | 63.8 | 24.9 | 9.8 | 156 |
| 10Base-T link-up (no traffic) | 7.1 | 11.5 | 3.6 | 44 |
| 10Base-T full-duplex @ 100% utilization | 7.7 | 25.3 | 5.6 | 83 |
| EEE Mode – 1000Mbps | 43.5 | 4.5 | 15.9 | 92 |
| EEE Mode – 100Mbps (TX and RX in LPI) | 25.6 | 4.1 | 9.1 | 57 |
| Software power-down mode (Reg. 0h.11 = 1) | 1.0 | 3.1 | 5.5 | 19 |

## Register Map

The register space within the KSZ9031RNX consists of two distinct areas.

- Standard registers // Direct register access
- MDIO manageable device (MMD) registers // Indirect register access

The KSZ9031RNX supports the following standard registers.

**Table 16. Standard Registers Supported by KSZ9031RNX**

| Register Number (Hex) | Description |
|---|---|
| **IEEE-Defined Registers** | |
| 0h | Basic Control |
| 1h | Basic Status |
| 2h | PHY Identifier 1 |
| 3h | PHY Identifier 2 |
| 4h | Auto-Negotiation Advertisement |
| 5h | Auto-Negotiation Link Partner Ability |
| 6h | Auto-Negotiation Expansion |
| 7h | Auto-Negotiation Next Page |
| 8h | Auto-Negotiation Link Partner Next Page Ability |
| 9h | 1000Base-T Control |
| Ah | 1000Base-T Status |
| Bh – Ch | Reserved |
| Dh | MMD Access – Control |
| Eh | MMD Access – Register/Data |
| Fh | Extended Status |
| **Vendor-Specific Registers** | |
| 10h | Reserved |
| 11h | Remote Loopback |
| 12h | LinkMD Cable Diagnostic |
| 13h | Digital PMA/PCS Status |
| 14h | Reserved |
| 15h | RXER Counter |
| 16h – 1Ah | Reserved |
| 1Bh | Interrupt Control/Status |
| 1Ch | Auto MDI/MDI-X |
| 1Dh – 1Eh | Reserved |
| 1Fh | PHY Control |

Table 17 highlights those MMD device addresses and their associated register addresses supported by the KSZ9031RNX, which make up the indirect MMD registers.

**Table 17. MMD Registers Supported by KSZ9031RNX**

| Device Address (Hex) | Register Address (Hex) | Description |
|---|---|---|
| 0h | 3h | AN FLP Burst Transmit – LO |
| | 4h | AN FLP Burst Transmit – HI |
| 1h | 5Ah | 1000Base-T Link-Up Time Control |
| 2h | 0h | Common Control |
| | 1h | Strap Status |
| | 2h | Operation Mode Strap Override |
| | 3h | Operation Mode Strap Status |
| | 4h | RGMII Control Signal Pad Skew |
| | 5h | RGMII RX Data Pad Skew |
| | 6h | RGMII TX Data Pad Skew |
| | 8h | RGMII Clock Pad Skew |
| | 10h | Wake-On-LAN – Control |
| | 11h | Wake-On-LAN – Magic Packet, MAC-DA-0 |
| | 12h | Wake-On-LAN – Magic Packet, MAC-DA-1 |
| | 13h | Wake-On-LAN – Magic Packet, MAC-DA-2 |
| | 14h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0 |
| | 15h | Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1 |
| | 16h | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0 |
| | 17h | Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1 |
| | 18h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0 |
| | 19h | Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1 |
| | 1Ah | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0 |
| | 1Bh | Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1 |
| | 1Ch | Wake-On-LAN – Customized Packet, Type 0, Mask 0 |
| | 1Dh | Wake-On-LAN – Customized Packet, Type 0, Mask 1 |
| | 1Eh | Wake-On-LAN – Customized Packet, Type 0, Mask 2 |
| | 1Fh | Wake-On-LAN – Customized Packet, Type 0, Mask 3 |
| | 20h | Wake-On-LAN – Customized Packet, Type 1, Mask 0 |
| | 21h | Wake-On-LAN – Customized Packet, Type 1, Mask 1 |
| | 22h | Wake-On-LAN – Customized Packet, Type 1, Mask 2 |
| | 23h | Wake-On-LAN – Customized Packet, Type 1, Mask 3 |
| | 24h | Wake-On-LAN – Customized Packet, Type 2, Mask 0 |
| | 25h | Wake-On-LAN – Customized Packet, Type 2, Mask 1 |
| | 26h | Wake-On-LAN – Customized Packet, Type 2, Mask 2 |
| | 27h | Wake-On-LAN – Customized Packet, Type 2, Mask 3 |
| | 28h | Wake-On-LAN – Customized Packet, Type 3, Mask 0 |
| | 29h | Wake-On-LAN – Customized Packet, Type 3, Mask 1 |
| | 2Ah | Wake-On-LAN – Customized Packet, Type 3, Mask 2 |
| | 2Bh | Wake-On-LAN – Customized Packet, Type 3, Mask 3 |
| 3h | 0h | PCS EEE – Control |
| | 1h | PCS EEE – Status |
| 7h | 3Ch | EEE Advertisement |
| | 3Dh | EEE Link Partner Advertisement |
| 1Ch | 4h | Analog Control 4 |
| | 23h | EDPD Control |

## Standard Registers

Standard registers provide direct read/write access to a 32-register address space, as defined in Clause 22 of the IEEE 802.3 Specification. Within this address space, the first 16 registers (Registers 0h to Fh) are defined according to the IEEE specification, while the remaining 16 registers (Registers 10h to 1Fh) are defined specific to the PHY vendor.

**IEEE Defined Registers – Descriptions**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| **Register 0h – Basic Control** | | | | |
| 0.15 | Reset | 1 = Software PHY reset<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.14 | Loopback | 1 = Loopback mode<br>0 = Normal operation | RW | 0 |
| 0.13 | Speed Select (LSB) | [0.6, 0.13]<br>[1,1] = Reserved<br>[1,0] = 1000Mbps<br>[0,1] = 100Mbps<br>[0,0] = 10Mbps<br>This bit is ignored if auto-negotiation is enabled (Reg. 0.12 = 1). | RW | 0 |
| 0.12 | Auto-Negotiation Enable | 1 = Enable auto-negotiation process<br>0 = Disable auto-negotiation process<br>If enabled, auto-negotiation result overrides settings in Reg. 0.13, 0.8 and 0.6.<br>If disabled, Auto MDI-X is also automatically disabled. Use Register 1Ch to set MDI/MDI-X. | RW | 1 |
| 0.11 | Power-Down | 1 = Power-down mode<br>0 = Normal operation<br>When this bit is set to '1', the link-down status might not get updated in the PHY register. Software should note link is down and should not rely on the PHY register link status.<br>After this bit is changed from '1' to '0', an internal global reset is automatically generated. Wait a minimum of 1ms before read/write access to the PHY registers. | RW | 0 |
| 0.10 | Isolate | 1 = Electrical isolation of PHY from RGMII<br>0 = Normal operation | RW | 0 |
| 0.9 | Restart Auto-Negotiation | 1 = Restart auto-negotiation process<br>0 = Normal operation<br>This bit is self-cleared after a '1' is written to it. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full-duplex<br>0 = Half-duplex | RW | 1 |
| 0.7 | Reserved | Reserved | RW | 0 |

**Note:**

5. RW = Read/Write.
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.
   LL = Latch low.

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| 0.6 | Speed Select (MSB) | [0.6, 0.13]<br>[1,1] = Reserved<br>[1,0] = 1000Mbps<br>[0,1] = 100Mbps<br>[0,0] = 10Mbps<br>This bit is ignored if auto-negotiation is enabled (Reg. 0.12 = 1). | RW | Set by MODE[3:0] strapping pins.<br>See the *Strapping Options* section for details. |
| 0.5:0 | Reserved | Reserved | RO | 00_0000 |
| **Register 1h – Basic Status** | | | | |
| 1.15 | 100Base-T4 | 1 = T4 capable<br>0 = Not T4 capable | RO | 0 |
| 1.14 | 100Base-TX Full-Duplex | 1 = Capable of 100Mbps full-duplex<br>0 = Not capable of 100Mbps full-duplex | RO | 1 |
| 1.13 | 100Base-TX Half-Duplex | 1 = Capable of 100Mbps half-duplex<br>0 = Not capable of 100Mbps half-duplex | RO | 1 |
| 1.12 | 10Base-T Full-Duplex | 1 = Capable of 10Mbps full-duplex<br>0 = Not capable of 10Mbps full-duplex | RO | 1 |
| 1.11 | 10Base-T Half-Duplex | 1 = Capable of 10Mbps half-duplex<br>0 = Not capable of 10Mbps half-duplex | RO | 1 |
| 1.10:9 | Reserved | Reserved | RO | 00 |
| 1.8 | Extended Status | 1 = Extended status info in Reg. 15h.<br>0 = No extended status info in Reg. 15h. | RO | 1 |
| 1.7 | Reserved | Reserved | RO | 0 |
| 1.6 | No Preamble | 1 = Preamble suppression<br>0 = Normal preamble | RO | 1 |
| 1.5 | Auto-Negotiation Complete | 1 = Auto-negotiation process completed<br>0 = Auto-negotiation process not completed | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault<br>0 = No remote fault | RO/LH | 0 |
| 1.3 | Auto-Negotiation Ability | 1 = Can perform auto-negotiation<br>0 = Cannot perform auto-negotiation | RO | 1 |
| 1.2 | Link Status | 1 = Link is up<br>0 = Link is down | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber detected<br>0 = Jabber not detected (default is low) | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Supports extended capability registers | RO | 1 |
| **Register 2h – PHY Identifier 1** | | | | |
| 2.15:0 | PHY ID Number | Assigned to Bits [3:18] of the organizationally unique identifier (OUI). KENDIN Communication's OUI is 0010A1h. | RO | 0022h |

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| **Register 3h – PHY Identifier 2** | | | | |
| 3.15:10 | PHY ID Number | Assigned to Bits [19:24] of the organizationally unique identifier (OUI). KENDIN Communication's OUI is 0010A1h. | RO | 0001_01 |
| 3.9:4 | Model Number | Six-bit manufacturer's model number | RO | 10_0010 |
| 3.3:0 | Revision Number | Four-bit manufacturer's revision number | RO | Indicates silicon revision |
| **Register 4h – Auto-Negotiation Advertisement** | | | | |
| 4.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RW | 0 |
| 4.14 | Reserved | Reserved | RO | 0 |
| 4.13 | Remote Fault | 1 = Remote fault supported<br>0 = No remote fault | RW | 0 |
| 4.12 | Reserved | Reserved | RO | 0 |
| 4.11:10 | Pause | [4.11, 4.10]<br>[0,0] = No pause<br>[1,0] = Asymmetric pause (link partner)<br>[0,1] = Symmetric pause<br>[1,1] = Symmetric and asymmetric pause (local device) | RW | 00 |
| 4.9 | 100Base-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 4.8 | 100Base-TX Full-Duplex | 1 = 100Mbps full-duplex capable<br>0 = No 100Mbps full-duplex capability | RW | 1 |
| 4.7 | 100Base-TX Half-Duplex | 1 = 100Mbps half-duplex capable<br>0 = No 100Mbps half-duplex capability | RW | 1 |
| 4.6 | 10Base-T Full-Duplex | 1 = 10Mbps full-duplex capable<br>0 = No 10Mbps full-duplex capability | RW | 1 |
| 4.5 | 10Base-T Half-Duplex | 1 = 10Mbps half-duplex capable<br>0 = No 10Mbps half-duplex capability | RW | 1 |
| 4.4:0 | Selector Field | [00001] = IEEE 802.3 | RW | 0_0001 |
| **Register 5h – Auto-Negotiation Link Partner Ability** | | | | |
| 5.15 | Next Page | 1 = Next page capable<br>0 = No next page capability | RO | 0 |
| 5.14 | Acknowledge | 1 = Link code word received from partner<br>0 = Link code word not yet received | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote fault detected<br>0 = No remote fault | RO | 0 |
| 5.12 | Reserved | Reserved | RO | 0 |

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| 5.11:10 | Pause | [5.11, 5.10]<br>[0,0] = No pause<br>[1,0] = Asymmetric pause (link partner)<br>[0,1] = Symmetric pause<br>[1,1] = Symmetric and asymmetric pause (local device) | RW | 00 |
| 5.9 | 100Base-T4 | 1 = T4 capable<br>0 = No T4 capability | RO | 0 |
| 5.8 | 100Base-TX Full-Duplex | 1 = 100Mbps full-duplex capable<br>0 = No 100Mbps full-duplex capability | RO | 0 |
| 5.7 | 100Base-TX Half-Duplex | 1 = 100Mbps half-duplex capable<br>0 = No 100Mbps half-duplex capability | RO | 0 |
| 5.6 | 10Base-T Full-Duplex | 1 = 10Mbps full-duplex capable<br>0 = No 10Mbps full-duplex capability | RO | 0 |
| 5.5 | 10Base-T Half-Duplex | 1 = 10Mbps half-duplex capable<br>0 = No 10Mbps half-duplex capability | RO | 0 |
| 5.4:0 | Selector Field | [00001] = IEEE 802.3 | RO | 0_0000 |
| **Register 6h – Auto-Negotiation Expansion** | | | | |
| 6.15:5 | Reserved | Reserved | RO | 0000_0000_000 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection<br>0 = No fault detected by parallel detection | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner has next page capability<br>0 = Link partner does not have next page capability | RO | 0 |
| 6.2 | Next Page Able | 1 = Local device has next page capability<br>0 = Local device does not have next page capability | RO | 1 |
| 6.1 | Page Received | 1 = New page received<br>0 = New page not received | RO/LH | 0 |
| 6.0 | Link Partner Auto-Negotiation Able | 1 = Link partner has auto-negotiation capability<br>0 = Link partner does not have auto-negotiation capability | RO | 0 |
| **Register 7h – Auto-Negotiation Next Page** | | | | |
| 7.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RW | 0 |
| 7.14 | Reserved | Reserved | RO | 0 |
| 7.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RW | 1 |
| 7.12 | Acknowledge2 | 1 = Will comply with message<br>0 = Cannot comply with message | RW | 0 |
| 7.11 | Toggle | 1 = Previous value of the transmitted link code word equaled logic one<br>0 = Logic zero | RO | 0 |

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| 7.10:0 | Message Field | 11-bit wide field to encode 2048 messages | RW | 000_0000_0001 |
| **Register 8h – Auto-Negotiation Link Partner Next Page Ability** | | | | |
| 8.15 | Next Page | 1 = Additional next pages will follow<br>0 = Last page | RO | 0 |
| 8.14 | Acknowledge | 1 = Successful receipt of link word<br>0 = No successful receipt of link word | RO | 0 |
| 8.13 | Message Page | 1 = Message page<br>0 = Unformatted page | RO | 0 |
| 8.12 | Acknowledge2 | 1 = Able to act on the information<br>0 = Not able to act on the information | RO | 0 |
| 8.11 | Toggle | 1 = Previous value of transmitted link code word equal to logic zero<br>0 = Previous value of transmitted link code word equal to logic one | RO | 0 |
| 8.10:0 | Message Field | | RO | 000_0000_0000 |
| **Register 9h – 1000Base-T Control** | | | | |
| 9.15:13 | Test Mode Bits | Transmitter test mode operations<br>[9.15:13] Mode<br>[000] Normal operation<br>[001] Test mode 1 –Transmit waveform test<br>[010] Test mode 2 –Transmit jitter test in master mode<br>[011] Test mode 3 –Transmit jitter test in slave mode<br>[100] Test mode 4 –Transmitter distortion test<br>[101] Reserved, operations not identified<br>[110] Reserved, operations not identified<br>[111] Reserved, operations not identified<br>To enable 1000Base-T Test Mode:<br>1) Set Register 0h = 0x0140 to disable auto-negotiation and select 1000Mbps speed.<br>2) Set Register 9h, bits [15:13] = 001, 010, 011, or 100 to select one of the 1000Base-T Test Modes.<br>After the above settings, the test waveform for the selected test mode is transmitted onto each of the 4 differential pairs. No link partner is needed. | RW | 000 |
| 9.12 | Master-Slave Manual Configuration Enable | 1 = Enable master-slave manual configuration value<br>0 = Disable master-slave manual configuration value | RW | 0 |

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[5] | Default |
|---|---|---|---|---|
| 9.11 | Master-Slave Manual Configuration Value | 1 = Configure PHY as master during master-slave negotiation<br>0 = Configure PHY as slave during master-slave negotiation<br>This bit is ignored if master-slave manual configuration is disabled (Reg. 9.12 = 0). | RW | 0 |
| 9.10 | Port Type | 1 = Indicate the preference to operate as multiport device (master)<br>0 = Indicate the preference to operate as single-port device (slave)<br>This bit is valid only if master-slave manual configuration is disabled (Reg. 9.12 = 0). | RW | 0 |
| 9.9 | 1000Base-T Full-Duplex | 1 = Advertise PHY is 1000Base-T full-duplex capable<br>0 = Advertise PHY is not 1000Base-T full-duplex capable | RW | 1 |
| 9.8 | 1000Base-T Half-Duplex | 1 = Advertise PHY is 1000Base-T half-duplex capable<br>0 = Advertise PHY is not 1000Base-T half-duplex capable | RW | Set by MODE[3:0] strapping pins.<br>See the *Strapping Options* section for details. |
| 9.7:0 | Reserved | Write as 0, ignore on read | RO | – |
| **Register Ah – 1000Base-T Status** | | | | |
| A.15 | Master-Slave Configuration Fault | 1 = Master-slave configuration fault detected<br>0 = No master-slave configuration fault detected | RO/LH/SC | 0 |
| A.14 | Master-Slave Configuration Resolution | 1 = Local PHY configuration resolved to master<br>0 = Local PHY configuration resolved to slave | RO | 0 |
| A.13 | Local Receiver Status | 1 = Local receiver OK (loc_rcvr_status = 1)<br>0 = Local receiver not OK (loc_rcvr_status = 0) | RO | 0 |
| A.12 | Remote Receiver Status | 1 = Remote receiver OK (rem_rcvr_status = 1)<br>0 = Remote receiver not OK (rem_rcvr_status = 0) | RO | 0 |
| A.11 | Link Partner 1000Base-T Full-Duplex Capability | 1 = Link partner is capable of 1000Base-T full-duplex<br>0 = Link partner is not capable of 1000Base-T full-duplex | RO | 0 |
| A.10 | Link Partner 1000Base-T Half-Duplex Capability | 1 = Link partner is capable of 1000Base-T half-duplex<br>0 = Link Partner is not capable of 1000Base-T half-duplex | RO | 0 |
| A.9:8 | Reserved | Reserved | RO | 00 |
| A.7:0 | Idle Error Count | Cumulative count of errors detected when receiver is receiving idles and PMA_TXMODE.indicate = SEND_N.<br>The counter is incremented every symbol period that rxerror_status = ERROR. | RO/SC | 0000_0000 |

**IEEE Defined Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[6] | Default |
|---|---|---|---|---|
| **Register Dh – MMD Access – Control** | | | | |
| D.15:14 | MMD – Operation Mode | For the selected MMD device address (Bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address. | RW | 0_0000 |
| **Register Eh – MMD Access – Register/Data** | | | | |
| E.15:0 | MMD – Register/Data | For the selected MMD device address (Reg. Dh, Bits [4:0]),<br>When Reg. Dh, Bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Reg. Dh, Bits [15:14], for descriptions of post increment reads and writes of this register for data operation. | RW | 0000_0000_0000_0000 |
| **Register Fh – Extended Status** | | | | |
| F.15 | 1000Base-X Full-Duplex | 1 = PHY can perform 1000Base-X full-duplex<br>0 = PHY cannot perform 1000Base-X full-duplex | RO | 0 |
| F.14 | 1000Base-X Half-Duplex | 1 = PHY can perform 1000Base-X half-duplex<br>0 = PHY cannot perform 1000Base-X half-duplex | RO | 0 |
| F.13 | 1000Base-T Full-Duplex | 1 = PHY can perform 1000Base-T full-duplex<br>0 = PHY cannot perform 1000Base-T full-duplex | RO | 1 |
| F.12 | 1000Base-T Half-Duplex | 1 = PHY can perform 1000Base-T half-duplex<br>0 = PHY cannot perform 1000Base-T half-duplex | RO | 1 |

**Note:**

6. RW = Read/Write.
   RC = Read-cleared
   RO = Read only.
   SC = Self-cleared.
   LH = Latch high.

**Vendor-Specific Registers – Descriptions**

| Address | Name | Description | Mode[6] | Default |
|---|---|---|---|---|
| F.11:0 | Reserved | Ignore when read | RO | – |
| **Register 11h – Remote Loopback** | | | | |
| 11.15:9 | Reserved | Reserved | RW | 0000_000 |
| 11.8 | Remote Loopback | 1 = Enable remote loopback<br>0 = Disable remote loopback | RW | 0 |
| 11.7:1 | Reserved | Reserved | RW | 1111_010 |
| 11.0 | Reserved | Reserved | RO | 0 |
| **Register 12h – LinkMD – Cable Diagnostic** | | | | |
| 12.15 | Cable Diagnostic Test Enable | Write value:<br>1 = Enable cable diagnostic test. After test has completed, this bit is self-cleared.<br>0 = Disable cable diagnostic test.<br>Read value:<br>1 = Cable diagnostic test is in progress.<br>0 = Indicates cable diagnostic test (if enabled) has completed and the status information is valid for read. | RW/SC | 0 |
| 12.14 | Reserved | This bit should always be set to ‘0’. | RW | 0 |
| 12.13:12 | Cable Diagnostic Test Pair | These two bits select the differential pair for testing:<br>00 = Differential pair A (Pins 2, 3)<br>01 = Differential pair B (Pins 5, 6)<br>10 = Differential pair C (Pins 7, 8)<br>11 = Differential pair D (Pins 10, 11) | RW | 00 |
| 12.11:10 | Reserved | These two bits should always be set to ‘00’. | RW | 00 |
| 12.9:8 | Cable Diagnostic Status | These two bits represent the test result for the selected differential pair in Bits [13:12] of this register.<br>00 = Normal cable condition (no fault detected)<br>01 = Open cable fault detected<br>10 = Short cable fault detected<br>11 = Reserved | RO | 00 |
| 12.7:0 | Cable Diagnostic Fault Data | For the open or short cable fault detected in Bits [9:8] of this register, this 8-bit value represents the distance to the cable fault. | RO | 0000_0000 |

**Vendor-Specific Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[6] | Default |
|---|---|---|---|---|
| **Register 13h – Digital PMA/PCS Status** | | | | |
| 13.15:3 | Reserved | Reserved | RO/LH | 0000_0000_0000_0 |
| 13.2 | 1000Base-T Link Status | 1000Base-T link status<br>1 = Link status is OK<br>0 = Link status is not OK | RO | 0 |
| 13.1 | 100Base-TX Link Status | 100Base-TX link status<br>1 = Link status is OK<br>0 = Link status is not OK | RO | 0 |
| 13.0 | Reserved | Reserved | RO | 0 |
| **Register 15h – RXER Counter** | | | | |
| 15.15:0 | RXER Counter | Receive error counter for symbol error frames | RO/RC | 0000_0000_0000_0000 |
| **Register 1Bh – Interrupt Control/Status** | | | | |
| 1B.15 | Jabber Interrupt Enable | 1 = Enable jabber interrupt<br>0 = Disable jabber interrupt | RW | 0 |
| 1B.14 | Receive Error Interrupt Enable | 1 = Enable receive error interrupt<br>0 = Disable receive error interrupt | RW | 0 |
| 1B.13 | Page Received Interrupt Enable | 1 = Enable page received interrupt<br>0 = Disable page received interrupt | RW | 0 |
| 1B.12 | Parallel Detect Fault Interrupt Enable | 1 = Enable parallel detect fault interrupt<br>0 = Disable parallel detect fault interrupt | RW | 0 |
| 1B.11 | Link Partner Acknowledge Interrupt Enable | 1 = Enable link partner acknowledge interrupt<br>0 = Disable link partner acknowledge interrupt | RW | 0 |
| 1B.10 | Link-Down Interrupt Enable | 1 = Enable link-down interrupt<br>0 = Disable link-down interrupt | RW | 0 |
| 1B.9 | Remote Fault Interrupt Enable | 1 = Enable remote fault interrupt<br>0 = Disable remote fault interrupt | RW | 0 |
| 1B.8 | Link-Up Interrupt Enable | 1 = Enable link-up interrupt<br>0 = Disable link-up interrupt | RW | 0 |
| 1B.7 | Jabber Interrupt | 1 = Jabber occurred<br>0 = Jabber did not occur | RO/RC | 0 |
| 1B.6 | Receive Error Interrupt | 1 = Receive error occurred<br>0 = Receive error did not occur | RO/RC | 0 |
| 1B.5 | Page Receive Interrupt | 1 = Page receive occurred<br>0 = Page receive did not occur | RO/RC | 0 |
| 1B.4 | Parallel Detect Fault Interrupt | 1 = Parallel detect fault occurred<br>0 = Parallel detect fault did not occur | RO/RC | 0 |

**Vendor-Specific Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[6] | Default |
|---|---|---|---|---|
| 1B.3 | Link Partner Acknowledge Interrupt | 1 = Link partner acknowledge occurred<br>0 = Link partner acknowledge did not occur | RO/RC | 0 |
| 1B.2 | Link-Down Interrupt | 1 = Link-down occurred<br>0 = Link-down did not occur | RO/RC | 0 |
| 1B.1 | Remote Fault Interrupt | 1 = Remote fault occurred<br>0 = Remote fault did not occur | RO/RC | 0 |
| 1B.0 | Link-Up Interrupt | 1 = Link-up occurred<br>0 = Link-up did not occur | RO/RC | 0 |
| **Register 1Ch – Auto MDI/MDI-X** | | | | |
| 1C.15:8 | Reserved | Reserved | RW | 0000_0000 |
| 1C.7 | MDI Set | When Swap-Off (Bit [6] of this register) is asserted (1),<br>1 = PHY is set to operate as MDI mode<br>0 = PHY is set to operate as MDI-X mode<br>This bit has no function when Swap-Off is de-asserted (0). | RW | 0 |
| 1C.6 | Swap-Off | 1 = Disable Auto MDI/MDI-X function<br>0 = Enable Auto MDI/MDI-X function | RW | 0 |
| 1C.5:0 | Reserved | Reserved | RW | 00_0000 |
| **Register 1Fh – PHY Control** | | | | |
| 1F.15 | Reserved | Reserved | RW | 0 |
| 1F.14 | Interrupt Level | 1 = Interrupt pin active high<br>0 = Interrupt pin active low | RW | 0 |
| 1F.13:12 | Reserved | Reserved | RW | 00 |
| 1F.11:10 | Reserved | Reserved | RO/LH/RC | 00 |
| 1F.9 | Enable Jabber | 1 = Enable jabber counter<br>0 = Disable jabber counter | RW | 1 |
| 1F.8:7 | Reserved | Reserved | RW | 00 |
| 1F.6 | Speed Status 1000Base-T | 1 = Indicate chip final speed status at 1000Base-T | RO | 0 |
| 1F.5 | Speed Status 100Base-TX | 1 = Indicate chip final speed status at 100Base-TX | RO | 0 |
| 1F.4 | Speed Status 10Base-T | 1 = Indicate chip final speed status at 10Base-T | RO | 0 |
| 1F.3 | Duplex Status | Indicate chip duplex status<br>1 = Full-duplex<br>0 = Half-duplex | RO | 0 |
| 1F.2 | 1000Base-T Master/Slave Status | Indicate chip master/slave status<br>1 = 1000Base-T master mode<br>0 = 1000Base-T slave mode | RO | 0 |
| 1F.1 | Reserved | Reserved | RW | 0 |
| 1F.0 | Link Status Check Fail | 1 = Fail<br>0 = Not failing | RO | 0 |

## MMD Registers

MMD registers provide indirect read/write access to up to 32 MMD device addresses with each device supporting up to 65,536 16-bit registers, as defined in Clause 22 of the IEEE 802.3 Specification. The KSZ9031RNX, however, uses only a small fraction of the available registers. See the *Register Map* section for a list of supported MMD device addresses and their associated register addresses.

The following two standard registers serve as the portal registers to access the indirect MMD registers.

- Standard Register Dh – MMD Access – Control
- Standard Register Eh – MMD Access – Register/Data

**Table 18. Portal Registers (Access to Indirect MMD Registers)**

| Address | Name | Description | Mode | Default |
|---|---|---|---|---|
| **Register Dh – MMD Access – Control** | | | | |
| D.15:14 | MMD – Operation Mode | For the selected MMD device address (Bits [4:0] of this register), these two bits select one of the following register or data operations and the usage for MMD Access – Register/Data (Reg. Eh).<br>00 = Register<br>01 = Data, no post increment<br>10 = Data, post increment on reads and writes<br>11 = Data, post increment on writes only | RW | 00 |
| D.13:5 | Reserved | Reserved | RW | 00_0000_000 |
| D.4:0 | MMD – Device Address | These five bits set the MMD device address. | RW | 0_0000 |
| **Register Eh – MMD Access – Register/Data** | | | | |
| E.15:0 | MMD – Register/Data | For the selected MMD device address (Reg. Dh, Bits [4:0]),<br>When Reg. Dh, Bits [15:14] = 00, this register contains the read/write register address for the MMD device address.<br>Otherwise, this register contains the read/write data value for the MMD device address and its selected register address.<br>See also Register Dh, Bits [15:14] descriptions for post increment reads and writes of this register for data operation. | RW | 0000_0000_0000_0000 |

Examples:

- MMD Register Write

  Write MMD – Device Address 2h, Register 10h = 0001h to enable link-up detection to trigger PME for WOL.

  1. Write Register Dh with 0002h // Set up register address for MMD – Device Address 2h.
  2. Write Register Eh with 0010h // Select Register 10h of MMD – Device Address 2h.
  3. Write Register Dh with 4002h // Select register data for MMD – Device Address 2h, Register 10h.
  4. Write Register Eh with 0001h // Write value 0001h to MMD – Device Address 2h, Register 10h.

- MMD Register Read

  Read MMD – Device Address 2h, Register 11h – 13h for the magic packet's MAC address

  1. Write Register Dh with 0002h // Set up register address for MMD – Device Address 2h.
  2. Write Register Eh with 0011h // Select Register 11h of MMD – Device Address 2h.
  3. Write Register Dh with 8002h // Select register data for MMD – Device Address 2h, Register 11h.
  4. Read Register Eh // Read data in MMD – Device Address 2h, Register 11h.
  5. Read Register Eh // Read data in MMD – Device Address 2h, Register 12h.
  6. Read Register Eh // Read data in MMD – Device Address 2h, Register 13h.

**MMD Registers – Descriptions**

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 0h, Register 3h – AN FLP Burst Transmit – LO** | | | | |
| 0.3.15:0 | AN FLP Burst Transmit – LO | This register and the following register set the Auto-Negotiation FLP burst transmit timing. The same timing must be set for both registers.<br>0x4000 = Select 8ms interval timing (default)<br>0x1A80 = Select 16ms interval timing<br>All other values are reserved. | RW | 0x4000 |
| **MMD Address 0h, Register 4h – AN FLP Burst Transmit – HI** | | | | |
| 0.4.15:0 | AN FLP Burst Transmit – HI | This register and the previous register set the Auto-Negotiation FLP burst transmit timing. The same timing must be set for both registers.<br>0x0003 = Select 8ms interval timing (default)<br>0x0006 = Select 16ms interval timing<br>All other values are reserved. | RW | 0x0003 |
| **MMD Address 1h, Register 5Ah – 1000Base-T Link-Up Time Control** | | | | |
| 1.5A.8:4 | Reserved | Reserved | RW | 1_0000 |
| 1.5A.3:1 | 1000Base-T Link-Up Time | When the link partner is another KSZ9031 device, the 1000Base-T link-up time can be long. These three bits provide an optional setting to reduce the 1000Base-T link-up time.<br>100 = Default power-up setting<br>011 = Optional setting to reduce link-up time when the link partner is a KSZ9031 device.<br>All other settings are reserved and should not be used.<br>The optional setting is safe to use with any link partner.<br>**Note**: Read/Write access to this register bit is available only when Reg. 0h is set to 0x2100 to disable auto-negotiation and force 100Base-TX mode. | RW | 100 |
| 1.5A.0 | Reserved | Reserved | RW | 0 |

**Note:**

7. RW = Read/Write.
   RO = Read only.
   WO = Write only.
   LH = Latch high.

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 0h – Common Control** | | | | |
| 2.0.15:5 | Reserved | Reserved | RW | 0000_0000_000 |
| 2.0.4 | LED Mode Override | Override strap-in for LED_MODE<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode<br>This bit is write-only and always reads back a value of '0'. The updated value is reflected in Bit [3] of this register. | WO | 0 |
| 2.0.3 | LED Mode Status | LED_MODE Status<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode | RO | Set by LED_MODE strapping pin.<br>See the *Strapping Options* section for details.<br>Can be updated by Bit [4] of this register after reset. |
| 2.0.2 | Reserved | Reserved | RW | 0 |
| 2.0.1 | CLK125_EN Status | Override strap-in for CLK125_EN<br>1 = CLK125_EN strap-in is enabled<br>0 = CLK125_EN strap-in is disabled | RW | Set by CLK125_EN strapping pin.<br>See the *Strapping Options* section for details. |
| 2.0.0 | Reserved | Reserved | RW | 0 |
| **MMD Address 2h, Register 1h – Strap Status** | | | | |
| 2.1.15:8 | Reserved | Reserved | RO | 0000_0000 |
| 2.1.7 | LED_MODE Strap-In Status | Strap to<br>1 = Single-LED mode<br>0 = Tri-color dual-LED mode | RO | Set by LED_MODE strapping pin.<br>See the *Strapping Options* section for details. |
| 2.1.6 | Reserved | Reserved | RO | 0 |
| 2.1.5 | CLK125_EN Strap-In Status | Strap to<br>1 = CLK125_EN strap-in is enabled<br>0 = CLK125_EN strap-in is disabled | RO | Set by CLK125_EN strapping pin.<br>See the *Strapping Options* section for details. |
| 2.1.4:3 | Reserved | Reserved | RO | 00 |
| 2.1.2:0 | PHYAD[2:0] Strap-In Value | Strap-in value for PHY address<br>Bits [4:3] of PHY address are always set to '00'. | RO | Set by PHYAD[2:0] strapping pin.<br>See the *Strapping Options* section for details. |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 2h – Operation Mode Strap Override** | | | | |
| 2.2.15 | RGMII All Capabilities Override | 1 = Override strap-in for RGMII to advertise all capabilities | RW | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.2.14 | RGMII No 1000BT_HD Override | 1 = Override strap-in for RGMII to advertise all capabilities except 1000Base-T half-duplex | RW | |
| 2.2.13 | RGMII 1000BT_H/FD Only Override | 1 = Override strap-in for RGMII to advertise 1000Base-T full- and half-duplex only | RW | |
| 2.2.12 | RGMII 1000BT_FD Only Override | 1 = Override strap-in for RGMII to advertise 1000Base-T full-duplex only | RW | |
| 2.2.11 | Reserved | Reserved | RW | 0 |
| 2.2.10 | PME_N2 Output Enable | For INT_N/PME_N2 (Pin 38),<br>1 = Enable PME output<br>0 = Disable PME output<br>This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for Pin 38. | RW | 0 |
| 2.2.9 | Reserved | Reserved | RW | 0 |
| 2.2.8 | PME_N1 Output Enable | For LED1/PME_N1 (Pin 17),<br>1 = Enable PME output<br>0 = Disable PME output<br>This bit works in conjunction with MMD Address 2h, Reg. 10h, Bits [15:14] to define the output for Pin 17. | RW | 0 |
| 2.2.7 | Chip Power-Down Override | 1 = Override strap-in for chip power-down mode | RW | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.2.6:5 | Reserved | Reserved | RW | 00 |
| 2.2.4 | NAND Tree Override | 1 = Override strap-in for NAND Tree mode | RW | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.2.3:0 | Reserved | Reserved | RW | 0000 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 3h – Operation Mode Strap Status** | | | | |
| 2.3.15 | RGMII All Capabilities Strap-In Status | 1 = Strap to RGMII to advertise all capabilities | RO | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.3.14 | RGMII No 1000BT_HD Strap-In Status | 1 = Strap to RGMII to advertise all capabilities except 1000Base-T half-duplex | RO | |
| 2.3.13 | RGMII Only 1000BT_H/FD Strap-In Status | 1 = Strap to RGMII to advertise 1000Base-T full-and half-duplex only | RO | |
| 2.3.12 | RGMII Only 1000BT_FD Strap-In Status | 1 = Strap to RGMII to advertise 1000Base-T full-duplex only | RO | |
| 2.3.11:8 | Reserved | Reserved | RO | 0000 |
| 2.3.7 | Chip Power-Down Strap-In Status | 1 = Strap to chip power-down mode | RO | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.3.6:5 | Reserved | Reserved | RO | 00 |
| 2.3.4 | NAND Tree Strap-In Status | 1 = Strap to NAND Tree mode | RO | Set by MODE[3:0] strapping pin.<br>See the *Strapping Options* section for details. |
| 2.3.3:0 | Reserved | Reserved | RO | 0000 |
| **MMD Address 2h, Register 4h – RGMII Control Signal Pad Skew** | | | | |
| 2.4.15:8 | Reserved | Reserved | RW | 0000_0000 |
| 2.4.7:4 | RX_DV Pad Skew | RGMII RX_CTL output pad skew control (0.06ns/step) | RW | 0111 |
| 2.4.3:0 | TX_EN Pad Skew | RGMII TX_CTL input pad skew control (0.06ns/step) | RW | 0111 |
| **MMD Address 2h, Register 5h – RGMII RX Data Pad Skew** | | | | |
| 2.5.15:12 | RXD3 Pad Skew | RGMII RXD3 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.11:8 | RXD2 Pad Skew | RGMII RXD2 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.7:4 | RXD1 Pad Skew | RGMII RXD1 output pad skew control (0.06ns/step) | RW | 0111 |
| 2.5.3:0 | RXD0 Pad Skew | RGMII RXD0 output pad skew control (0.06ns/step) | RW | 0111 |

**MMD Registers – Descriptions (Continued)**

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 6h – RGMII TX Data Pad Skew** | | | | |
| 2.6.15:12 | TXD3 Pad Skew | RGMII TXD3 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.11:8 | TXD2 Pad Skew | RGMII TXD2 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.7:4 | TXD1 Pad Skew | RGMII TXD1 input pad skew control (0.06ns/step) | RW | 0111 |
| 2.6.3:0 | TXD0 Pad Skew | RGMII TXD0 input pad skew control (0.06ns/step) | RW | 0111 |
| **MMD Address 2h, Register 8h – RGMII Clock Pad Skew** | | | | |
| 2.8.15:10 | Reserved | Reserved | RW | 0000_00 |
| 2.8.9:5 | GTX_CLK Pad Skew | RGMII GTX_CLK input pad skew control (0.06ns/step) | RW | 01_111 |
| 2.8.4:0 | RX_CLK Pad Skew | RGMII RX_CLK output pad skew control (0.06ns/step) | RW | 0_1111 |
| **MMD Address 2h, Register 10h – Wake-On-LAN – Control** | | | | |
| 2.10.15:14 | PME Output Select | These two bits work in conjunction with MMD Address 2h, Reg. 2h, Bits [8] and [10] for PME_N1 and PME_N2 enable, to define the output for Pins 17 and 38, respectively.<br>LED1/PME_N1 (Pin 17)<br>00 = PME_N1 output only<br>01 = LED1 output only<br>10 = LED1 and PME_N1 output<br>11 = Reserved<br>INT_N/PME_N2 (Pin 38)<br>00 = PME_N2 output only<br>01 = INT_N output only<br>10 = INT_N and PME_N2 output<br>11 = Reserved | RW | 00 |
| 2.10.13:7 | Reserved | Reserved | RW | 00_0000_0 |
| 2.10.6 | Magic Packet Detect Enable | 1 = Enable magic-packet detection<br>0 = Disable magic-packet detection | RW | 0 |
| 2.10.5 | Custom-Packet Type 3 Detect Enable | 1 = Enable custom-packet, Type 3 detection<br>0 = Disable custom-packet, Type 3 detection | RW | 0 |
| 2.10.4 | Custom-Packet Type 2 Detect Enable | 1 = Enable custom-packet, Type 2 detection<br>0 = Disable custom-packet, Type 2 detection | RW | 0 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| 2.10.3 | Custom-Packet Type 1 Detect Enable | 1 = Enable custom-packet, Type 1 detection<br>0 = Disable custom-packet, Type 1 detection | RW | 0 |
| 2.10.2 | Custom-Packet Type 0 Detect Enable | 1 = Enable custom-packet, Type 0 detection<br>0 = Disable custom-packet, Type 0 detection | RW | 0 |
| 2.10.1 | Link-Down Detect Enable | 1 = Enable link-down detection<br>0 = Disable link-down detection | RW | 0 |
| 2.10.0 | Link-Up Detect Enable | 1 = Enable link-up detection<br>0 = Disable link-up detection | RW | 0 |
| **MMD Address 2h, Register 11h – Wake-On-LAN – Magic Packet, MAC-DA-0** | | | | |
| 2.11.15:0 | Magic Packet MAC-DA-0 | This register stores the lower two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 2 (MAC Address [15:8])<br>Bit [7:0] = Byte 1 (MAC Address [7:0])<br>The upper four bytes of the destination MAC address are stored in the following two registers. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 12h – Wake-On-LAN – Magic Packet, MAC-DA-1** | | | | |
| 2.12.15:0 | Magic Packet MAC-DA-1 | This register stores the middle two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 4 (MAC Address [31:24])<br>Bit [7:0] = Byte 3 (MAC Address [23:16])<br>The lower two bytes and upper two bytes of the destination MAC address are stored in the previous and following registers, respectively. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 13h – Wake-On-LAN – Magic Packet, MAC-DA-2** | | | | |
| 2.13.15:0 | Magic Packet MAC-DA-2 | This register stores the upper two bytes of the destination MAC address for the magic packet.<br>Bit [15:8] = Byte 6 (MAC Address [47:40])<br>Bit [7:0] = Byte 5 (MAC Address [39:32])<br>The lower four bytes of the destination MAC address are stored in the previous two registers. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 14h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 0**<br>**MMD Address 2h, Register 16h – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 0**<br>**MMD Address 2h, Register 18h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 0**<br>**MMD Address 2h, Register 1Ah – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 0** | | | | |
| 2.14.15:0<br>2.16.15:0<br>2.18.15:0<br>2.1A.15:0 | Custom Packet Type X CRC 0 | This register stores the lower two bytes for the expected CRC.<br>Bit [15:8] = Byte 2 (CRC [15:8])<br>Bit [7:0] = Byte 1 (CRC [7:0])<br>The upper two bytes for the expected CRC are stored in the following register. | RW | 0000_0000_0000_0000 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 15h – Wake-On-LAN – Customized Packet, Type 0, Expected CRC 1**<br>**MMD Address 2h, Register 17h – Wake-On-LAN – Customized Packet, Type 1, Expected CRC 1**<br>**MMD Address 2h, Register 19h – Wake-On-LAN – Customized Packet, Type 2, Expected CRC 1**<br>**MMD Address 2h, Register 1Bh – Wake-On-LAN – Customized Packet, Type 3, Expected CRC 1** | | | | |
| 2.15.15:0<br>2.17.15:0<br>2.19.15:0<br>2.1B.15:0 | Custom Packet Type X CRC 1 | This register stores the upper two bytes for the expected CRC.<br>Bit [15:8] = Byte 4 (CRC [31:24])<br>Bit [7:0] = Byte 3 (CRC [23:16])<br>The lower two bytes for the expected CRC are stored in the previous register. | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Ch – Wake-On-LAN – Customized Packet, Type 0, Mask 0**<br>**MMD Address 2h, Register 20h – Wake-On-LAN – Customized Packet, Type 1, Mask 0**<br>**MMD Address 2h, Register 24h – Wake-On-LAN – Customized Packet, Type 2, Mask 0**<br>**MMD Address 2h, Register 28h – Wake-On-LAN – Customized Packet, Type 3, Mask 0** | | | | |
| 2.1C.15:0<br>2.20.15:0<br>2.24.15:0<br>2.28.15:0 | Custom Packet Type X Mask 0 | This register selects the bytes in the first 16 bytes of the packet (bytes 1 thru 16) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15] : Byte 16<br>… : …<br>Bit [2] : Byte 2<br>Bit [0] : Byte 1 | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Dh – Wake-On-LAN – Customized Packet, Type 0, Mask 1**<br>**MMD Address 2h, Register 21h – Wake-On-LAN – Customized Packet, Type 1, Mask 1**<br>**MMD Address 2h, Register 25h – Wake-On-LAN – Customized Packet, Type 2, Mask 1**<br>**MMD Address 2h, Register 29h – Wake-On-LAN – Customized Packet, Type 3, Mask 1** | | | | |
| 2.1D.15:0<br>2.21.15:0<br>2.25.15:0<br>2.29.15:0 | Custom Packet Type X Mask 1 | This register selects the bytes in the second 16 bytes of the packet (bytes 17 thru 32) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15] : Byte 32<br>… : …<br>Bit [2] : Byte 18<br>Bit [0] : Byte 17 | RW | 0000_0000_0000_0000 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 2h, Register 1Eh – Wake-On-LAN – Customized Packet, Type 0, Mask 2**<br>**MMD Address 2h, Register 22h – Wake-On-LAN – Customized Packet, Type 1, Mask 2**<br>**MMD Address 2h, Register 26h – Wake-On-LAN – Customized Packet, Type 2, Mask 2**<br>**MMD Address 2h, Register 2Ah – Wake-On-LAN – Customized Packet, Type 3, Mask 2** | | | | |
| 2.1E.15:0<br>2.22.15:0<br>2.26.15:0<br>2.2A.15:0 | Custom Packet Type X Mask 2 | This register selects the bytes in the third 16 bytes of the packet (bytes 33 thru 48) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15] : Byte 48<br>… : …<br>Bit [2] : Byte 34<br>Bit [0] : Byte 33 | RW | 0000_0000_0000_0000 |
| **MMD Address 2h, Register 1Fh – Wake-On-LAN – Customized Packet, Type 0, Mask 3**<br>**MMD Address 2h, Register 23h – Wake-On-LAN – Customized Packet, Type 1, Mask 3**<br>**MMD Address 2h, Register 27h – Wake-On-LAN – Customized Packet, Type 2, Mask 3**<br>**MMD Address 2h, Register 2Bh – Wake-On-LAN – Customized Packet, Type 3, Mask 3** | | | | |
| 2.1F.15:0<br>2.23.15:0<br>2.27.15:0<br>2.2B.15:0 | Custom Packet Type X Mask 3 | This register selects the bytes in the fourth 16 bytes of the packet (bytes 49 thru 64) that will be used for CRC calculation.<br>For each bit in this register,<br>1 = Byte is selected for CRC calculation<br>0 = Byte is not selected for CRC calculation<br>The register-bit to packet-byte mapping is as follows:<br>Bit [15] : Byte 64<br>… : …<br>Bit [2] : Byte 50<br>Bit [0] : Byte 49 | RW | 0000_0000_0000_0000 |
| **MMD Address 3h, Register 0h – PCS EEE – Control** | | | | |
| 3.0.15:12 | Reserved | Reserved | RW | 0000 |
| 3.0.11 | 1000Base-T Force LPI | 1 = Force 1000Base-T low-power idle transmission<br>0 = Normal operation | RW | 0 |
| 3.0.10 | 100Base-TX RX_CLK Stoppable | During receive lower-power idle mode,<br>1 = RX_CLK stoppable for 100Base-TX<br>0 = RX_CLK not stoppable for 100Base-TX | RW | 0 |
| 3.0.9:0 | Reserved | Reserved | RW | 00_0000_0000 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 3h, Register 1h – PCS EEE – Status** | | | | |
| 3.1.15:12 | Reserved | Reserved | RO | 0000 |
| 3.1.11 | Transmit Low-Power Idle Received | 1 = Transmit PCS has received low-power idle<br>0 = Low-power idle not received | RO/LH | 0 |
| 3.1.10 | Receive Low-Power Idle Received | 1 = Receive PCS has received low-power idle<br>0 = Low-power idle not received | RO/LH | 0 |
| 3.1.9 | Transmit Low-Power Idle Indication | 1 = Transmit PCS is currently receiving low-power idle<br>0 = Transmit PCS is not currently receiving low-power idle | RO | |
| 3.1.8 | Receive Low-Power Idle Indication | 1 = Receive PCS is currently receiving low-power idle<br>0 = Receive PCS is not currently receiving low-power idle | RO | |
| 3.1.7:0 | Reserved | Reserved | RO | 0000_0000 |
| **MMD Address 7h, Register 3Ch – EEE Advertisement** | | | | |
| 7.3C.15:3 | Reserved | Reserved | RW | 0000_0000_0000_0 |
| 7.3C.2 | 1000Base-T EEE | 1 = 1000Mbps EEE capable<br>0 = No 1000Mbps EEE capability<br>This bit is set to '0' as the default after power-up or reset. Set this bit to '1' to enable 1000Mbps EEE mode. | RW | 0 |
| 7.3C.1 | 100Base-TX EEE | 1 = 100Mbps EEE capable<br>0 = No 100Mbps EEE capability<br>This bit is set to '0' as the default after power-up or reset. Set this bit to '1' to enable 100Mbps EEE mode. | RW | 0 |
| 7.3C.0 | Reserved | Reserved | RW | 0 |
| **MMD Address 7h, Register 3Dh – EEE Link Partner Advertisement** | | | | |
| 7.3D.15:3 | Reserved | Reserved | RO | 0000_0000_0000_0 |
| 7.3D.2 | 1000Base-T EEE | 1 = 1000Mbps EEE capable<br>0 = No 1000Mbps EEE capability | RO | 0 |
| 7.3D.1 | 100Base-TX EEE | 1 = 100Mbps EEE capable<br>0 = No 100Mbps EEE capability | RO | 0 |
| 7.3D.0 | Reserved | Reserved | RO | 0 |
| **MMD Address 1Ch, Register 4h – Analog Control 4** | | | | |
| 1C.4.15:11 | Reserved | Reserved | RW | 0000_0 |
| 1C.4.10 | 10Base-Te Mode | 1 = EEE 10Base-Te (1.75V TX amplitude)<br>0 = Standard 10Base-T (2.5V TX amplitude) | RW | 0 |
| 1C.4.9:0 | Reserved | Reserved | RW | 00_1111_1111 |

MMD Registers – Descriptions (Continued)

| Address | Name | Description | Mode[7] | Default |
|---|---|---|---|---|
| **MMD Address 1Ch, Register 23h – EDPD Control** | | | | |
| 1C.23.15:1 | Reserved | Reserved | RW | 0000_0000_0000_000 |
| 1C.23.0 | EDPD Mode Enable | Energy-detect power-down mode<br>1 = Enable<br>0 = Disable | RW | 0 |

## Absolute Maximum Ratings[8]

Supply Voltage ($V_{IN}$)
- (DVDDL, AVDDL, AVDDL_PLL) ..... –0.5V to +1.8V
- (AVDDH) ..... –0.5V to +5.0V
- (DVDDH) ..... –0.5V to +5.0V

Input Voltage (all inputs) ..... –0.5V to +5.0V
Output Voltage (all outputs) ..... –0.5V to +5.0V
Lead Temperature (soldering, 10s) ..... 260°C
Storage Temperature ($T_S$) ..... –55°C to +150°C

## Operating Ratings[9]

Supply Voltage
- (DVDDL, AVDDL, AVDDL_PLL) ..... +1.140V to +1.260V
- (AVDDH @ 3.3V) ..... +3.135V to +3.465V
- (AVDDH @ 2.5V, C-temp only) ..... +2.375V to +2.625V
- (DVDDH @ 3.3V) ..... +3.135V to +3.465V
- (DVDDH @ 2.5V) ..... +2.375V to +2.625V
- (DVDDH @ 1.8V) ..... +1.710V to +1.890V

Ambient Temperature
- ($T_A$ Commercial: KSZ9031RNXC) ..... 0°C to +70°C
- ($T_A$ Industrial: KSZ9031RNXI) ..... –40°C to +85°C
- ($T_A$ Automotive: KSZ9031RNXU) ..... –40°C to +85°C
- ($T_A$ Automotive: KSZ9031RNXV) ..... –40°C to +105°C

Maximum Junction Temperature ($T_{J\_MAX}$) ..... 125°C
Thermal Resistance ($\theta_{JA}$) ..... 36.34°C/W
Thermal Resistance ($\theta_{JC}$) ..... 9.47°C/W

## Electrical Characteristics[10]

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Supply Current – Core / Digital I/Os** | | | | | | |
| $I_{CORE}$ | 1.2V Total of: DVDDL (digital core) + AVDDL (analog core) + AVDDL_PLL (PLL) | 1000Base-T link-up (no traffic) | | 210 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 221 | | mA |
| | | 100Base-TX link-up (no traffic) | | 63.6 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 63.8 | | mA |
| | | 10Base-T link-up (no traffic) | | 7.1 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 7.7 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 1.0 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 0.7 | | mA |
| $I_{DVDDH\_1.8}$ | 1.8V for Digital I/Os (RGMII operating @ 1.8V) | 1000Base-T link-up (no traffic) | | 11.2 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 23.6 | | mA |
| | | 100Base-TX link-up (no traffic) | | 8.4 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 9.8 | | mA |
| | | 10Base-T link-up (no traffic) | | 3.6 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 5.6 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 5.5 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 0.3 | | mA |

**Notes:**

8. Exceeding the absolute maximum rating can damage the device. Stresses greater than the absolute maximum rating can cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.
9. The device is not guaranteed to function outside its operating rating.
10. $T_A$ = 25°C. Specification is for packaged product only.

## Electrical Characteristics[10] (Continued)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{DVDDH\_2.5}$ | 2.5V for Digital I/Os (RGMII operating @ 2.5V) | 1000Base-T link-up (no traffic) | | 14.7 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 31.5 | | mA |
| | | 100Base-TX link-up (no traffic) | | 10.5 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 13.0 | | mA |
| | | 10Base-T link-up (no traffic) | | 6.3 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 9.0 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 6.7 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 0.7 | | mA |
| $I_{DVDDH\_3.3}$ | 3.3V for Digital I/Os (RGMII operating @ 3.3V) | 1000Base-T link-up (no traffic) | | 19.5 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 41.5 | | mA |
| | | 100Base-TX link-up (no traffic) | | 13.9 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 17.2 | | mA |
| | | 10Base-T link-up (no traffic) | | 11.5 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 13.7 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 9.3 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 2.2 | | mA |
| **Supply Current – Transceiver (Equivalent to current draw through external transformer center taps for PHY transceivers with current-mode transmit drivers.)** | | | | | | |
| $I_{AVDDH\_2.5}$ | 2.5V for Transceiver (Recommended for commercial temperature range operation only) | 1000Base-T link-up (no traffic) | | 58.8 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 57.9 | | mA |
| | | 100Base-TX link-up (no traffic) | | 24.9 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 24.9 | | mA |
| | | 10Base-T link-up (no traffic) | | 11.5 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 25.3 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 3.1 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 0.02 | | mA |
| $I_{AVDDH\_3.3}$ | 3.3V for Transceiver | 1000Base-T link-up (no traffic) | | 67.4 | | mA |
| | | 1000Base-T full-duplex @ 100% utilization | | 66.3 | | mA |
| | | 100Base-TX link-up (no traffic) | | 28.7 | | mA |
| | | 100Base-TX full-duplex @ 100% utilization | | 28.6 | | mA |
| | | 10Base-T link-up (no traffic) | | 15.9 | | mA |
| | | 10Base-T full-duplex @ 100% utilization | | 28.6 | | mA |
| | | Software power-down mode (Reg. 0.11 = 1) | | 4.2 | | mA |
| | | Chip power-down mode (strap-in pins MODE[3:0] = 0111) | | 0.02 | | mA |

## Electrical Characteristics[10] (Continued)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **CMOS Inputs** | | | | | | |
| $V_{IH}$ | Input High Voltage | DVDDH (digital I/Os) = 3.3V | 2.0 | | | V |
| | | DVDDH (digital I/Os) = 2.5V | 1.5 | | | V |
| | | DVDDH (digital I/Os) = 1.8V | 1.1 | | | V |
| $V_{IL}$ | Input Low Voltage | DVDDH (digital I/Os) = 3.3V | | | 1.3 | V |
| | | DVDDH (digital I/Os) = 2.5V | | | 1.0 | V |
| | | DVDDH (digital I/Os) = 1.8V | | | 0.7 | V |
| $I_{IHL}$ | Input High Leakage Current | DVDDH = 3.3V and $V_{IH}$ = 3.3V<br>All digital input pins | -2.0 | | 2.0 | µA |
| $I_{ILL}$ | Input Low Leakage Current | DVDDH = 3.3V and $V_{IL}$ = 0.0V<br>All digital input pins, except MDC, MDIO, RESET_N. | -2.0 | | 2.0 | µA |
| | | DVDDH = 3.3V and $V_{IL}$ = 0.0V<br>MDC, MDIO, RESET_N pins with internal pull-ups | -120 | | -40 | µA |
| **CMOS Outputs** | | | | | | |
| $V_{OH}$ | Output High Voltage | DVDDH (digital I/Os) = 3.3V, $I_{OH}$ (min) = 10mA<br>All digital output pins | 2.7 | | | V |
| | | DVDDH (digital I/Os) = 2.5V, $I_{OH}$ (min) = 10mA<br>All digital output pins | 2.0 | | | V |
| | | DVDDH (digital I/Os) = 1.8V, $I_{OH}$ (min) = 13mA<br>All digital output pins, except LED1, LED2 | 1.5 | | | V |
| $V_{OL}$ | Output Low Voltage | DVDDH (digital I/Os) = 3.3V, $I_{OL}$ (min) = 10mA<br>All digital output pins | | | 0.3 | V |
| | | DVDDH (digital I/Os) = 2.5V, $I_{OL}$ (min) = 10mA<br>All digital output pins | | | 0.3 | V |
| | | DVDDH (digital I/Os) = 1.8V, $I_{OL}$ (min) = 13mA<br>All digital output pins, except LED1, LED2 | | | 0.3 | V |
| $\|I_{oz}\|$ | Output Tri-State Leakage | | | | 10 | µA |
| **LED Outputs** | | | | | | |
| $I_{LED}$ | Output Drive Current | DVDDH (digital I/Os) = 3.3V or 2.5V and $V_{OL}$ at 0.3V<br>Each LED pin (LED1, LED2) | 10 | | | mA |
| Pull-Up Pins<br>(Measured with pin input voltage level at 1/2 DVDDH) | | | | | | |
| pu | Internal Pull-Up Resistance (MDC, MDIO, RESET_N pins) | DVDDH (digital I/Os) = 3.3V | 13 | 22 | 31 | kΩ |
| | | DVDDH (digital I/Os) = 2.5V | 16 | 28 | 39 | kΩ |
| | | DVDDH (digital I/Os) = 1.8V | 26 | 44 | 62 | kΩ |

## Electrical Characteristics[10] (Continued)

| | | | | | | |
|---|---|---|---|---|---|---|
| **100Base-TX Transmit (Measured differentially after 1:1 transformer)** | | | | | | |
| $V_O$ | Peak Differential Output Voltage | 100Ω termination across differential output | 0.95 | | 1.05 | V |
| $V_{IMB}$ | Output Voltage Imbalance | 100Ω termination across differential output | | | 2 | % |
| $t_r$, $t_f$ | Rise/Fall Time | | 3 | | 5 | ns |
| | Rise/Fall Time Imbalance | | 0 | | 0.5 | ns |
| | Duty Cycle Distortion | | | | ±0.25 | ns |
| | Overshoot | | | | 5 | % |
| | Output Jitter | Peak-to-peak | | 0.7 | | ns |
| **10Base-T Transmit (Measured differentially after 1:1 transformer)** | | | | | | |
| $V_P$ | Peak Differential Output Voltage | 100Ω termination across differential output | 2.2 | | 2.8 | V |
| | Jitter Added | Peak-to-peak | | | 3.5 | ns |
| | Harmonic Rejection | Transmit all-one signal sequence | | –31 | | dB |
| **10Base-T Receive** | | | | | | |
| $V_{SQ}$ | Squelch Threshold | 5MHz square wave | 300 | 400 | | mV |
| **Transmitter – Drive Setting** | | | | | | |
| $V_{SET}$ | Reference Voltage of $I_{SET}$ | $R(I_{SET})$ = 12.1kΩ | | 1.2 | | V |
| **LDO Controller – Drive Range** | | | | | | |
| $V_{LDO\_O}$ | Output Drive Range for LDO_O (Pin 43) to Gate Input of P-Channel MOSFET | AVDDH = 3.3V for MOSFET source voltage | 0.85 | | 2.8 | V |
| | | AVDDH = 2.5V for MOSFET source voltage (recommended for commercial temperature range operation only) | 0.85 | | 2.0 | |

# Timing Diagrams

### RGMII Timing

As the default, after power-up or reset, the KSZ9031RNX RGMII timing conforms to the timing requirements in the RGMII Version 2.0 Specification for internal PHY chip delay.

For the transmit path (MAC to KSZ9031RNX), the KSZ9031RNX does not add any delay locally at its GTX_CLK, TX_EN and TXD[3:0] input pins, and expects the GTX_CLK delay to be provided on-chip by the MAC. If MAC does not provide any delay or insufficient delay for the GTX_CLK, the KSZ9031RNX has pad skew registers that can provide up to 1.38ns on-chip delay.

For the receive path (KSZ9031RNX to MAC), the KSZ9031RNX adds 1.2ns typical delay to the RX_CLK output pin with respect to RX_DV and RXD[3:0] output pins. If necessary, the KSZ9031RNX has pad skew registers that can adjust the RX_CLK on-chip delay up to 2.58ns from the 1.2ns default delay.

It is common to implement RGMII PHY-to-MAC designs that either PHY, MAC, or both PHY and MAC are not fully RGMII v2.0 compliant with on-chip clock delay. These combinations of mixed RGMII v1.3/v2.0 designs and plus sometimes non-matching RGMII PCB trace routings require a review of the entire RGMII system timings (PHY on-chip, PCB trace delay, MAC on-chip) to compute the aggregate clock delay and determine if the clock delay timing is met. If timing adjustment is needed, pad skew registers are provided by the KSZ9031RNX. Refer to RGMII Pad Skew Registers section.

The following Figure 12, Figure 13 and Table 19 from the RGMII v2.0 Specification are provided as references to understanding RGMII v1.3 external delay and RGMII v2.0 on-chip delay timings.

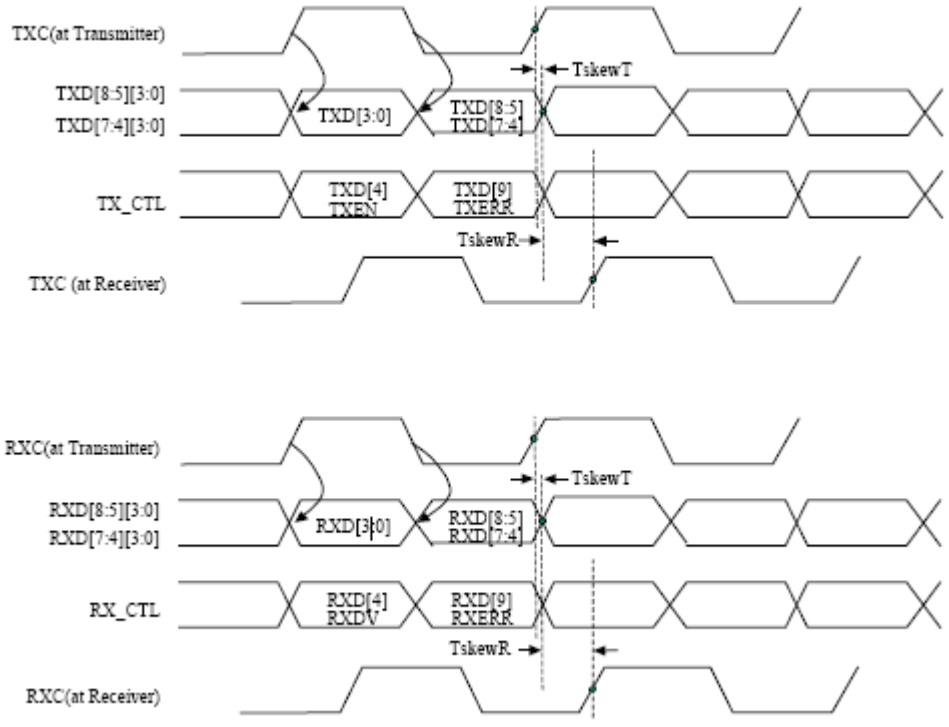



**Figure 12. RGMII v2.0 Spec (Figure 2 – Multiplexing and Timing Diagram – Original RGMII (v1.3) with external delay)**

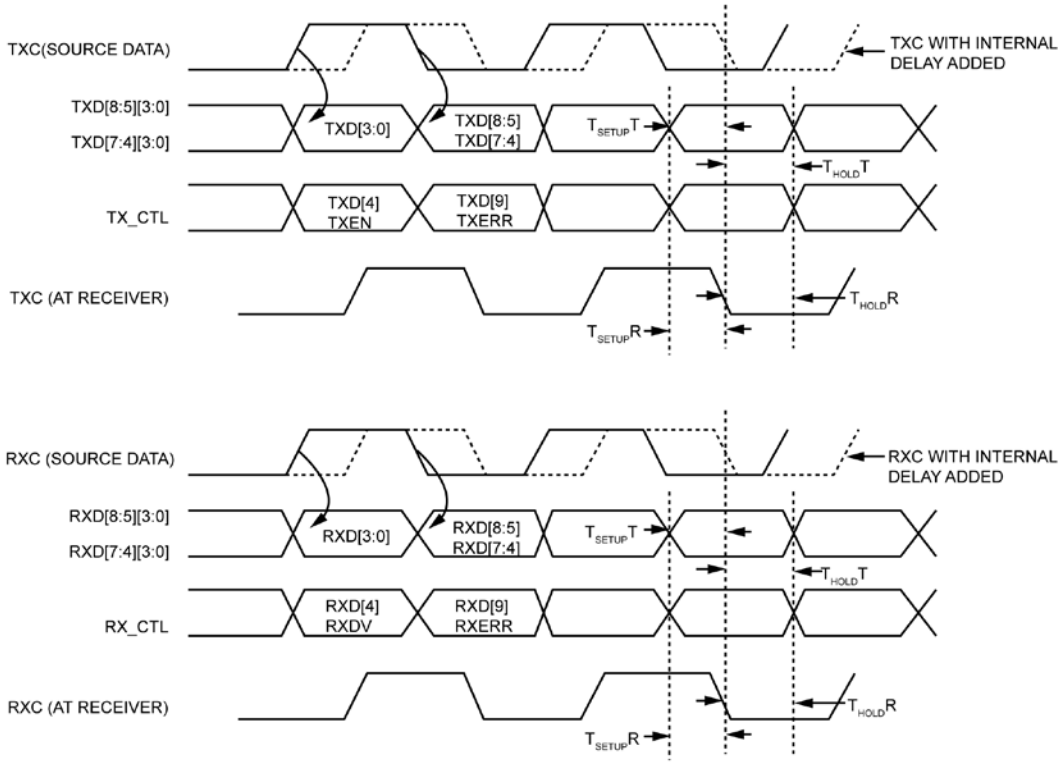



**Figure 13. RGMII v2.0 Spec (Figure 3 – Multiplexing and Timing Diagram – RGMII-ID (v2.0) with internal chip delay)**

The following notes provides clarification for Figure 13.

**TXC (SOURCE DATA)**, solid line, is the MAC GTX_CLK clock output timing per RGMII v1.3 Specification (PCB delay line required or PHY internal delay required)

**TXC (SOURCE DATA) WITH INTERNAL DELAY ADDED**, dotted line, is the MAC GTX_CLK clock output timing per RGMII v2.0 Specification (no PCB delay required and no PHY internal delay required)

**RXC (SOURCE DATA)**, solid line, is the PHY RX_CLK clock output timing per RGMII v1.3 Specification (PCB delay line required or MAC internal delay required)

**RXC (SOURCE DATA) WITH INTERNAL DELAY ADDED**, dotted line, is the PHY RX_CLK clock output timing per RGMII v2.0 Specification (no PCB delay required and no MAC internal delay required)

**Table 19. RGMII v2.0 Specification (Timing Specifics from Table 2)**

| Timing Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{skew}T$ | Data to clock output skew (at transmitter) per RGMII v1.3 (external delay) | –500 | | 500 | ps |
| $T_{skew}R$ | Data to clock input skew (at receiver) per RGMII v1.3 (external delay) | 1.0 | | 2.6 | ns |
| $T_{setup}T$ | Data to clock output setup (at transmitter – integrated delay) | 1.2 | 2.0 | | ns |
| $T_{hold}T$ | Clock to data output hold (at transmitter – integrated delay) | 1.2 | 2.0 | | ns |
| $T_{setup}R$ | Data to clock input setup (at receiver – integrated delay) | 1.0 | 2.0 | | ns |
| $T_{hold}R$ | Clock to data input hold (at receiver – integrated delay) | 1.0 | 2.0 | | ns |
| $T_{cyc}$ (1000Base-T) | Clock cycle duration for 1000Base-T | 7.2 | 8 | 8.8 | ns |
| $T_{cyc}$ (100Base-TX) | Clock cycle duration for 100Base-TX | 36 | 40 | 44 | ns |
| $T_{cyc}$ (10Base-T) | Clock cycle duration for 10Base-T | 360 | 400 | 440 | ns |

The RGMII Version 2.0 Specification defines the RGMII data-to-clock skews only for 1000Mbps operation, which uses both clock edges for sampling the data and control signals at the 125MHz clock frequency (8ns period). For 10/100Mbps operations, the data signals are sampled on the rising clock edge and the control signals are sampled on both clock edges. With slower clock frequencies, 2.5MHz (400ns period) for 10Mbps and 25MHz (40ns period) for 100Mbps, the RGMII data-to-clock skews for 10/100Mbps operations will have greater timing margins than for 1000Mbps operation, and therefore can be relaxed from 2.6ns (maximum) for 1000Mbps to 160ns (maximum) for 10Mbps and 16ns (maximum) for 100Mbps.

### Auto-Negotiation Timing

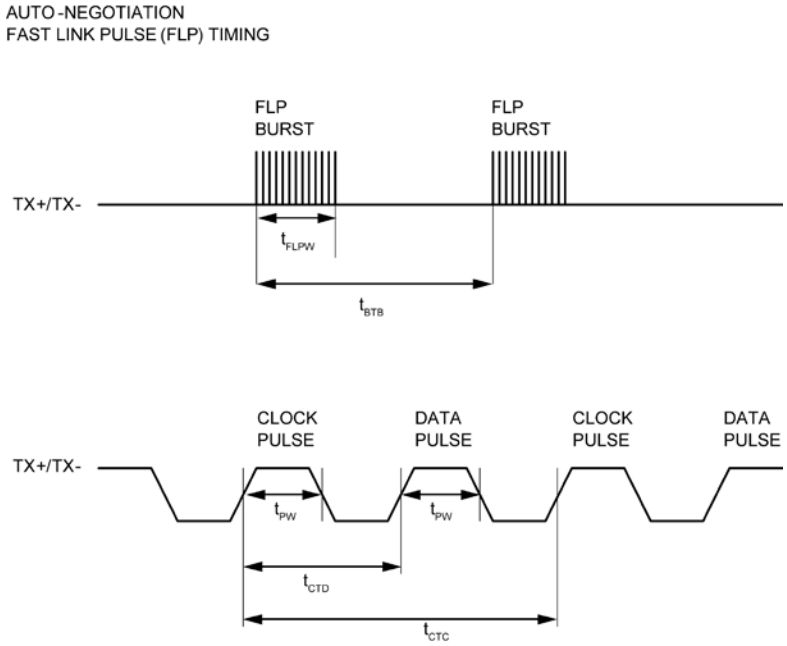



**Figure 14. Auto-Negotiation Fast Link Pulse (FLP) Timing**

**Table 20. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters**

| Timing Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $t_{BTB}$ | FLP burst to FLP burst | 8 | 16 | 24 | ms |
| $t_{FLPW}$ | FLP burst width | | 2 | | ms |
| $t_{PW}$ | Clock/data pulse width | | 100 | | ns |
| $t_{CTD}$ | Clock pulse to data pulse | 55.5 | 64 | 69.5 | µs |
| $t_{CTC}$ | Clock pulse to clock pulse | 111 | 128 | 139 | µs |
| | Number of clock/data pulses per FLP burst | 17 | | 33 | |

The KSZ9031RNX Fast Link Pulse (FLP) burst-to-burst transmit timing for Auto-Negotiation defaults to 8ms. IEEE 802.3 Standard specifies this timing to be 16ms +/-8ms. Some PHY link partners need to receive the FLP with 16ms centered timing; otherwise, there can be intermittent link failures and long link-up times.

After KSZ9031RNX power-up/reset, program the following register sequence to set the FLP timing to 16ms:

1. Write Register Dh = 0x0000 // Set up register address for MMD – Device Address 0h
2. Write Register Eh = 0x0004 // Select Register 4h of MMD – Device Address 0h
3. Write Register Dh = 0x4000 // Select register data for MMD – Device Address 0h, Register 4h
4. Write Register Eh = 0x0006 // Write value 0x0006 to MMD – Device Address 0h, Register 4h
5. Write Register Dh = 0x0000 // Set up register address for MMD – Device Address 0h
6. Write Register Eh = 0x0003 // Select Register 3h of MMD – Device Address 0h
7. Write Register Dh = 0x4000 // Select register data for MMD – Device Address 0h, Register 3h
8. Write Register Eh = 0x1A80 // Write value 0x1A80 to MMD – Device Address 0h, Register 3h
9. Write Register 0h, Bit [9] = 1// Restart Auto-Negotiation

The above setting for 16ms FLP transmit timing is compatible with all PHY link partners.

**MDC/MDIO Timing**

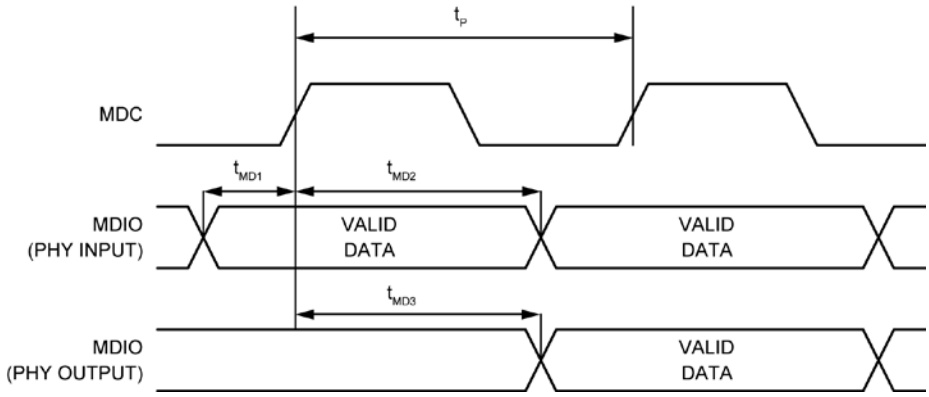



**Figure 15. MDC/MDIO Timing**

**Table 21. MDC/MDIO Timing Parameters**

| Timing Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $t_P$ | MDC period | 120 | 400 | | ns |
| $t_{1MD1}$ | MDIO (PHY input) setup to rising edge of MDC | 10 | | | ns |
| $t_{MD2}$ | MDIO (PHY input) hold from rising edge of MDC | 10 | | | ns |
| $t_{MD3}$ | MDIO (PHY output) delay from rising edge of MDC | 0 | | | ns |

The typical MDC clock frequency is 2.5MHz (400ns clock period).

The KSZ9031RNX can operate with MDC clock frequencies generated from bit banging with GPIO pin in the 10s/100s of Hertz and have been tested up to a MDC clock frequency of 8.33MHz (120ns clock period). Test condition for 8.33MHz is for one KSZ9031RNX PHY on the MDIO line with a 1.0kΩ pull-up to the DVDDH supply rail.

**Power-Up/Power-Down/Reset Timing**

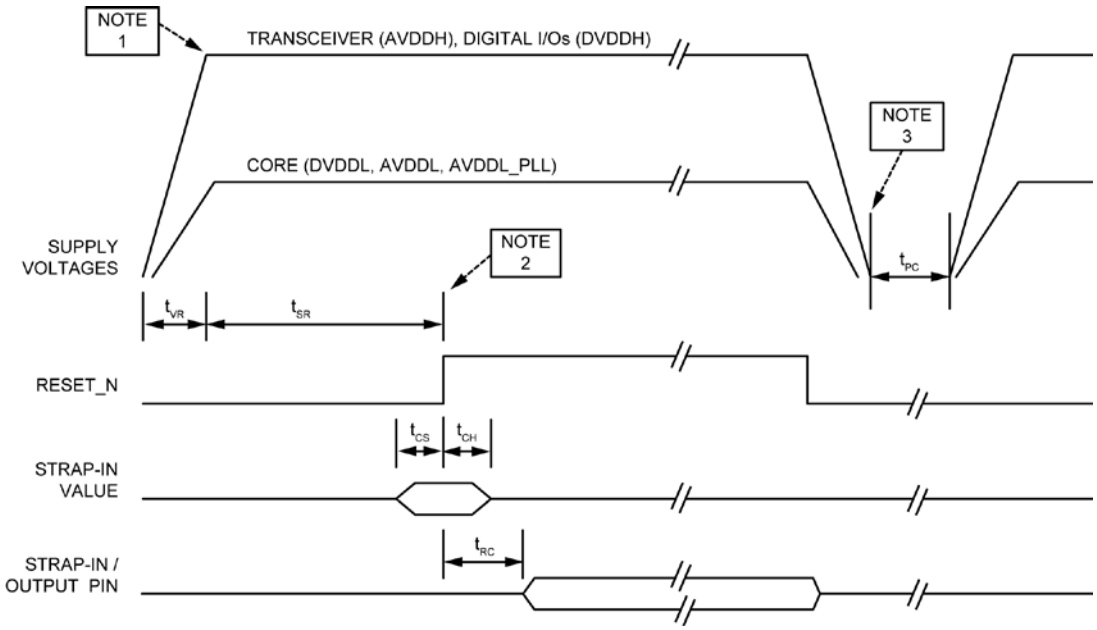



**Figure 16. Power-Up/Power-Down/Reset Timing**

**Note 1:**

The recommended power-up sequence is to have the transceiver (AVDDH) and digital I/O (DVDDH) voltages power up before the 1.2V core (DVDDL, AVDDL, AVDDL_PLL) voltage. If the 1.2V core must power up first, the maximum lead time for the 1.2V core voltage with respect to the transceiver and digital I/O voltages should be 200µs.

There is no power sequence requirement between transceiver (AVDDH) and digital I/O (DVDDH) power rails.

The power-up waveforms should be monotonic for all supply voltages to the KSZ9031RNX.

**Note 2:**

After the de-assertion of reset, wait a minimum of 100µs before starting programming on the MIIM (MDC/MDIO) interface.

**Note 3:**

The recommended power-down sequence is to have the 1.2V core voltage power-down before powering down the transceiver and digital I/O voltages.

**Table 22. Power-Up/Power-Down/Reset Timing Parameters**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_{VR}$ | Supply voltages rise time (must be monotonic) | 200 | | µs |
| $t_{SR}$ | Stable supply voltages to de-assertion of reset | 10 | | ms |
| $t_{CS}$ | Strap-in pin configuration setup time | 5 | | ns |
| $t_{CH}$ | Strap-in pin configuration hold time | 5 | | ns |
| $t_{RC}$ | De-assertion of reset to strap-in pin output | 6 | | ns |
| $t_{PC}$ | Supply voltages cycle off-to-on time | 150 | | ms |

Before the next power-up cycle, all supply voltages to the KSZ9031RNX should reach less than 0.4V and there should be a minimum wait time of 150ms from power-off to power-on.

## Reset Circuit

The following are some reset circuit suggestions.

Figure 17 illustrates the reset circuit for powering up the KSZ9031RNX if reset is triggered by the power supply.

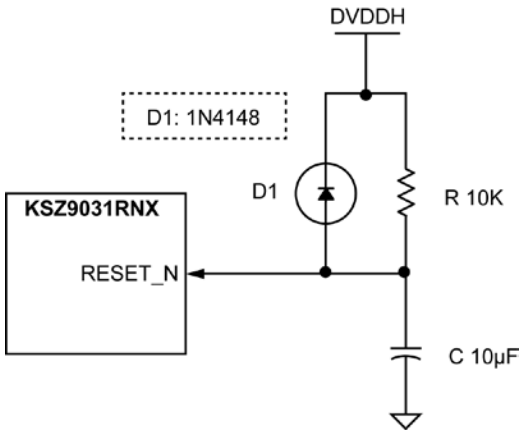



**Figure 17. Reset Circuit for triggering by Power Supply**

Figure 18 illustrates the reset circuit for applications where reset is driven by another device (for example, the CPU or an FPGA). At power-on-reset, R, C, and D1 provide the monotonic rise time to reset the KSZ9031RNX device. The RST_OUT_N from the CPU/FPGA provides the warm reset after power-up.

The KSZ9031RNX and CPU/FPGA references the same digital I/O voltage (DVDDH).

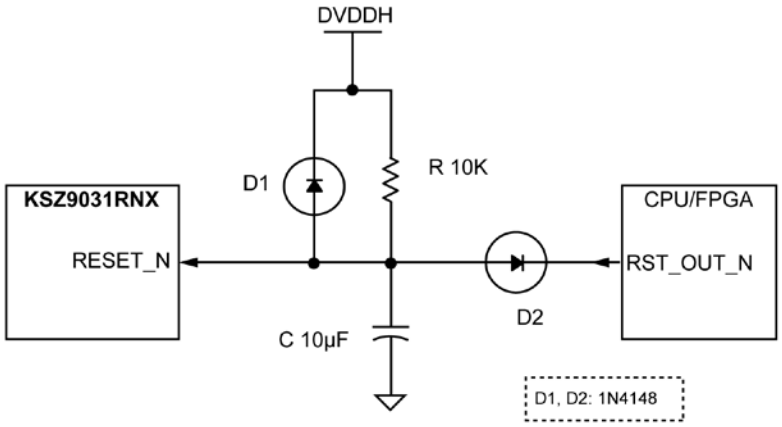



**Figure 18. Reset Circuit for Interfacing with CPU/FPGA Reset Output**

Figure 19 illustrates the reset circuit with MIC826 Voltage Supervisor driving the KSZ9031RNX reset input.

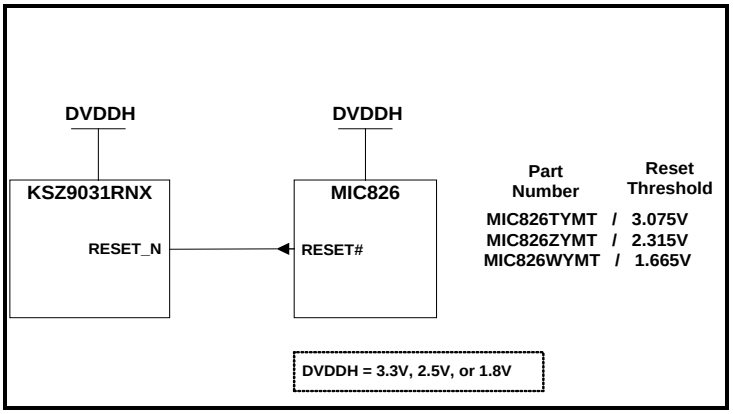



**Figure 19. Rest Circuit with MIC826 Voltage Supervisor**

## Reference Circuits – LED Strap-In Pins

The pull-up and pull-down reference circuits for the LED2/PHYAD1 and LED1/PHYAD0 strapping pins are shown in Figure 20 for 3.3V and 2.5V DVDDH.

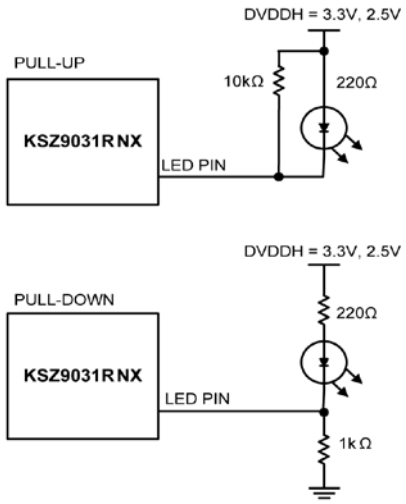



**Figure 20. Reference Circuits for LED Strapping Pins**

For 1.8V DVDDH, LED indication support requires voltage level shifters between LED[2:1] pins and LED indicator diodes to ensure the multiplexed PHYAD[1:0] strapping pins are latched in high/low correctly. If LED indicator diodes are not implemented, the PHYAD[1:0] strapping pins just need 10kΩ pull-up to 1.8V DVDDH for a value of 1, and 1.0kΩ pull-down to ground for a value of 0.

## Reference Clock – Connection and Selection

A crystal or external clock source, such as an oscillator, is used to provide the reference clock for the KSZ9031RNX. The reference clock is 25MHz for all operating modes of the KSZ9031RNX.

The KSZ9031RNX uses the AVDDH supply, analog 3.3V (or analog 2.5V option for commercial temp only), for the crystal/clock pins (XI, XO). If the 25MHz reference clock is provided externally, the XI input pin should have a minimum clock voltage peak-to-peak (Vp-p) swing of 2.5V reference to ground. If Vp-p is less than 2.5V, series capacitive coupling is recommended. With capacitive coupling, the Vp-p swing can be down to 1.5V. Maximum Vp-p swing is 3.3V +5%.

Figure 21 and Table 23 shows the reference clock connection to XI and XO of the KSZ9031RNX, and the reference clock selection criteria.

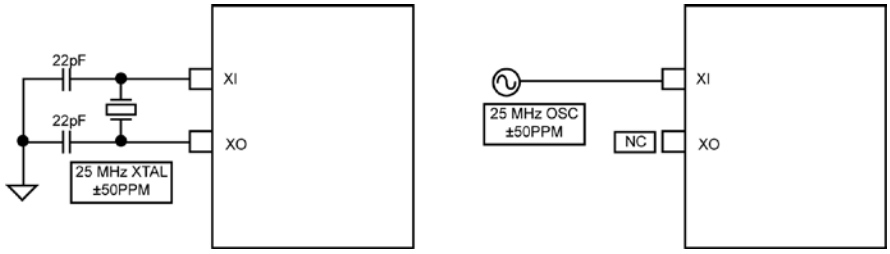



**Figure 21. 25MHz Crystal/Oscillator Reference Clock Connection**

**Table 23. Reference Crystal/Clock Selection Criteria**

| Characteristics | Value | Units |
|---|---|---|
| Frequency | 25 | MHz |
| Frequency tolerance (maximum) | ±50 | ppm |
| Crystal series resistance (typical) | 40 | Ω |
| Crystal load capacitance (typical) | 22 | pF |

## On-Chip LDO Controller – MOSFET Selection

If the optional LDO controller is used to generate 1.2V for the core voltage, the selected MOSFET should exceed the following minimum requirements:

- P-channel
- 500mA (continuous current)
- 3.3V or 2.5V (source – input voltage)
- 1.2V (drain – output voltage)
- $V_{GS}$ in the range of:
  (-1.2V to -1.5V) @ 500mA for 3.3V source voltage
  (-1.0V to -1.1V) @ 500mA for 2.5V source voltage

The $V_{GS}$ for the MOSFET needs to be operating in the constant current saturated region, and not towards the $V_{GS(th)}$, the threshold voltage for the cut-off region of the MOSFET.

See the end of Electrical Characteristics section for LDO controller output driving range to the gate input of the MOSFET.

Refer to application note ANLAN206 – KSZ9031 Gigabit PHY Optimized Power Scheme for High Efficiency, Low-Power Consumption and Dissipation as design reference.

## Magnetic – Connection and Selection

A 1:1 isolation transformer is required at the line interface. Use one with integrated common-mode chokes for designs exceeding FCC requirements. An optional auto-transformer stage following the chokes provides additional common-mode noise and signal attenuation.

The KSZ9031RNX design incorporates voltage-mode transmit drivers and on-chip terminations.

With the voltage-mode implementation, the transmit drivers supply the common-mode voltages to the four differential pairs. Therefore, the four transformer center tap pins on the KSZ9031RNX side should not be connected to any power supply source on the board; rather, the center tap pins should be separated from one another and connected through separate 0.1µF common-mode capacitors to ground. Separation is required because the common-mode voltage could be different between the four differential pairs, depending on the connected speed mode.

Figure 22 shows the typical gigabit magnetic interface circuit for the KSZ9031RNX.

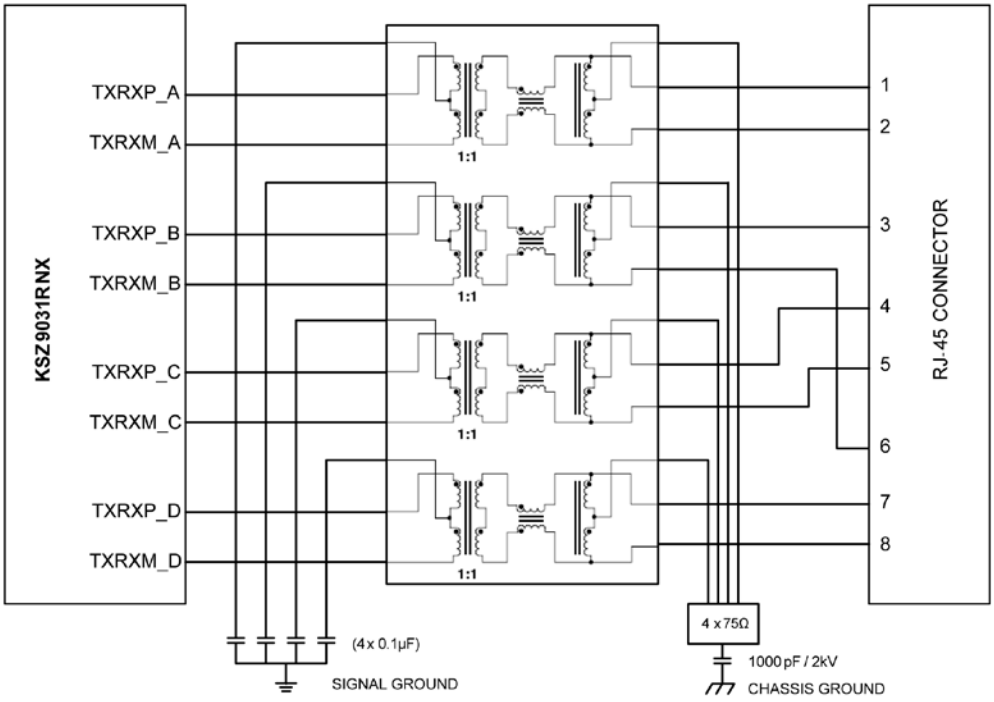



**Figure 22. Typical Gigabit Magnetic Interface Circuit**

Table 24 lists recommended magnetic characteristics.

**Table 24. Magnetics Selection Criteria**

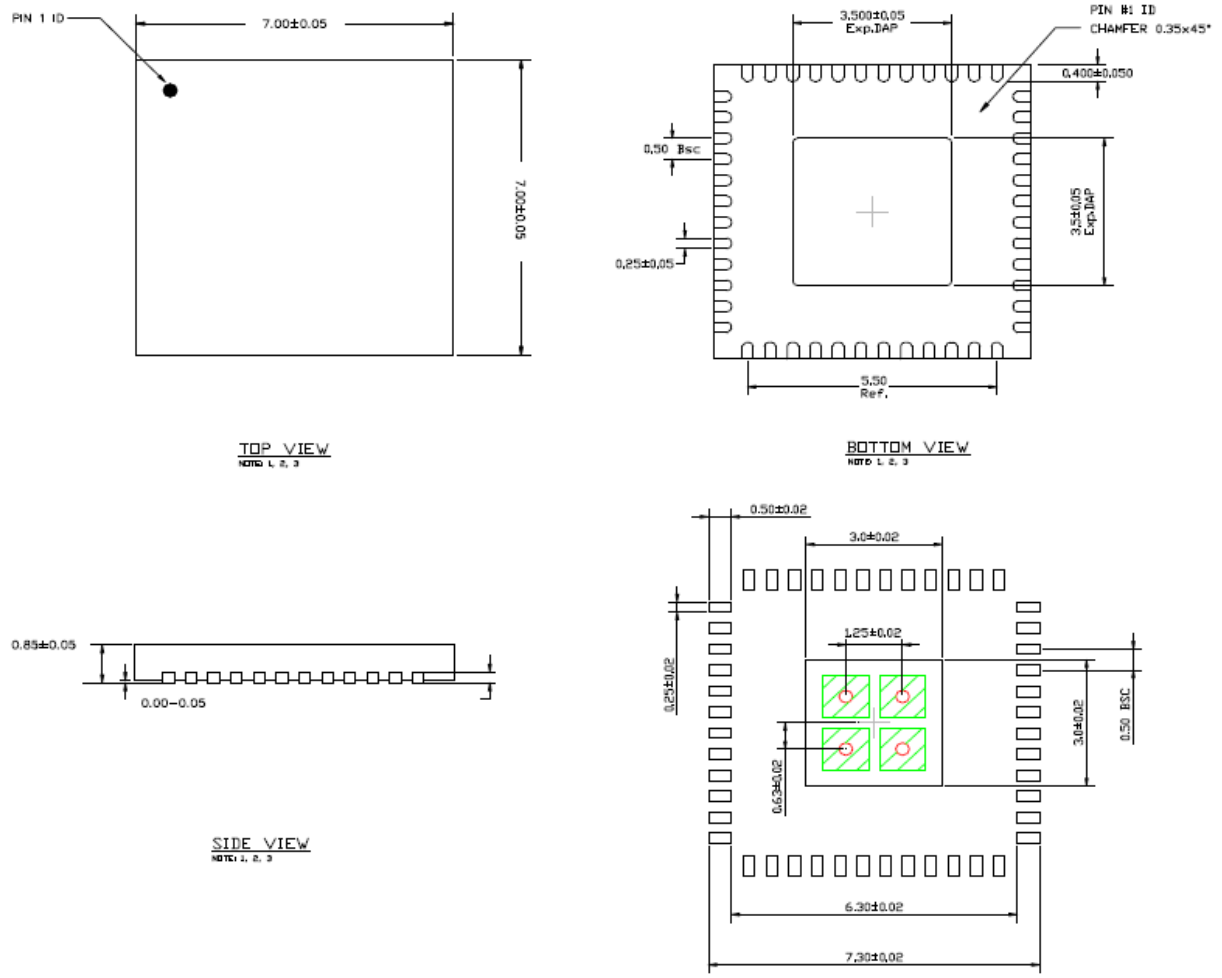
| Parameter | Value | Test Condition |
|---|---|---|
| Turns ratio | 1 CT : 1 CT | |
| Open-circuit inductance (minimum) | 350µH | 100mV, 100kHz, 8mA |
| Insertion loss (maximum) | 1.0dB | 0MHz to 100MHz |
| HIPOT (minimum) | 1500Vrms | |

Table 25 is a list of compatible single-port magnetics with separated transformer center tap pins on the G-PHY chip side that can be used with the KSZ9031RNX.

**Table 25. Compatible Single-Port 10/100/1000 Magnetics**

| Manufacturer | Part Number | Auto-Transformer | Temperature Range | Magnetic + RJ-45 |
|---|---|---|---|---|
| Bel Fuse | 0826-1G1T-23-F | Yes | 0°C to 70°C | Yes |
| HALO | TG1G-E001NZRL | No | –40°C to 85°C | No |
| HALO | TG1G-S001NZRL | No | 0°C to 70°C | No |
| HALO | TG1G-S002NZRL | Yes | 0°C to 70°C | No |
| Pulse | H5007NL | Yes | 0°C to 70°C | No |
| Pulse | H5062NL | Yes | 0°C to 70°C | No |
| Pulse | HX5008NL | Yes | –40°C to 85°C | No |
| Pulse | JK0654219NL | Yes | 0°C to 70°C | Yes |
| Pulse | JK0-0136NL | No | 0°C to 70°C | Yes |
| TDK | TLA-7T101LF | No | 0°C to 70°C | No |
| Wurth/Midcom | 000-7093-37R-LF1 | Yes | 0°C to 70°C | No |

## Package Information[11] and Recommended Land Pattern



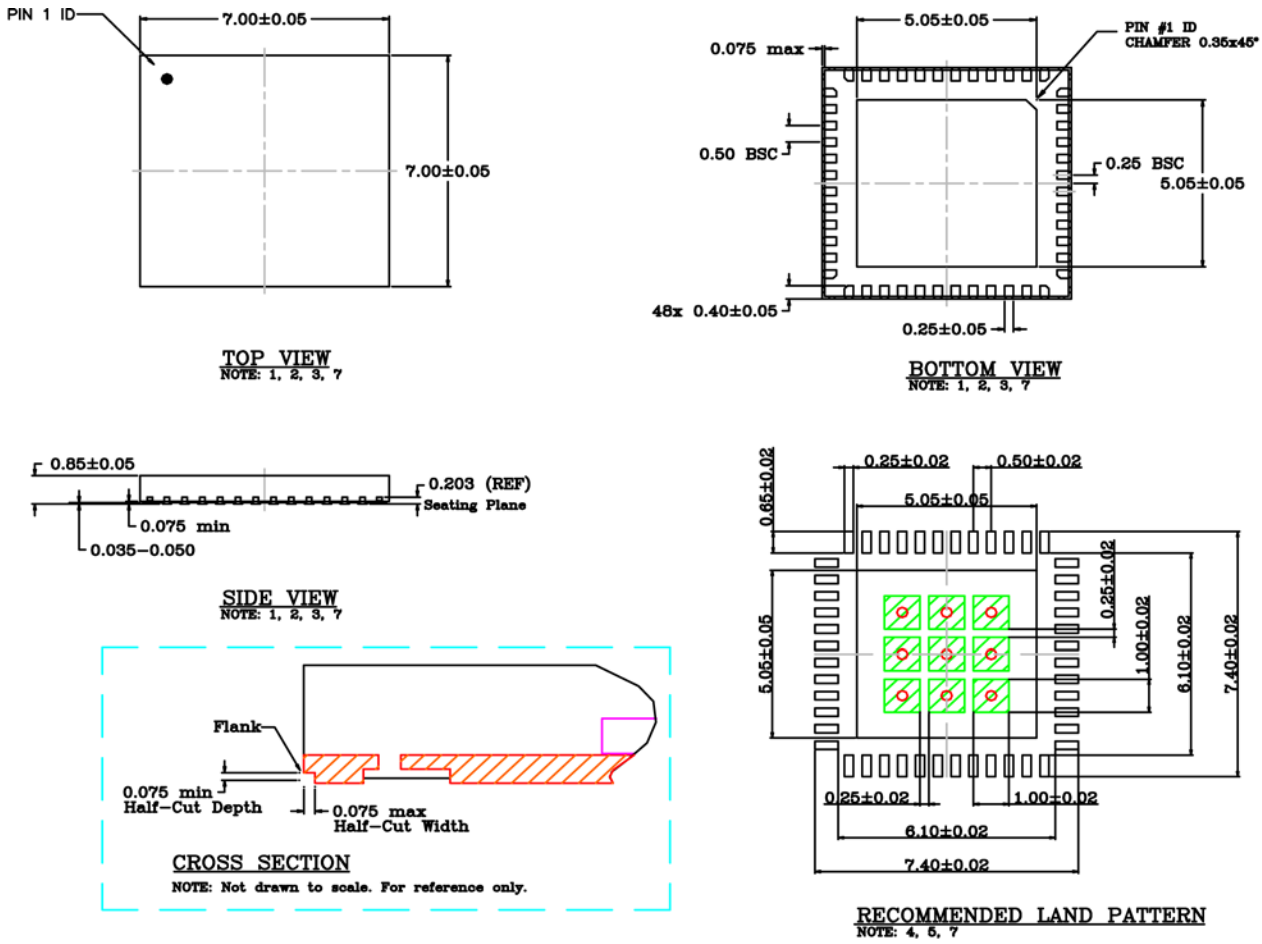

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.3mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. 1.00mm PITCH
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 0.93mm x 0.93mm, SPACING IS 0.25mm, 1.25mm PITCH.

**48-Pin (7mm × 7mm) QFN**

**Note:**

11. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

## Package Information[11] and Recommended Land Pattern (Continued)




NOTE:
1. MAX PACKAGE WARPAGE IS 0.05mm.
2. MAX ALLOWABLE BURR IS 0.076mm IN ALL DIRECTIONS.
3. PIN #1 IS ON TOP WILL BE LASER MARKED.
4. RED CIRCLES IN LAND PATTERN INDICATES THERMAL VIA. SIZE SHOULD BE 0.30-0.35mm IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE. PITCH = 1.00mm
5. GREEN RECTANGLES (SHADED AREA) REPRESENT SOLDER STENCIL OPENING ON EXPOSED PAD AREA. RECOMMENDED SIZE IS 1.0x1.0mm, SPACING = 0.25mm.
6. "W" IN WQFN IS WETTABLE FLANK PACKAGE.

**48-Pin (7mm × 7mm) WQFN**

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