L5150GJ

5 V low dropout voltage regulator

Datasheet – production data

Features

Max DC supply voltage	V_S	40 V
Max output voltage tolerance	ΔV_o	+/-2%
Max dropout voltage	V_{dp}	500 mV
Output current	I_o	150 mA
Quiescent current	I_{qn}	5 µA(1) 55 µA(2)

1. Typical value with regulator disabled.
2. Typical value with regulator enabled.

- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Precision output voltage 5 V +/- 2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Adjustable reset threshold
- Early warning
- Very wide stability range with low value output capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range (T_j = -40 °C to 150 °C)
- Enable input for enabling / disabling the voltage regulator

PowerSSO-12

GAPGP01380

Description

L5150GJ is a low dropout linear regulator with microprocessor control functions such as power on reset, low voltage reset, early warning, on/off control. Typical quiescent current is 55 µA in very low output current mode and enabled regulator. It drops to 5 µA with not enabled regulator.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line and load variation. Early warning circuit monitors the input voltage and compares it with an internal voltage reference.

Output voltage reset threshold can be adjusted down to 3.5 V by means of an external voltage divider.

The maximum input voltage is 40 V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output. In addition, only low-value ceramic capacitor on output is required for stability.

Table 1. Device summary

Package	Order codes	
	Tube	Tape & reel
PowerSSO-12	L5150GJ	L5150GJTR

Contents

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1 Block diagram and pins description

Figure 1. Block diagram

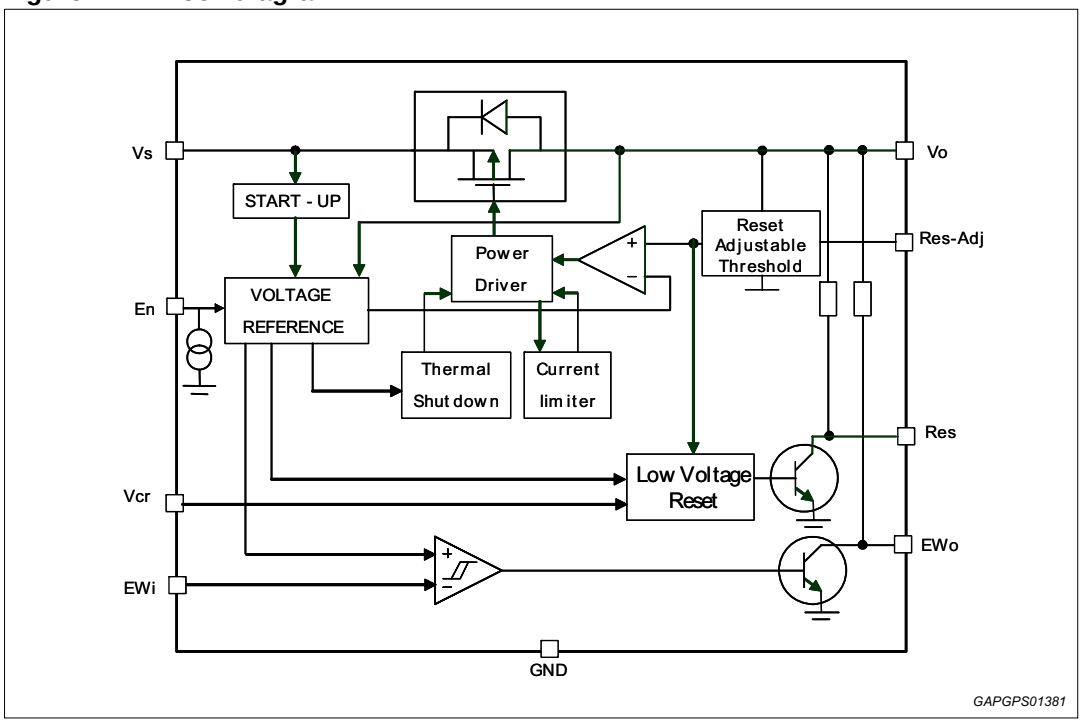


Figure 2. Configuration diagram (top view)

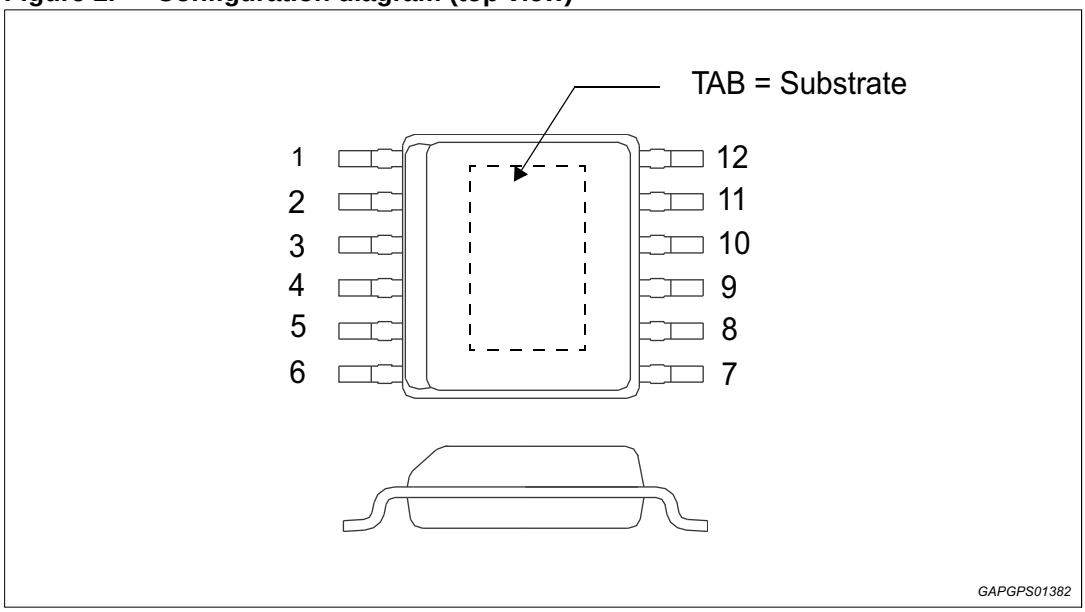


Table 2. Pins description

Pin	Name	Function
1	R_{es_Adj}	Reset adjustable threshold. Connected to an appropriate external voltage divider, it allows to properly set the reset threshold down to 3.5 V. Connect to GND if not needed.
2	R_{es}	Reset output. Internally connected to Vo through a 20 KΩ pull-up resistor. This pin is pulled low when $V_o < V_{o\_th}$. Keep open if not needed.
3	V_{cr}	Reset delay. Connect an external capacitor between V_{cr} pin and ground to adjust the reset delay time. Keep open if not needed.
4	GND	Ground reference.
5	NC	Not connected.
6	V_o	5 V regulated output. Block to GND with a ceramic capacitor ($C_o \geq 220$ nF for regulator stability).
7	V_S	Supply voltage, block directly to GND on the IC with a capacitor.
8	NC	Not connected.
9	E_n	Enable input. A high signal switches the regulator on. Connect to V_S if not needed.
10	EW_i	Early warning input. This pin monitors the V_S voltage level through a resistor divider. Connect to V_S if not needed.
11	NC	Not connected.
12	EW_o	Early warning output. Internally connected to V_o through 20 KΩ pull up resistor. This pin is pulled low when EW_i is below bandgap reference voltage. Keep open if not needed.
-	TAB	TAB is connected to the substrate of the chip: connect to GND or leave open (see *Figure 2*).

2 Electrical specifications

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 3: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{sdc}	DC supply voltage	-0.3 to 40	V
I_{sdc}	Input current	Internally limited	
V_{odc}	DC output voltage	-0.3 to 6	V
I_{odc}	DC output current	Internally limited	
$V_{od\ Res}$	Open drain output voltage R_{es}	-0.3 to Vodc + 0.3	V
$I_{od\ Res}$	Open drain output current R_{es}	Internally limited	
V_{Res_adj}	V_{Res_adj} voltage	-0.3 to Vodc + 0.3	V
$V_{od\ EWo}$	Open drain output voltage EW_o	-0.3 to Vodc + 0.3	V
$I_{od\ EWo}$	Open drain output current EW_o	Internally limited	
V_{cr}	V_{cr} voltage	-0.3 to Vo + 0.3	V
V_{EWi}	Early warning input voltage	-0.3 to 40	V
V_{En}	Enable input	-0.3 to 40	V
T_j	Junction temperature	-40 to 150	°C
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
VESD CDM	ESD CDM voltage level (CDM-)	+/- 750	V

2.2 Thermal data

Table 4. Thermal data(1)

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction to case: PowerSSO-12	20	°K/W
$R_{thj\text{-}amb}$	Thermal resistance junction to ambient: PowerSSO-12	52	°K/W

1. The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, double copper layer with single heatsink layer, copper thickness 70 µm, thermal vias, copper area 2 cm^2.

2.3 Electrical characteristics

Values specified in this section are for V_S = 5.6 V to 31 V, T_j = -40 °C to +150 °C unless otherwise stated.

Table 5. General

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_o	V_{o_ref}	Output voltage	V_S = 8 V to 18 V, I_o = 8 mA to 150 mA	4.9	5.0	5.1	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 V to 31 V, I_o = 8 mA to 150 mA	4.85	5.0	5.15	V
V_o	V_{o_ref}	Output voltage	V_S = 5.6 V to 31 V, I_o = 0.1 mA to 8 mA	4.75	5.0	5.25	V
V_o	I_{short}	Short-circuit current	V_S = 13.5 V	0.65	0.95	1.25	A
V_o	I_{lim}	Output current capability (1)	V_S = 13.5 V	280	470	660	mA
V_S, V_o	V_{line}	Line regulation voltage	V_S = 6 V to 28 V, I_o = 30 mA			40	mV
V_o	V_{load}	Load regulation voltage	V_S = 8 V to 18 V, I_o = 8 mA to 150 mA			55	mV
			V_S = 13.5 V, T_j = 25 °C, I_o = 8 mA to 150 mA			40	
V_S, V_o	V_{dp}	Drop voltage (2)	I_o = 150 mA			500	mV
V_S, V_o	SVR	Ripple rejection	f_r = 100 Hz (3)		60		dB
V_o	I_{oth_H}	Normal consumption mode output current	V_S = 8 V to 18 V	8			mA
V_o	I_{oth_L}	Very low consumption mode output current	V_S = 8 V to 18 V			1.1	mA
V_o	I_{oth_Hyst}	Output current switching threshold hysteresis	V_S = 13.5 V, T_j = 25 °C		0.8		mA
V_S, V_o	Iqs	Current consumption with regulator disabled Iqs = I_{Vs} – I_o	V_S = 13.5 V, E_n = low		5	10	µA
V_S, V_o	I_{qn_1}	Current consumption with regulator enabled Iqn_1 = I_{Vs} – Io	V_S = 13.5 V, I_o = 0.1 mA to 1 mA, E_n = high Tj = 25 °C		55	80	µA
			V_S = 13.5 V, I_o = 0.1 mA to 1 mA, E_n = high			95	
V_S, V_o	I_{qn_150}	Current consumption with regulator enabled Iqn_150 = I_{Vs} – I_o	V_S = 13.5 V, I_o = 150 mA, E_n = high		3.2	4.2	mA

Table 5. General (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	T_w	Thermal protection temperature		150		190	°C
	T_{w_hy}	Thermal protection temperature hysteresis			10		°C

1. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and I_o = 75 mA.
2. Vs - V_o measured dropout when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and I_o = 75 mA.
3. Guaranteed by design.

Table 6. Reset

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{es}	V_{res_l}	Reset output low voltage	Rext = 5 kW, V_o > 1 V			0.4	V
R_{es}	I_{Res_lkg}	Reset output high leakage current	VRes = 5 V			1	µA
R_{es}	R_{Res}	Pull up internal resistance	Versus V_o	10	20	40	kΩ
R_{es}	V_{o_th}	V_o out of regulation threshold	V_{Res_adj} < 0.2 V, V_o decreasing	6	8	10	% Below V_{o_ref}
R_{es_adj}	V_{Res_adj}	Reset adjustable switching threshold		2.35	2.5	2.65	V
R_{es_adj}	V_{Res_adjl}	Reset adjustable low voltage		0.4	0.9	1.3	V
R_{es_adj}	$I_{Res\_adj\_lkg}$	Reset adjustable leakage current	V_{Res_adj} = 2.5 V	-1		1	µA
V_{cr}	V_{Rlth}	Reset timing low threshold	V_S = 13.5 V	15	18	22	% V_{o_ref}
V_{cr}	V_{Rhth}	Reset timing high threshold	V_S = 13.5 V	47	50	53	% V_{o_ref}
V_{cr}	I_{cr}	Charge current	V_S = 13.5 V	10	20	30	µA
V_{cr}	I_{dr}	Discharge current	V_S = 13.5 V	10	20	30	µA
R_{es}	T_{rr}	Reset reaction time				2	µs
R_{es}	T_{rd}	Reset delay time	V_S = 13.5 V, Ctr = 1000 pF	2	4	11	ms

Table 7. Early warning

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_{Wi}	V_{EWi_thl}	EW input low threshold voltage		2.35	2.50	2.65	V
EW_i	V_{EWi_thh}	EW input high threshold voltage		2.42	2.57	2.72	V
EW_i	V_{EWi_thhyst}	EW input threshold hysteresis			70		mV
EW_i	I_{EWi_lkg}	EW input leakage current	V_{EWi} = 2.5 V, V_S > 4 V	-1		1	µA
EW_o	R_{EWo}	Pull up internal resistance	Versus V_o	10	20	40	kΩ
EW_o	V_{EWo_lv}	EW output low voltage (with external pull up)	V_{EWi} < 2.35 V, V_S > 4 V, R_{ext} = 5 kΩ			0.4	V
EW_o	I_{EWo_lkg}	EW output leakage current	V_{EWo} = 5 V			1	µA

Table 8. Enable

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_n	V_{En_low}	E_n input low voltage				1	V
E_n	V_{En_high}	E_n input high voltage		3			V
E_n	V_{En_hyst}	E_n input hysteresis			500		mV
E_n	$I_{\_leak}$	Pull-down current	V_{En} = 5 V		1.8	10	µA

2.4 Electrical characteristics curves

Figure 3. Output voltage vs. T_j

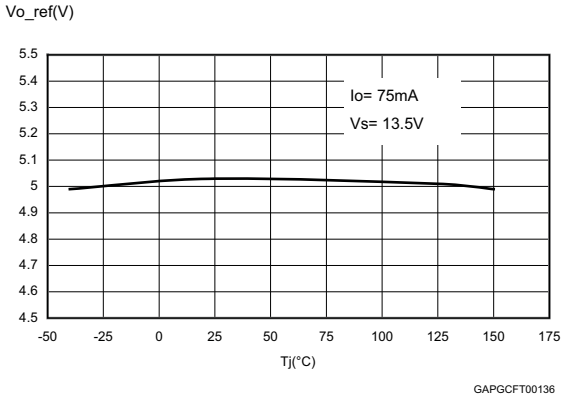


Figure 4. Output voltage vs. V_S

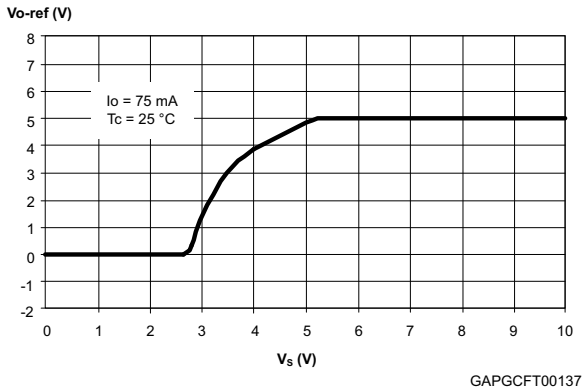


Figure 5. Output voltage vs. V_{En}

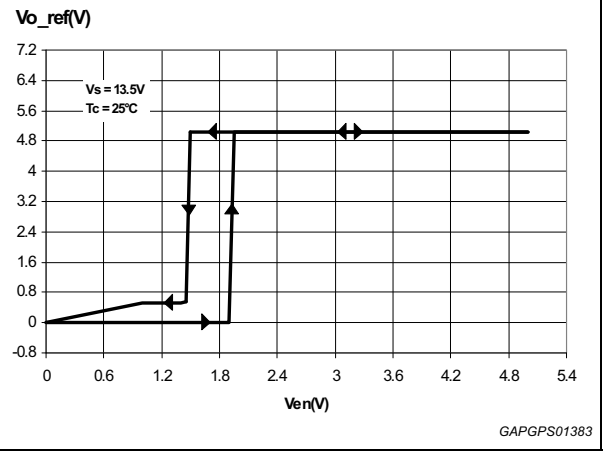


Figure 6. Drop voltage vs. output current

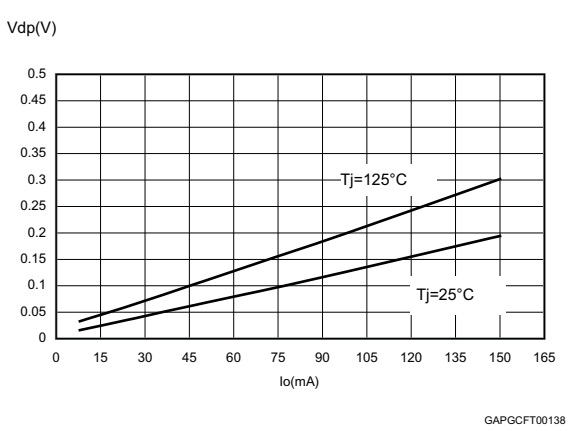


Figure 7. Current consumption vs. output current

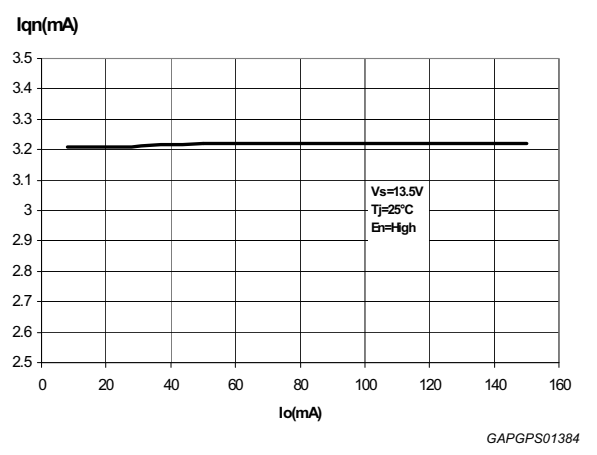


Figure 8. Current consumption vs. output current (at light load condition)

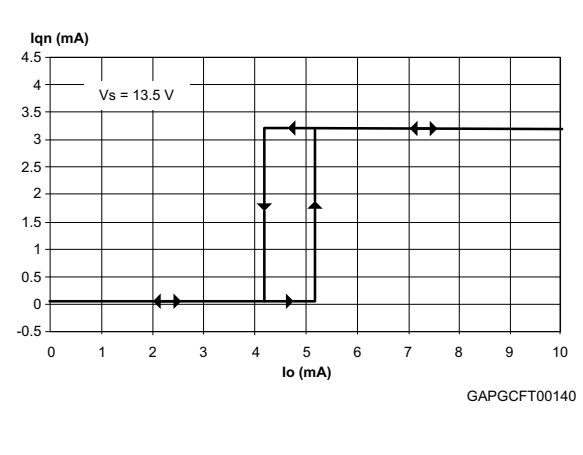


Figure 9. Current consumption vs. input voltage (Io = 0.1 mA)

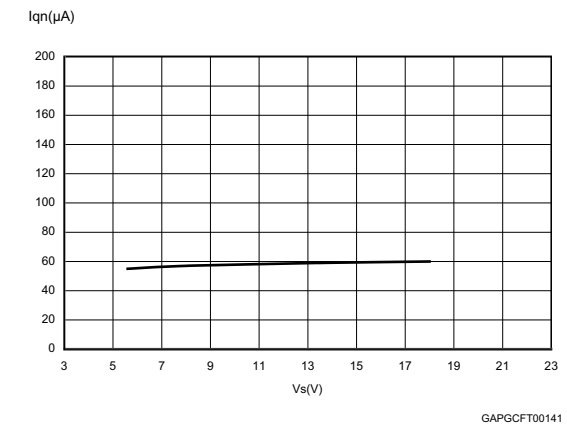


Figure 10. Current consumption vs. input voltage (Io = 75 mA)

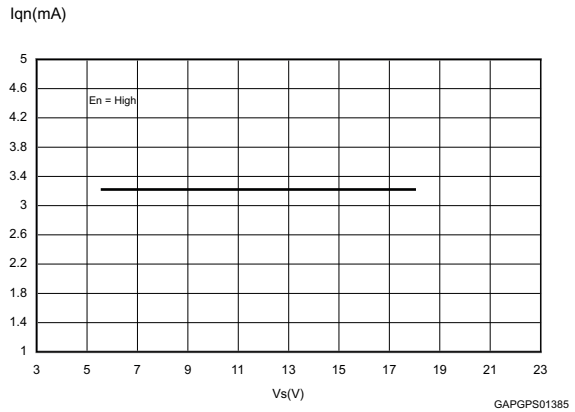


Figure 11. Current limitation vs. T_j

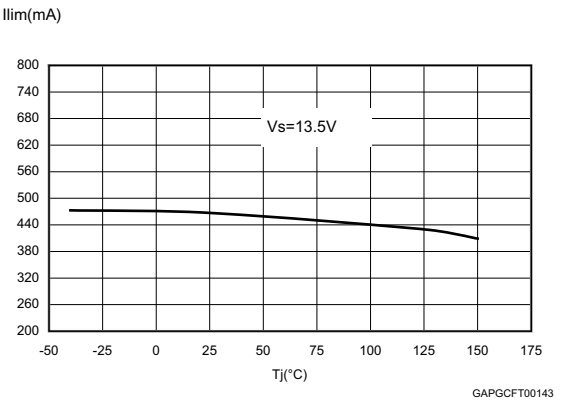


Figure 12. Current limitation vs. input voltage

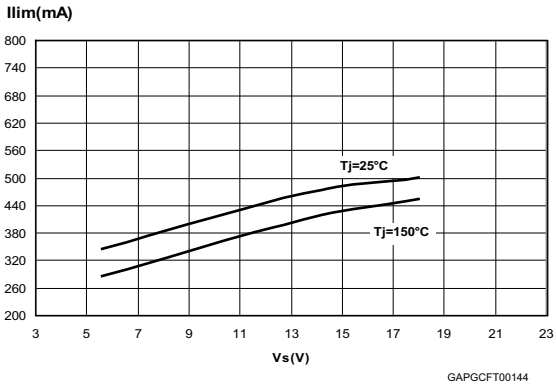


Figure 13. Short-circuit current vs. T_j

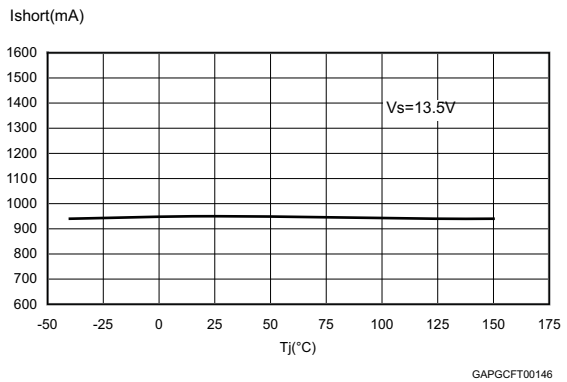


Figure 14. Short-circuit current vs. input voltage

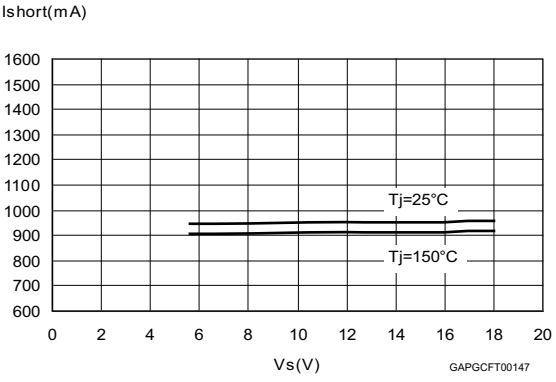


Figure 15. V_{En_high} vs. T_j

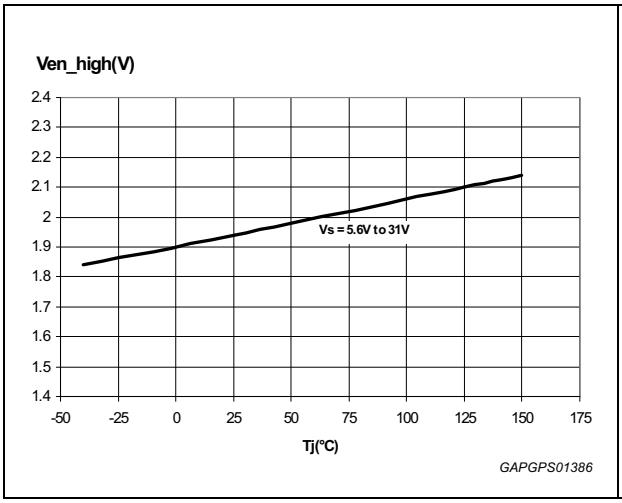


Figure 16. V_{En_low} vs. T_j

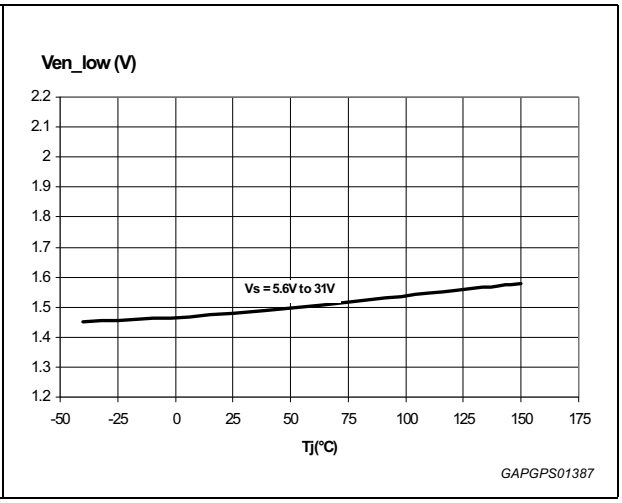


Figure 17. V_{Rhth} vs. T_j

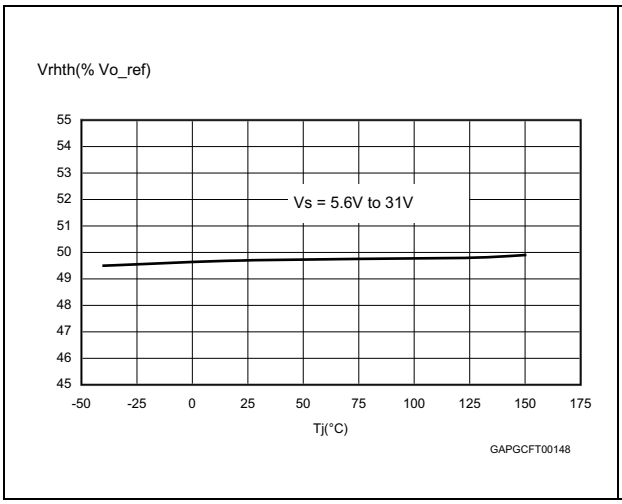


Figure 18. V_{Rlth} vs. T_j

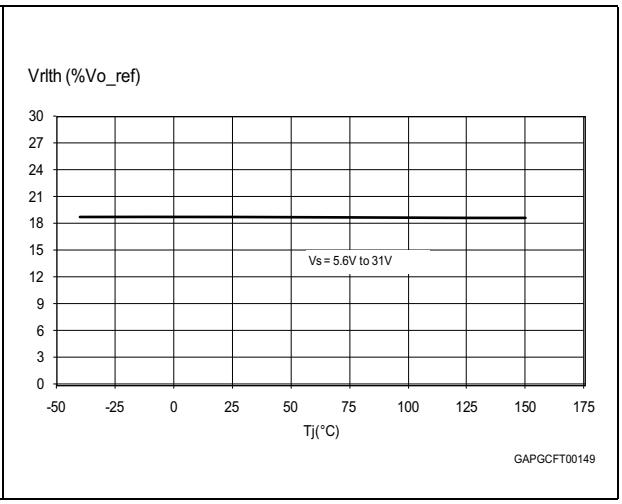


Figure 19. V_{EWi_thh} vs. T_j

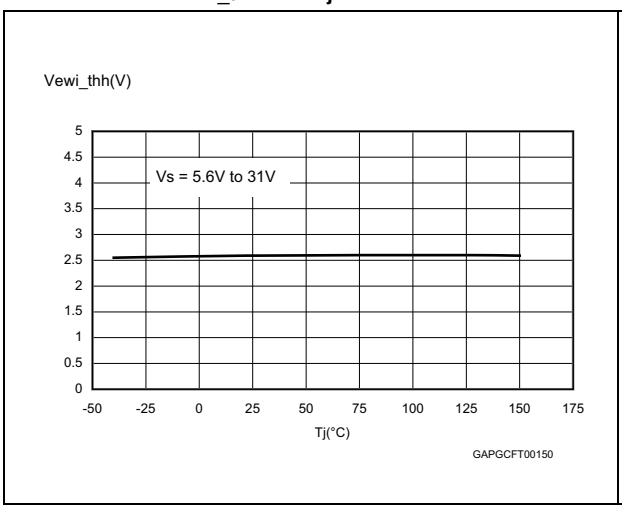


Figure 20. V_{EWi_thl} vs. T_j

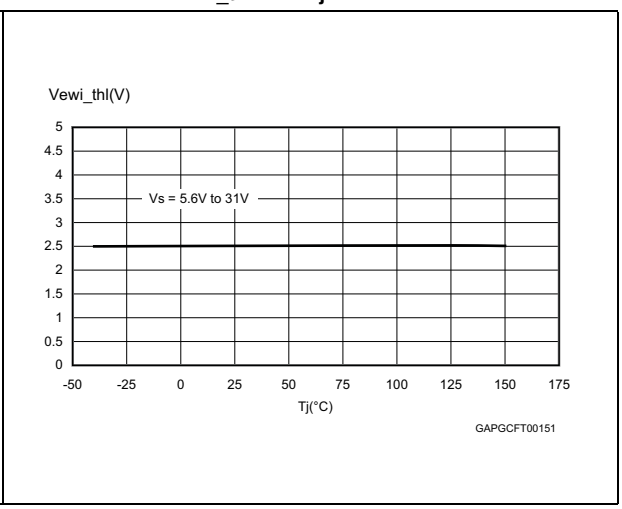


Figure 21. I_{cr} vs. T_j

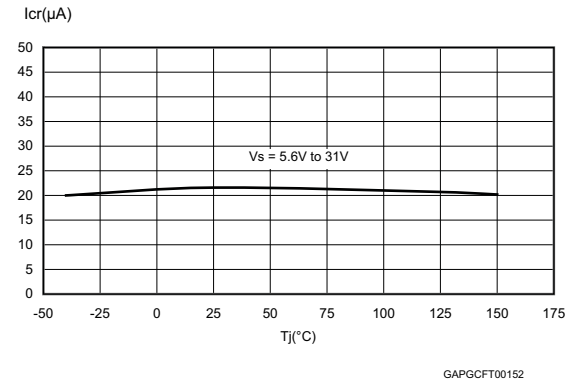


Figure 22. I_{dr} vs. T_j

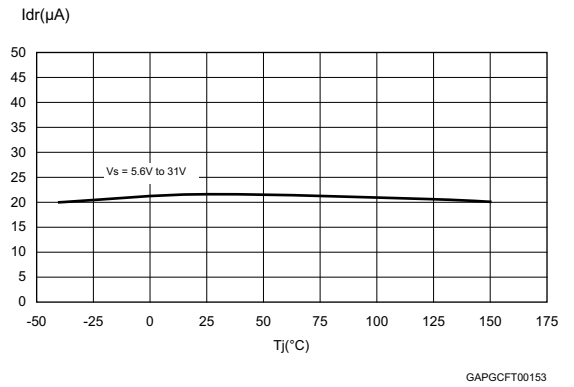
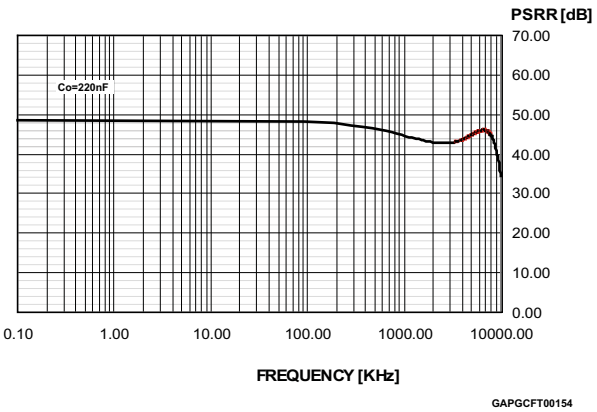


Figure 23. PSRR

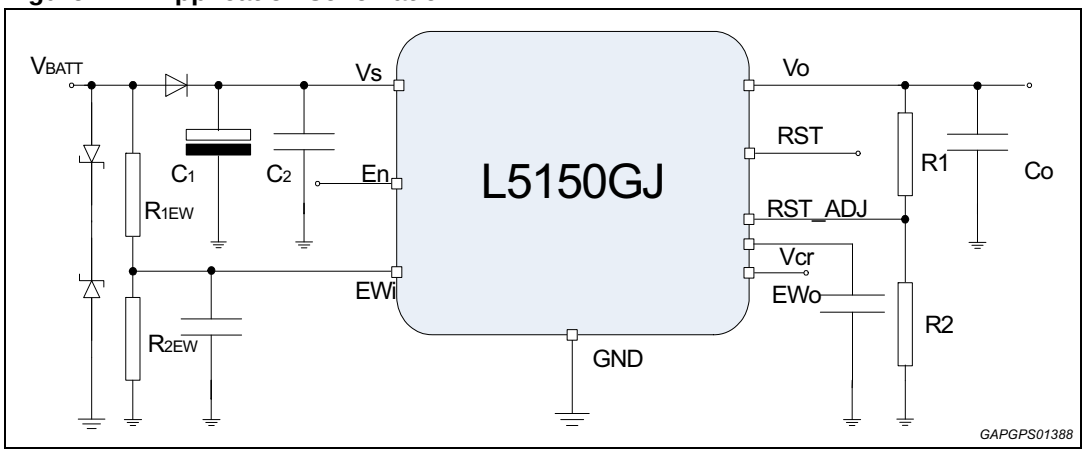


3 Application information

3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to 55 µA only (low consumption mode). This procedure features a certain hysteresis on the output current (see *Figure 8*). Short-circuit protection to GND and a thermal shutdown are provided.

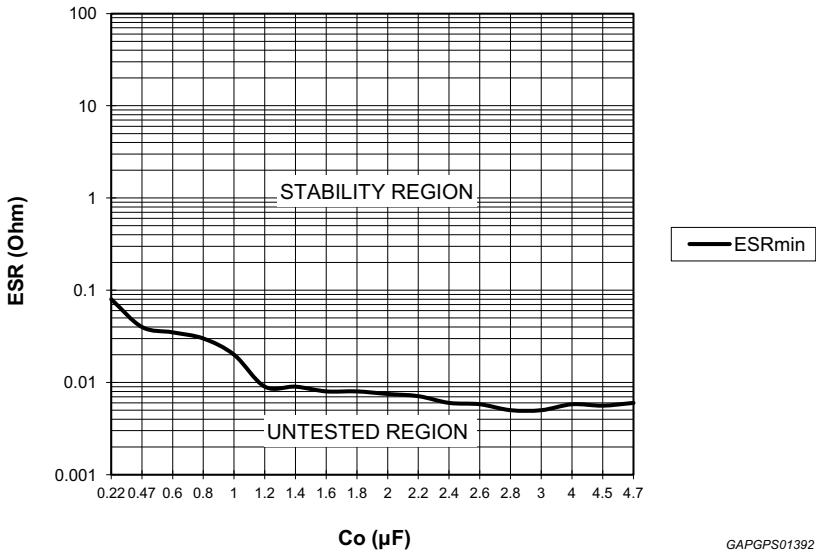
Figure 24. Application schematic



The input capacitor $C_1 \geq 100$ µF is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor $C_2 \geq 220$ nF is needed when the C_1 is too distant from the V_S pin and it compensates smooth line disturbances. The C_0 ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is $C_0 = 220$ nF?with $ESR \geq 100$ mΩ.

Stability region is reported in *Figure 25*.

Figure 25. Stability region



Note: The curve which describes the minimum ESR is derived from characterization data on the regulator with connected ceramic capacitors which feature low ESR values (at 100 kHz). Any capacitor with further lower ESR than the given plot value must be evaluated in each and every case.

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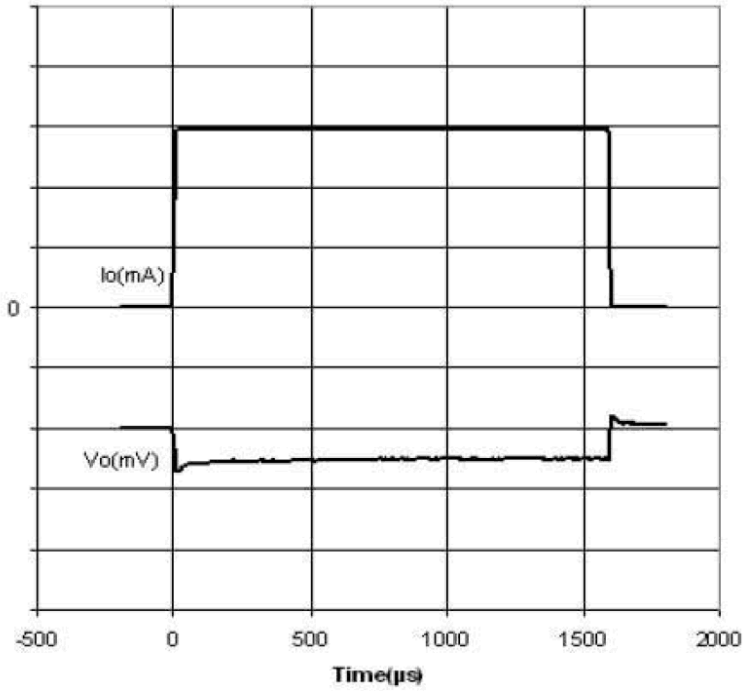
Figure 26. Maximum load variation response



V_o = 50 mV/div
I_o = 50 mA/div

V_S = 13.5 V
I_o = 8 to 150 mA
T_c = 25 °C
C_o = 220 nF

3.2 Reset

The reset circuit monitors the output voltage V_o. If the output voltage becomes lower than V_{o_th} then R_{es} goes low with a delay time (t_{rr}). When the output voltage becomes higher than V_{o_th} then R_{es} goes high with a delay time t_{rd}. This delay is obtained by 32 periods of oscillator.

The oscillator period is given by:

Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

I_{cr} = 20 µA is an internally generated charge current,

I_{dr} = 20 µA is an internally generated discharge current,

V_{Rhth} = 2.5 V (typ) and **V_{Rlth}** = 0.9 V (typ) are two voltage thresholds,

C_{tr} is an external capacitor put between V_{cr} pin and GND.

Reset pulse delay T_{rd} is given by:

Equation 2

$$t_{rd} = 32 \times T_{osc}$$

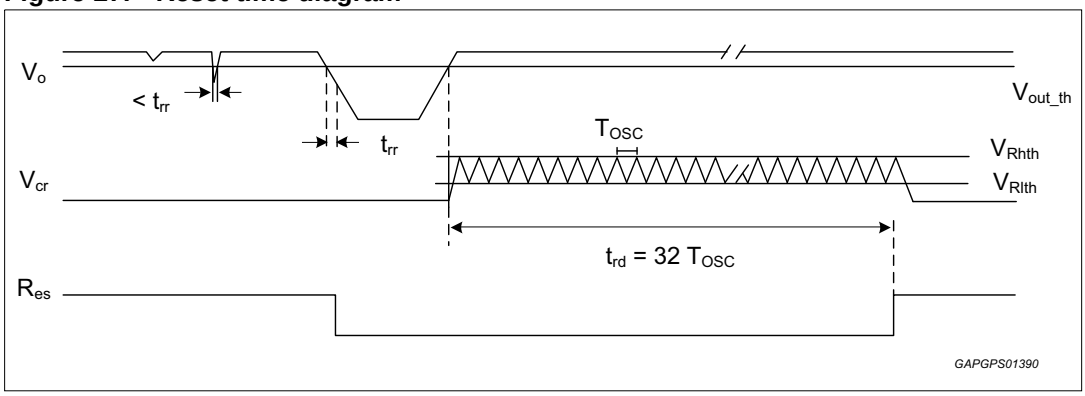
The Output Voltage Reset threshold can be adjusted via an external voltage divider $R_1 + R_2$ (R_1 connected between R_{es_Adj} and V_0, R_2 connected between R_{es_Adj} and GND) according to the following formula:

Equation 3

$$V_{thre} = [(R_1 + R_2) / R_2] * V_{Res\_adj}$$

The Output Voltage Reset threshold can be decreased down to 3.5 V. If it is needed to maintain it to its default value (8% below V_{o_ref} typical), it is enough to connect the R_{es_Adj} pin directly to GND.

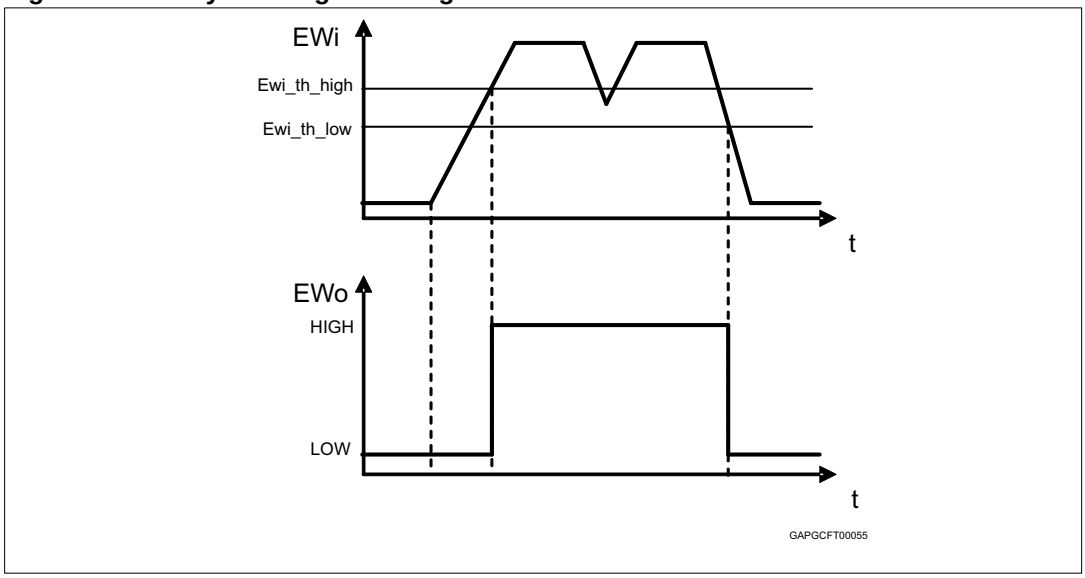
Figure 27. Reset time diagram



3.3 Early warning

This circuit compares the EW_i input signal with the internal voltage reference (typically 2.5 V). The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the supply input voltage either before or after the protection diode and to give additional information to the microprocessor such as low voltage warnings.

Figure 28. Early warning time diagram



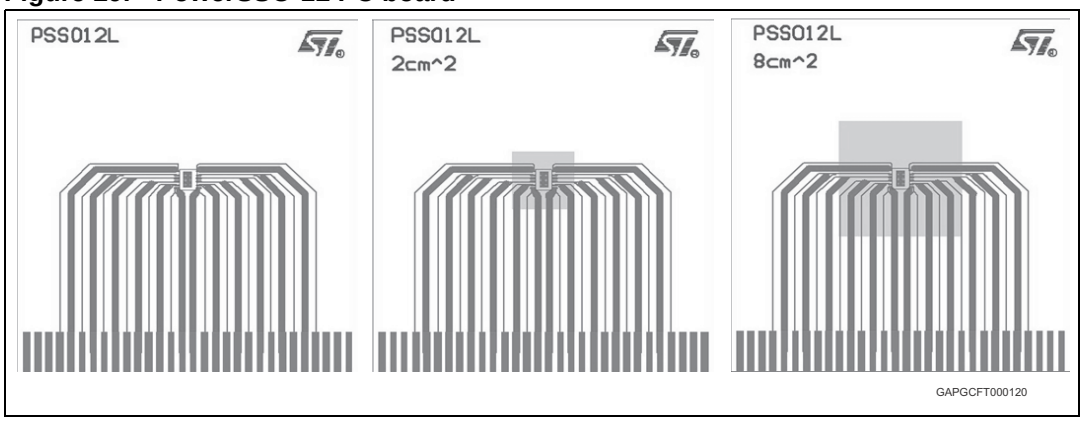
3.4 Enable

L5150GJ is also provided with an enable input, an high signal switches the regulator on. When the enable pin is set to low the output is switched-off and the current consumption of the device is 5 µA typical.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 29. PowerSSO-12 PC board



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness =1.6 mm, Cu thickness = 70 µm (front and back side) thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25 µm, footprint dimension 4.1 mm x 6.5 mm).

Figure 30. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition

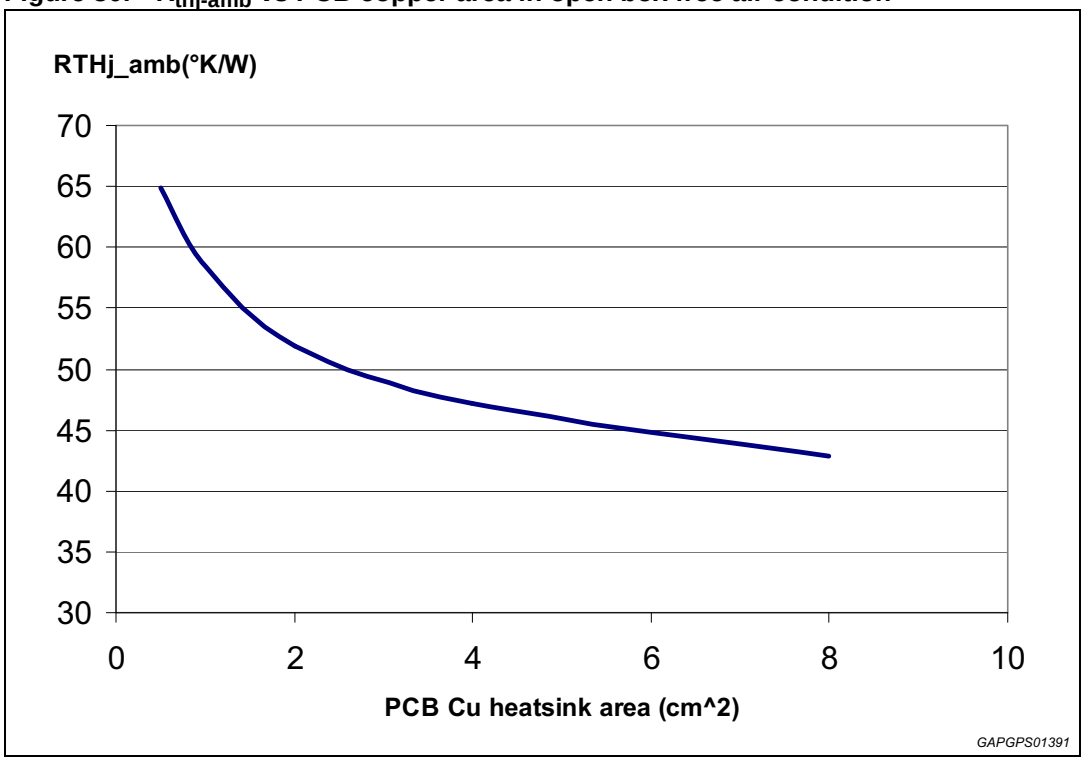
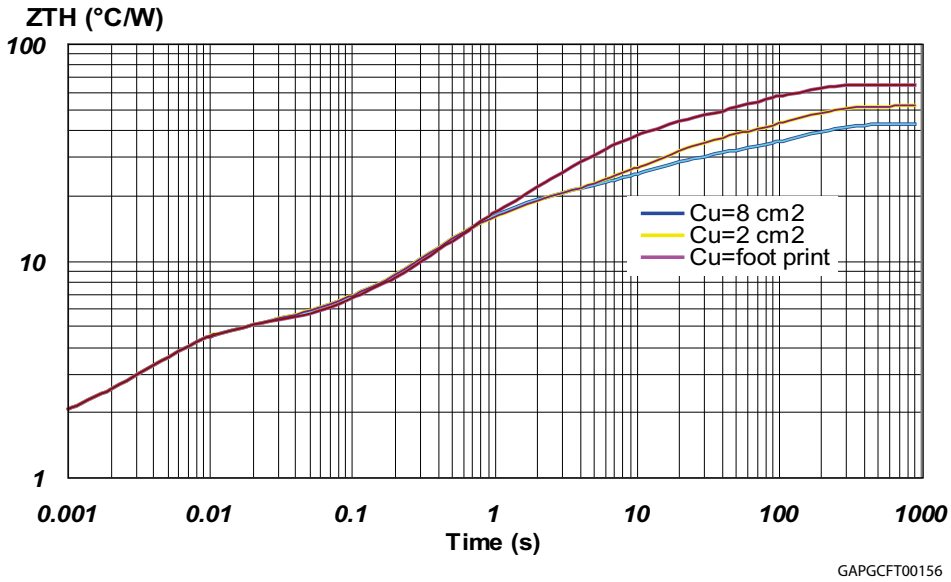


Figure 31. PowerSSO-12 thermal impedance junction ambient single pulse



Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 32. Thermal fitting model of Vreg in PowerSSO-12

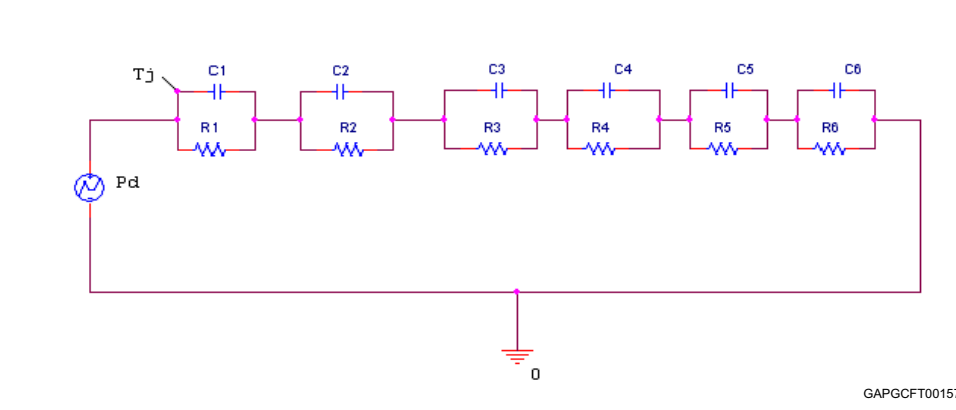


Table 9. PowerSSO-12 thermal parameter

Area (cm^2)	Footprint	2	8
R1 (°K/W)	1.53		
R2 (°K/W)	3.21		
R3 (°K/W)	5.2		
R4 (°K/W)	7	7	8
R5 (°K/W)	22	15	10
R6 (°K/W)	26	20	15
C1 (W.s/°K)	0.00004		
C2 (W.s/°K)	0.0016		
C3 (W.s/°K)	0.08		
C4 (W.s/°K)	0.2	0.1	0.1
C5 (W.s/°K)	0.27	0.8	1
C6 (W.s/°K)	3	6	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.2 PowerSSO-12 mechanical data

Figure 33. PowerSSO-12 package dimensions

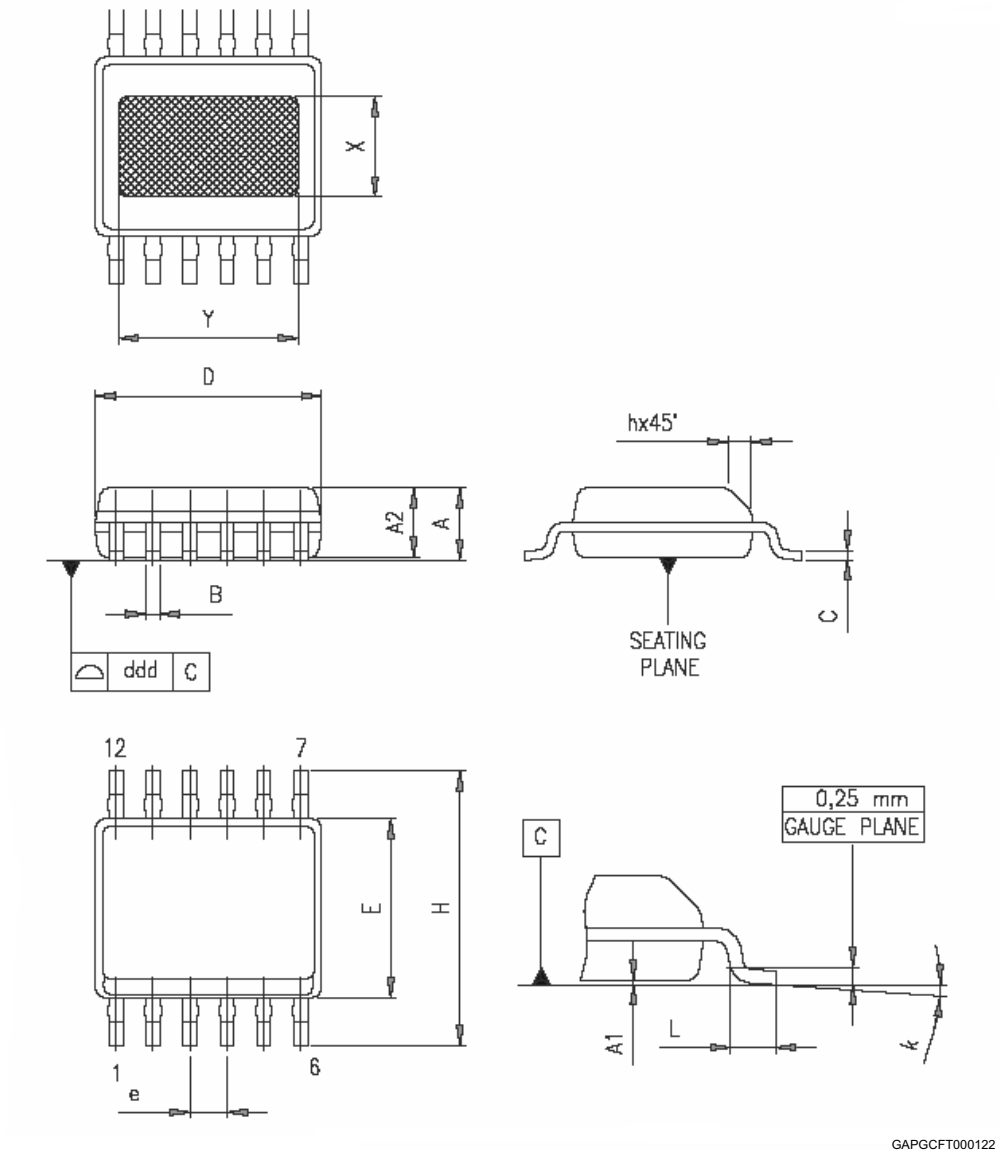
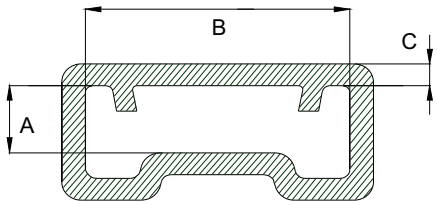


Table 10. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100

5.3 PowerSSO-12 packing information

Figure 34. PowerSSO-12 tube shipment (no suffix)



Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

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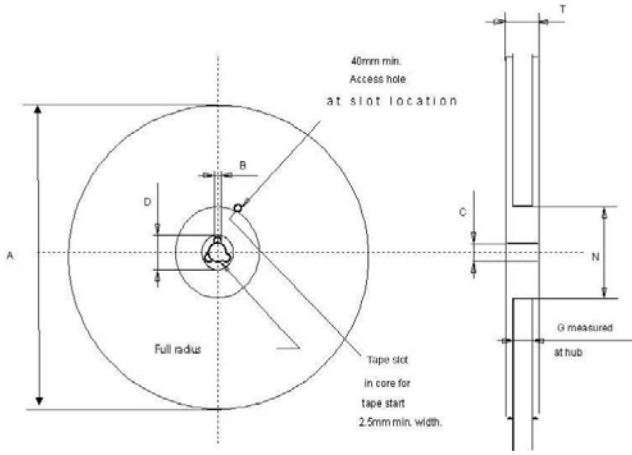
Figure 35. PowerSSO-12 tape and reel shipment (suffix "TR")



Reel dimensions

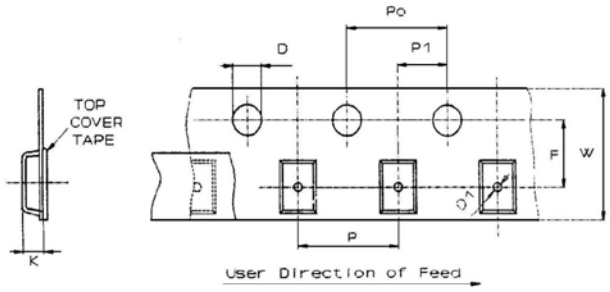
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

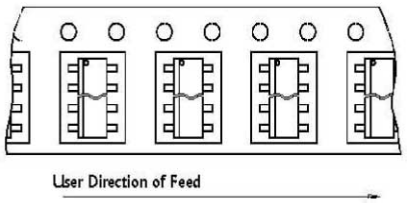
Tape dimensions

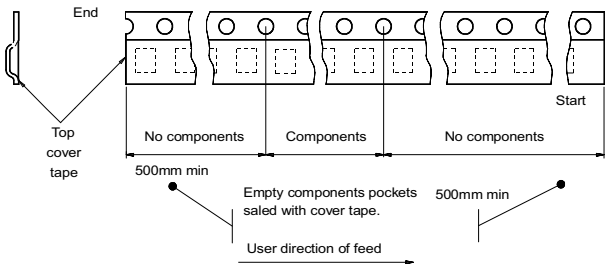
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.05)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.1)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2

All dimensions are in mm.







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6 Revision history

Table 11. Document revision history

Date	Revision	Changes
09-Aug-2007	1	Initial release.
06-Mar-2008	2	Modified *Description* on cover page. Updated *Table 5.: General*: – changed V_{o_ref}, Vline, Vload test conditions – added notes to Ilim and Vdp parameters – added I_{oth_H}, I_{oth_L}, I_{oth} parameters. Updated *Table 6.: Reset*: – added V_{Res_adj} parameter – changed V_{Rlth} values (min./ typ./ max.) from 17/20/23 to 20/23/26 (% V_{o_ref}). Updated *Table 8.: Enable*: – changed V_{En_hyst} typ. value from 800 mV to 500 mV – changed $I_{\_leak}$ typ. value from 3 µA to 1.8 µA. Modified *Section 3.2: Reset*.
09-May-2008	3	Updated *Table 5.: General* : – changed I_{lim} values (Min./Typ./Max.) from 0.7/1/1.30 A to 280/470/660 mA. – V_{o_ref} parameter : updated Io test condition Old -> I_o= 0.1 mA to I0mA New -> I_o= 0.1 mA to 8 mA.
13-Oct-2008	4	Updated *Table 5.: General* : – Vload parameter : updated I_o test condition Old -> I_o= 5 mA to I50 mA New -> I_o= 8 mA to 150 mA

Table 11. Document revision history (continued)

Date	Revision	Changes
15-Apr-2009	5	Updated corporate template Updated *Figure 2: Configuration diagram (top view)* *Table 2: Pins description* – Added new row *Table 4: Thermal data* – $R_{thj-amb}$: changed value – Updated TableFootnote *Table 5: General* – V_{load}: changed max value for Vs = 8 V to 18 V, added new row – I_{qn_1}: changed Test conditions (added T_j = 25 °C), added new row *Table 6: Reset* – V_{Rlth}: changed min/typ/max value – V_{Res_adjl}: replaced with V_{Rlth}, changed Parameter *Table 7: Early warning* – Updated symbols Added *Figure 3: Output voltage vs. T_j* Added *Figure 4: Output voltage vs. V_S* Added *Figure 5: Output voltage vs. V_{En}* Added *Figure 6: Drop voltage vs. output current* Added *Figure 7: Current consumption vs. output current* Added *Figure 8: Current consumption vs. output current (at light load condition)* Added *Figure 9: Current consumption vs. input voltage (Io = 0.1 mA)* Added *Figure 10: Current consumption vs. input voltage (Io = 75 mA)* Added *Figure 11: Current limitation vs. T_j* Added *Figure 12: Current limitation vs. input voltage* Added *Figure 13: Short-circuit current vs. T_j* Added *Figure 14: Short-circuit current vs. input voltage* Added *Figure 15: V_{En_high} vs. T_j* Added *Figure 16: V_{En_low} vs. T_j* Added *Figure 17: V_{Rhth} vs. T_j* Added *Figure 18: V_{Rlth} vs. T_j* Added *Figure 19: V_{EWi_thh} vs. T_j* Added *Figure 20: V_{EWi_thl} vs. T_j* Added *Figure 21: I_{cr} vs. T_j* Added *Figure 22: I_{dr} vs. T_j* Added *Figure 23: PSRR* *Section 3.1: Voltage regulator* – Updated text – Added *Figure 24: Application schematic* – Added *Figure 26: Maximum load variation response* *Section 3.2: Reset* – V_{Rlth}: changed value from 1.15 V to 0.9 V in *Equation 1* Updated *Section 3.4: Enable* Added *Section 4: Package and PCB thermal data* Changed *Section 5.1: ECOPACK®*

Table 11. Document revision history (continued)

Date	Revision	Changes
09-Jun-2009	6	Changed document title *Table 5: General* – I_{oth_H}, I_{oth_L}: added test condition Updated *Figure 4: Output voltage vs. V_S* *Section 3.3: Early warning* – changed internal voltage reference typical value from 1.23 V to 2.5 V Updated *Figure 31: PowerSSO-12 thermal impedance junction ambient single pulse*
04-Dec-2009	7	Updated features list. Updated *Table 2: Pins description*. Updated *Section 3.1: Voltage regulator*. Corrected *Equation 3* on *Section 3.2: Reset*.
19-Apr-2010	8	Updated footnote description of *Table 4: Thermal data*. Updated *Figure 30: Rthj-amb vs PCB copper area in open box free air condition*. Updated *Table 9: PowerSSO-12 thermal parameter*.
30-Jan-2012	9	Updated *Figure 25: Stability region on page 16*.
07-Feb-2012	10	Modified *Figure 25: Stability region on page 16*.
02-Oct-2012	11	Updated *Table 6: Reset*: – T_{rd}: updated maximum value
19-Sep-2013	12	Updated disclaimer.

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