

OCTAL LINE DRIVER

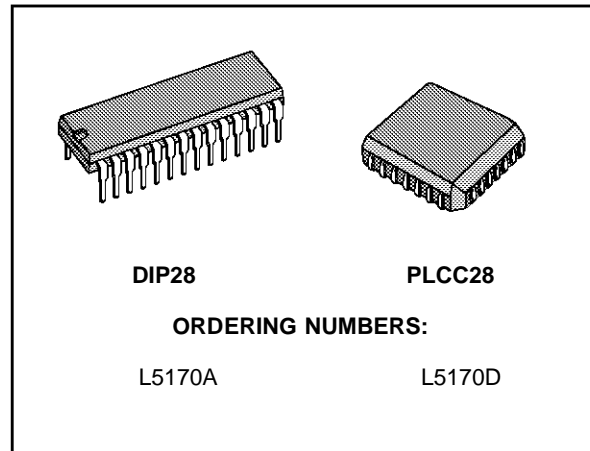
ADVANCE DATA

- OCTAL LINE DRIVER FOR:
 - EIA STD: RS232D; RS423A
 - CCIT: V.10; V.28
- NO EXTERNAL COMPONENTS
- VERY LONG TRANSMISSION LINE (5000ft)
- 50V EOS OUTPUT PROTECTION

DESCRIPTION

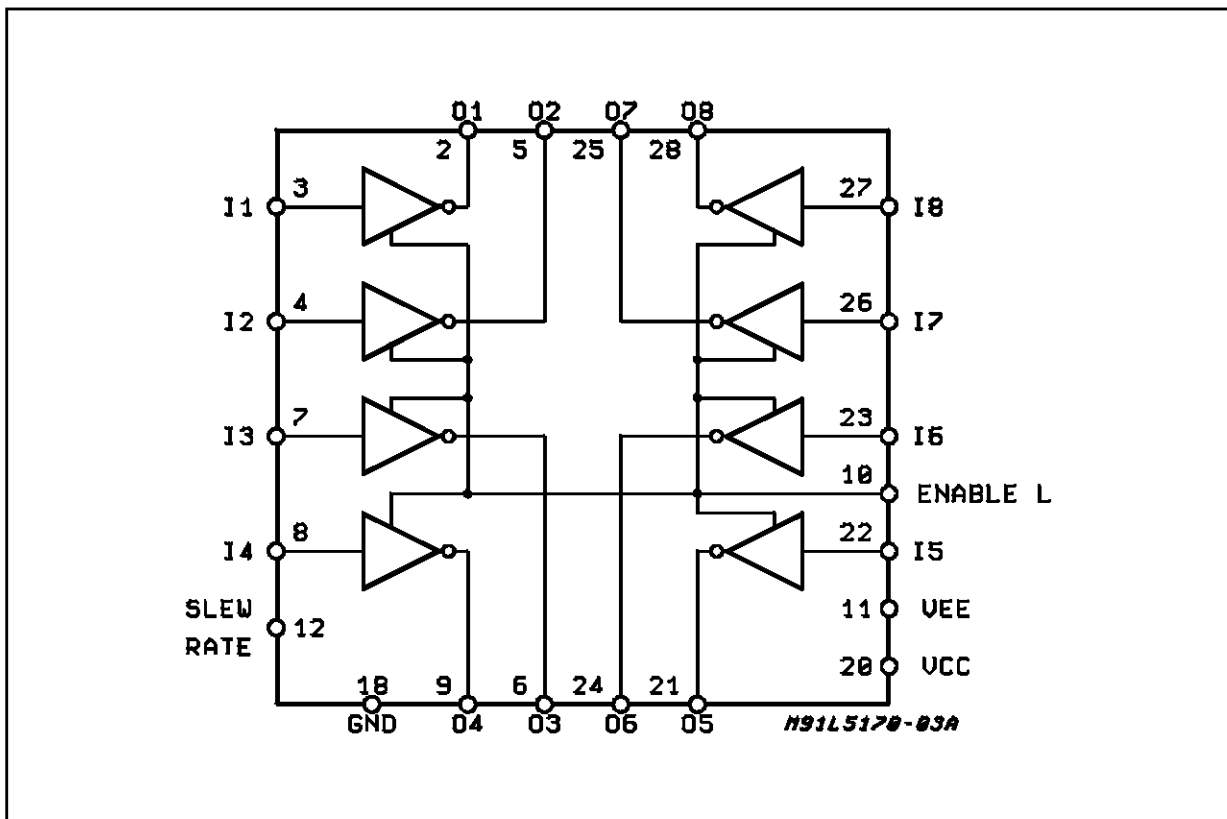
L5170 is an octal line driver unit in DIP28 and PLCC28 packages intended for use in the EIA std RS232D, RS423A and CCITT V.10 and V.28 applications.

With no external components L5170 is able to drive a line up to 5000ft assuming the line capacitance is 35pF per ft and the capacitance of the filter connectors/protection components add up to



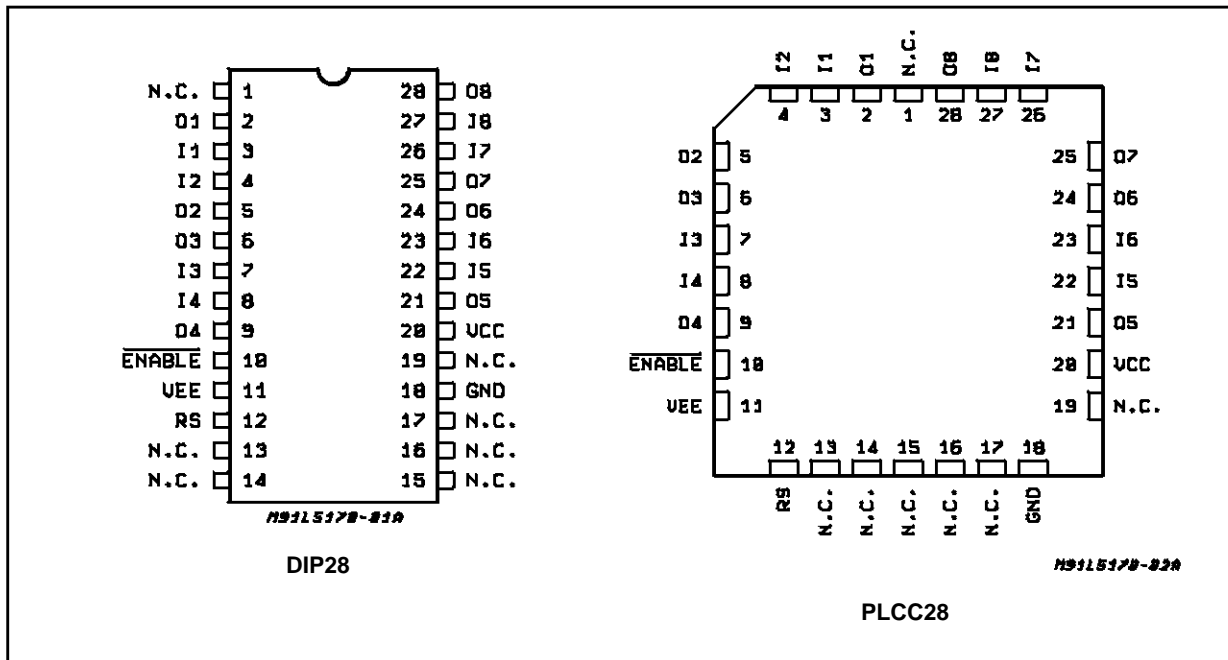
the total capacitance load. The drivers typically run in short circuit current mode whenever the cable attached is over 500ft.

BLOCK DIAGRAM



L5170

PIN CONNECTIONS (Top views)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	+15	V
V _{EE}	Supply Voltage	-15	V
V _i	Input Voltage (Enable Data)	-1.5 to 7	V
V _o	Output Voltage	±6	V
I _o	Output Current (**)	±150	mA
SR	Minimum Slew Resistor (***)	1.5	1KΩ
P _{tot}	Power Dissipation at T _{amb} = 70°C (PLCC28) (*) (DIP28) (*)	1.2 1.3	W
T _{op}	Operating Free Air Temperature Range	0 to +70	°C
T _{stg}	Storage Temperature Range	-65 to 150	°C

Notes:

(*) Mounted on board with minimized dissipating copper area.

(**) Minimum Current per driver. Do not exceed maximum power dissipation if more than one input is on.

(***) Minimum value of the resistor used to set the slew rate.

THERMAL DATA

Symbol	Description	PLCC28	DIP28	Unit
R _{th j-amb}	Thermal Resistance Junction-ambient (*)	Max. 67	62	°C/W

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 9$ to $11V$; $V_{EE} = -9$ to $-11V$ $T_{amb} = 0$ to $70^{\circ}C$, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage	$V_{in} = 0.8V$	5		6	V
		$R_L = \text{inf}$	5		6	V
		$R_L = 3K\Omega$	5		6	V
		$R_L = 450\Omega$ (see note 1)	4.5		6	V
V_{OL}	Low Level Output Voltage	$V_{in} = 2.4V$	-6		-5	V
		$R_L = \text{inf}$	-6		-5	V
		$R_L = 3K\Omega$	-6		-5	V
		$R_L = 450\Omega$ (see note 1)	-6		-4.5	V
V_{OI}	Output Voltage Balance	$ V_{CC} = V_{EE} $; $R_L = 450\Omega$			0.4	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IK}	Input Clamp Voltage	$I_{IN} = -15mA$	-1.5			V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$	-400			μA
I_{CC}	Positive Supply Current	$V_{IN} = 2.4V$; $R_S = 2K\Omega$; $R_L = 3K\Omega$ $C_L = 2.5nF$; (See note 2)			30	mA
I_{CC1}	Positive Supply Current	$V_{IN} = 0.4V$; $R_S = 2K\Omega$; $R_L = 3K\Omega$ $C_L = 2.5nF$; (See note 2)			40	mA
I_{EE}	Negative Supply Current	$V_{IN} = 2.4V$; $R_S = 2K\Omega$; $R_L = 3K\Omega$ $C_L = 2.5nF$; (See note 2)	-30			mA
I_{EE1}	Negative Supply Current	$V_{IN} = 0.4V$; $R_S = 2K\Omega$; $R_L = 3K\Omega$ $C_L = 2.5nF$; (See note 2)	-40			mA
I_{sh}	Output Short Circuit Current	$V_O = 0V$; $V_{IN} = 2.4V$; (see fig.1)	25		100	mA
I_{sl}	Output Short Circuit Current	$V_O = 0V$; $V_{IN} = 2.4V$; (see fig.1)	-100		-25	mA
I_{bal}	Output Current Balance	$I_{sh}/I_{sl} = I_{bal}$	0.625		1.6	mA/mA
I_x	Output Leakage Current	See fig.2,3 and note 3			70	μA
		$V_O = 6V$	-70			μA
		$V_O = -6V$				
t_r	Rise time (see note 4 and 5; see figure 4A)	$R_L = 450\Omega$; $C_L = 50pF$ $R_{slew} = 5.34K\Omega \pm 1\%$	2		2.7	μs
		$R_L = 450\Omega$; $C_L = 0.01\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			10	μs
		$R_L = 450\Omega$; $C_L = 0.1\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			50	μs
		$R_L = 450\Omega$; $C_L = 2.5nF$ $R_{slew} = 2K\Omega \pm 1\%$	0.65		1.2	μs
		$R_L = 450\Omega$; $C_L = 2.5nF$ $R_{slew} = 10K\Omega \pm 1\%$	3.25		6	μs
		$R_L = 450\Omega$; $C_L = 50pF$ $R_{slew} = 5.34K\Omega \pm 1\%$	2		2.7	μs
		$R_L = 450\Omega$; $C_L = 0.01\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			10	μs
		$R_L = 450\Omega$; $C_L = 0.1\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			50	μs
		$R_L = 450\Omega$; $C_L = 2.5nF$ $R_{slew} = 2K\Omega \pm 1\%$	0.65		1.2	μs
t_f	Fall time (see note 4 and 5; see figure 4A)	$R_L = 450\Omega$; $C_L = 50pF$ $R_{slew} = 5.34K\Omega \pm 1\%$	2		2.7	μs
		$R_L = 450\Omega$; $C_L = 0.01\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			10	μs
		$R_L = 450\Omega$; $C_L = 0.1\mu F$ $R_{slew} = 10K\Omega \pm 1\%$			50	μs
		$R_L = 450\Omega$; $C_L = 2.5nF$ $R_{slew} = 2K\Omega \pm 1\%$	0.65		1.2	μs
		$R_L = 450\Omega$; $C_L = 2.5nF$ $R_{slew} = 10K\Omega \pm 1\%$	3.25		6	μs

Note 1: The Output under load must not drop below 90% of the open circuit drive level.

Note 2: This represents the static condition only. Applications can see 130mA normal current draw for clock and data lines with up to 500mA transients when all lines are transitioning at the same time. Over 500ft of cable slew rate is governed by the drivers ability to sink current. The currents are roughly equivalent to the short circuit current.

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{lz}	Output Enable to Output (see figure 4B)	$R_L = 450\Omega$; $C_L = 50pF$ $R_{slew} = 10K\Omega$			5	μs
t_{nz}					5	μs
t_{zl}					150	μs
t_{zh}					150	μs
t_{plh}	Propagation (see figure 4C)	$R_L = 450\Omega$; $C_L = 50pF$ $R_{slew} = 2K\Omega$	0.3		0.9	μs
t_{ph1}			0.3		0.9	μs

LINE TRANSIENT IMMUNITY (Considering the following cases: Powered ON, Powered OFF-Low impedance power supply and Powered OFF-High impedance supply).

ESD	Eletrostatic Discharge	Tested per MIL-STD-883 (see note 6)	2			KV
EOS	Electrical Overstress	Transient pulse both polarities for 100 μs (see note 7)	50			V

Note 3: The output leakage is measured under the following conditions:

- a) The Driver tristated
- b) Power supply OFF, and the power pins shorted to Ground
- c) Power supply OFF. Impedances between power pins open and power pins shorted to Ground.

Note 4: The output waveform should not show any signs of oscillations under any load variation between 0.1V_{SS} and 0.9V_{SS}. The oscillation allowed when V_{SS} < 0.1V_{SS} and V_{SS} > 0.9V_{SS} shall be 10% of V_{SS}.

Note 5: t_{c1} thru t_{c4} shall be within $\pm 20\%$ of t_{c1} thru t_{c4} respectively.

Note 6: All pins are required to withstand parameter.

Note 7: Output pins are required to withstand fig.5 without any degradation to the circuit.

TEST CIRCUIT

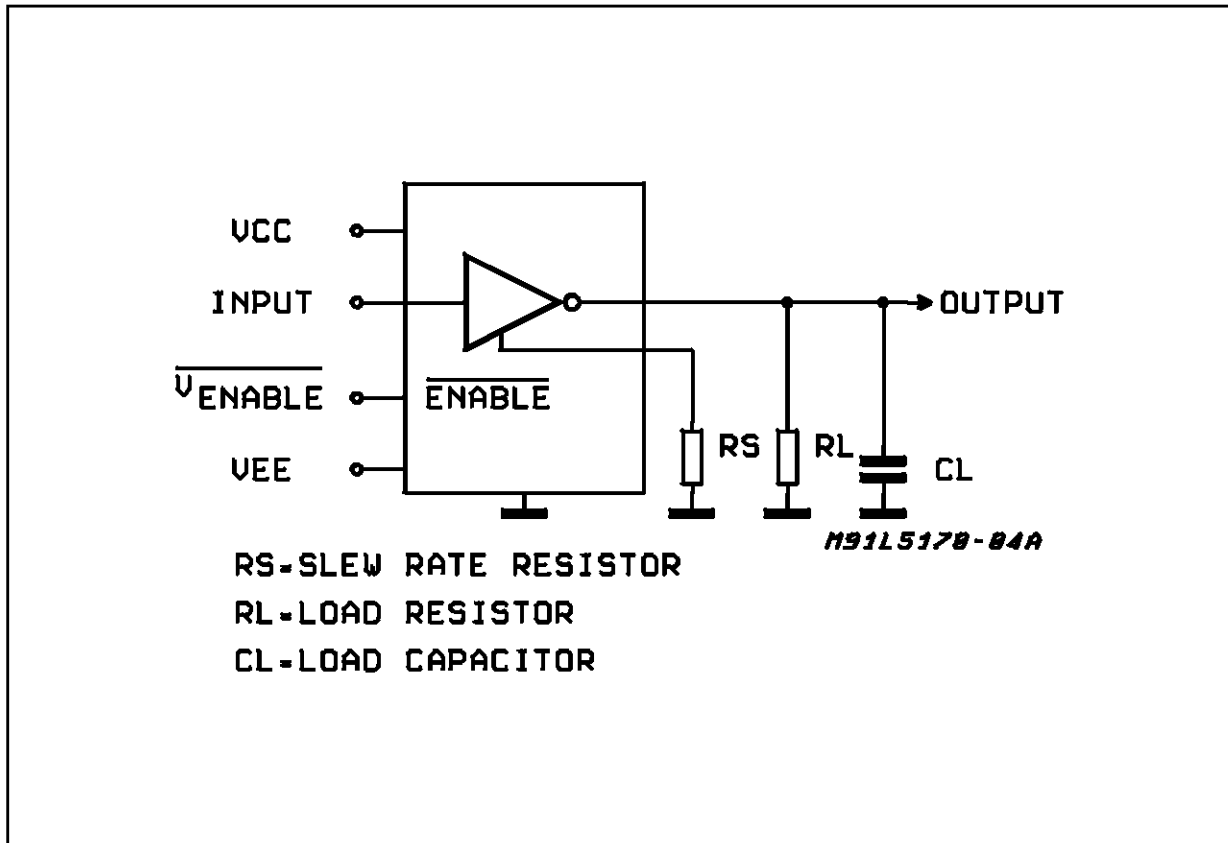


Figure 1: Output Leakage Test Circuit

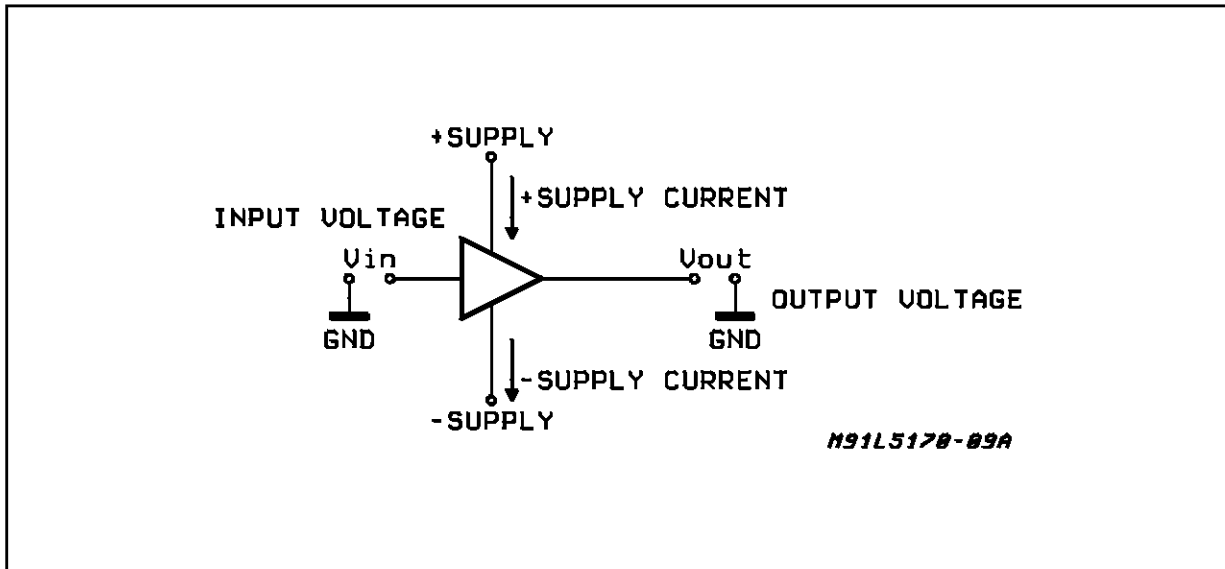


Figure 2: Output Voltage Rise Time

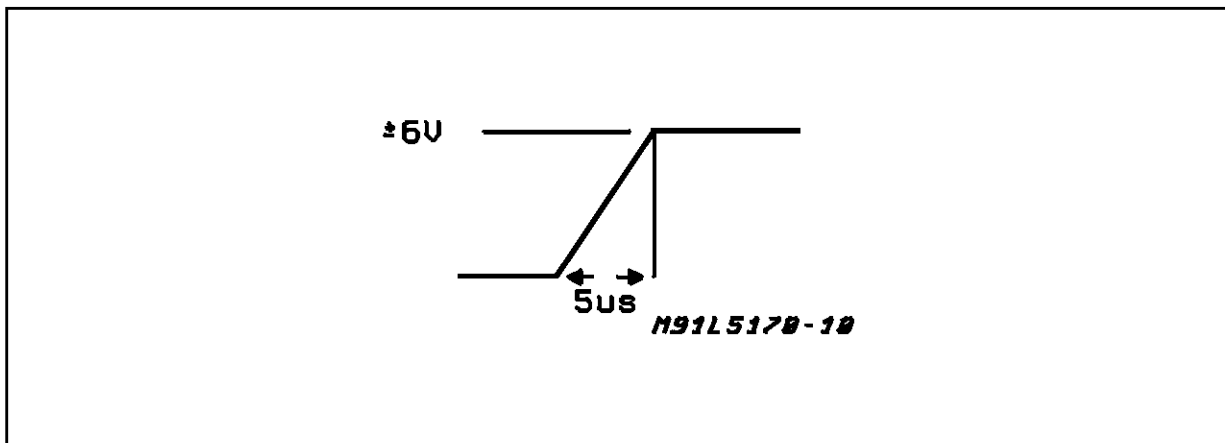


Figure 3: EOS Requirements

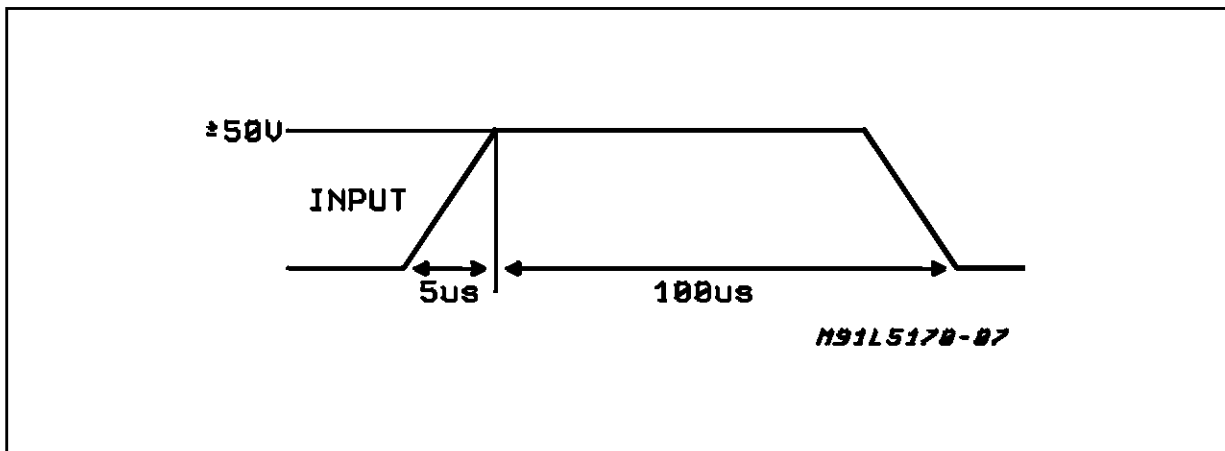
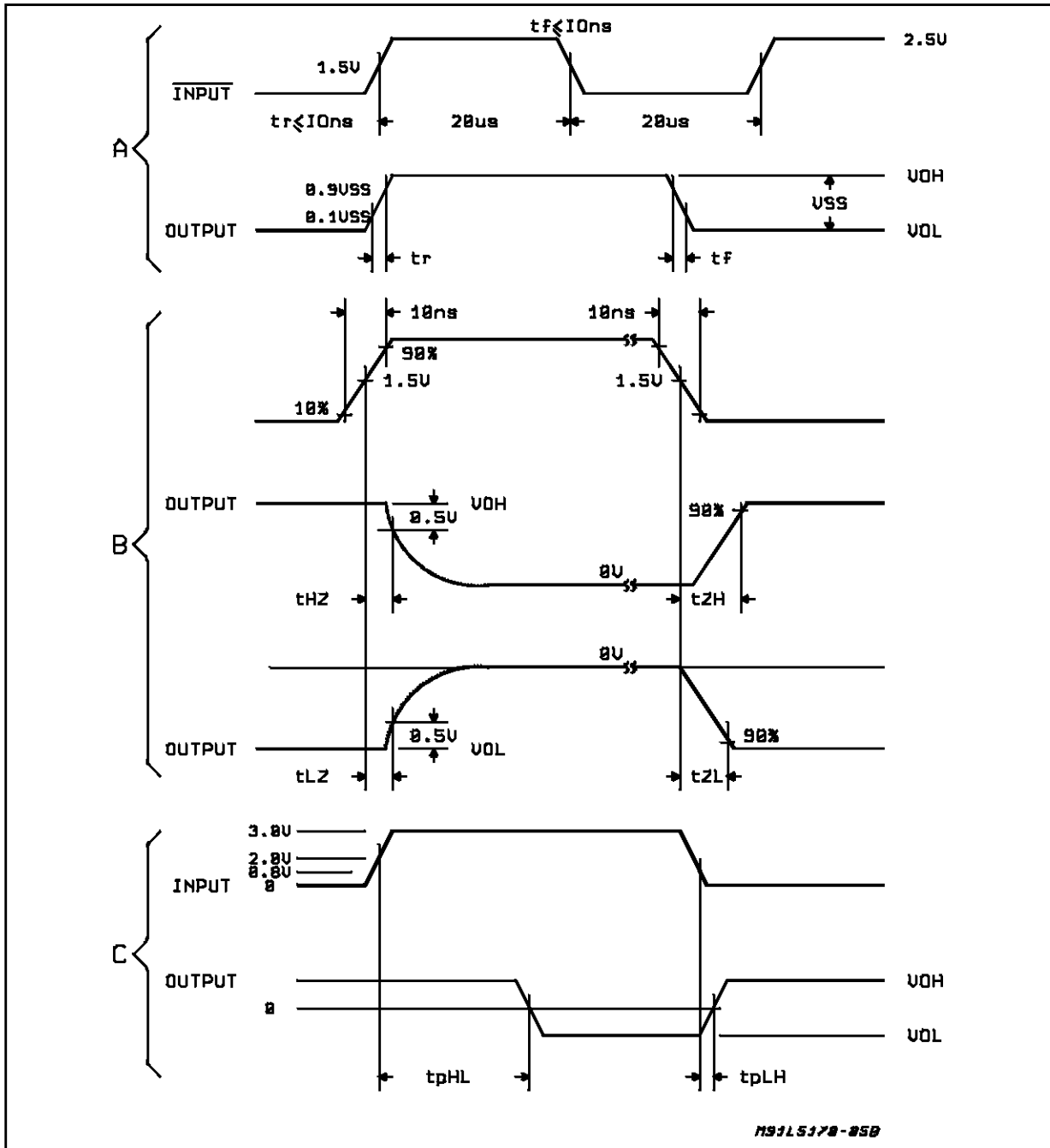
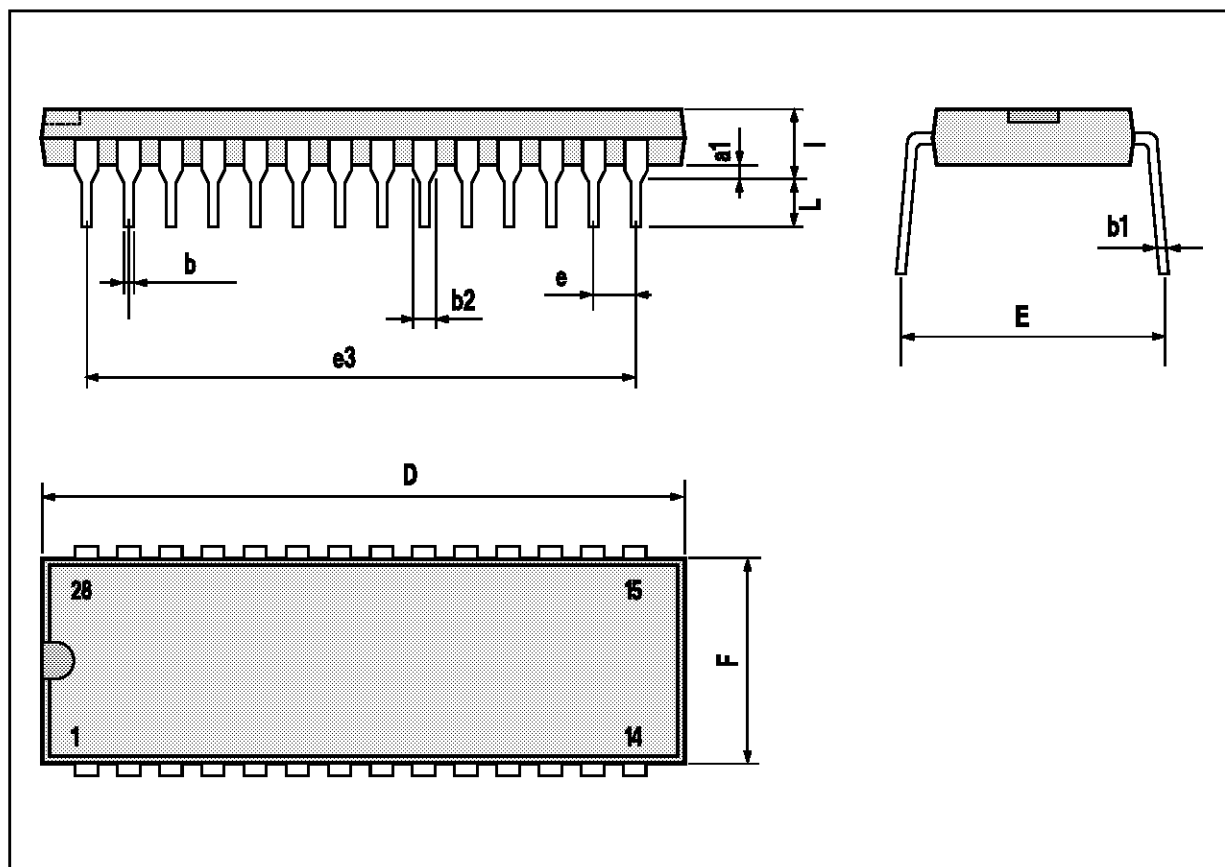


Figure 4: Waveforms



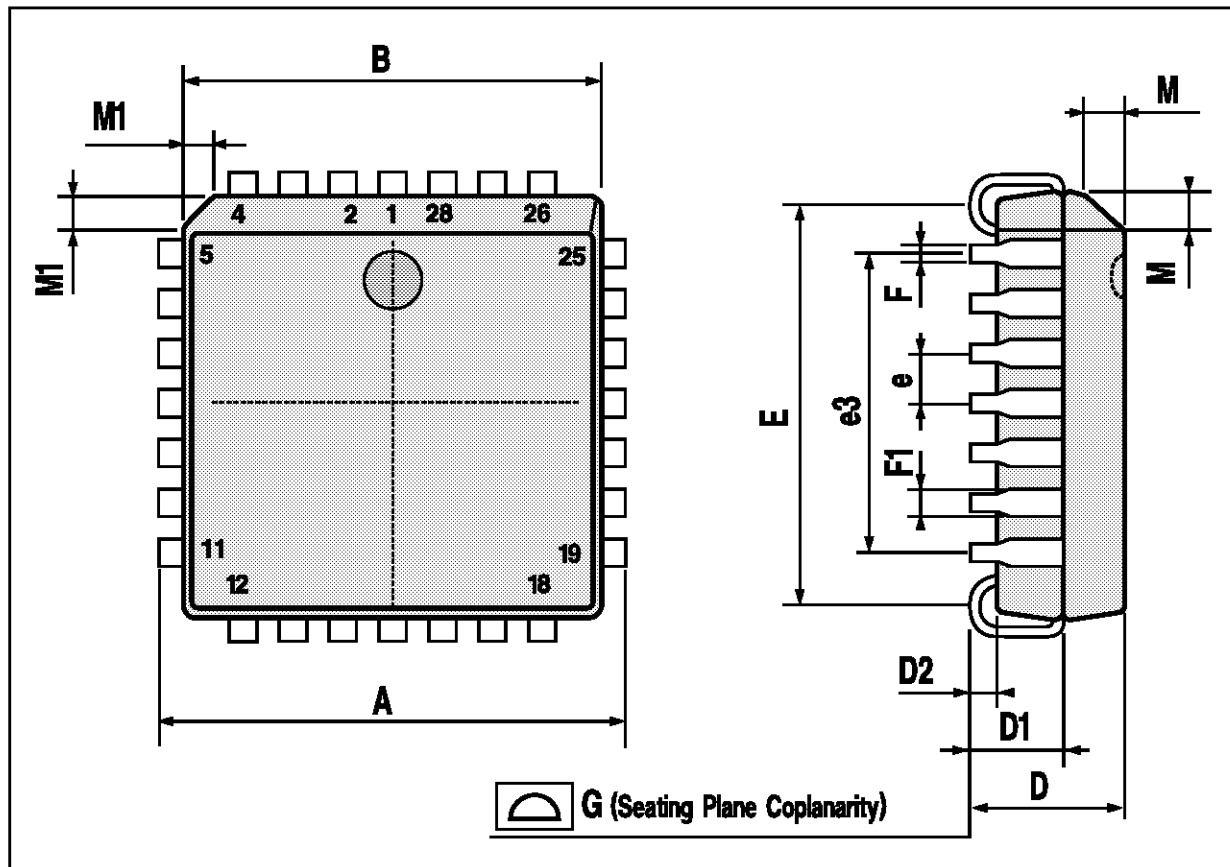
DIP28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			37.34			1.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		33.02			1.300	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



PLCC28 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	



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