



LA5312V

## Variable Divided Voltage Generator for LCDs

## Overview

The LA5312V is a variable divided voltage generator IC for multiple drive of LCD matrix.

## Features

- Power supply for variable bias LCD drive (1/5 to 1/19 bias available by internal resistors)
- Four voltage outputs generated by four operational amplifiers.
- Low current drain (0.18 mA typ.)
- Miniflat package for miniaturization.

## Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{EE \text{ max}}$	$V_{CC} - V_{EE}$	36	V
Maximum output current	$I_{OUT \text{ max}}$	V1 - V4	*Internal	mA
Allowable power dissipation	$P_d \text{ max}$		330	mW
Operating temperature	$T_{opr}$		-20 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-30 to +125	$^\circ\text{C}$

Note 1: Continuous operation (without damage) is guaranteed in the above ranges.

Note 2: \*The maximum output current is the value stipulated under the test conditions on page 4.

Note 3: Output pins V1 to V4-to- $V_{CC}$  or GND short not exceeding 1 ms is acceptable. ( $|V_{CC} - V_{EE}| < 35 \text{ V}$ )

Operating Conditions at  $T_a = 25^\circ\text{C}$ 

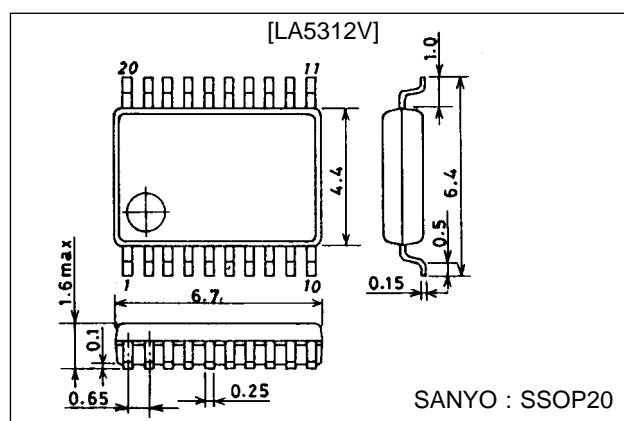
Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{EE}$	$V_{CC} - V_{EE}$	-35.5 to -6	V
Input voltage	$V_{REF}$	$V_{REF} \cong V_{EE} : V_{CC} - V_{REF}$	-35 to -6	V
Output current	$I_{OUT1,2}$	V1, V2	-0.5 to +5	mA
	$I_{OUT3,4}$	V3, V4	-10 to +5	mA

Note 4: Set  $V_{CC}$  and  $V_{EE}$  so that  $|V1|$  and  $|V_{EE} - V4|$  are 1 V or more.

## Package Dimensions

unit : mm

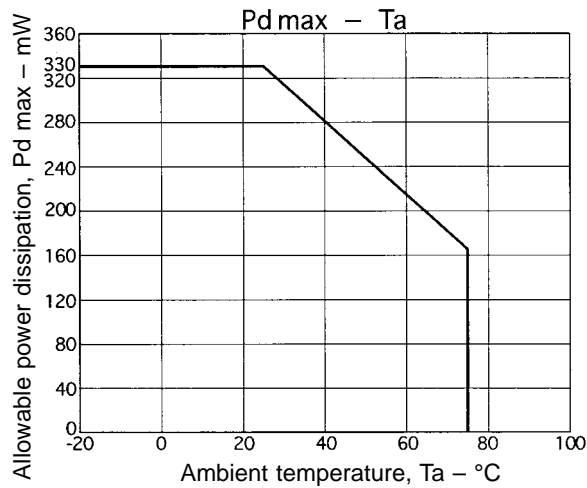
## 3179-SSOP20



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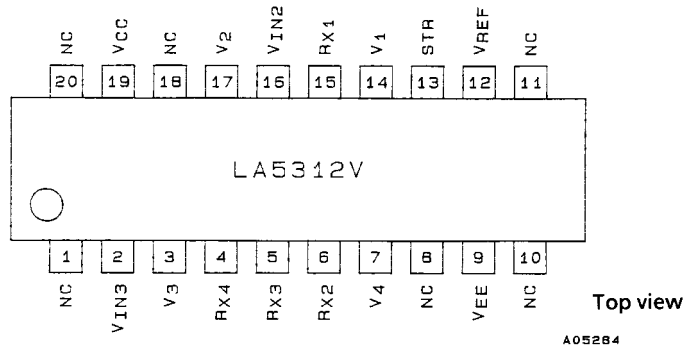
**Operating Characteristics at Ta = 25°C, V<sub>CC</sub> - V<sub>EE</sub> = 20 V, V<sub>REF</sub> = V<sub>EE</sub>, R<sub>X</sub> = 8 R**

Parameter	Symbol	Conditions	min	typ	max	Unit
Current drain	I <sub>CC</sub> , I <sub>EE</sub>	STR = 5 V : V <sub>CC</sub> , V <sub>EE</sub>		0.18	0.3	mA
Input current	I <sub>STR</sub>	STR = 5 V : STR		9	12	μA
Output voltage ratio	Ra1	V2 / V1	1.96	2.00	2.04	—
	Ra2	(V <sub>REF</sub> - V3) / (V <sub>REF</sub> - V4)	1.96	2.00	2.04	—
	Rb1	V <sub>REF</sub> / V1	11.64	12.00	12.36	—
	Rb2	V <sub>REF</sub> / V2	5.82	6.00	6.18	—
	Rb3	V <sub>REF</sub> / (V <sub>REF</sub> - V3)	5.82	6.00	6.18	—
Internal resistance ratio	R <sub>X1</sub>	Referenced to R across : R <sub>X1</sub> - R <sub>X2</sub> : R <sub>X1</sub> - R <sub>X3</sub> : R <sub>X1</sub> - R <sub>X4</sub> : R <sub>X1</sub> - V <sub>IN3</sub>		8		—
	R <sub>X2</sub>			12		—
	R <sub>X3</sub>			14		—
	R <sub>X4</sub>			15		—
Resistance value	R	R value when voltage is applied across R <sub>X4</sub> and V <sub>IN3</sub> is 0.5 V : R <sub>X4</sub> - V <sub>IN3</sub>		30		kΩ
Load regulation	ΔV1	+0.1 mA < I <sub>OUT1</sub> < +5 mA : V1			±20	mV
	ΔV2	+0.1 mA < I <sub>OUT2</sub> < +5 mA : V2			±20	mV
	ΔV3	+0.1 mA < I <sub>OUT3</sub> < +5 mA : V3			±20	mV
	ΔV4	+0.1 mA < I <sub>OUT4</sub> < +5 mA : V4			±20	mV
	-ΔV1	-0.5 mA < I <sub>OUT1</sub> < -0.1 mA : V1			±20	mV
	-ΔV2	-0.5 mA < I <sub>OUT2</sub> < -0.1 mA : V2			±20	mV
	-ΔV3	-10 mA < I <sub>OUT3</sub> < -0.1 mA : V3			±20	mV
	-ΔV4	-10 mA < I <sub>OUT4</sub> < -0.1 mA : V4 (Source I <sub>OUT</sub> is negative and sink I <sub>OUT</sub> is positive).			±20	mV

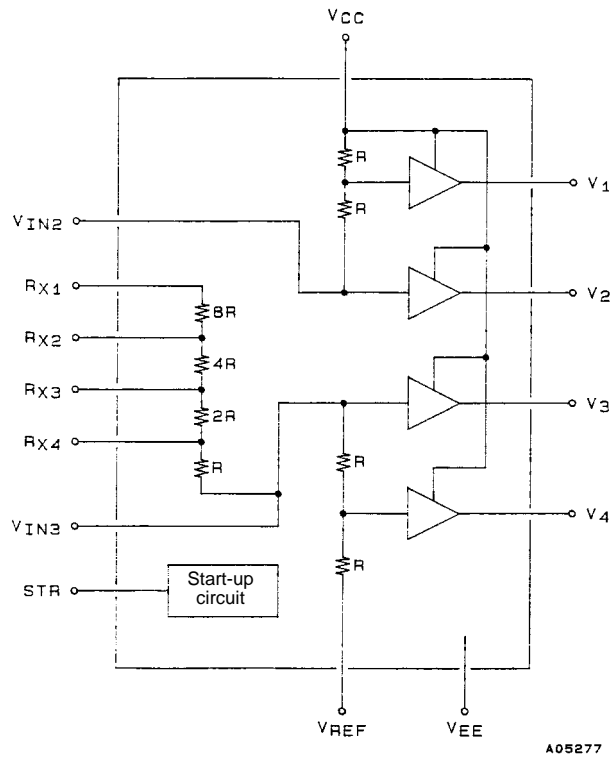


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## Pin Assignment

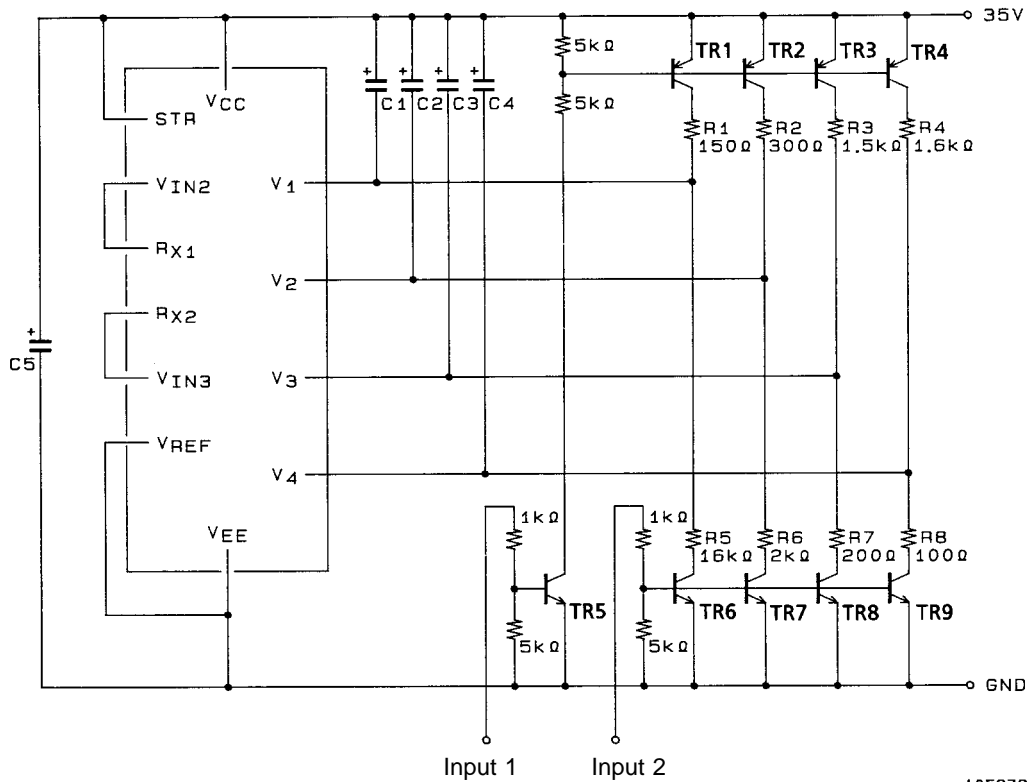


## Block Diagram



(The voltages  $V_{RX1}$ ,  $V_{RX2}$ ,  $V_{RX3}$ , and  $V_{RX4}$  must obey the relationship  $V_{RX1} \geq V_{RX2} \geq V_{RX3} \geq V_{RX4}$ ).

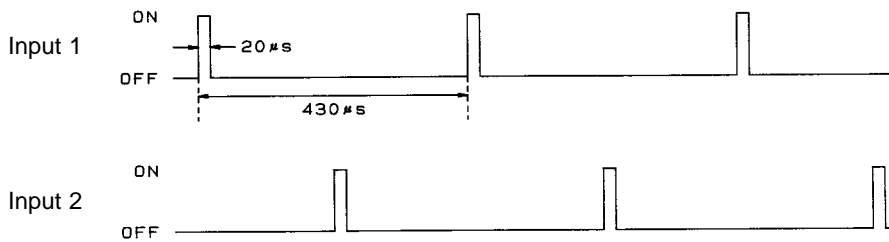
Maximum Output Current Load Test Conditions



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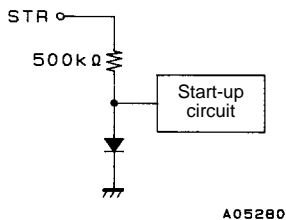
$V_{CC} - V_{EE} = 35\text{ V}$       $R_X = 8 R$       $C1 \text{ to } 4 = 10\ \mu\text{F}$       $C5 = 33\ \mu\text{F}$       $R: 1\text{ W or more}$   
 TR1 to 4: 2SA984     E or F rank  
 TR5 to 9: 2SC2274     E or F rank

The output load resistor values (R1 to R8) are set so that when an “on” level signal is input to inputs 1 and 2, a current of 15 to 30 mA max. flows to the sink side and the source side (approximately 2 mA on the V1 source side).



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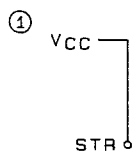
STR Pin Usage



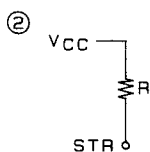
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The STR input is configured as shown left.

- The STR is either shorted with  $V_{CC}$  or connected to  $V_{CC}$  via an external resistor.
- It is possible to use a separate power supply ( $V_{IN}$ ) such that  $2\text{ V} < V_{IN} < V_{CC}$  for current saving.

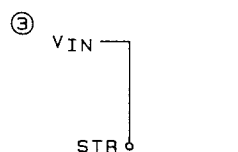


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(2 V or more required for STR)

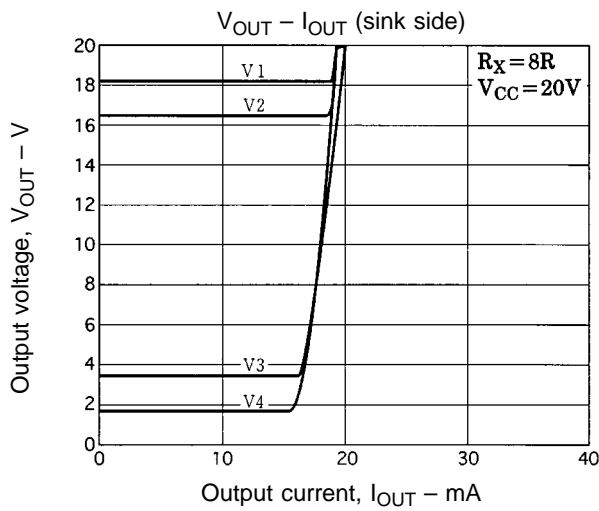
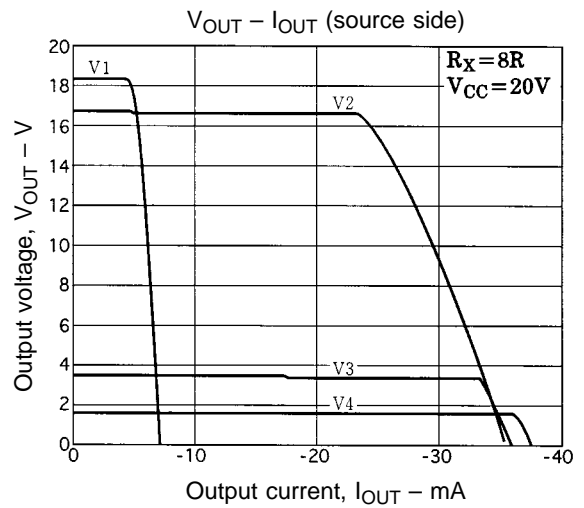
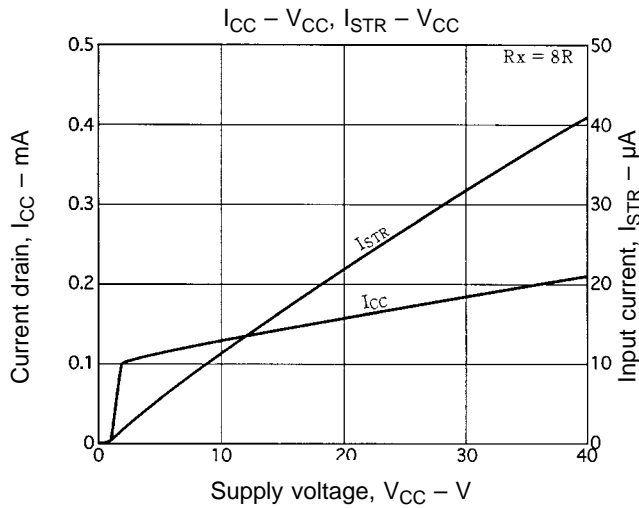
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( $2\text{ V} < V_{IN} < V_{CC}$ )

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