Ordering number : EN5639

Monolithic Linear IC

LA5620

Regulator for Multiple Power Supply Systems

Overview

The LA5620 is a multi-system power supply regulator IC that includes four regulator circuits on chip: two 3.3-V regulator circuits and two 5-V regulator circuits. The LA5620 is optimal for use in audio and video systems that use a microcontroller, such as MD players and stereo components.

Functions and Features

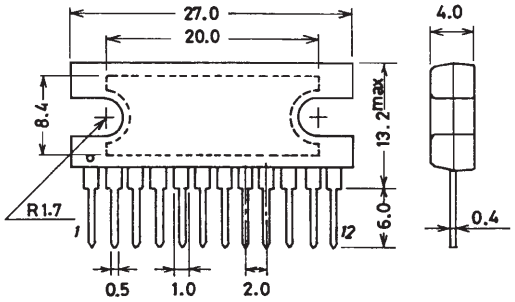
- Two 3.3-V regulator circuits (I_O = 40 mA, 150 mA)
- Two 5-V regulator circuits (I_O = 1000 mA, 100 mA)
- Power on/off detection circuit
- Reset circuit

Package Dimensions

unit: mm

3049A-SIP12H

[LA5620]



SANYO: SIP12H

Specifications

Maximum Ratings at Ta = 25°C

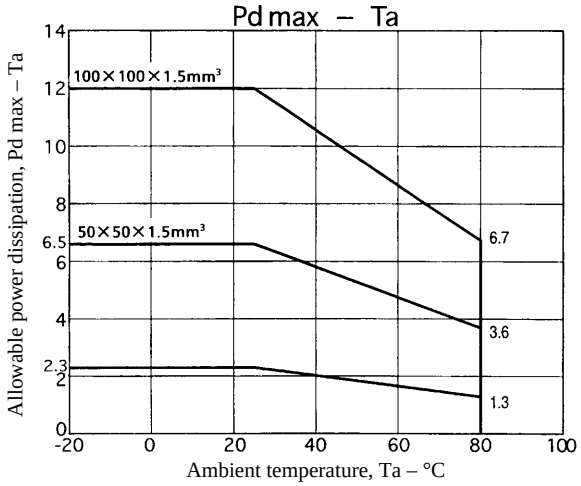
Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{CC} max		14	V
AC input voltage	AC max		2	V
Allowable power dissipation	Pd max	Independent IC	2.3	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

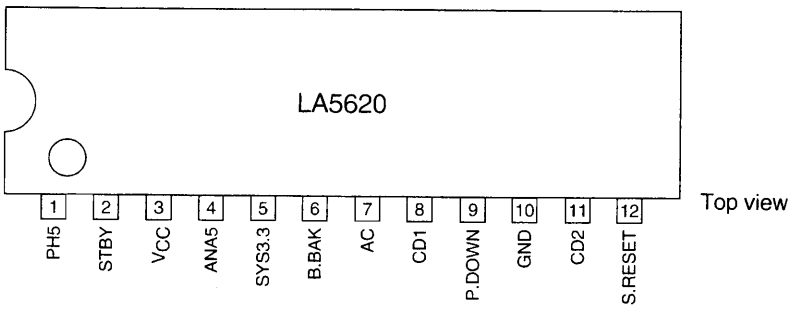
Parameter	Symbol	Conditions	Ratings	Unit
Input voltage	V_{CC}		6.25 to 12	V
PH5 output current	I_{PH5}		0 to 1000	mA
B.BAK output current	$I_{B.BAK}$		0 to 40	mA
ANA5 output current	I_{ANA5}		0 to 100	mA
SYS3.3 output current	$I_{SYS3.3}$		0 to 150	mA
S.RESET sink current	$I_{SINK\ S}$		0 to 1	mA
P.DOWN sink current	$I_{SINK\ P}$		0 to 1	mA
AC input current	I_{AC}		0 to 1	mA

Electrical Characteristics at Ta = 25°C

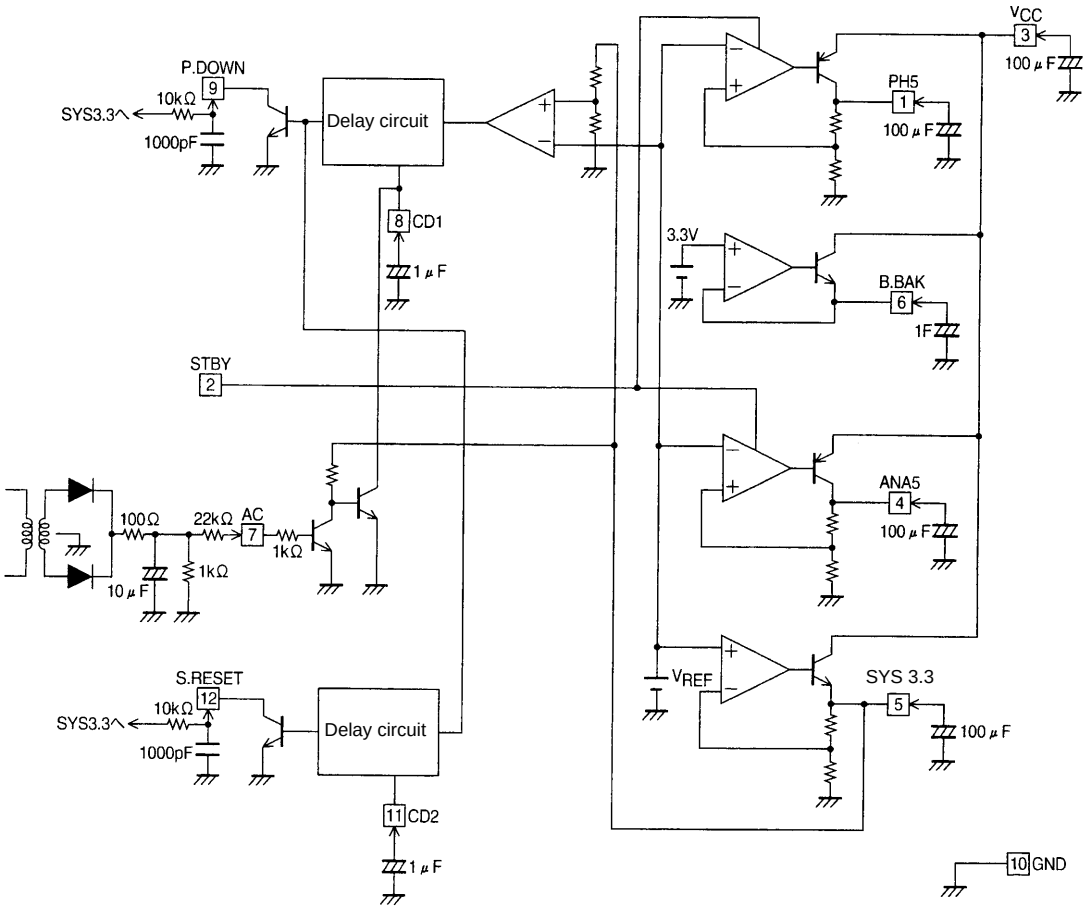
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[PH5 Regulator Block] V_{CC} = 10 V, I_{PH5} = 1 A						
Output voltage	$V_{O\ PH5}$		4.75	5	5.25	V
Dropout voltage	$V_{DROP\ PH5}$		–	0.5	1	V
Line regulation	$\Delta V_{OLN\ PH5}$	V_{CC} = 6.25 to 12 V	–	–	200	mV
Load regulation	$\Delta V_{OLD\ PH5}$	I_{PH5} = 0.5 to 1 A	–	–	200	mV
Peak output current	I_{OP}		1.0	1.4	–	A
Output shorted current	$I_{OSC\ PH5}$		–	400	1000	mA
Current drain	$I_{Q\ PH5}$		–	70	112	mA
[SYS3.3 Regulator Block] V_{CC} = 10 V, $I_{SYS3.3}$ = 150 mA						
Output voltage	$V_{O\ SYS3.3}$		3.13	3.3	3.47	V
Dropout voltage	$V_{DROP\ SYS3.3}$		–	2	2.5	V
Line regulation	$\Delta V_{OLN\ SYS3.3}$	V_{CC} = 6.25 to 12 V	–	–	200	mV
Load regulation	$\Delta V_{OLD\ SYS3.3}$	$I_{SYS3.3}$ = 5 to 150 mA	–	–	200	mV
Peak output current	$I_{OP\ SYS3.3}$		150	210	–	mA
Output shorted current	$I_{OSC\ SYS3.3}$		–	200	450	mA
Current drain	$I_{Q\ SYS3.3}$		–	17.5	28	mA
[ANA5 Regulator Block] V_{CC} = 10 V, I_{ANA5} = 100 mA						
Output voltage	$V_{O\ ANA5}$		4.75	5	5.25	V
Dropout voltage	$V_{DROP\ ANA5}$		–	0.5	1	V
Line regulation	$\Delta V_{OLN\ ANA5}$	V_{CC} = 6.25 to 12 V	–	–	200	mV
Load regulation	$\Delta V_{OLD\ ANA5}$	I_{ANA5} = 5 to 100 mA	–	–	200	mV
Peak output current	$I_{OP\ ANA5}$		100	140	–	mA
Output shorted current	$I_{OSC\ ANA5}$		–	40	100	mA
Current drain	$I_{Q\ ANA5}$		–	17.5	28	mA
[B.BAK Regulator Block] V_{CC} = 10 V, I_{BAK} = 40 mA						
Output voltage	$V_{O\ BAK}$		3.13	3.3	3.47	V
Dropout voltage	$V_{DROP\ BAK}$		–	2	2.5	V
Line regulation	$\Delta V_{OLN\ BAK}$	V_{CC} = 6.25 to 12 V	–	–	200	mV
Load regulation	$\Delta V_{OLD\ BAK}$	I_{BAK} = 5 to 40 mA	–	–	200	mV
Peak output current	$I_{OP\ BAK}$		40	56	–	mA
Output shorted current	$I_{OSC\ BAK}$		–	40	120	mA
Current drain	$I_{Q\ BAK}$		–	15	24	mA
BAK pin input current	$I_{IN\ BAK}$	V_{CC} = 0 V, V_{BAK} = 3.3 V	–	–	100	nA
[P.DOWN Detection Circuit] V_{CC} = 10 V						
P.DOWN threshold voltage	$V_{TH\ P.DOWN}$		3.0	3.16	3.32	V
P.DOWN residual voltage	$Vsat_{\ P.DOWN}$	cd1 pin = shorted, P.DOWN pin = 1 mA	–	–	200	mV
P.DOWN delay time	Td1	cd1 = 1 µF	75	100	125	ms
[S.RESET Detection Circuit] V_{CC} = 10 V						
S.RESET residual voltage	$V_{TH\ S.RESET}$	cd1 pin = shorted, S.RESET pin = 1 mA	–	–	200	mV
S.RESET delay time	Td2	cd2 = 1 µF	75	100	125	ms
[AC Detection Circuit] V_{CC} = 10 V						
AC threshold voltage	$V_{TH\ AC}$		0.5	0.7	0.9	V
[STBY Detection Circuit] V_{CC} = 10 V						
STBY threshold voltage	$V_{TH\ STBY}$		1.3	1.8	2.3	V



Pin Assignment



Block Diagram



Note: Use capacitors with minimal temperature variations for all capacitors in application circuits.

Timing Chart