No. 5630

LA6539M

Three-Channel CD-ROM Bridge Driver (BTL)

Overview

The LA6539M is a three-channel bridge driver (BTL) developed for use in CD-ROM drives.

Functions

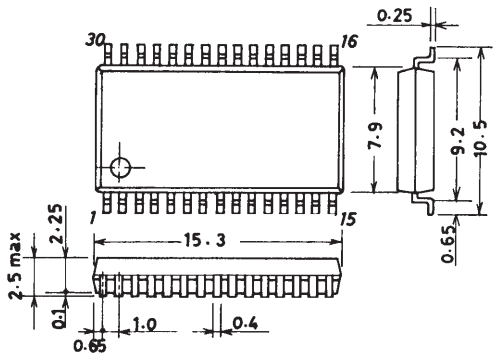
- Three-channel balanced transformerless (BTL) power amplifier
- I_O max: 1 A
- Muting circuit
- Thermal shutdown function
- Slew rate (SR): 0.5 V/μs (typical)

Package Dimensions

unit: mm

3073A-MFP30SLF

[LA6539M]



SANYO: MFP30SLF

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
	V_S max	Maximum rating for V_S1 and V_S2	14	V
Maximum input voltage	V_{IN}	$V_{IN}1$ to $V_{IN}3$	13	V
Mute pin voltage	V_{MUTE}	MUTE1, 2	13	V
Allowable power dissipation	Pd max		0.9	W
Operating temperature	Topr		–20 to +75	°C
Storage temperature	Tstg		–55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		4 to 13	V
Operating voltage 2-1	V_S1	The channel U operating voltage	4 to 13	V
Operating voltage 2-2	V_S2	The channel U and W operating voltage	4 to 13	V

Operating Characteristics at Ta = 25°C, V_{CC} = 12 V, V_S1 = V_S2 = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
V_{CC} no-load current drain	$I_{CC}1$	All outputs on (mute 1 and 2: high) *1, 2	4	8	15	mA
	$I_{CC}2$	All outputs off (mute 1 and 2: low) *1		4	10	mA
V_S1 no-load current drain	I_S1-1	Channel U: on (mute 1: high)		5	10	mA
	I_S1-2	Channel U: off (mute 1: low)			1	mA
V_S2 no-load current drain	I_S2-1	Channels V and W: on (mute 2: high) *2		10	20	mA
	I_S2-2	Channels V and W: off (mute 2: low)			1	mA
Output offset voltage	$V_{OF}1$ to $V_{OF}3$	Voltage differential between the channel U and W outputs	–50		+50	mV
Input voltage range	V_{IN}	Voltage range for $V_{IN}1$ to $V_{IN}3$	0.5		5	V
Buffer amplifier output voltage	$V_{BUFFER}1$	Voltage difference relative to 1/2 V_S1	–50	0	+50	mV
	$V_{BUFFER}2$	Voltage difference relative to 1/2 V_S2	–50	0	+50	mV
Output source voltage	V_O1	Output high, I_O = 700 mA, all + outputs	4.4	4.7		V
Output sink voltage	V_O2	Output low, I_O = 700 mA, all + outputs		0.3	0.6	V
Closed circuit voltage gain	VG	Bridge amplifier		6		dB
Slew rate	SR			0.5		V/μs
Mute on voltage	$V_{MUTE1, 2}$	The voltage applied to MUTE1 or MUTE2 at the point where the output goes on.		1.5	2	V
Mute on current	$I_{MUTE1, 2}$	The influx current to MUTE1 or MUTE2 at the point where the output goes on.		6	10	μA

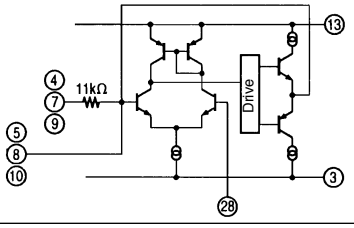
Notes: 1. When MUTE1 is high, the channel U output will be on.
2. When MUTE2 is high, the channel V and W outputs will be on.

Truth Table

Input (V_{IN} pins)	MUTE (MUTE1, 2)	CH-U		CH-V		CH-W	
		$U_{OUT}+$	$U_{OUT}-$	$V_{OUT}+$	$V_{OUT}-$	$W_{OUT}+$	$W_{OUT}-$
H	H	H	L	H	L	H	L
	L	—	—	—	—	—	—
L	H	L	H	L	H	L	H
	L	—	—	—	—	—	—

Note: MUTE1 only operates for channel U, and MUTE2 only operates for channels V and W. MUTE1 and MUTE2 operate independently.

Pin Functions

Pin No.	Pin	Function	Equivalent circuit
1, 2, 14, 15, 16, 17, 29, 30	RF	Substrate (lowest potential)	
3	GND	Ground	
4	$V_{IN}1$	Channel U input	
5	$V_{IN}1A$	Channel U input (for gain adjustment)	
7	$V_{IN}2$	Channel V input	
8	$V_{IN}2A$	Channel V input (for gain adjustment)	
9	$V_{IN}3$	Channel W input	
10	$V_{IN}3A$	Channel W input (for gain adjustment)	
6	MUTE1	Channel U output on/off control	
11	BUFFER OUT1	Buffer amplifier 1 output (1/2 V_S1: typical), Generates the output stage reference voltage for channel U.	
12	BUFFER OUT2	Buffer amplifier 2 output (1/2 V_S2: typical), Generates the output stage reference voltage for channels V and W.	
13	V_{CC}	Power supply	
18	NC	Unused	
19	MUTE2	Channels V and W on/off control	
20	V_S2	Channels V and W output stage power supply	

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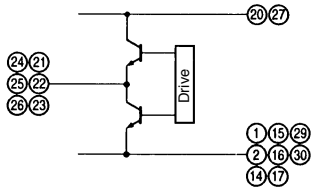
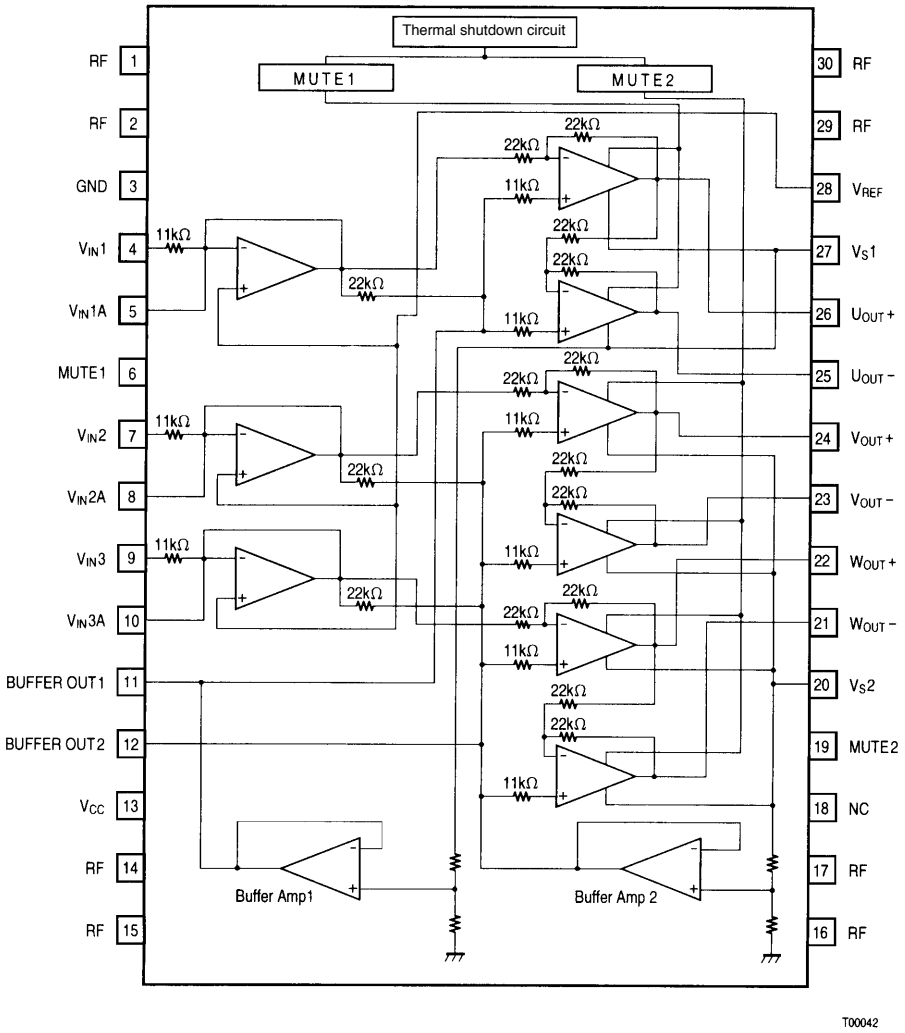
Pin No.	Pin	Function	Equivalent circuit
21	$W_{OUT}-$	Channel W inverting output	
22	$W_{OUT}+$	Channel W noninverting output	
23	$V_{OUT}-$	Channel V inverting output	
24	$V_{OUT}+$	Channel V noninverting output	
25	$U_{OUT}-$	Channel U inverting output	
26	$U_{OUT}+$	Channel U noninverting output	
27	V_S1	Channel U output stage power supply	
28	V_{REF}	Reference voltage for the level shifting circuit (shared by all channels)	

Block Diagram



Sample Application Circuit