No. 5647

LA7415

VHS VCR Playback Head and Record Amplifiers

Overview

The LA7415 is a record and playback amplifier IC for VHS format VCR decks. In combination with a Sanyo LC7420 or LA7430 Series video signal processing IC, the LA7415 can provide an adjustment-free Y/C record current.

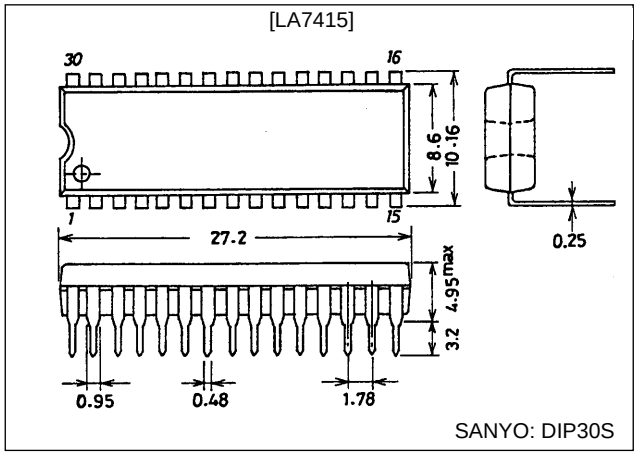
Features

- Record amplifier: Provides stable recording characteristics using a fixed-current drive technique that is resistant to load variations.
- REC-AMP: Includes a built-in AGC circuit.
- Can use the same printed circuit board as the LA7411.

Package Dimension

unit: mm

3061-DIP30S



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 65 °C	650	W
Operating temperature	Topr		–10 to +65	°C
Storage temperature	Tstg		–40 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.0	V
Operating voltage range	V_{CC}op		4.8 to 5.5	V

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Electrical Characteristics at Ta = 25°C

Parameter			Symbol	Input	Output	Conditions	T2	T4	T5	Ratings min	Ratings typ	Ratings max	Unit
[Playback Mode]						T15: 5.0 V, T13: OPEN, T7: OPEN	TRCK	HA	SW30 MUTE				
Current drain			I_{CCP}			Pin 15 influx current	OPEN	0	0	24	30	36	mA
Voltage gain	SP L	CH1	VG_P1	T20A	T10A	V_{IN} = 38 mVp-p, f = 1 MHz	OPEN	0	0	54.0	57.0	60.0	dB
	SP H	CH2	VG_P2	T23A	T10A		OPEN	0	2.5	54.0	57.0	60.0	dB
	EP L	CH3	VG_P3	T27A	T10A		OPEN	5.0	0	56.0	59.0	62.0	dB
	EP H	CH4	VG_P4	T30A	T10A		OPEN	5.0	2.5	56.0	59.0	62.0	dB
Voltage gain differential 1			ΔVG_P1	–	–	$VG_P1 - VG_P2$	–	–	–	–1	0	+1	dB
Voltage gain differential 2			ΔVG_P2	–	–	$VG_P3 - VG_P4$	–	–	–	–1	0	+1	dB
Inter-mode gain difference			$\Delta VG_{P\ EP-SP}$	–	–	$VG_P3 - VG_P1$	–	–	–	1	2	3	dB
Equivalent input noise voltage		CH1	$V_{NIN}1$	T20A	T10A	After the 1.1-MHz LPF $\frac{V_{OUT}}{VG_P1, 2, 3, 4}$	OPEN	0	0	–	1.1	1.5	µVrms
		CH2	$V_{NIN}2$	T23A	T10A		OPEN	0	2.5	–	1.1	1.5	µVrms
		CH3	$V_{NIN}3$	T27A	T10A		OPEN	5.0	0	–	1.1	1.5	µVrms
		CH4	$V_{NIN}4$	T30A	T10A		OPEN	5.0	2.5	–	1.1	1.5	µVrms
Frequency characteristics		CH1	$\Delta Vfp1$	T20A	T10A	V_{IN} = 38 mVp-p, f = 7 MHz $\frac{V_{OUT}}{VG_P1, 2, 3, 4}$ output ratio	OPEN	0	0	–2.5	0	–	dB
		CH2	$\Delta Vfp2$	T23A	T10A		OPEN	0	2.5	–2.5	0	–	dB
		CH3	$\Delta Vfp3$	T27A	T10A		OPEN	5.0	0	–2.5	0	–	dB
		CH4	$\Delta Vfp4$	T30A	T10A		OPEN	5.0	2.5	–2.5	0	–	dB
Second harmonic distortion		CH1	$V_{HDP}1$	T20A	T10A	V_{IN} = 38 mVp-p, f = 4 MHz (8-MHz component)/(4-MHz component) output ratio	OPEN	0	0	–	–40	–35	dB
		CH2	$V_{HDP}2$	T23A	T10A		OPEN	0	2.5	–	–40	–35	dB
		CH3	$V_{HDP}3$	T27A	T10A		OPEN	5.0	0	–	–40	–35	dB
		CH4	$V_{HDP}4$	T30A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
Maximum output level		CH1	$V_{OMP}1$	T20A	T10A	f = 1 MHz The output level when the third harmonic in the output is –30 dB	OPEN	0	0	1.0	1.2	–	Vp-p
		CH2	$V_{OMP}2$	T23A	T10A		OPEN	0	2.5	1.0	1.2	–	Vp-p
		CH3	$V_{OMP}3$	T27A	T10A		OPEN	5.0	0	1.0	1.2	–	Vp-p
		CH4	$V_{OMP}4$	T30A	T10A		OPEN	5.0	2.5	1.0	1.2	–	Vp-p
Crosstalk SP (Note 1)		CH1	$V_{CR}1$	T23A	T10A	V_{IN} = 38 mVp-p, f = 4 MHz $\frac{V_{OUT}}{VG_P1, 2}$	OPEN	0	0	–	–40	–35	dB
				T27A	T10A		OPEN	0	0	–	–40	–35	dB
				T30A	T10A		OPEN	0	0	–	–40	–35	dB
		CH2	$V_{CR}2$	T20A	T10A		OPEN	0	2.5	–	–40	–35	dB
				T27A	T10A		OPEN	0	2.5	–	–40	–35	dB
				T30A	T10A		OPEN	0	2.5	–	–40	–35	dB
Crosstalk EP (Note 1)		CH3	$V_{CR}3$	T23A	T10A	V_I = 38 mVp-p, f = 4 MHz $\frac{V_{OUT}}{VG_P3, 4}$	OPEN	5.0	0	–	–40	–35	dB
				T27A	T10A		OPEN	5.0	0	–	–40	–35	dB
				T30A	T10A		OPEN	5.0	0	–	–40	–35	dB
		CH4	$V_{CR}4$	T20A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
				T27A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
				T30A	T10A		OPEN	5.0	2.5	–	–40	–35	dB
Output DC offset			$\Delta V_{ODC}1$	–	T10	CH1-CH2	OPEN	–	0	–100	0	+100	mV
							OPEN	0	2.5	–100	0	+100	mV
			$\Delta V_{ODC}2$	–	T10	CH3-CH4	OPEN	–	0	–100	0	+100	mV
							OPEN	5.0	2.5	–100	0	+100	mV
			$\Delta V_{ODC}3$	–	T10	CH1-CH3	OPEN	0	–	–100	0	+100	mV
							OPEN	5.0	0	–100	0	+100	mV
			$\Delta V_{ODC}4$	–	T10	CH2-CH4	OPEN	0	–	–100	0	+100	mV
							OPEN	5.0	2.5	–100	0	+100	mV
			$\Delta V_{ODC}5$	–	T10	CH1-CH4	OPEN	0	0	–100	0	+100	mV
							OPEN	5.0	2.5	–100	0	+100	mV
			$\Delta V_{ODC}6$	–	T10	CH2-CH3	OPEN	0	2.5	–100	0	+100	mV
							OPEN	5.0	0	–100	0	+100	mV

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Note 1. With the input inductor L (8.2 µH) shorted.
2. Since the T4 (HA) control switch timing is synchronized with T6 (H-Sync), a T6 trigger (0 - 5 V - 0) must be input before measuring each of these items.

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Parameter	Symbol	Input	Output	Conditions	T2	T4	T5	Ratings min	Ratings typ	Ratings max	Unit
				T15: 5.0 V, T13: OPEN, T7: OPEN	TRCK	HA	SW30 MUTE				
Enveloped detector output pin voltage	V_{ENV}		T8	The T8 DC voltage with no input	OPEN	0	0	0	0.4	0.8	V
Enveloped detector voltage SP1	V_{ENVSP1}	T20A	T8	f = 4 MHz T10A: Adjusted to 300 mV p-p	OPEN	0	0	2.1	2.6	3.1	V
Enveloped detector voltage SP2	V_{ENVSP2}	T20A	T8	f = 4 MHz T10A: Adjusted to 600 mV p-p	OPEN	0	0	4.5	4.8	5.0	V
Enveloped detector voltage EP1	V_{ENVEP1}	T27A	T8	f = 4 MHz T10A: Adjusted to 200 mV p-p	OPEN	5.0	0	2.0	2.6	3.0	V
Enveloped detector voltage EP2	V_{ENVEP2}	T27A	T8	f = 4 MHz T10A: Adjusted to 450 mV p-p	OPEN	5.0	0	4.5	4.8	5.0	V
Comparator output voltage 1	V_{COMP1}	T20A	T3	f = 4 MHz, V_{IN} = 38 mVp-p The T3 DC voltage	5.0	0	0	–	0.4	0.7	V
Comparator output voltage 2	V_{COMP2}	T20A	T3	f = 4 MHz, V_{IN} = 38 mVp-p The T3 DC voltage	5.0	5.0	0	4.5	4.8	–	V
Playback mode on switching transistor on resistance	$R_{PON}17$		P-17	The difference in the DC measurement for 1-mA and 2-mA influx currents	–	–	–	–	4.0	6.0	Ω
	$R_{PON}18$		P-18		–	–	–	–	4.0	6.0	Ω
Playback mode mode switching transistor on resistance	$R_{PON}21$		P-21	The difference in the DC measurement for 1-mA and 2-mA influx currents	OPEN	5.0	–	–	4.0	6.0	Ω
	$R_{PON}24$		P-24		OPEN	5.0	–	–	4.0	6.0	Ω
	$R_{PON}26$		P-26		OPEN	0	–	–	4.0	6.0	Ω
	$R_{PON}29$		P-29		OPEN	0	–	–	4.0	6.0	Ω
Trick 1 threshold level	TR1-1		T2	Normal → Trick1	*	–	–	3.2	–	5.0	V
	TR1-2		T2	Trick1 → Normal	*	–	–	1.2	–	2.8	V
Trick 2 threshold level	TR2-1		T2	Normal → Trick2	*	–	–	0.0	–	0.8	V
	TR2-2		T2	Trick2 → Normal	*	–	–	1.2	–	2.8	V
HAPB threshold level	HAP-1		T4	SP → EP	–	*	–	1.8	–	5.0	V
	HAP-2		T4	EP → SP	–	*	–	0.0	–	1.4	V
SW30 threshold level	SW30-1		T5	Lch → Hch	–	–	*	1.2	–	5.0	V
	SW30-2		T4	Hch → Lch	–	–	*	0.0	–	0.8	V
					T2	T4	T5				
[Record Mode]				T15: 5.0 V, T2: OPEN, T6: 5.0 V, T7: 5.0 V	REC Adj2	HA	SW30 MUTE				
Current drain	I_{CCR}			The pin 15 influx current	OPEN	0	0	44	55	66	mA
AGC amplifier output level	V_{RSP}	T11A	T21A	f = 4 MHz V_{IN} = 200 mVp-p	OPEN	0	0	147	156	165	mVp-p
	V_{REP}	T11A	T26A		OPEN	5.0	0	116	123	130	mVp-p
Inter-mode gain difference	ΔVG_R	–	–	V_{RSP}/V_{REP}	–	–	–	1.30	2.05	2.80	dB
AGC amplifier control characteristics 1	$\Delta V_{AGC}1$-SP	T11A	T21A	f = 4 MHz, V_{IN} = 400 mVp-p The output level/$V_{RSP, EP}$ ratio	OPEN	0	0	–	0.5	1.0	dB
	$\Delta V_{AGC}1$-EP	T11A	T26A		OPEN	5.0	0	–	0.5	1.0	dB
AGC amplifier control characteristics 2	$\Delta V_{AGC}2$-SP	T11A	T21A	f = 4 MHz, V_{IN} = 100 mVp-p The output level/$V_{RSP, EP}$ ratio	OPEN	0	0	–1.0	–0.5	–	dB
	$\Delta V_{AGC}2$-EP	T11A	T26A		OPEN	5.0	0	–1.0	–0.5	–	dB
AGC amplifier frequency characteristics	ΔV_{FRS}	T11A	T21A	f = 1 MHz, 7 MHz, V_{IN} = 100 mVp-p The 7 MHz/1 MHz output ratio	OPEN	0	0	–1.0	–0.0	+1.0	dB
	ΔV_{FRE}	T11A	T26A		OPEN	5.0	0	–1.0	–0.0	+1.0	dB
AGC amplifier second harmonic distortion	ΔV_{HDRS}	T11A	T21A	f = 4 MHz, V_{IN} = 200 mVp-p The (8 MHz component)/(4 MHz component) output ratio	OPEN	0	0	–	–45	–40	dB
	ΔV_{HDRE}	T11A	T21A		OPEN	5.0	0	–	–45	–40	dB
AGC amplifier maximum output level	ΔV_{OMRS}	T11A	T21A	f = 4 MHz, The output level for which the second harmonic is –35 dB	Adj.	0	0	20	22	–	mAp-p
	ΔV_{OMRE}	T11A	T26A		Adj.	5.0	0	20	22	–	mAp-p
AGC amplifier muting attenuation	ΔV_{MRS}	T11A	T21A	f = 4 MHz, VI = 200 mVp-p The output level/$V_{RSP, EP}$ ratio	OPEN	0	5.0	–	–45	–40	dB
	ΔV_{MRE}	T11A	T26A		OPEN	5.0	5.0	–	–45	–40	dB

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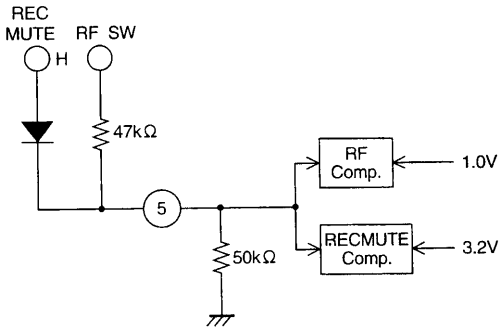
Parameter	Symbol	Input	Output	Conditions	T2	T4	T5	Ratings min	Ratings typ	Ratings max	Unit
[Record Mode]				T15: 5.0 V, T2: OPEN, T6: 5.0 V, T7: 5.0 V	REC Adj2	HA	SW30 MUTE				
AGC amplifier relative cross modulation level	ΔV_{CYS}	T10A	T21A	T10A: f = 629 kHz, V_{IN} = 360 mVp-p T11A: f = 4 MHz, V_{IN} = 200 mVp-p (4 MHz ±629 kHz)/(4 MHz) output ratio	OPEN	0	0	–	–45	–40	dB
	ΔV_{CYE}	T11A	T26A		OPEN	5.0	0	–	–45	–40	dB
Record mode mode switching transistor on resistance	$R_{RON}17$		P-17	The difference in the DC measurement for 1-mA and 2-mA influx currents	OPEN	5.0	–	–	4.0	6.0	Ω
	$R_{RON}18$		P-18		OPEN	0	–	–	4.0	6.0	Ω
	$R_{RON}21$		P-21		OPEN	5.0	–	–	4.0	6.0	Ω
	$R_{RON}24$		P-24		OPEN	5.0	–	–	4.0	6.0	Ω
	$R_{RON}26$		P-26		OPEN	0	–	–	4.0	6.0	Ω
	$R_{RON}29$		P-29		OPEN	0	–	–	4.0	6.0	Ω
HA record threshold level	HAR-1		T4	SP → EP	–	*	–	1.8	–	5.0	V
	HAR-2		T4	EP → SP	–	*	–	0.0	–	1.4	V
Record MUTE threshold level	MUTE-1		T5	MUTE OFF → ON	–	–	*	3.4	–	5.0	V
	MUTE-2		T5	MUTE ON → OFF	–	–	*	0.0	–	3.0	V
Record/playback threshold level	SW REC/PB			T7: control voltage	–	–	–	2.2	–	5.0	V

Notes 3. Measure with a DC voltage of about 1.8 V applied to the AGC detector filter pin (pin 12) and with the AGC amplifier gain fixed.
4. Adjust the output level by applying a DC voltage to T13 (REC CUR.Adj2)
5. Use a resistor with a ±1.0% tolerance between pins 14 and 15.

Usage Notes

1. Control Pin Logic

RF SW, REC MUTE: pin 5



Playback mode

If the pin 5 DC voltage is < 1.0 V: Lch

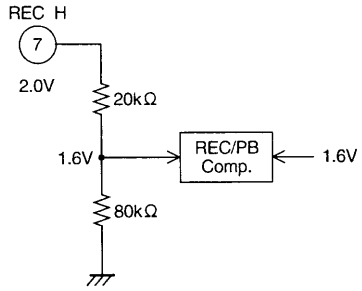
If the pin 5 DC voltage is > 1.0 V: Hch

Record mode

If the pin 5 DC voltage is < 3.2 V: Muting will be off

If the pin 5 DC voltage is > 3.2 V: Muting will be on

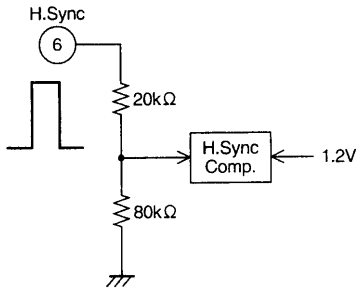
Record/playback mode switching: pin 7



If the pin 7 DC voltage is < 2.0 V: Playback mode

If the pin 7 DC voltage is > 2.0 V: Record mode

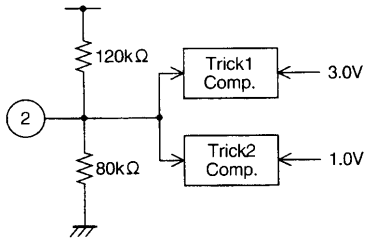
H.Sync input: pin 6



If the pin 6 DC voltage is > 1.5 V: Currently the signal is in an H.Sync period

*: Playback mode: Used for switching timing in SP search.
Record mode: Used as the record amplifier AGC synchronization block gate pulse.

(4) Playback trick mode switching: pin 2



If the pin 2 DC voltage is > 3.0 V: Trick 1
If the pin 2 DC voltage is < 1.0 V: Trick 2
If the pin 2 DC voltage is > 1.0 V and < 3.0 V: Normal

*: Normal mode: Two channels controlled (EP/SP) by pin 4: ON
Envelope comparator: OFF

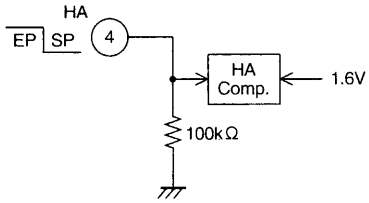
In trick 1 and 2 modes: All 4 channels: ON
Envelope comparator: ON

*: The difference between trick 1 and trick 2 is that:

Trick1 [Envelope comparator (pin 3) output] → [Servo (microcontroller)] (or)
→ [Pin 4 HA] →SP search is performed in the [HA switch] path.

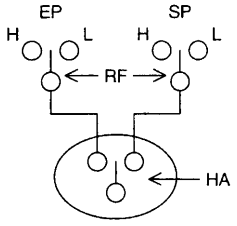
Trick2 [Envelope comparator output] → SP search is performed in the [HA switch] path. (See the block diagram.)

HA SW (EP/SP mode switching): pin 4



If the pin 4 DC voltage is < 1.6 V: SP mode

If the pin 4 DC voltage is > 1.6 V: EP mode



*: H.Sync synchronization for HA switching:

The switching of the HA SW circuit show in the figure at the right is synchronized with the H.Sync signal input to pin 6.
(Other EP/SP switching is performed in real time.)

Comp.OUT (pin 3)

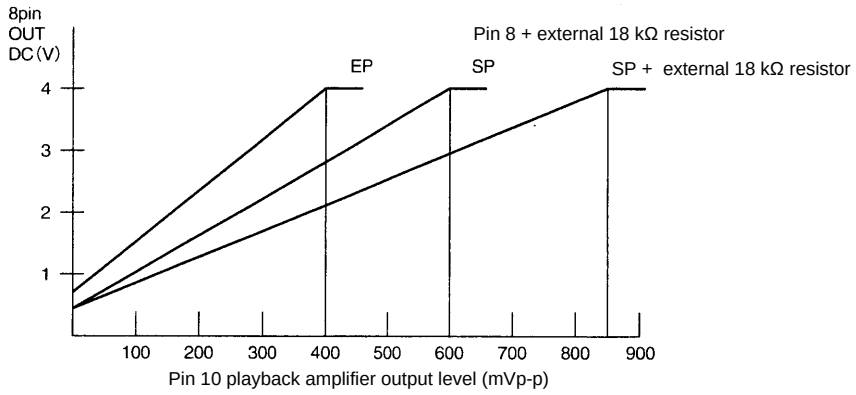
If the EP envelope is > SP: High (4.0 V or higher)

If the EP envelope is < SP: Low (0.7 V or lower)

2. Envelope Detector Characteristics: pin 8

The LA6529M includes an on-chip playback signal envelope detector circuit used to achieve automatic tracking adjustment with essentially linear characteristics.

Envelope Detector Characteristics (design target values) f = 4 MHz

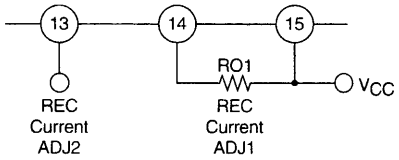


3. Record Amplifier Gain Control

The LA6529M achieves an adjustment-free record current by adding an AGC circuit in the record amplifier block. The record current can be modified using the circuit shown below.

(1) REC Current.Adj2: When open

The pin 13 DC level is set to 1/2 V_{CC} (about 2.5 V) by an internal bias and the record current is determined by RO1.



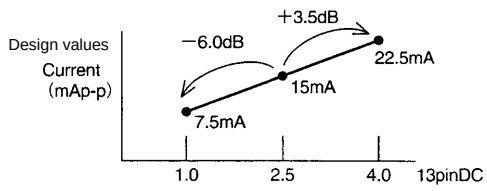
Design values: RO1: 1.5 kΩ = 15.6 mAp-p (SP) (per channel)
= 12.3 mAp-p (EP)

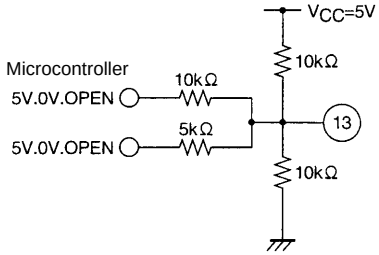
(2) REC Current.Adj2: When used

The value determined by RO1 can be adjusted from –6.0 dB to +3.5 dB by applying a control DC level (1 to 4 V) to pin 13.

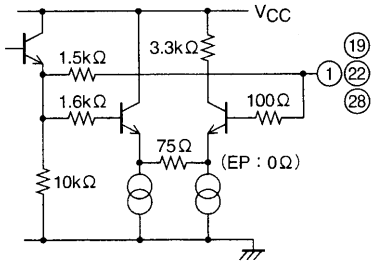
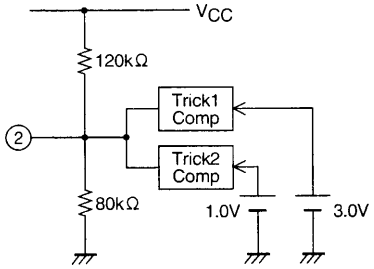
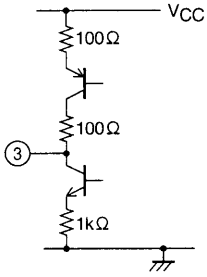
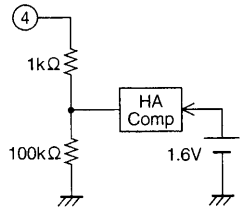
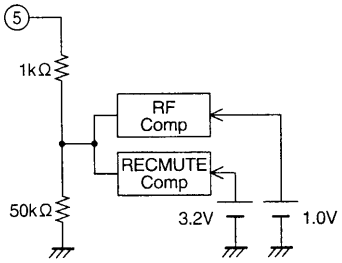
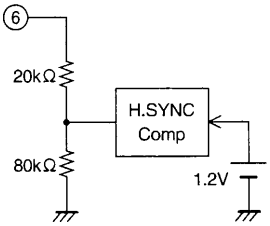
(Reference)

The circuit below can be used to apply the DC control level to pin 13.
This allows 9 modes (1 to 4 V) to be applied.





Pin Functions

Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes
1 19 22 28	PB Amp Second filter	PB	2.0		
		REC	3.6		
2	TRICK-H				3.0 V / 1.0 V Trick1 NORMAL Trick2
3	COMP-OUT	PB	High: 4.5 V or higher		EP > SP ENV: High
			Low: 0.7 V or lower		
		REC	OPEN		
4	HA (EP/SP)				1.6 V EP SP
5	RF-SW (REC-MUTE)				SW30 REC MUTE Hch / ON / 3.2 (V) 1.0 (V) / Lch / OFF
6	H-SYNC				1.5 V Sync H L

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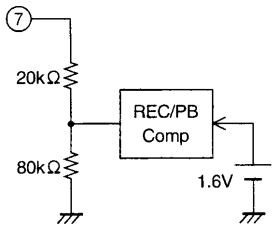
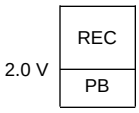
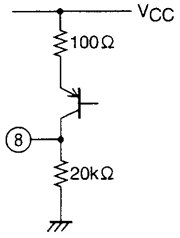
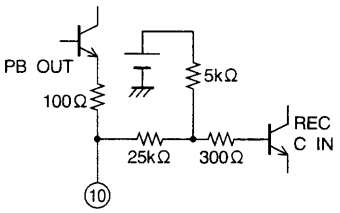
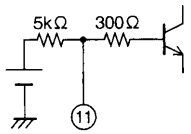
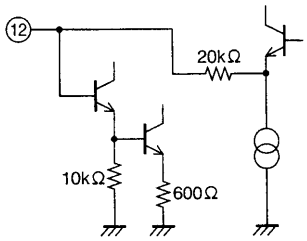
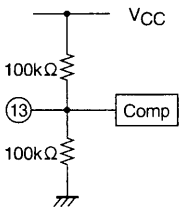
Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes
7	REC-H	PB	0		
		REC	5		
8	ENV DET OUT	PB	Described in a separate document.		
		REC	0		
9	GND				
10	PB-OUT	PB	2.3		
	REC-C-IN	REC	3.6		
11	REC-Y-IN	REC	3.6		
12	AGC-FLT	PB	1.6		
		REC	1.6		
13	REC-CURRENT ADJ2	PB	2.5		4 V: +3.5 dB 2.5 V: ±0 dB (OPEN) 1 V: –6 dB
		REC	2.5		

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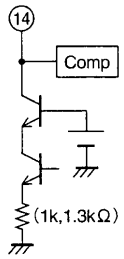
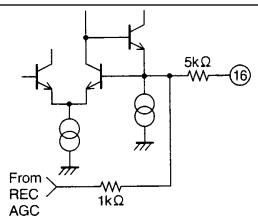
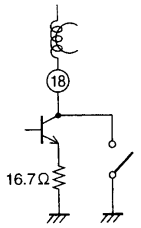
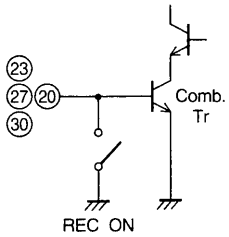
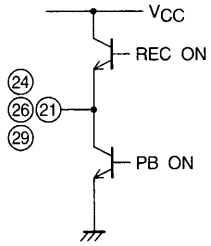
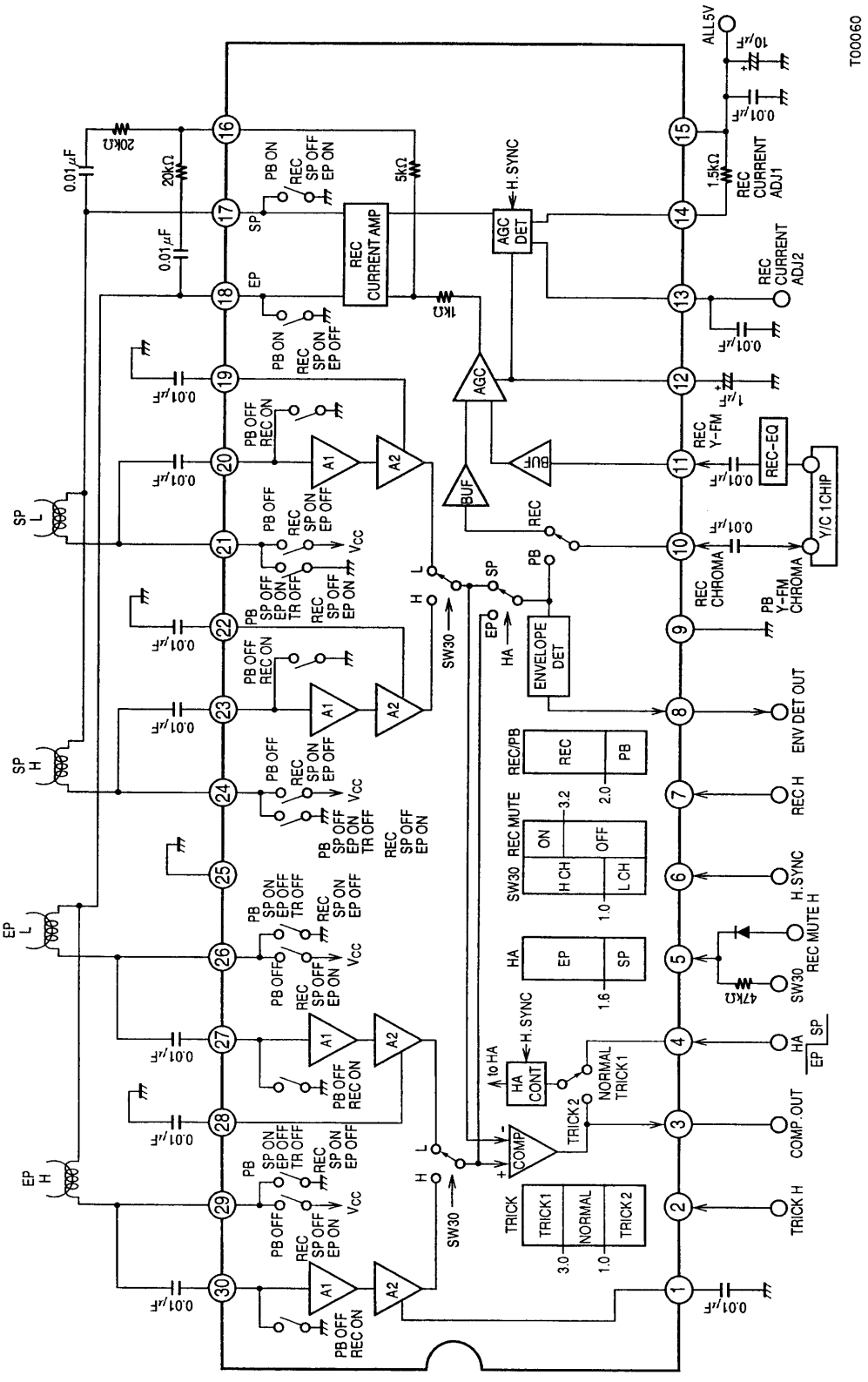
Pin No.	Pin	Standard DC voltage (V)		Pin circuit	Notes
14	REC-CURRENT ADJ1	PB	4.5		
		REC	5.0		
15	V_{CC}				
16	REC-BIAS	PB	2.5		
		REC	1.7		
17 18	REC-SP OUT REC-EP OUT	PB	0		
		REC	4.2		
20 23 27 30	SP-L-IN SP-H-IN EP-L-IN EP-H-IN	PB	0.7		
		REC	0		
21 24 26 29	SP-L-SW SP-H-SW EP-L-SW EP-H-SW	PB	0		
		REC	4.2		
25	PRE-GND				

Block Diagram



Test Circuit