



ON Semiconductor®

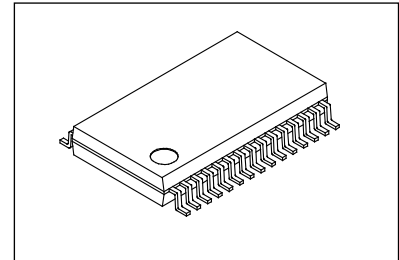
www.onsemi.com

# LB11696V

## Monolithic Digital IC Direct PWM Drive Brushless Motor Predriver IC

### Overview

The LB11696V is a direct PWM drive predriver IC designed for three-phase power brushless motors. A motor driver circuit with the desired output power (voltage and current) can be implemented by adding discrete transistors in the output circuits. Furthermore, the LB11696V provides a full complement of protection circuits allowing it to easily implement high-reliability drive circuits. This device is optimal for driving all types of large-scale motors such as those used in air conditioners and on-demand water heaters.



SSOP30 (275mil)

### Features

- Three-phase bipolar drive
- Direct PWM drive (controlled either by control voltage or PWM variable duty pulse input)
- Built-in forward/reverse switching circuit
- Start/stop mode switching circuit (stop mode power saving function)
- Built-in input amplifier
- 5 V regulator output (VREG pin)
- Current limiter circuit (Supports 0.25 V (typical) reference voltage sensing based high-precision detection)
- Undervoltage protection circuit (The operating voltage can be set with a zener diode)
- Automatic recovery type constraint protection circuit with protection operating state discrimination output (RD pin)
- Four types of Hall signal pulse outputs
- Supports thermistor based thermal protection of the output transistors

### Specifications

**Absolute Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	unit
Supply voltage 1	$V_{CC\ max}$	$V_{CC}$ pin	18	V
Output current	$I_O\ max$	UL, VL, WL, UH, VH, and WH pins	30	mA
LVS pin applied voltage	LVS max	LVS pin	18	V
Allowable power dissipation 1	$P_d\ max\ 1$	Independent IC	0.45	W
Allowable power dissipation 2	$P_d\ max\ 2$	When mounted on a 114.3 × 76.1 × 1.6 mm glass epoxy board	1.05	W
Operating temperature	$T_{opr}$		-20 to +100	°C
Storage temperature	$T_{stg}$		-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

## Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V <sub>CC1-1</sub>	V <sub>CC</sub> pin	8 to 17	V
Supply voltage range 1-2	V <sub>CC1-2</sub>	V <sub>CC</sub> pin, when V <sub>CC</sub> is shorted to VREG.	4.5 to 5.5	V
Output current	I <sub>O</sub>	UL, VL, WL, UH, VH, and WH pins	25	mA
5 V constant voltage output current	I <sub>REG</sub>		-30	mA
HP pin applied voltage	V <sub>HP</sub>		0 to 17	V
HP pin output current	I <sub>HP</sub>		0 to 15	mA
RD pin applied voltage	V <sub>RD</sub>		0 to 17	V
RD pin output current	I <sub>RD</sub>		0 to 15	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 12 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	I <sub>CC1</sub>			12	16	mA
Current drain 2	I <sub>CC2</sub>	Stop mode		2.5	4	mA
[5 V Constant Voltage Output (VREG pin)]						
Output voltage	V <sub>REG</sub>		4.7	5.0	5.3	V
Line regulation	ΔV <sub>REG1</sub>	V <sub>CC</sub> = 8 to 17 V		40	100	mV
Load regulation	ΔV <sub>REG2</sub>	I <sub>O</sub> = -5 to -20 mA		10	30	mV
Temperature coefficient	ΔV <sub>REG3</sub>	Design target value		0		mV/°C
[Output Block]						
Output voltage 1-1	V <sub>OUT1-1</sub>	Low level, I <sub>O</sub> = 400 μA		0.2	0.5	V
Output voltage 1-2	V <sub>OUT1-2</sub>	Low level, I <sub>O</sub> = 10 mA		0.9	1.2	V
Output voltage 2	V <sub>OUT2</sub>	High level, I <sub>O</sub> = -20 mA	V <sub>CC</sub> - 1.1	V <sub>CC</sub> - 0.9		V
Output leakage current	I <sub>Oleak</sub>				10	μA
[Hall Amplifier Block]						
Input bias current	I <sub>HB</sub> (HA)		-2	-0.5		μA
Common-mode input voltage range 1	V <sub>ICM1</sub>	When a Hall effect device is used	0.5		V <sub>CC</sub> - 2.0	V
Common-mode input voltage range 2	V <sub>ICM2</sub>	Single-sided input bias mode (when a Hall IC is used)	0		V <sub>CC</sub>	V
Hall Input Sensitivity			80			mVp-p
Hysteresis	ΔV <sub>IN</sub> (HA)		15	24	40	mV
Input voltage low → high	V <sub>SLH</sub> (HA)		5	12	20	mV
Input voltage high → low	V <sub>SHL</sub> (HA)		-20	-12	-5	mV
[CTL Amplifier]						
Input offset voltage	V <sub>IO</sub> (CTL)		-10		10	mV
Input bias current	I <sub>B</sub> (CTL)		-1		1	μA
Common-mode input voltage range	V <sub>ICM</sub>		0		V <sub>REG</sub> - 1.7	V
High-level output voltage	V <sub>OH</sub> (CTL)	I <sub>TOC</sub> = -0.2 mA	V <sub>REG</sub> - 1.2	V <sub>REG</sub> - 0.8		V
Low-level output voltage	V <sub>OL</sub> (CTL)	I <sub>TOC</sub> = 0.2 mA		0.8	1.05	V
Open-loop gain	G (CTL)	f (CTL) = 1 kHz	45	51		dB
[PWM Oscillator (PWM pin)]						
High-level output voltage	V <sub>OH</sub> (PWM)		2.75	3.0	3.25	V
Low-level output voltage	V <sub>OL</sub> (PWM)		1.2	1.35	1.5	V
External capacitor charge current	I <sub>CHG</sub>	V <sub>PWM</sub> = 2.1 V	-120	-90	-65	μA
Oscillator frequency	f (PWM)	C = 2000 pF		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-p
[TOC pin]						
Input voltage 1	V <sub>TOC1</sub>	Output duty: 100%	2.68	3.0	3.34	V
Input voltage 2	V <sub>TOC2</sub>	Output duty: 0%	1.2	1.35	1.5	V
Input voltage 1 low	V <sub>TOC1L</sub>	Design target value, when V <sub>REG</sub> = 4.7 V, 100%	2.68	2.82	2.96	V
Input voltage 2 low	V <sub>TOC2L</sub>	Design target value, when V <sub>REG</sub> = 4.7 V, 0%	1.23	1.29	1.34	V
Input voltage 1 high	V <sub>TOC1H</sub>	Design target value, when V <sub>REG</sub> = 5.3 V, 100%	3.02	3.18	3.34	V
Input voltage 2 high	V <sub>TOC2H</sub>	Design target value, when V <sub>REG</sub> = 5.3 V, 0%	1.37	1.44	1.50	V
[HP Pin]						
Output saturation voltage	V <sub>HPL</sub>	I <sub>O</sub> = 10 mA		0.2	0.5	V
Output leakage current	I <sub>HPL</sub> leak	V <sub>O</sub> = 18 V			10	μA

Continued on next page.

# LB11696V

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
<b>[CSD Oscillator (CSD pin)]</b>						
High-level output voltage	$V_{OH}$ (CSD)		2.7	3.0	3.3	V
Low-level output voltage	$V_{OL}$ (CSD)		0.7	1.0	1.3	V
External capacitor charge current	ICHG1	VCSD = 2 V	-3.15	-2.5	-1.85	$\mu$ A
External capacitor discharge current	ICHG2	VCSD = 2 V	0.1	0.14	0.18	$\mu$ A
Charge/discharge current ratio	RCSD	(Charge current)/(discharge current)	15	18	21	times
<b>[RD Pin]</b>						
Low-level output voltage	VRDL	$I_O = 10$ mA		0.2	0.5	V
Output leakage current	$I_L$ (RD)	$V_O = 18$ V			10	$\mu$ A
<b>[Current Limiter Circuit (RF pin)]</b>						
Limiter voltage	VRF	RF-RFGND	0.225	0.25	0.275	V
<b>[Undervoltage Protection Circuit (LVS pin)]</b>						
Operating voltage	VSDL		3.5	3.7	3.9	V
Release voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	$\Delta$ VSD		0.3	0.45	0.6	V
<b>[PWMIN Pin]</b>						
Input frequency	f (PI)				50	kHz
High-level input voltage	$V_{IH}$ (PI)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (PI)		0		1.0	V
Input open voltage	$V_{IO}$ (PI)		VREG - 0.5		VREG	V
Hysteresis	$V_{IS}$ (PI)		0.2	0.25	0.4	V
High-level input current	$I_{IH}$ (PI)	VPWMIN = VREG	-10	0	+10	$\mu$ A
Low-level input current	$I_{IL}$ (PI)	VPWMIN = 0 V	-130	-90		$\mu$ A
<b>[S/S Pin]</b>						
High-level input voltage	$V_{IH}$ (SS)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (SS)		0		1.0	V
Hysteresis	$V_{IS}$ (SS)		0.2	0.25	0.4	V
High-level input current	$I_{IH}$ (SS)	VS/S = VREG	-10	0	+10	$\mu$ A
Low-level input current	$I_{IL}$ (SS)	VS/S = 0 V	-10	-1		$\mu$ A
<b>[F/R Pin]</b>						
High-level input voltage	$V_{IH}$ (FR)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (FR)		0		1.0	V
Input open voltage	$V_{IO}$ (FR)		VREG - 0.5		VREG	V
Hysteresis	$V_{IS}$ (FR)		0.2	0.25	0.4	V
High-level input current	$I_{IH}$ (FR)	VF/R = VREG	-10	0	+10	$\mu$ A
Low-level input current	$I_{IL}$ (FR)	VF/R = 0 V	-130	-90		$\mu$ A
<b>[N1 Pin]</b>						
High-level input voltage	$V_{IH}$ (N1)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (N1)		0		1.0	V
Input open voltage	$V_{IO}$ (N1)		VREG - 0.5		VREG	V
High-level input current	$I_{IH}$ (N1)	VN1 = VREG	-10	0	+10	$\mu$ A
Low-level input current	$I_{IL}$ (N1)	VN1 = 0 V	-130	-100		$\mu$ A
<b>[N2 Pin]</b>						
High-level input voltage	$V_{IH}$ (N2)		2.0		VREG	V
Low-level input voltage	$V_{IL}$ (N2)		0		1.0	V
Input open voltage	$V_{IO}$ (N2)		VREG - 0.5		VREG	V
High-level input current	$I_{IH}$ (N2)	VN2 = VREG	-10	0	+10	$\mu$ A
Low-level input current	$I_{IL}$ (N2)	VN2 = 0 V	-130	-100		$\mu$ A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Three-Phase Logic Truth Table (“IN = ‘H’” indicates the state where IN+ > IN–.)

	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	—
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

S/S Pin

Input state	State
H	Stop
L	Start

PWMIN Pin

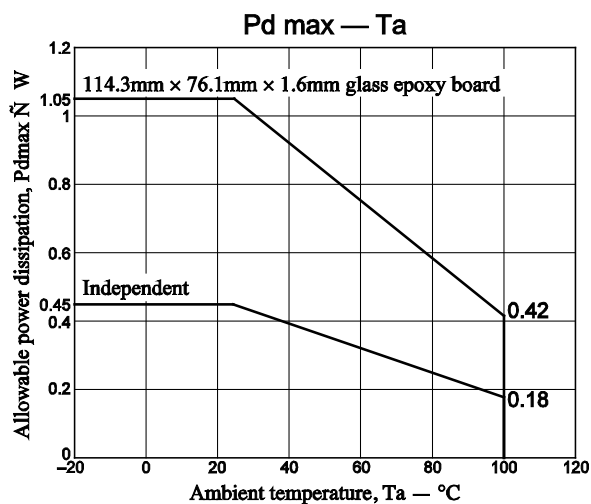
Input state	State
High or open	Output off
L	Output on

N1 and N2 Pins

Input state		HP output
N1 pin	N2 pin	
L	L	Single Hall sensor period divided by 2
L	High or open	Single Hall sensor period
High or open	L	Three Hall sensor synthesized period divided by 2
High or open	High or open	Three Hall sensor synthesized period

Since the S/S pin does not have an internal pull-up resistor, an external pull-up resistor or equivalent is required to set the IC to the stop state. If either the S/S or PWMIN pins are not used, the unused pin input must be set to the low-level voltage.

The HP output can be selected (by the N1 and N2 settings) to be one of the following four functions: the IN1 Hall input converted to a pulse output (one-Hall output), the one-Hall output divided by two, the three-phase output synthesized from the Hall inputs (three-Hall synthesized output) or the three-Hall synthesized output divided by two.



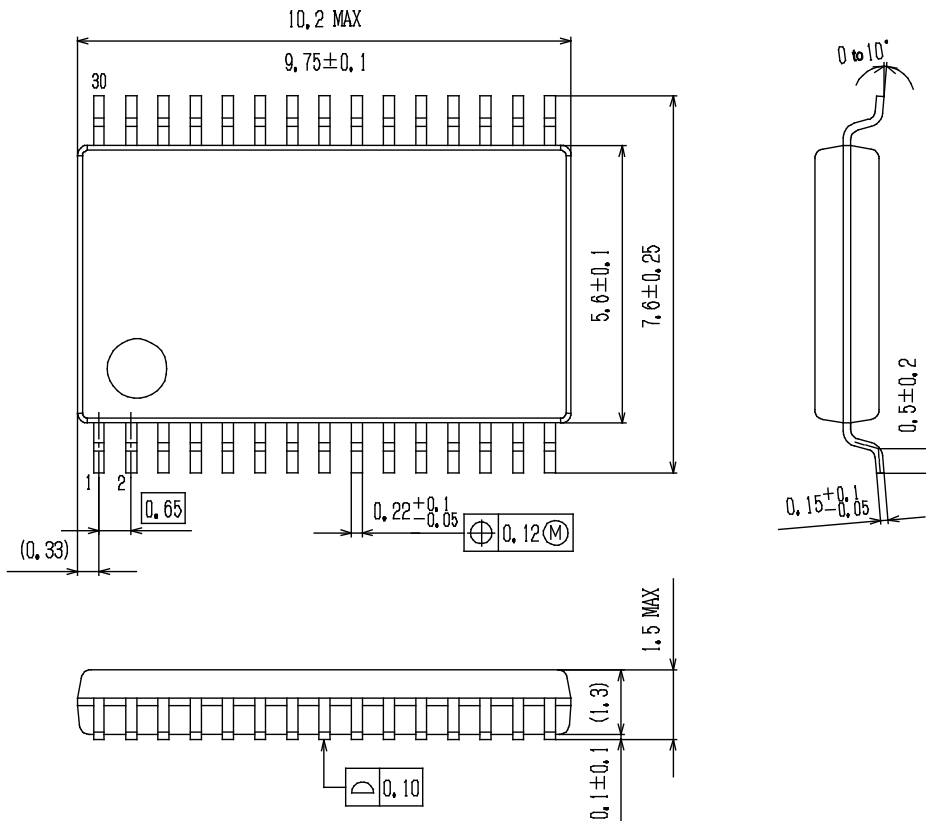
**Package Dimensions**

unit : mm

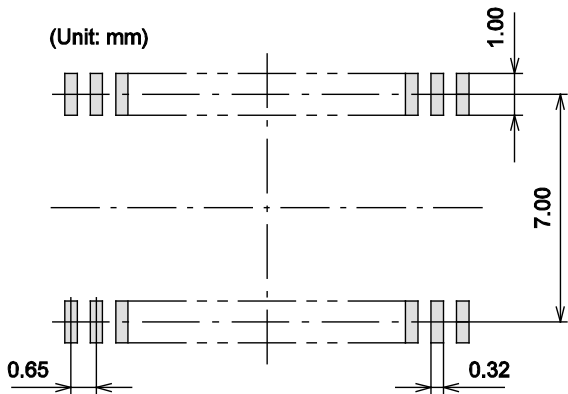
**SSOP30 (275mil)**

CASE 565AT

ISSUE A



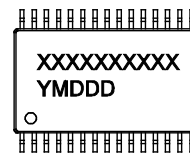
**SOLDERING FOOTPRINT\***



NOTE: The measurements are not to guarantee but for reference only.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC MARKING DIAGRAM\***



XXXXX = Specific Device Code  
 Y = Year  
 M = Month  
 DDD = Additional Traceability Data

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present.

**ORDERING INFORMATION**

Device	Package	Wire bond	Shipping (Qty / Packing)
LB11696V-MPB-E	SSOP30 (275mil) (Pb-Free)	Au wire	48 / Fan-Fold
LB11696V-TLM-E	SSOP30 (275mil) (Pb-Free)	Au wire	1000 / Tape & Reel
LB11696V-TRM-E	SSOP30 (275mil) (Pb-Free)	Au wire	1000 / Tape & Reel
LB11696V-TLM-H	SSOP30 (275mil) (Pb-Free / Halogen Free)	Au wire	1000 / Tape & Reel
LB11696V-W-AH	SSOP30 (275mil) (Pb-Free / Halogen Free)	Cu wire	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. [http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.