Ordering number : ENA0604

# LB11921T

**Monolithic Digital IC**

## Three-Phase Brushless Motor Driver

ON Semiconductor®

http://onsemi.com

### Overview

The LB11921T is a pre-driver IC designed for variable-speed control of 3-phase brushless motors. It can be used to implement a motor drive circuit with the desired output capacity (voltage, current) by using discrete transistors for the output stage. It implements direct PWM drive for minimal power loss. Since the LB11921T includes a built-in VCO circuit, applications can control the motor speed arbitrarily by varying the external clock frequency.

### Functions

- Direct PWM drive output
- Speed discriminator + PLL speed control circuit
- Speed lock detection output
- Built-in VCO circuit
- Forward/reverse switching circuit
- Braking circuit (short braking)
- Full complement of on-chip protection circuits, including lock protection, current limiter, and thermal shutdown protection circuits.

### Specifications

**Absolute Maximum Ratings** at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max | | 8 | V |
| Output current | $I_O$ max | UH, VH, WH, UL, VL, WL output | 10 | mA |
| Allowable power dissipation 1 | Pd max1 | Independent IC | 0.4 | W |
| Allowable power dissipation 2 | Pd max2 | Mounted on a circuit board* | 0.9 | W |
| Operating temperature | Topr | | -20 to +80 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

* Mounted on a specified board: 114.3mm×76.1mm×1.6mm, glass epoxy.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Allowable Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| FG Schmitt output applied voltage | VFGS | | 0 to 7 | V |
| FG Schmitt output current | IFGS | | 0 to 5 | mA |
| Lock detection applied voltage | VLD | | 0 to 7 | V |
| Lock detection output current | ILD | | 0 to 20 | mA |
| Supply voltage | $V_{CC}$ | | 4.4 to 7.0 | V |

## Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 5V

| Parameter | Symbol | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply current 1 | $I_{CC}1$ | | | 23 | 32 | mA |
| Supply current 2 | $I_{CC}2$ | In stop mode | | 2.1 | 2.9 | mA |
| **Output Block** | | | | | | |
| Output saturation voltage 1-1 | $V_O$sat1-1 | At low level: $I_O$ = 500µA | | 0.1 | 0.2 | V |
| Output saturation voltage 1-2 | $V_O$sat1-2 | At low level: $I_O$ = 5mA | | 0.3 | 0.5 | V |
| Output saturation voltage 2-1 | $V_O$sat2-1 | At high level: $I_O$ = -500µA | $V_{CC}$-0.2 | $V_{CC}$-0.1 | | V |
| Output saturation voltage 2-2 | $V_O$sat2-2 | At high level: $I_O$ = -5mA | $V_{CC}$-0.4 | $V_{CC}$-0.2 | | V |
| **Hall Amplifier** | | | | | | |
| Input bias current | IHB(HA) | | -2 | -0.1 | | µA |
| Common-mode input voltage range 1 | VICM1 | When Hall-effect sensors are used | 0.5 | | $V_{CC}$-2.0 | V |
| Common-mode input voltage range 2 | VICM2 | When one-side biased inputs are used (Hall-effect IC applications) | 0 | | $V_{CC}$ | V |
| Hall input sensitivity | | Sine wave | 50 | | | mVp-p |
| Hysteresis | ΔVIN(HA) | | 9 | 15 | 26 | mV |
| Input voltage low → high | VSLH | | 4 | 7 | 13 | mV |
| Input voltage high → low | VSHL | | -13 | -8 | -4 | mV |
| **PWM Oscillator** | | | | | | |
| Output high-level voltage | $V_{OH}$(PWM) | | 2.75 | 3.0 | 3.25 | V |
| Output low-level voltage | $V_{OL}$(PWM) | | 1.45 | 1.65 | 1.9 | V |
| Oscillator frequency | f(PWM) | C = 680pF | | 23 | | kHz |
| Amplitude | V(PWM) | | 1.1 | 1.35 | 1.6 | Vp-p |
| **CSD Oscillator** | | | | | | |
| Output high-level voltage | $V_{OH}$(CSD) | | 3.15 | 3.5 | 3.85 | V |
| Output low-level voltage | $V_{OL}$(CSD) | | 0.9 | 1.1 | 1.3 | V |
| External capacitor charge current | ICHG1 | | -9.0 | -6.5 | -3.9 | µA |
| External capacitor discharge current | ICHG2 | | 2.4 | 4.0 | 6.0 | µA |
| Oscillator frequency | f(RK) | C = 0.047µF | | 20 | | Hz |
| Amplitude | V(RK) | | 2.1 | 2.4 | 2.65 | Vp-p |
| **VCO Oscillator C pin** | | | | | | |
| Output high-level voltage | $V_{OH}$(C) | | 2.00 | 2.30 | 2.55 | V |
| Output low-level voltage | $V_{OL}$(C) | | 1.55 | 1.80 | 2.05 | V |
| Oscillator frequency | f(C) | | | | 1.2 | MHz |
| Amplitude | V(C) | | 0.3 | 0.5 | 0.7 | Vp-p |

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| Parameter | Symbol | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **Current Limiter Operation** | | | | | | |
| Limiter | VRF | | 0.24 | 0.26 | 0.28 | V |
| **Thermal Shutdown Operation** | | | | | | |
| Thermal shutdown operating temperature | TSD | Design target value * | 150 | 180 | | °C |
| Hysteresis | ΔTSD | Design target value * | | 30 | | °C |
| **Low-voltage Protection Circuit** | | | | | | |
| Operating voltage | VSDL | | 3.40 | 3.74 | 4.00 | V |
| Release voltage | VSDH | | 3.55 | 3.93 | 4.23 | V |
| Hysteresis | ΔVSD | | 0.12 | 0.19 | 0.26 | V |
| **FG Amplifier** | | | | | | |
| Input offset voltage | $V_{IO}$(FG) | | -10 | | 10 | mV |
| Input bias current | IB(FG) | | -1 | | 1 | μA |
| Output high-level voltage | $V_{OH}$(FG) | IFGI = -0.1mA, No load | 3.6 | 3.95 | 4.3 | V |
| Output low-level voltage | $V_{OL}$(FG) | IFGI = 0.1mA, No load | 0.7 | 1.05 | 1.4 | V |
| FG input sensitivity | | Gain: 100× | 3 | | | mV |
| Schmitt amplitude for the next stage | | | 100 | 180 | 250 | mV |
| Operating frequency range | | | | | 2.34 | kHz |
| Open-loop gain | | f(FG) = 2kHz | 45 | 51 | | dB |
| Reference voltage | VB(FG) | | -5% | $V_{CC}$/2 | 5% | V |
| **FGS Output** | | | | | | |
| Output saturation voltage | $V_O$(FGS) | $I_O$(FGS) =2mA | | 0.2 | 0.4 | V |
| Output leakage current | $I_L$(FGS) | $V_O = V_{CC}$ | | | 10 | μA |
| **Speed Discriminator Output** | | | | | | |
| Output high-level voltage | $V_{OH}$(D) | | $V_{CC}$-1.0 | $V_{CC}$-0.7 | | V |
| Output low-level voltage | $V_{OL}$(D) | | | 0.8 | 1.1 | V |
| Counts | | | | 512 | | |
| **Speed Control PLL Output** | | | | | | |
| Output high-level voltage | $V_{OH}$(P) | | 3.25 | 3.50 | 3.85 | V |
| Output low-level voltage | $V_{OL}$(P) | | 1.25 | 1.60 | 1.85 | V |
| **Lock Detection** | | | | | | |
| Output saturation voltage | $V_{OL}$(LD) | ILD = 10mA | | 0.25 | 0.4 | V |
| Output leakage current | $I_L$(LD) | $V_O = V_{CC}$ | | | 10 | μA |
| Lock range | | | -6.25 | | +6.25 | % |
| **Integrator** | | | | | | |
| Input offset voltage | $V_{IO}$(INT) | | -10 | | 10 | mV |
| Input bias current | IB(INT) | | -0.4 | | 0.4 | μA |
| Output high-level voltage | $V_{OH}$(INT) | IINTI = -0.1mA, No load | 3.45 | 3.7 | 3.95 | V |
| Output low-level voltage | $V_{OL}$(INT) | IINT = 0.1mA, No load | 1.1 | 1.3 | 1.5 | V |
| Open-loop gain | | | 45 | 51 | | dB |
| Gain-bandwidth product | | Design target value * | | 1.0 | | MHz |
| Reference voltage | VB(INT) | | -5% | $V_{CC}$/2 | 5% | V |

*: Design target value and no measurement was made.

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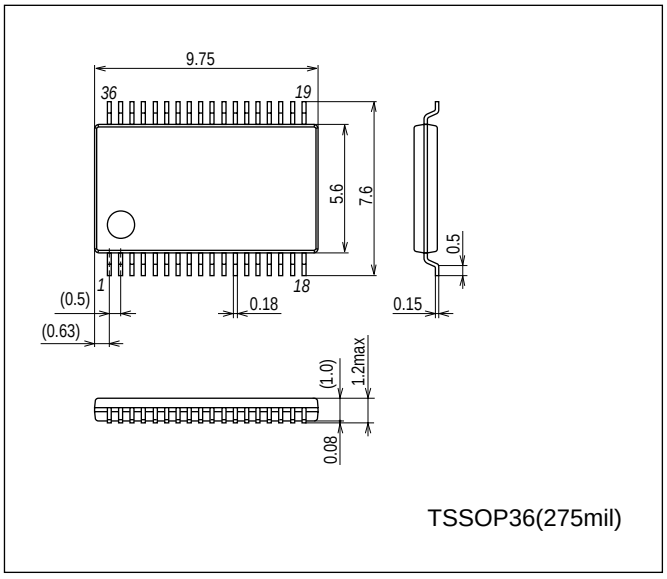
| Parameter | Symbol | Conditions | Ratings | | | unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| **FIL Output** | | | | | | |
| Output source current | $I_{OH}$(FIL) | | -17 | -13 | -7 | μA |
| Output sink current | $I_{OL}$(FIL) | | 7 | 12 | 17 | μA |
| **S/S Pin** | | | | | | |
| Input high-level voltage | $V_{IH}$(S/S) | | 2.0 | | $V_{CC}$ | V |
| Input low-level voltage | $V_{IL}$(S/S) | | 0 | | 1.0 | V |
| Input open voltage | $V_{IO}$(S/S) | | $V_{CC}$-0.5 | | $V_{CC}$ | V |
| Hysteresis | $\Delta V_{IN}$(S/S) | | 0.13 | 0.22 | 0.31 | V |
| Input high-level current | $I_{IH}$(S/S) | VS/S = $V_{CC}$ | -10 | 0 | 10 | μA |
| Input low-level current | $I_{IL}$(S/S) | VS/S = 0V | -135 | -93 | | μA |
| Pull-up resistance | RU(S/S) | | 37 | 53.5 | 70 | kΩ |
| **F/R Pin** | | | | | | |
| Input high-level voltage | $V_{IH}$(F/R) | | 2.0 | | $V_{CC}$ | V |
| Input low-level voltage | $V_{IL}$(F/R) | | 0 | | 1.0 | V |
| Input open voltage | $V_{IO}$(F/R) | | $V_{CC}$-0.5 | | $V_{CC}$ | V |
| Hysteresis | $\Delta V_{IN}$(F/R) | | 0.13 | 0.22 | 0.31 | V |
| Input high-level current | $I_{IH}$(F/R) | VF/R = $V_{CC}$ | -10 | 0 | 10 | μA |
| Input low-level current | $I_{IL}$(F/R) | VF/R = 0V | -135 | -93 | | μA |
| Pull-up resistance | RU(F/R) | | 37 | 53.5 | 70 | kΩ |
| **BR Pin** | | | | | | |
| Input high-level voltage | $V_{IH}$(BR) | | 2.0 | | $V_{CC}$ | V |
| Input low-level voltage | $V_{IL}$(BR) | | 0 | | 1.0 | V |
| Input open voltage | $V_{IO}$(BR) | | $V_{CC}$-0.5 | | $V_{CC}$ | V |
| Hysteresis | $\Delta V_{IN}$(BR) | | 0.13 | 0.22 | 0.31 | V |
| Input high-level | $I_{IH}$(BR) | VBR = $V_{CC}$ | -10 | 0 | 10 | μA |
| Input low-level current | $I_{IL}$(BR) | VBR = 0V | -135 | -93 | | μA |
| Pull-up resistance | RU(BR) | | 37 | 53.5 | 70 | kΩ |
| **CLK Pin** | | | | | | |
| Input high-level voltage | $V_{IH}$(CLK) | | 2.0 | | $V_{CC}$ | V |
| Input low-level voltage | $V_{IL}$(CLK) | | 0 | | 1.0 | V |
| Input open voltage | $V_{IO}$(CLK) | | $V_{CC}$-0.5 | | $V_{CC}$ | V |
| Hysteresis | $\Delta V_{IN}$(CLK) | Design target value * | 0.13 | 0.22 | 0.31 | V |
| Input high-level current | $I_{IH}$(CLK) | VCLK = $V_{CC}$ | -10 | 0 | 10 | μA |
| Input low-level current | $I_{IL}$(CLK) | VCLK = 0V | -135 | -93 | | μA |
| Input frequency | f(CLK) | | | | 2.34 | kHz |
| Pull-up resistance | RU(CLK) | | 37 | 53.5 | 70 | kΩ |

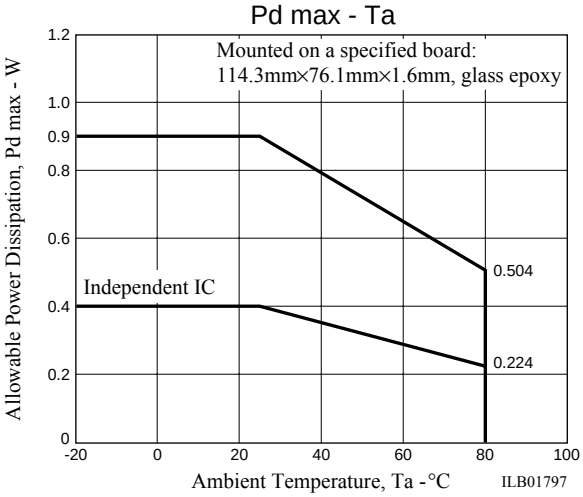
*: Design target value and no measurement was made.

## Package Dimensions

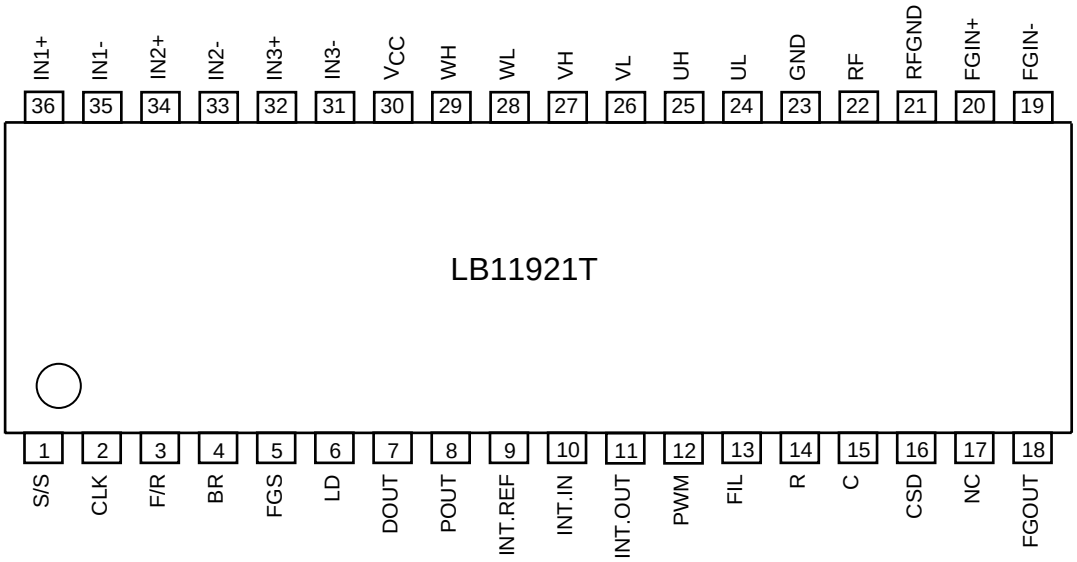
unit : mm (typ)

3253B




## Pin Assignment

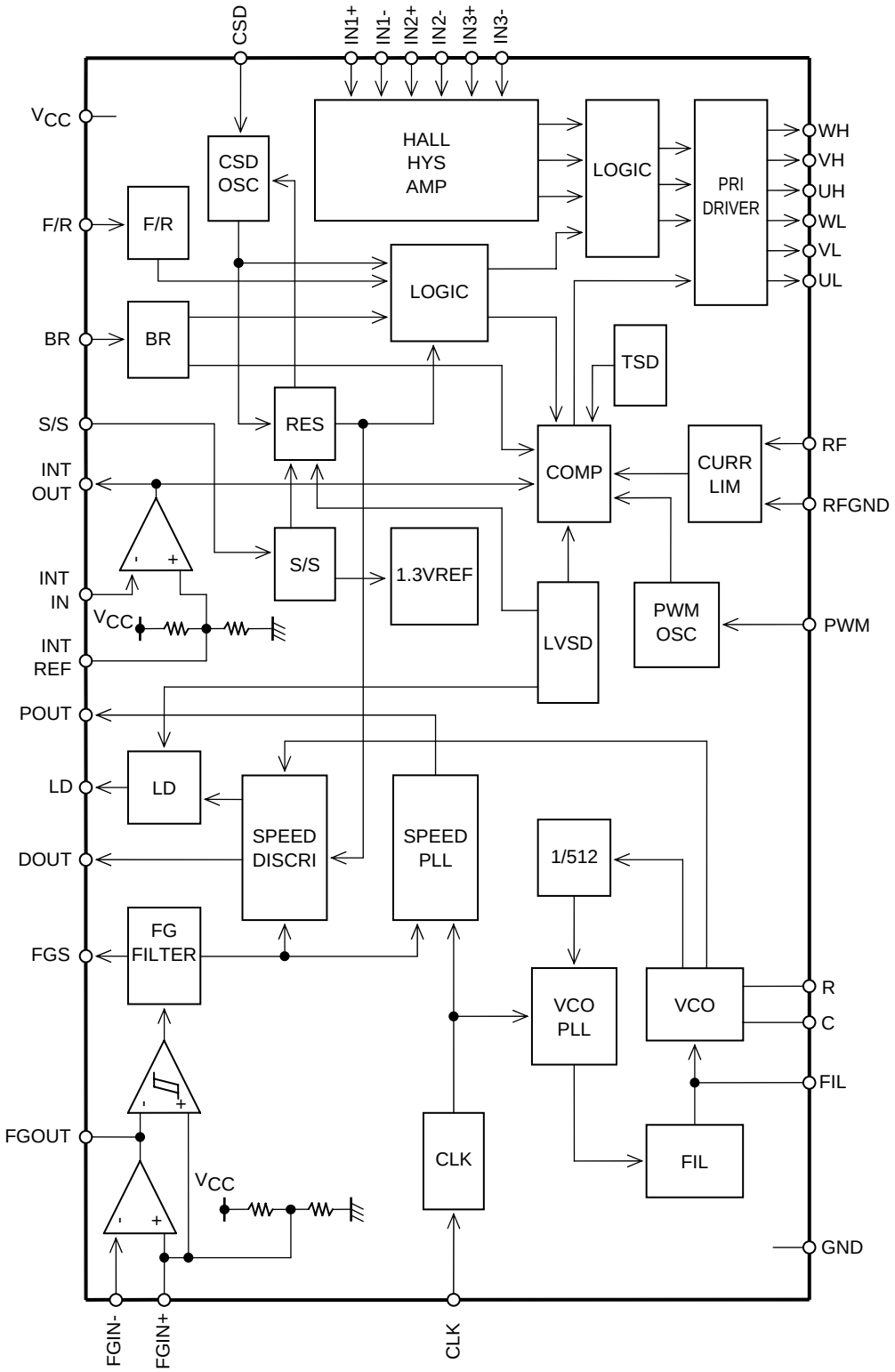



Top view

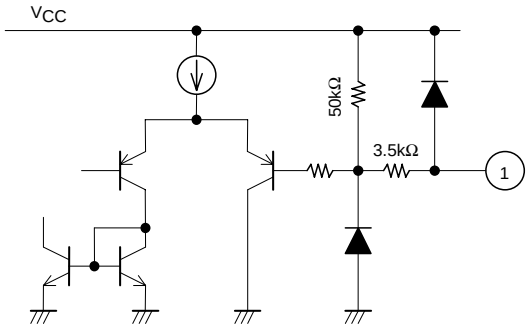
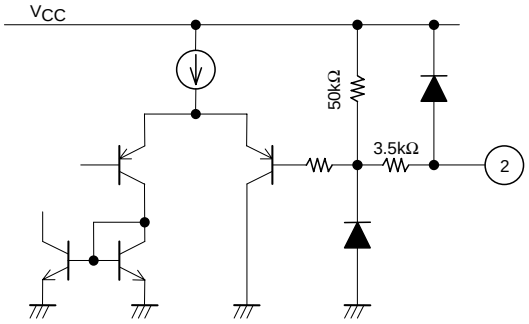
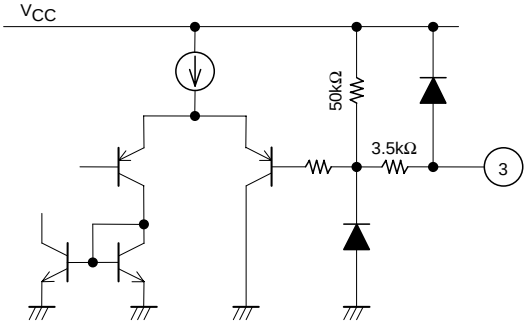
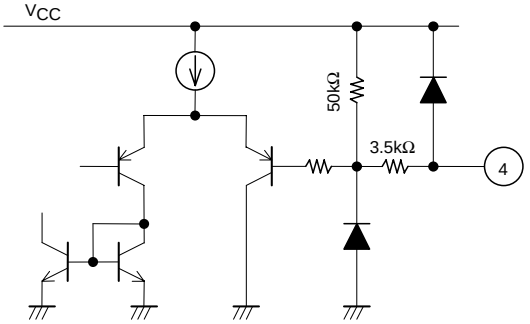
## Three-Phase Logic Truth Table (A high (H) input is the state where IN+ > IN–.)

| | F/R=L | | | F/R=H | | | Output | |
|---|---|---|---|---|---|---|---|---|
| | IN1 | IN2 | IN3 | IN1 | IN2 | IN3 | PWM | - |
| 1 | H | L | H | L | H | L | VH | UL |
| 2 | H | L | L | L | H | H | WH | UL |
| 3 | H | H | L | L | L | H | WH | VL |
| 4 | L | H | L | H | L | H | UH | VL |
| 5 | L | H | H | H | L | L | UH | WL |
| 6 | L | L | H | H | H | L | VH | WL |

## Block Diagram



## Pin Functions

| Pin No. | Symbol | Pin Description | Equivalent Circuit |
|---|---|---|---|
| 1 | S/S | Start/stop control<br>Low: 0V to 1.0V<br>High: 2.0V to $V_{CC}$<br>Goes high when left open.<br>Low for start.<br>The hysteresis is about 0.22V |  |
| 2 | CLK | External clock signal input<br>Low: 0V to 1.0V<br>High: 2.0V to $V_{CC}$<br>Goes high when left open.<br>The hysteresis is about 0.22V.<br>f = 2.34kHz, maximum |  |
| 3 | F/R | Forward/reverse control<br>Low: 0V to 1.0V<br>High: 2.0V to $V_{CC}$<br>Goes high when left open.<br>Low for forward.<br>The hysteresis is about 0.22V. |  |
| 4 | BR | Brake pin (short braking operation)<br>Low: 0V to 1.0V<br>High: 2.0V to $V_{CC}$<br>Goes high when left open.<br>High or open for brake mode operation.<br>The hysteresis is about 0.22V. |  |

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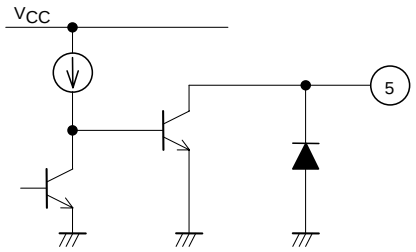
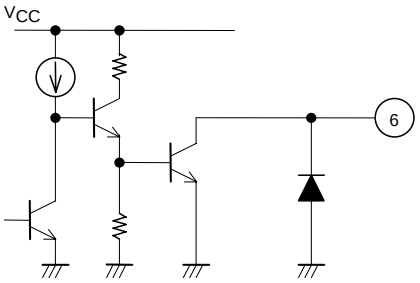
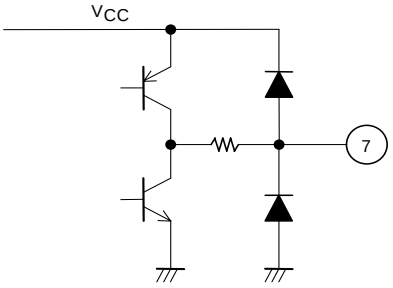
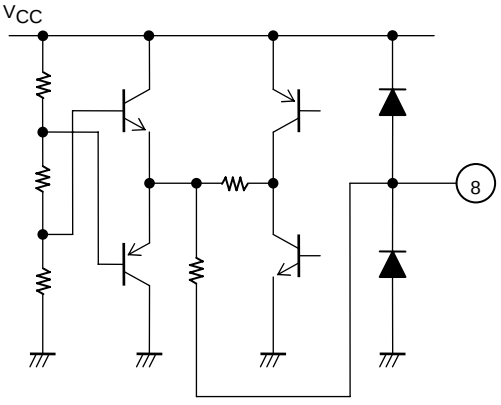
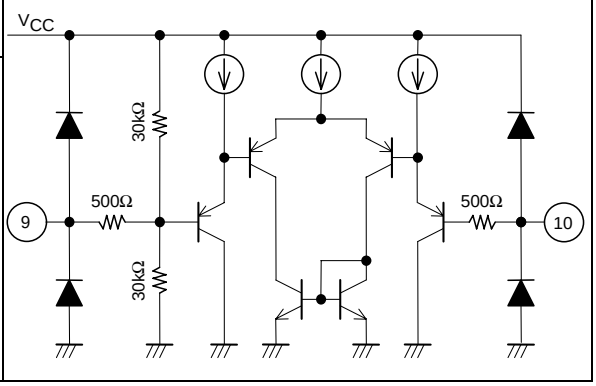
| Pin No. | Symbol | Pin Description | Equivalent Circuit |
|---|---|---|---|
| 5 | FGS | FG schmitt comparator circuit output<br>This is an open collector output. |  |
| 6 | LD | Speed lock detection output<br>Goes low when the motor speed is within the speed lock range (±6.25%). |  |
| 7 | DOUT | Speed discriminator output<br>Acceleration → high, deceleration → low |  |
| 8 | POUT | Speed control system PLL output<br>Outputs the phase comparison result for CLK and FG. |  |
| 9 | INT REF | Integrating amplifier non-inverting input<br>(1/2 $V_{CC}$ potential) |  |
| 10 | INT IN | Integrating amplifier inverting input | |

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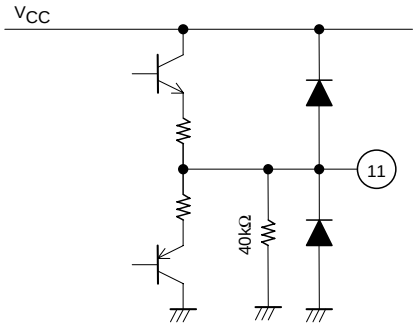
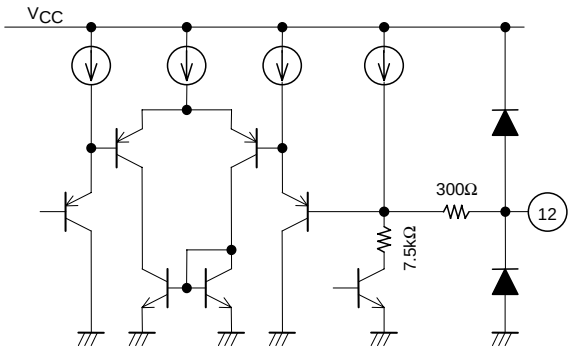
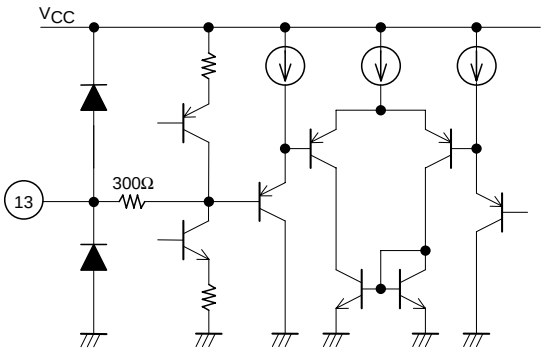
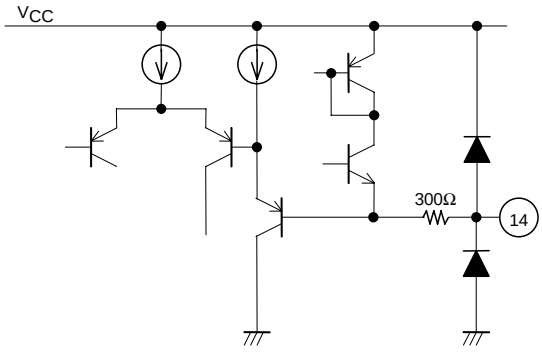
| Pin No. | Symbol | Pin Description | Equivalent Circuit |
|---|---|---|---|
| 11 | INT OUT | Integrating amplifier output |  |
| 12 | PWM | PWM oscillator frequency setting.<br>Connect a capacitor between this pin and ground. |  |
| 13 | FIL | VCO system PLL output filter connection |  |
| 14 | R | Set the value of the charge/discharge current from the VCO circuit C pin.<br>Insert a resistor between this pin and ground. |  |

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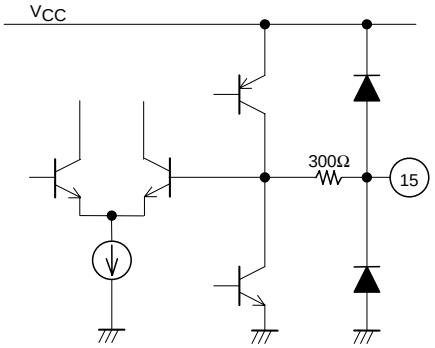
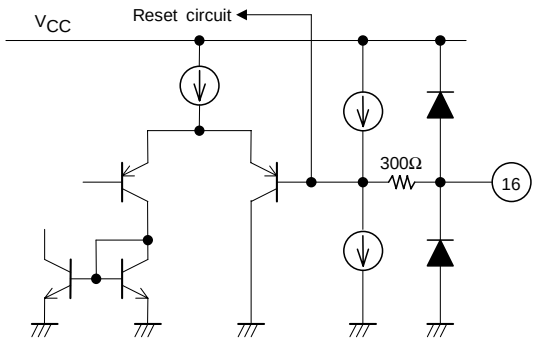
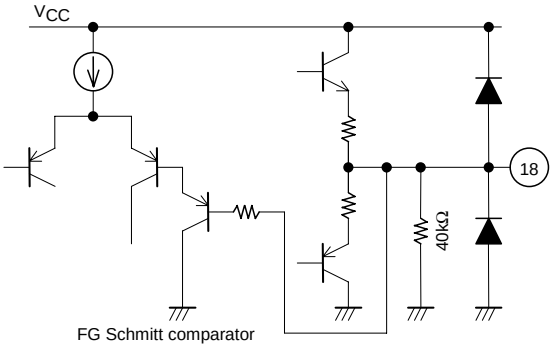
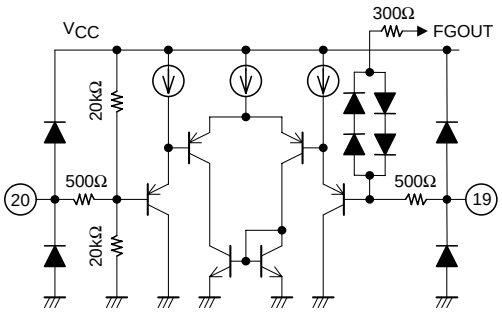
| Pin No. | Symbol | Pin Description | Equivalent Circuit |
|---|---|---|---|
| 15 | C | VCO oscillator connection<br>Insert a capacitor between this pin and ground.<br>The oscillation frequency of the C pin must not exceed 1.2MHz. |  |
| 16 | CSD | Set the operating time of the constrained-rotor protection circuit.<br>Insert a capacitor between this pin and ground.<br>This pin also functions as the logic circuit block power-on reset pin. |  |
| 17 | NC | There is unconnected pin, and can be used for wiring. | |
| 18 | FGOUT | FG amplifier output<br>This pin is connected to the FG Schmitt comparator circuit internally in the IC. |  |
| 19 | FGIN⁻ | FG amplifier inverting input |  |
| 20 | FGIN⁺ | FG amplifier noninverting input.<br>Insert a capacitor between this pin and ground.<br>The 1/2 $V_{CC}$ potential. | |

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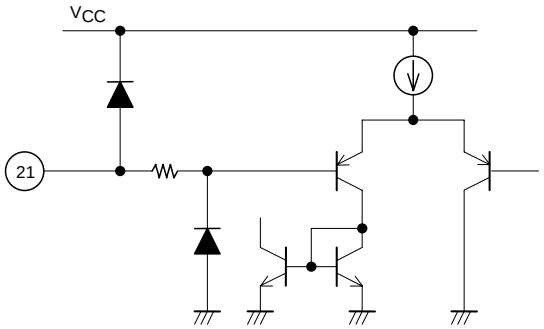
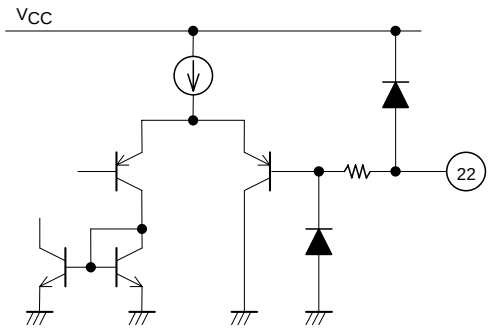
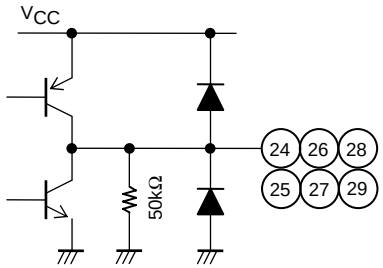
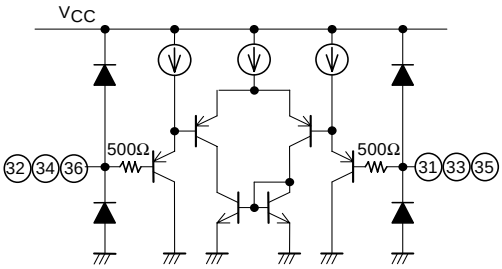
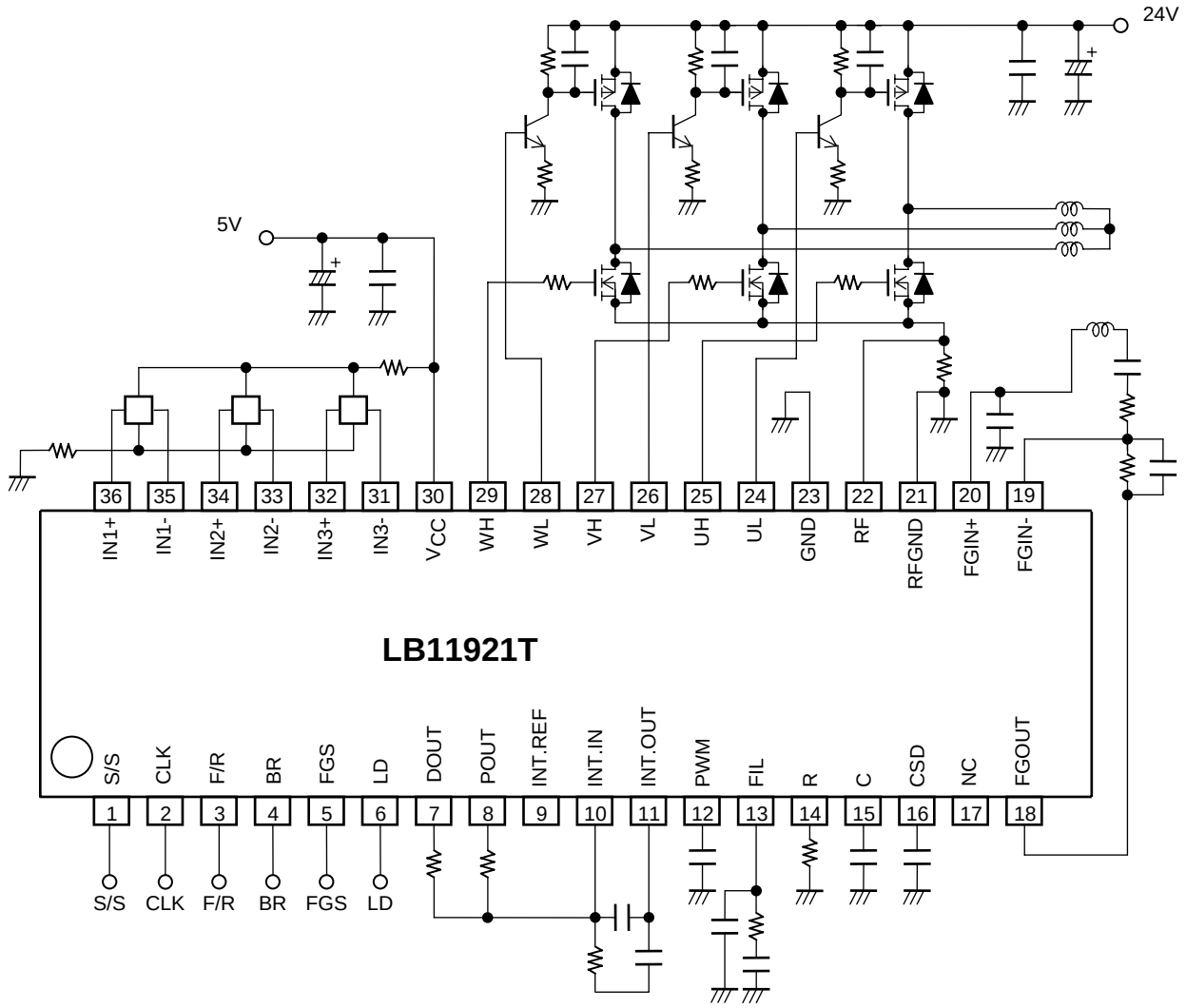
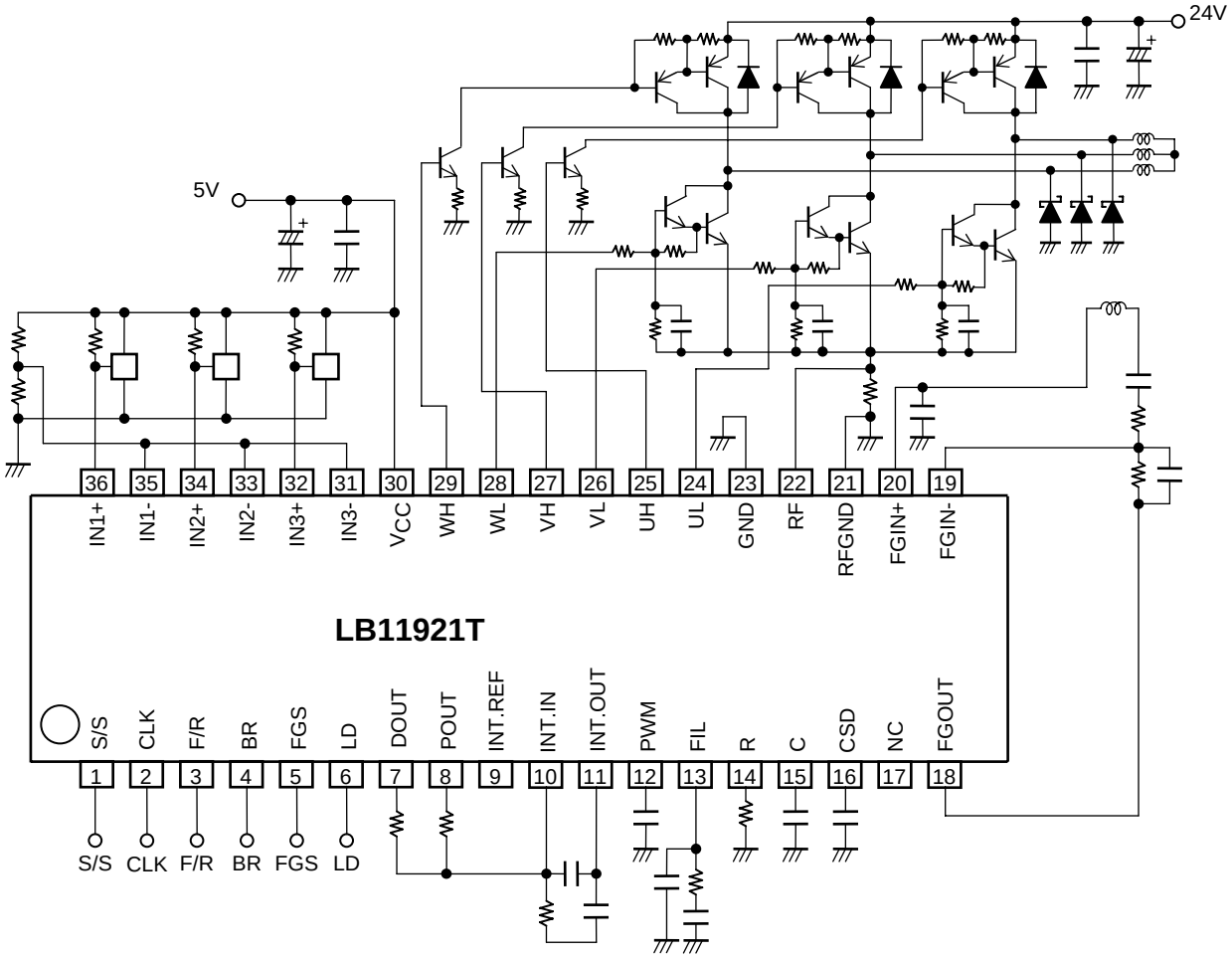
| Pin No. | Symbol | Pin Description | Equivalent Circuit |
|---|---|---|---|
| 21 | RF GND | Output current detection reference<br>Connect to GND of the external resistor Rf. |  |
| 22 | RF | Output current detection<br>Connect a low resistance resistor Rf between this pin and Rf GMD pin.<br>This resistor sets the maximum output current $I_{OUT}$ to be 0.26/Rf. |  |
| 23 | GND | GND pin | |
| 24<br>25<br>26<br>27<br>28<br>29 | UL<br>UH<br>VL<br>VH<br>WL<br>WH | Outputs (that are used to drive external transistors).<br>Duty cycle is controlled on the UH, VH, and WH side of these output. |  |
| 30 | $V_{CC}$ | Power supply<br>Connect a capacitor between this pin and ground for stabilization. | |
| 31<br>32<br>33<br>34<br>35<br>36 | $IN3^-$<br>$IN3^+$<br>$IN2^-$<br>$IN2^+$<br>$IN1^-$<br>$IN1^+$ | Hall-effect device inputs.<br>The input is seen as a high-level input when IN+ > IN-, and as a low-level input for the opposite state.<br>If noise on the Hall-effect device signals is a problem, insert capacitors between the corresponding IN+ and IN- inputs. |  |

## Sample Application Circuit 1 (P-channel + N-channel, Hall-effect sensor application)



## Sample Application Circuit 2 (PNP + NPN, Hall-IC application)



## LB11921T Overview

1. Speed Control Circuit

This IC implements speed control using the combination of a speed discriminator circuit and a PLL circuit. The speed discriminator circuit outputs (This counts a single FG period.) an error signal once every two FG periods. The PLL circuit outputs an error signal once every one FG Period. As compared to the earlier technique in which only a speed discriminator circuit was used, the combination of a speed discriminator and a PLL circuit allows variations in motor speed to be better suppressed when a motor that has large load variations is used. The FG servo frequency ($f_{FG}$) is controlled to have the equal frequency with the clock signal ($f_{CLK}$) which is input through the CLK pin.

$$f_{FG} = f_{CLK}$$

2. VCO Circuit

The LB11921T includes a built-in VCO circuit to generate the speed discriminator circuit reference signal. The reference signal frequency is given by the following formula.

$$f_{VCO} = f_{CLK} \times 512$$

$f_{VCO}$: Reference signal frequency
$f_{CLK}$: Externally input clock frequency

The range over which the reference signal frequency can be varied is determined by the resistor and capacitor components connected to the R and C pins (pins 14 and 15) and by the VCO loop filter constant (the values of the external components connected to pin 13).

Reference value at $V_{CC}$ = 5V

| fFG in the high-speed rotation mode | R(kΩ) | C(pF) |
|---|---|---|
| 1.5kHz | 5.6 | 330 |
| 2.0kHz | 5.6 | 220 |

The components connected to the R, C, and FIL pins must be connected with lines to their ground pin (pin 23) that are as short as possible.

3. Output Drive Circuit

To reduce power loss in the output, this IC adopts the direct PWM drive technique. The output transistors (which are external to the IC) are always saturated when on, and the motor drive output is adjusted by changing the duty with which the output is on. The PWM switching is performed on the UH, VH, and WH pins. The PWM switching side in the output can be selected to be either the high or low side depending on how the external transistors are connected.

4. Current Limiter Circuit

The current limiter circuit limits the (peak) current at the value $I = V_{RF}/Rf$ ($V_{RF}$ = 0.26V (typical), Rf: current detection resistor). The current limitation operation consists of reducing the output duty to suppress the current. High accuracy detection can be achieved by connecting the RF and RFGND pin lines near the ends of the current detection resistor (Rf).

5. Speed Lock Range

The speed lock range is ±6.25% of the fixed speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the motor on duty is adjusted according to the speed error to control the motor speed to be within the lock range.

6. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor (F) connected to the PWM pin.

$$f_{PWM} \approx 1/(64000 \times C)$$

A PWM frequency of between 15 and 25kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency during motor control, and if that frequency is in the audible range, that resonation may result in audible noise. If the PWM frequency is too high, the output transistor switching loss will increase. To make the circuit less susceptible to noise, the connected capacitors must be connected to the GND pin (pin 23) with lines that are as short as possible.

7. Hall effect sensor input signals

An input amplitude of over 100mVp-p is desirable in the Hall effect sensor inputs. The closer the input waveform is to a square wave, the lower the required input amplitude. Inversely, a higher input amplitude is required the closer the input waveform is to a triangular wave. Also note that the input DC voltage must be set to be within the commonmode input voltage range.

If noise on the Hall inputs is a problem, that noise must be excluded by inserting capacitors across the inputs. Those capacitors must be located as close as possible to the input pins.

When the Hall inputs for all three phases are in the same state, all the outputs will be in the off state.

If a Hall sensor IC is used to provide the Hall inputs, those signals can be input to one side (either the + or - side) of the Hall effect sensor signal inputs as 0 to $V_{CC}$ level signals if the other side is held fixed at a voltage within the common-mode input voltage range that applies when a Hall effect sensors are used.

8. Forward/Reverse Switching

The motor rotation direction can be switched using the F/R pin. However, the following notes must be observed if the motor direction is switched while the motor is turning.

- This IC is designed to avoid through currents when switching directions. However, increases in the motor supply voltage (due to instantaneous return of motor current to the power supply) during direction switching may cause problems. The values of the capacitors inserted between power and ground must be increased if this increase is excessive.
- If the motor current after direction switching exceeds the current limit value, the PWM drive side outputs will be turned off, but the opposite side output will be in the short-circuit braking state, and a current determined by the motor back EMF voltage and the coil resistance will flow. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which the direction is switched, the more severe this problem becomes.)

9. Brake Switching

The LB11921T provides a short-circuit brake implemented by turning the output transistors for the UH, VH, and WH pins for all phases on. (The opposite side transistors are turned off for all phases.) Note that the current limiter does not operate during braking. During braking, the duty is set to 100%, regardless of the motor speed. The current that flows in the output transistors during braking is determined by the motor back EMF voltage and the coil resistance. Applications must be designed so that this current does not exceed the ratings of the output transistors used. (The higher the motor speed at which braking is applied, the more severe this problem becomes.)

The braking function can be applied and released with the IC in the start state. This means that motor startup and stop control can be performed using the brake pin with the S/S pin held at the low level (the start state). If the startup time becomes excessive, it can be reduced by controlling motor startup and stop with the brake pin rather than with the S/S pin. (Since the IC goes to the power saving state when stopped, enough time for the VCO circuit to stabilize will be required at the beginning of the motor start operation.)

10. Constraint Protection Circuit

The LB11921T includes an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. If the LD output remains high (indicating the unlocked state) for a fixed period in the start state, the PWM output (external) transistors are turned off. This time is set by the capacitance of the capacitor attached to the CSD pin.

The set time (in seconds) is $15.1 \times C\ (\mu F)$

To clear the motor constrained protection state, the application must either switch to the stop or brake state for a fixed period (about 1ms or longer), or the power must be turned off and reapplied.

If the motor constrained protection circuit is not used, a 360kΩ resistor and a 3300pF capacitor must be connected in parallel between the CSD pin and ground. However, in that case, the clock disconnect protection circuit described below will no longer function. Since the CSD pin also functions as the power-on reset pin, if the CSD pin were connected directly to ground, the IC would go to the power-on reset state and motor drive operation would remain off. The power-on reset state is cleared when the CSD pin voltage rises above a level of about 0.25V.

11. Clock Disconnect Protection Circuit

If the clock input goes to the no input state when the IC is in the start state, this protection circuit will operate and turn off the PWM output. If the clock is resupplied before the motor constraint protection circuit operates, the IC will return to the drive state, but if the motor constraint protection circuit does operate, the IC must either be set temporarily (approximately 1 ms or over) to the stop or brake state, or the power must be turned off and reapplied.

12. Low-Voltage Protection Circuit

The LB11921T includes a low-voltage protection circuit to protect against incorrect operation when $V_{CC}$ power is applied or if the power supply voltage falls below its operating level. The (external) all output transistors are turned off if $V_{CC}$ falls under about 3.74 volts, and the protection function is cleared at about 3.93 volts or higher.

13. Power Supply Stabilization

Since this IC is used in applications that draw large output currents, the power-supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the $V_{CC}$ pin and ground. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.

14. Ground Lines

The signal system ground and the output system ground must be separated and a single ground point must be taken at the connector. Since the output system ground carries large currents, this ground line must be made as short as possible.

Output system ground --- Ground for Rf, output diodes, and 24V line capacitors
Signal system ground --- Ground for the IC, external components, and 5V line capacitors

15. FG Amplifier

The FG amplifier is normally implemented as a filter amplifier such as that shown in the application circuits to reject noise. Since a clamp circuit has been added at the FG amplifier output, the output amplitude is clamped at about 3Vp-p, even if the gain is increased.

Since a Schmitt comparator is inserted after the FG amplifier, applications must set the gain so that the amplifier output amplitude is at least 250mVp-p. (It is desirable that the gain be set so that the amplitude is over 0.5Vp-p at the lowest controlled speed to be used.)

The capacitor inserted between the FGIN+ pin (pin 20) and ground is required for bias voltage stabilization. To make the connected capacitor as immune from noise as possible, connect this capacitor to the GND pin (pin 23) with a line that is as short as possible.

16. Integrating Amplifier

The integrating amplifier integrates the speed error pulses and phase error pulses and converts them to the speed controlling voltage. At the same time it also sets the control loop gain and frequency characteristics.

External components necessary for the integrating amplifier must be placed as close to the IC as possible to reduce influence of noise.

17. FIL Pin External Components

The capacitor inserted between the FIL pin and ground is used to suppress ripple on the FIL pin voltage. Therefore, application designers must select a capacitance value that provides fully adequate smoothing of the FIL pin voltage even at the lowest external clock input frequency used. Also, the FIL pin voltage convergence time (the time until the reference signal stabilizes) when the input clock frequency is switched is shortened by connecting a resistor and a capacitor in series between the FIL pin and ground. Therefore, designers must select values for the resistor and capacitor that give the required convergence time.

18. R and C Pin External Components

The maximum range over which the reference signal frequency $f_{VCO}$ can be varied when 5V is used as the $V_{CC}$ supply voltage is about a factor of three.

When it is desirable to make this range as wide as possible, since the values of the R pin external resistor (R) and the C pin external capacitor (C) are determined by the maximum value of the reference signal frequency ($f_{VCO}1$) and the minimum value ($V_{CC}L$) of the $V_{CC}$ power supply due to unit-to-unit variations, R and C can be determined using the following procedure as a reference.

(1) Calculate R1 and C1 using the following formulas and determine values for R and C such that the conditions R ≤ R1 and C ≤ C1 will hold taking the sample-to-sample variations (including other issues such as temperature characteristics) into account.

$R1 = (V_{CC}L\text{-}2.2\ V)/370\mu A$

$C1 = (370\mu A/0.9V) \times (1/f_{VCO}1) \times 0.7$

(2) The minimum value ($f_{VCO}2$) for the reference signal frequency that can be set for the R and C values determined in step (1) can be calculated from the following formula if we let R2 and C2 be the smallest values for R and C due to the sample-to-sample variations (including other issues such as temperature characteristics). Therefore, the range over which the reference signal frequency can be set is $f_{VCO}1$ to $f_{VCO}2$.

$f_{VCO}2 = 0.38/(R2 \times C2)$

(3) The following are the conditions that must be met and the points that require care when determining the values of the external components connected to the R and C pins.

1. The maximum value of the set reference signal frequency must not exceed 1.2MHz.
2. The R pin voltage and the FIL pin voltage must be in the range 0.3V to ($V_{CC}L$-2.2V). ($V_{CC}L$ is the lowest value of the $V_{CC}$ supply voltage given the unit-to-unit variations. $V_{CC}L$ is always greater than or equal to 4.4V.) However, the lower the R pin voltage, the more susceptible the system will be to ground line noise, and the reference signal frequency may become unstable as a result. Therefore the lower end of the R pin voltage range must not be used if there is much ground line noise in the system.
3. Set the value of the R pin external resistor to a value in the range 5.6kΩ to 10kΩ. Also, assure that the R pin current remains under 370μA.
4. Set the value of the C pin external capacitor to a value in the range 220pF to 1000pF.
5. When it is desirable to make the range of the reference signal frequency as wide as possible, set the values of R and C to the largest possible values. (However, those values must be lower than the calculated values R1 and C1.) Use components with the smallest sample-to-sample variations possible. The $V_{CC}$ voltage must be made as much higher than 5V as possible to acquire the widest possible range for the reference signal frequency.

19. NC pin

Since the NC pins are electrically open with respect to the IC itself, they can be used as intermediate connection points for lines in the PCB pattern.