



LB11946 — Monolithic Digital IC

PWM Current Control Stepping Motor Driver

Overview

The LB11946 is a stepping motor driver IC that implements PWM current control bipolar drive with a fixed off time. This IC features 15 current setting levels using a fixed VREF voltage and support for microstepping drive from 1-2 phase excitation drive to 4W1-2 phase excitation drive. This device is optimal for driving stepping motors such as those used for carriage drive and paper feed in printers.

Features

- PWM current control (with a fixed off time)
- Logic input serial-parallel converter (allows 1-2, W1-2, 2W1-2, and 4W1-2 phase excitation drive)
- Current attenuation switching function (with slow decay, fast decay, and mixed decay modes)
- Built-in upper and lower side diodes
- Simultaneous on state prevention function (through current prevention)
- Noise canceller function
- Thermal shutdown circuit
- Shutoff on low logic system voltage circuit
- Low-power mode control pin

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	VBB		50	V
Peak output current	IO peak	tw ≤ 20 μS	1.2	A
Continuous output current	IO max		1.0	A
Logic system supply voltage	VCC		7.0	V
Logic input voltage range	VIN		-0.3 to VCC	V
Emitter output voltage	VE	VCC = 5 V specifications	1.0	V
	VE	VCC = 3.3 V specifications	0.5	V
Allowable power dissipation (IC internal)	Pdmax	Ta = 25°C, independent IC	3.0	W
Operating temperature	Topr		-20 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

■ Any and all SANYO Semiconductor products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO Semiconductor representative nearest you before using any SANYO Semiconductor products described or contained herein in such applications.

■ SANYO Semiconductor assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor products described or contained herein.

LB11946

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Motor supply voltage	V _{BB}		10 to 45	V
Logic system supply voltage	V _{CC}	V _{CC} = 5 V specifications	4.5 to 5.5	V
		V _{CC} = 3.3 V specifications	3.0 to 3.6	V
Reference voltage	V _{REF}	V _{CC} = 5 V specifications	0.0 to 3.0	V
		V _{CC} = 3.3 V specifications	0.0 to 1.0	V

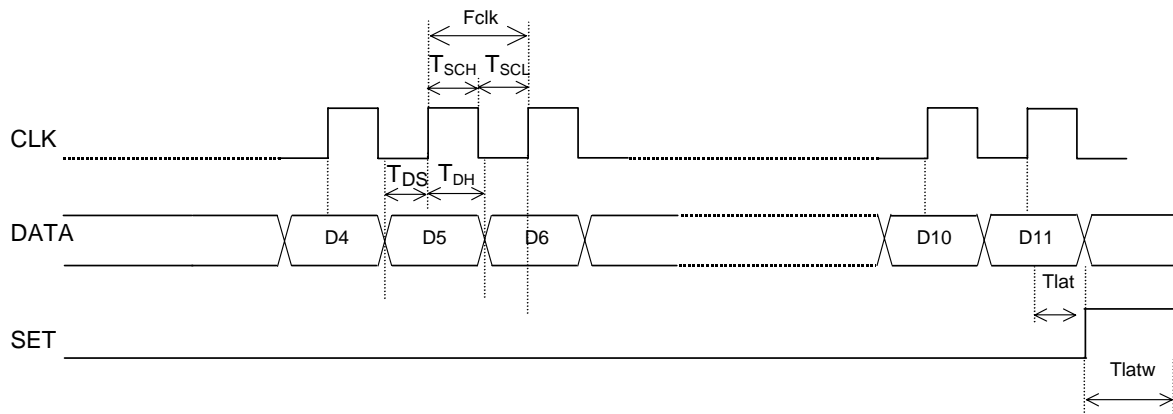
Electrical Characteristics at Ta = 25°C, V_{CC} = 5 V, V_{BB} = 42 V, V_{REF} = 1.52 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Output Block]						
Output stage supply current	IBB-ON		0.9	1.3	1.7	mA
	IBB-OFF		0.52	0.7	1.05	mA
Output saturation voltage 1	V _{O(sat) 1}	I _O = +0.5 A (sink)		1.1	1.4	V
Output saturation voltage 2	V _{O(sat) 2}	I _O = +1.0 A (sink)		1.4	1.7	V
Output saturation voltage 3	V _{O(sat) 3}	I _O = -0.5 A (source)		1.9	2.2	V
Output saturation voltage 4	V _{O(sat) 4}	I _O = -1.0 A (source)		2.2	2.5	V
Output leakage current	I _{O1} (leak)	V _O = V _{BB} (sink)			50	μA
	I _{O2} (leak)	V _O = 0V (source)	-50			μA
Output sustain voltage	V _{SUS}	L = 15 mH, I _O = 1.0 A *	45			V
[Logic Block]						
Logic system supply current	I _{CC ON}	D0 = 1, D1 = 1, D2 = 1, D3 = 1 When these data values are set	24	35	46	mA
	I _{CC OFF1}	D0 = 0, D1 = 0, D2 = 0, D3 = 0	22	32	42	mA
	I _{CC OFF2}	ST = LOW		0.05	0.1	mA
Input voltage	V _{IH}		2			V
	V _{IL}				0.8	V
Input current	I _{IH}	V _{IH} = 2 V			35	μA
	I _{IL}	V _{IL} = 0.8 V	6			μA
Sense voltages	V _E	D0 = 1, D1 = 1, D2 = 1, D3 = 1 When these data values are set	0.470	0.50	0.525	V
		D0 = 1, D1 = 1, D2 = 1, D3 = 0	0.445	0.48	0.505	V
		D0 = 1, D1 = 1, D2 = 0, D3 = 1	0.425	0.46	0.485	V
		D0 = 1, D1 = 1, D2 = 0, D3 = 0	0.410	0.43	0.465	V
		D0 = 1, D1 = 0, D2 = 1, D3 = 1	0.385	0.41	0.435	V
		D0 = 1, D1 = 0, D2 = 1, D3 = 0	0.365	0.39	0.415	V
		D0 = 1, D1 = 0, D2 = 0, D3 = 1	0.345	0.37	0.385	V
		D0 = 1, D1 = 0, D2 = 0, D3 = 0	0.325	0.35	0.365	V
		D0 = 0, D1 = 1, D2 = 1, D3 = 1	0.280	0.30	0.325	V
		D0 = 0, D1 = 1, D2 = 1, D3 = 0	0.240	0.26	0.285	V
		D0 = 0, D1 = 1, D2 = 0, D3 = 1	0.195	0.22	0.235	V
		D0 = 0, D1 = 1, D2 = 0, D3 = 0	0.155	0.17	0.190	V
		D0 = 0, D1 = 0, D2 = 1, D3 = 1	0.115	0.13	0.145	V
D0 = 0, D1 = 0, D2 = 1, D3 = 0	0.075	0.09	0.100	V		
Reference current	I _{REF}	V _{REF} = 1.5 V	-0.5			μA
CR pin current	ICR	CR = 1.0 V	-1.6	-1.2	-0.8	mA
MD pin current	IMD	MD = 1.0 V, CR = 4.0 V	-5.0			μA
Logic system on voltage	VLSDON		2.6	2.8	3.0	V
Logic system off voltage	VLSDOFF		2.45	2.65	2.85	V
LVSD hysteresis	VLHIS		0.03	0.15	0.35	V
Thermal shutdown temperature	T _s	Design guarantee		170		°C

LB11946

AC Electrical Characteristics at $V_{CC} = 5\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock frequency	Fclk	$V_{CC} = 5.0\text{ V}$		200	550	kHz
Data setup time	T_{DS}	$V_{CC} = 5.0\text{ V}$	0.9	2.5		μS
Data hold time	T_{DH}	$V_{CC} = 5.0\text{ V}$	0.9	2.5		μS
Minimum clock high-level pulse width	T_{SCH}	$V_{CC} = 5.0\text{ V}$	0.9	2.5		μS
Minimum clock low-level pulse width	T_{SCL}	$V_{CC} = 5.0\text{ V}$	0.9	2.5		μS
SET pin stipulated time	Tlat	$V_{CC} = 5.0\text{ V}$	0.9	2.5		μS
SET pin signal pulse width	Tlatw	$V_{CC} = 5.0\text{ V}$	1.9	5.0		μS



LB11946

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$, $V_{BB} = 42\text{ V}$, $V_{REF} = 1.0\text{ V}$

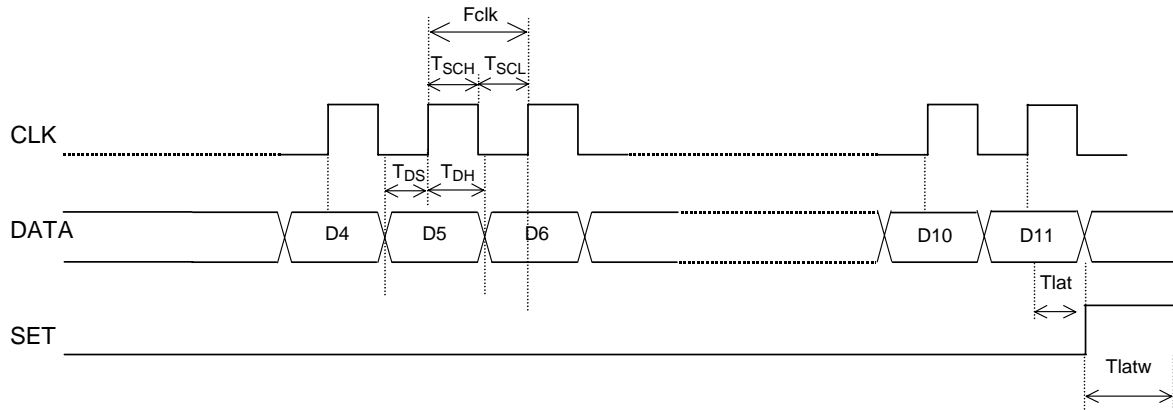
(When measuring the sense voltage: $V_{REF} = 1.03\text{ V}$)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Output Block]						
Output stage supply current	$I_{BB\text{ ON}}$		0.9	1.3	1.7	mA
	$I_{BB\text{ OFF}}$		0.52	0.7	1.05	mA
Output saturation voltage 1	$V_{O(\text{sat})\ 1}$	$I_O = +0.5\text{ A}$ (sink)		1.2	1.5	V
Output saturation voltage 2	$V_{O(\text{sat})\ 2}$	$I_O = +1.0\text{ A}$ (sink)		1.5	1.8	V
Output saturation voltage 3	$V_{O(\text{sat})\ 3}$	$I_O = -0.5\text{ A}$ (source)		2.0	2.3	V
Output saturation voltage 4	$V_{O(\text{sat})\ 4}$	$I_O = -1.0\text{ A}$ (source)		2.3	2.6	V
Output leakage current	I_{O1} (leak)	$V_O = V_{BB}$ (sink)			50	μA
	I_{O2} (leak)	$V_O = 0\text{ V}$ (source)	-50			μA
Output sustain voltage	V_{SUS}	$L = 15\text{ mH}$ $I_O = -1.5\text{ A}$ *	45			V
[Logic Block]						
Logic system supply current	$I_{CC\text{ ON}}$	$D0 = 1, D1 = 1, D2 = 1, D3 = 1$ When these data values are set	21	30	39	mA
	$I_{CC\text{ OFF}1}$	$D0 = 0, D1 = 0, D2 = 0, D3 = 0$	19	28	36.5	mA
	$I_{CC\text{ OFF}2}$	$ST = 0.8\text{ V}$		0.03	0.1	mA
Input voltage	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	I_{IH}	$V_{IH} = 2\text{ V}$			35	μA
	I_{IL}	$V_{IL} = 0.8\text{ V}$	6			μA
Sense voltages	VE	$D0 = 1, D1 = 1, D2 = 1, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.303	0.330	0.356	V
		$D0 = 1, D1 = 1, D2 = 1, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.290	0.315	0.341	V
		$D0 = 1, D1 = 1, D2 = 0, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.276	0.300	0.324	V
		$D0 = 1, D1 = 1, D2 = 0, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.263	0.286	0.309	V
		$D0 = 1, D1 = 0, D2 = 1, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.250	0.272	0.294	V
		$D0 = 1, D1 = 0, D2 = 1, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.236	0.257	0.278	V
		$D0 = 1, D1 = 0, D2 = 0, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.223	0.243	0.263	V
		$D0 = 1, D1 = 0, D2 = 0, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.209	0.228	0.247	V
		$D0 = 0, D1 = 1, D2 = 1, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.183	0.200	0.217	V
		$D0 = 0, D1 = 1, D2 = 1, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.155	0.170	0.185	V
		$D0 = 0, D1 = 1, D2 = 0, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.128	0.143	0.158	V
		$D0 = 0, D1 = 1, D2 = 0, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.102	0.114	0.126	V
		$D0 = 0, D1 = 0, D2 = 1, D3 = 1$ $V_{REF} = 1.03\text{ V}$	0.074	0.085	0.096	V
		$D0 = 0, D1 = 0, D2 = 1, D3 = 0$ $V_{REF} = 1.03\text{ V}$	0.047	0.057	0.067	V
Reference current	I_{REF}	$V_{REF} = 1.0\text{ V}$	-0.5			μA
CR pin current	ICR	$CR = 1.0\text{ V}$	-0.91	-0.7	-0.49	mA
MD pin current	IMD	$MD = 1.0\text{ V}$, $CR = 4.0\text{ V}$	-5.0			μA
LVSD voltage	VLSDON		2.6	2.8	3.0	V
Logic system off voltage	VLSDOFF		2.45	2.65	2.85	V
LVSD hysteresis	VLHIS		0.03	0.15	0.35	V
Thermal shutdown temperature	T_s	Design guarantee		170		$^\circ\text{C}$

LB11946

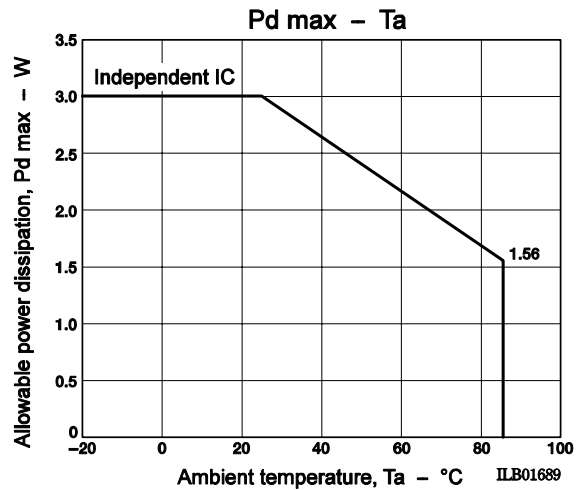
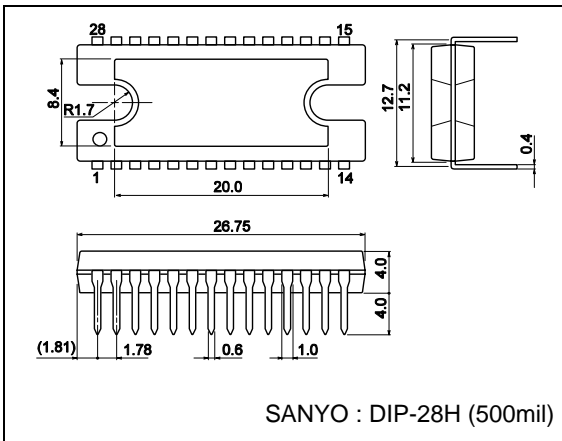
AC Electrical Characteristics at $V_{CC} = 3.3\text{ V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock frequency	Fclk	$V_{CC} = 3.3\text{ V}$		200	550	kHz
Data setup time	T_{DS}	$V_{CC} = 3.3\text{ V}$	0.9	2.5		μS
Data hold time	T_{DH}	$V_{CC} = 3.3\text{ V}$	0.9	2.5		μS
Minimum clock high-level pulse width	T_{SCH}	$V_{CC} = 3.3\text{ V}$	0.9	2.5		μS
Minimum clock low-level pulse width	T_{SCL}	$V_{CC} = 3.3\text{ V}$	0.9	2.5		μS
SET pin stipulated time	Tlat	$V_{CC} = 3.3\text{ V}$	0.9	2.5		μS
SET pin signal pulse width	Tlatw	$V_{CC} = 3.3\text{ V}$	1.9	5.0		μS



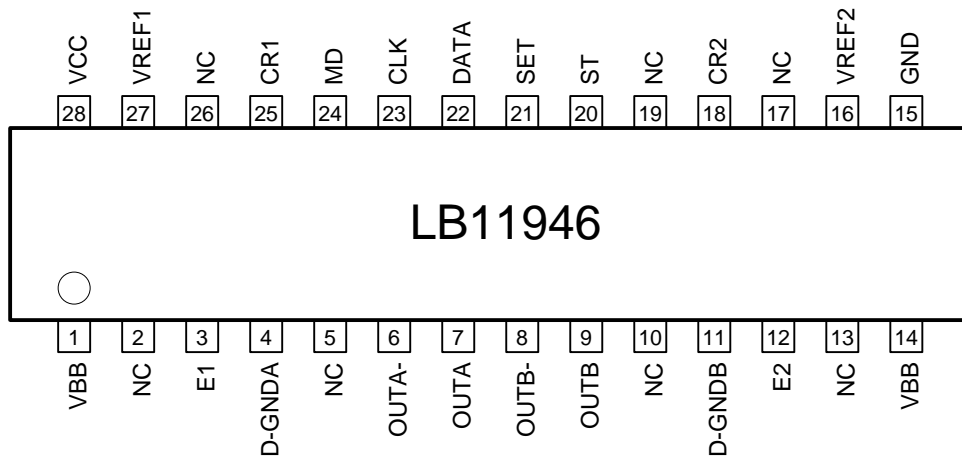
Package Dimensions

unit: mm
3147C



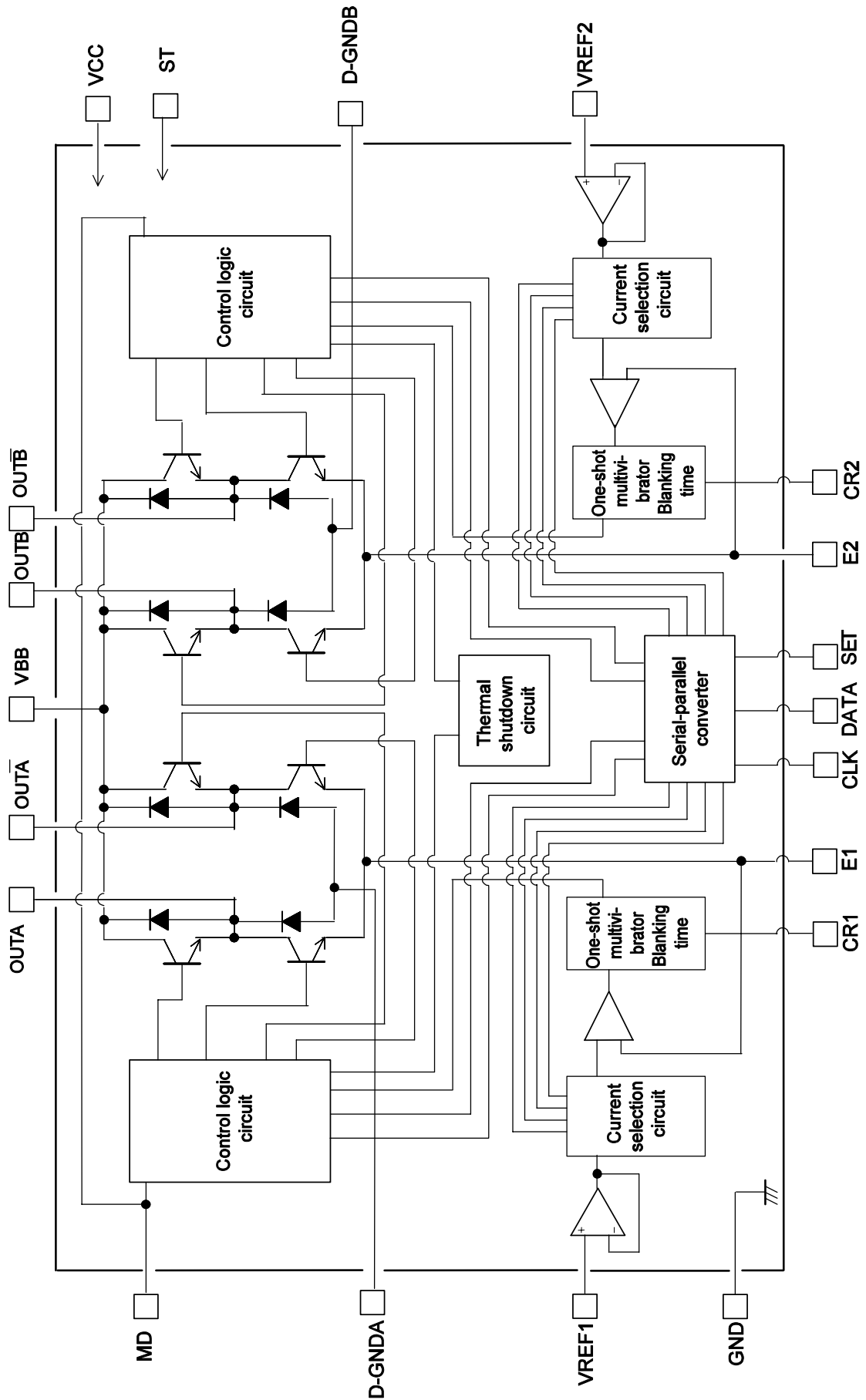
LB11946

Pin Assignment

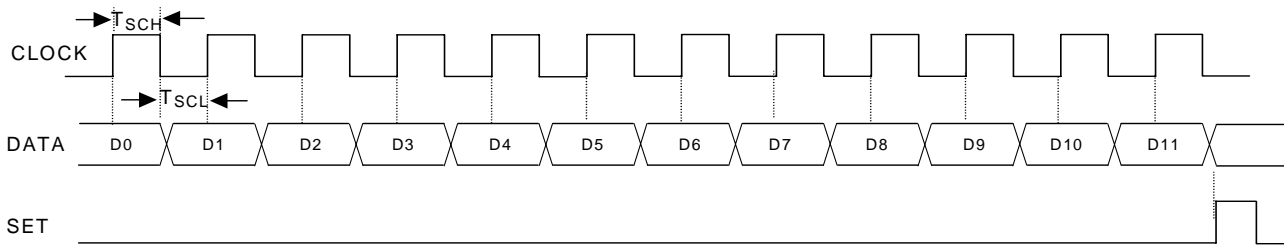


Note *: The D-GNDA and D-GNDB pins are the anode sides of the lower side diodes.

Block Diagram



Timing Chart



Serially Transferred Data Definition

No.	IA4	IA3	IA2	IA1	DE1	PH1	IB4	IB3	IB2	IB1	DE2	PH2	Output mode				I/O ratio	DEC MODE
	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	OUTA	OUTA	OUTB	OUTB		
0	1	1	1	1	1	1	1	1	1	1	1	1	H	L	H	L	100%	SLOW
1	1	1	1	0	1	1	1	1	1	0	1	1	H	L	H	L	96	SLOW
2	1	1	0	1	1	1	1	1	0	1	1	1	H	L	H	L	91	SLOW
3	1	1	0	0	1	1	1	1	0	0	1	1	H	L	H	L	87	SLOW
4	1	0	1	1	1	1	1	0	1	1	1	1	H	L	H	L	83	SLOW
5	1	0	1	0	1	1	1	0	1	0	1	1	H	L	H	L	78	SLOW
6	1	0	0	1	1	1	1	0	0	1	1	1	H	L	H	L	74	SLOW
7	1	0	0	0	1	1	1	0	0	0	1	1	H	L	H	L	70	SLOW
8	0	1	1	1	1	1	0	1	1	1	1	1	H	L	H	L	61	SLOW
9	0	1	1	0	1	1	0	1	1	0	1	1	H	L	H	L	52	SLOW
10	0	1	0	1	1	1	0	1	0	1	1	1	H	L	H	L	44	SLOW
11	0	1	0	0	1	1	0	1	0	0	1	1	H	L	H	L	35	SLOW
12	0	0	1	1	1	1	0	0	1	1	1	1	H	L	H	L	26	SLOW
13	0	0	1	0	1	1	0	0	1	0	1	1	H	L	H	L	17	SLOW
14	1	1	1	1	0	0	1	1	1	1	0	0	L	H	L	H	100	FAST
15	1	1	1	0	0	0	1	1	1	0	0	0	L	H	L	H	96	FAST
16	1	1	0	1	0	0	1	1	0	1	0	0	L	H	L	H	91	FAST
17	1	1	0	0	0	0	1	1	0	0	0	0	L	H	L	H	87	FAST
18	1	0	1	1	0	0	1	0	1	1	0	0	L	H	L	H	83	FAST
19	1	0	1	0	0	0	1	0	1	0	0	0	L	H	L	H	78	FAST
20	1	0	0	1	0	0	1	0	0	1	0	0	L	H	L	H	74	FAST
21	1	0	0	0	0	0	1	0	0	0	0	0	L	H	L	H	70	FAST
22	0	1	1	1	0	0	0	1	1	1	0	0	L	H	L	H	61	FAST
23	0	1	1	0	0	0	0	1	1	0	0	0	L	H	L	H	52	FAST
24	0	1	0	1	0	0	0	1	0	1	0	0	L	H	L	H	44	FAST
25	0	1	0	0	0	0	0	1	0	0	0	0	L	H	L	H	35	FAST
26	0	0	1	1	0	0	0	0	1	1	0	0	L	H	L	H	26	FAST
27	0	0	1	0	0	0	0	0	1	0	0	0	L	H	L	H	17	FAST
28	0	0	0	0	*	*	0	0	0	0	*	*	OFF	OFF	OFF	OFF	0	-

Note *: Either 0 or 1.

Note *1: In mixed decay mode, set D4 and D10 to 0 and set the MD pin to a level in the range 1.5 to 4.0 V.

LB11946

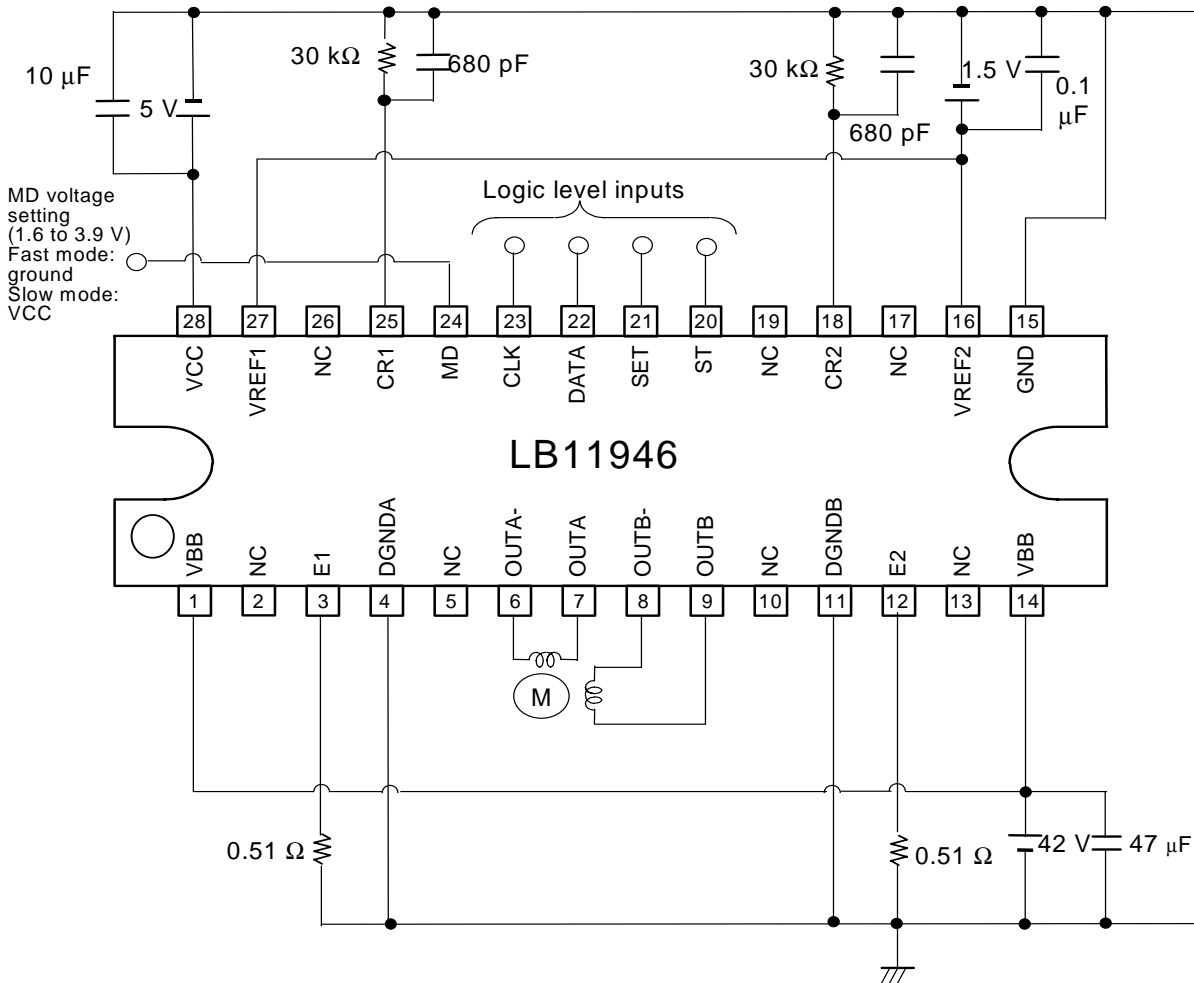
Current Settings Truth Table

Current Settings Truth Table * Items in parentheses are defined by the serial data.

IA4 (D0)	IA3 (D1)	IA2 (D2)	IA1 (D3)	Set current Iout	Current ratio (%)
1	1	1	1	$11.5/11.5 \times VREF/3.04RE = Iout$	100
1	1	1	0	$11.0/11.5 \times VREF/3.04RE = Iout$	95.65
1	1	0	1	$10.5/11.5 \times VREF/3.04RE = Iout$	91.30
1	1	0	0	$10.0/11.5 \times VREF/3.04RE = Iout$	86.95
1	0	1	1	$9.5/11.5 \times VREF/3.04RE = Iout$	82.61
1	0	1	0	$9.0/11.5 \times VREF/3.04RE = Iout$	78.26
1	0	0	1	$8.5/11.5 \times VREF/3.04RE = Iout$	73.91
1	0	0	0	$8.0/11.5 \times VREF/3.04RE = Iout$	69.56
0	1	1	1	$7.0/11.5 \times VREF/3.04RE = Iout$	60.87
0	1	1	0	$6.0/11.5 \times VREF/3.04RE = Iout$	52.17
0	1	0	1	$5.0/11.5 \times VREF/3.04RE = Iout$	43.48
0	1	0	0	$4.0/11.5 \times VREF/3.04RE = Iout$	34.78
0	0	1	1	$3.0/11.5 \times VREF/3.04RE = Iout$	26.08
0	0	1	0	$2.0/11.5 \times VREF/3.04RE = Iout$	17.39

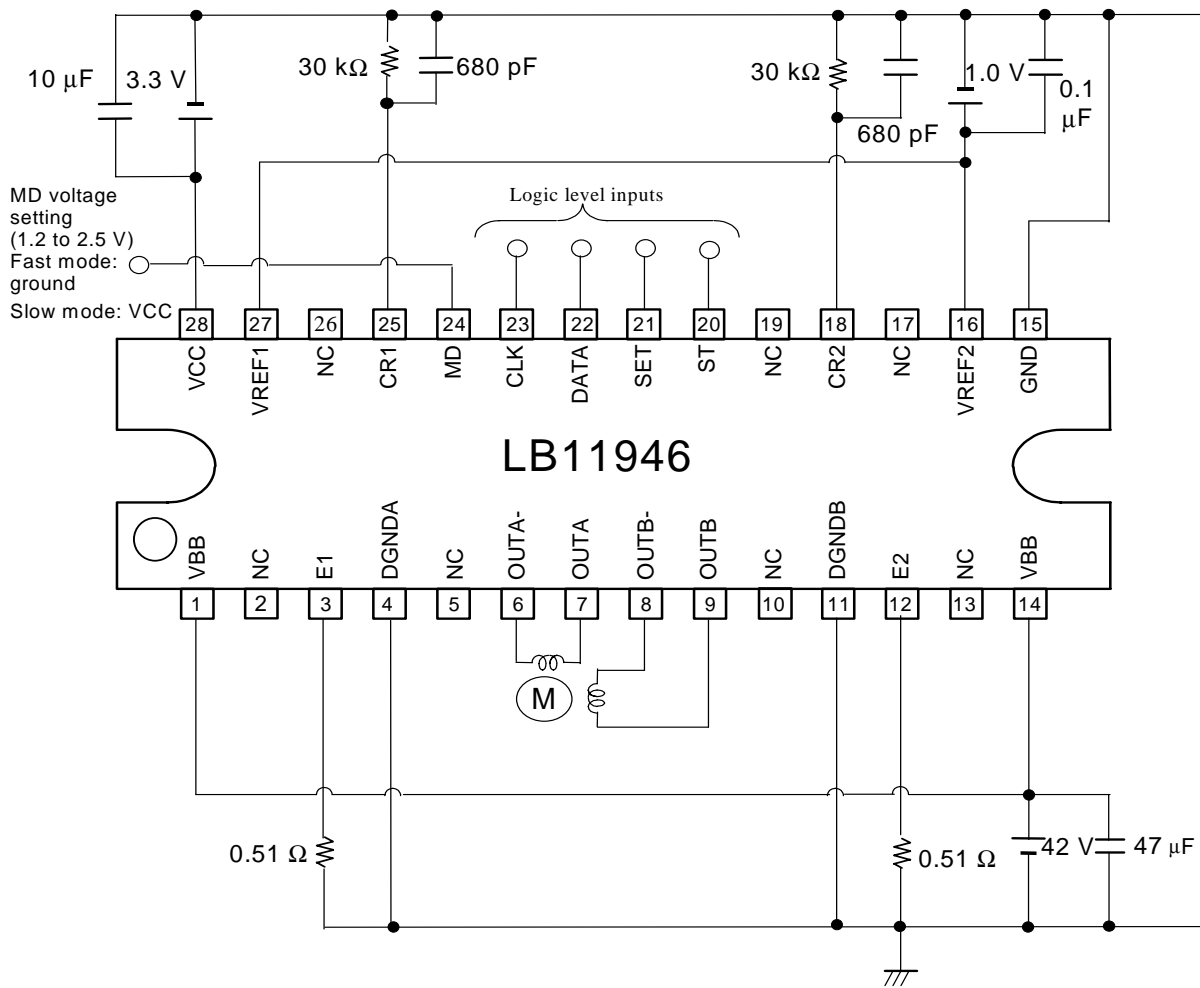
Note *: The current ratios shown are calculated values.

Sample Application Circuit at $V_{CC} = 5 V$



LB11946

Sample Application Circuit at $V_{CC} = 3.3\text{ V}$



Switching Off Time and Noise Canceller Time Calculations

Notes on the CR Pin Setting (switching off time and noise canceller time)

The noise canceller time (Tn) and the switching off time (Toff) are set using the following formulas.

- When V_{CC} is 5 V

Noise canceller time (Tn)

$$T_n \approx C \cdot R \cdot \ln\{(1.5 - RI)/(4.0 - RI)\} [s]$$

CR pin charge current: 1.25 mA

Switching off time (Toff)

$$T_{off} \approx -C \cdot R \cdot \ln(1.5/4.8) [s]$$

Component value ranges

R: 5.6 kΩ to 100 kΩ

C: 470 pF to 2000 pF

- When V_{CC} is 3.3 V

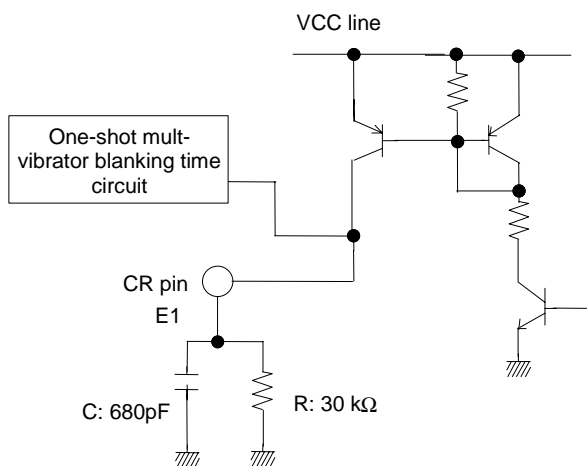
Noise canceller time (Tn)

$$T_n \approx C \cdot R \cdot \ln\{(1.06 - RI)/(2.66 - RI)\} [s]$$

CR pin charge current: 0.7 mA

Switching off time (Toff)

$$T_{off} \approx -C \cdot R \cdot \ln(1.06/3.1) [s]$$



CR Pin Internal Circuit Structure

Notes on the MD Pin

- If slow decay mode is set up by setting the D4 and D10 bits in the input serial data to 1, the MD pin must be shorted to ground.
- If fast decay mode is set up by setting the D4 and D10 bits in the input serial data to 0, mixed decay mode can be set with the MD pin.
 When the V_{CC} = 5 V specifications are used the setting voltage range for mixed decay mode is 1.6 to 3.9 V.
 When the V_{CC} = 3.3 V specifications are used the setting voltage range for mixed decay mode is 1.2 to 2.5 V.
 If mixed decay mode will not be used with the fast decay mode setting, either:
 - (a) Short the MD pin to ground to select fast decay mode, or
 - (b) Short the MD pin to V_{CC} to select slow decay mode.

Usage Notes

- Notes on the V_{REF} pin

Since the V_{REF} pin inputs the reference voltage used to set the current, applications must be designed so that noise does not occur at this pin.

- Notes on the ground pins

Since this IC switches large currents, care is required with respect to the ground pins.

The PCB pattern in sections where large currents flow must be designed with low impedances and must be kept separate from the small-signal system.

In particular, the ground terminals of the E1 and E2 pin sense resistors (RE) and the external Schottky barrier diode ground terminals must be located as close as possible to the IC ground. The capacitors between V_{CC} and ground and between V_{BB} and ground must be as close as possible to the corresponding V_{CC} and V_{BB} pin in the pattern.

- Power on sequence

When turning the power systems on

$V_{CC} \rightarrow$ logic level inputs (CLK, DATA, SET, and ST) $\rightarrow V_{REF} \rightarrow V_{BB}$

When turning the power systems off

$V_{BB} \rightarrow V_{REF} \rightarrow$ logic level inputs (CLK, DATA, SET, and ST) $\rightarrow V_{CC}$

Note that if the power supply for the logic level inputs is on when the V_{CC} power supply is off, a bias with an unstable state will be applied due to the protection diodes at the V_{CC} pins, and this can cause incorrect operation.

- Specifications of any and all SANYO Semiconductor products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Semiconductor Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Semiconductor Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO Semiconductor believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of July, 2004. Specifications and information herein are subject to change without notice.