



Three-Phase Brushless Motor Driver for DC Fan

Overview

The LB1695D is a driver IC for 3-phase brushless DC fan motors such as used in water heaters and other domestic electrical appliances.

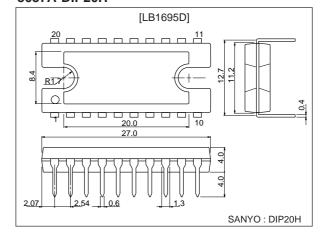
Features

- · Three-phase brushless motor driver
- Withstand voltage 45V, output current 2A
- Built-in current limiter
- Built-in low-voltage protection circuit
- · Built-in thermal shutdown circuit
- Built-in Hall amplifier with hysteresis
- FG output function

Package Dimensions

unit: mm

3037A-DIP20H



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum aunah valtaga	V _{CC} max		10	V
Maximum supply voltage	V _M max		45	V
Maximum output current	I _O max		2.0	А
Allowahla nawan diadinatian	Pd max1	IC only	3	W
Allowable power dissipation	Pd max2	With an arbitrary large heat sink	20	W
Operating temperature	Topr		-20 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Dower cumply voltage range	V _{CC}		4.5 to 9.0	V
Power supply voltage range	V _M		5 to 42	V
Power supply startup voltage slew	$\Delta V_{CC}/\Delta t$	$V_{CC} = V_{LVSD}$ (OFF) point *1	Up to 0.04	V / μs
rate	$\Delta V_{M}/\Delta t$	$V_{M} = 0V \text{ point}$ *1	Up to 0.16	V / μs

^{*1} After power-on, if the power supply voltage rise is fast, there may be some feedthrough current in the output.

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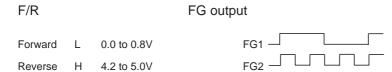
LB1695D

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, V_{M} = 30V

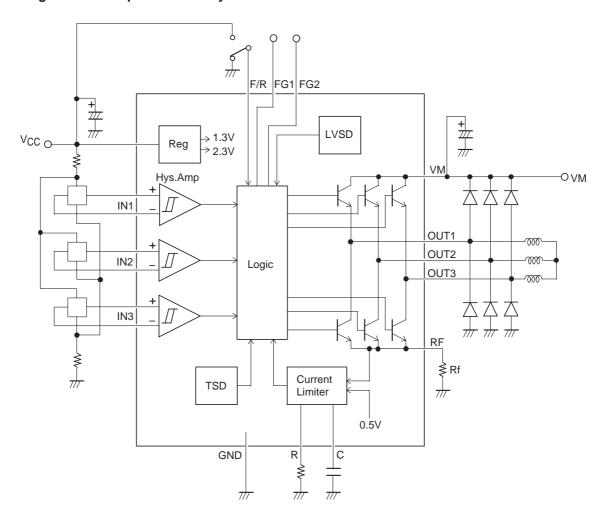
Power supply current I_{CC} Forward		Symbol	Conditions	Ratings			11-7	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Parameter			min	typ	max	Unit	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Power supply current	I _{CC}	Forward		13	19	mA	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Outside a femalia and the sea	V _O sat1	$I_O = 0.5A V_O (sink) + V_O (source)$		1.8	2.4	V	
Hall amplifier] Input bias current I HB Common mode input voltage range VI _{CM} Input bias current VI _{CM} Input bias current VI _{CM} Input bias current VI _{CM} Input voltage range VI _{CM} Input voltage L > H V _{CC} -1.8 V V-C-1.8	Output saturation voltage	V _O sat2	I _O = 1.0A V _O (sink) + V _O (source)		2.1	2.8	V	
The common mode input voltage range V V V V V V V V V	Output leakage current	I _O leak				100	μΑ	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	[Hall amplifier]							
	Input bias current	I HB			1	4	μΑ	
Hysteresis width $\Delta V_{ N}$	Common mode input voltage range	V _{ICM}		1.5		V _{CC} -1.8	V	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Hysteresis width	ΔV_{IN}		21	30		mV	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input voltage L -> H	V _{SLH}		5	15	25	mV	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Input voltage H -> L	V _{SHL}		-25	-15	-5	mV	
Pull-up resistor value R_{FG} 7.5 10 12.5 R_{C} 7.5 Forward/reverse operation] Forward V_{FR1} 0 0 0.8 V_{C} 7.5 Forward/reverse operation] Forward V_{FR2} 4.2 V_{CC} V_{C}	[FG pin (Speed pulse output)]							
Pull-up resistor value R_{FG} 7.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 12.5 10 10 10 10 10 10 10 10	Output Low level voltage	V _{FGL}	I _{FG} = 5 mA			0.4	V	
Forward V_{FR1} 0	Pull-up resistor value	R _{FG}		7.5	10	12.5	kΩ	
Reverse V_{FR2} 4.2 V_{CC} V Current limiter operation] Limiter V_{RF} 0.42 0.5 0.6 V Thermal shutdown operation] Operating temperature TSD Design target value 150 180 °C Hysteresis width ΔTSD Design target value 40 °C Low-voltage protection circuit operation] Operating voltage V_{LVSD} 3.5 3.8 4.1 V Release voltage V_{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 1 ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 2 ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 2 ΔV_{LVSD} (OFF) 0.4 0.5 ΔV_{LVSD} (OFF) Charge current I_{CL} R = 33 kΩ 30 40 50 μ A <td col<="" td=""><td>[Forward/reverse operation]</td><td></td><td></td><td></td><td></td><td></td><td></td></td>	<td>[Forward/reverse operation]</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	[Forward/reverse operation]						
Reverse V_{FR2} 4.2 V_{CC} V Current limiter operation] Limiter V_{RF} 0.42 0.5 0.6 V Thermal shutdown operation] Operating temperature TSD Design target value 150 180 °C Hysteresis width ΔTSD Design target value 40 °C Low-voltage protection circuit operation] Operating voltage V_{LVSD} 3.5 3.8 4.1 V Release voltage V_{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 1 ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 2 ΔV_{LVSD} (OFF) 0.4 0.5 0.6 V Cip in June 2 ΔV_{LVSD} (OFF) 0.4 0.5 ΔV_{LVSD} (OFF) Charge current I_{CL} R = 33 kΩ 30 40 50 μ A <td col<="" td=""><td>Forward</td><td>V_{FR1}</td><td></td><td>0</td><td></td><td>0.8</td><td>V</td></td>	<td>Forward</td> <td>V_{FR1}</td> <td></td> <td>0</td> <td></td> <td>0.8</td> <td>V</td>	Forward	V _{FR1}		0		0.8	V
Current limiter operation] Limiter V_{RF} 0.42 0.5 0.6 V Thermal shutdown operation] Operating temperature TSD Design target value	Reverse	V _{FR2}		4.2		V _{CC}	V	
Thermal shutdown operation] Operating temperature TSD Design target value 150 180 °C Hysteresis width Δ TSD Design target value 40 °C Hysteresis width Δ TSD Design target value 40 °C How-voltage protection circuit operation] Operating voltage V_{LVSD} 3.5 3.8 4.1 V Release voltage V_{LVSD} 4.3 4.5 V Hysteresis width Δ VLVSD 4.3 4.5 V Hysteresis width Δ VLVSD 5.0 6 V 6.5 V 6.6 V 7.6 V 7.6 V 8.7 V 8.7 V 8.7 V 9.7 V 9.8 V 9.9 V 9.1 V 9.9 V 9.1 V 9.	[Current limiter operation]	•						
Operating temperatureTSDDesign target value150180°CHysteresis width Δ TSDDesign target value40°C(Low-voltage protection circuit operation)Operating voltage V_{LVSD} 3.53.84.1VRelease voltage V_{LVSD} (OFF)4.34.5VHysteresis width Δ V $_{LVSD}$ 0.40.50.6VC pin]Charge currentICLR = 33 kΩ304050μADischarge currentICHR = 33 kΩ90120150μACharge start voltageVCLR = 33 kΩ0.30.40.5VDischarge start voltageVCHR = 33 kΩ1.52.02.5VOutput current ignore timet smR = 33 kΩ, C = 4700 pF586878μs	Limiter	V _{RF}		0.42	0.5	0.6	V	
Hysteresis width ΔTSD Design target value 40 °C How-voltage protection circuit operation] Operating voltage V_{LVSD} 3.5 3.8 4.1 V Release voltage V_{LVSD} 4.3 4.5 V Hysteresis width ΔV_{LVSD} 4.3 4.5 V Hysteresis width ΔV_{LVSD} 4.3 4.5 V Homeometric relationship in the product of the	[Thermal shutdown operation]							
Cov-voltage protection circuit operation V _{LVSD} 3.5 3.8 4.1 V Release voltage V _{LVSD} 0.4 0.5 0.6 V V V V V V V V V	Operating temperature	TSD	Design target value	150	180		°C	
Operating voltage V_{LVSD} 3.5 3.8 4.1 V Release voltage V_{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V (C pin] Charge current I CL R = 33 kΩ 30 40 50 μA Discharge current I CH R = 33 kΩ 90 120 150 μA Charge start voltage V CL R = 33 kΩ 0.3 0.4 0.5 V Discharge start voltage V CH R = 33 kΩ 1.5 2.0 2.5 V Output current ignore time t sm R = 33 kΩ, C = 4700 pF 58 68 78 μs	Hysteresis width	ΔTSD	Design target value		40		°C	
Release voltage $V_{LVSD}(OFF)$ 4.3 4.5 V Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V C pin] Charge current I_{CL} R = 33 k Ω 30 40 50 μ A Charge current I_{CH} R = 33 k Ω 90 120 150 μ A Charge start voltage V_{CL} R = 33 k Ω 0.3 0.4 0.5 V Discharge start voltage V_{CH} R = 33 k Ω 1.5 2.0 2.5 V Output current ignore time t sm R = 33 k Ω , C = 4700 pF 58 68 78 μ s	[Low-voltage protection circuit operati	on]						
Release voltage V_{LVSD} (OFF) 4.3 4.5 V Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V IC pin] Charge current ICL R = 33 k Ω 30 40 50 μ A Discharge current ICH R = 33 k Ω 90 120 150 μ A Charge start voltage VCL R = 33 k Ω 0.3 0.4 0.5 V Discharge start voltage VCH R = 33 k Ω 1.5 2.0 2.5 V Output current ignore time t sm R = 33 k Ω , C = 4700 pF 58 68 78 μ s	Operating voltage	V _{LVSD}		3.5	3.8	4.1	V	
Hysteresis width ΔV_{LVSD} 0.4 0.5 0.6 V (C pin] Charge current I _{CL} R = 33 kΩ 30 40 50 μA Discharge current I _{CH} R = 33 kΩ 90 120 150 μA Charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V Discharge start voltage V _{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current ignore time t sm R = 33 kΩ, C = 4700 pF 58 68 78 μs	Release voltage	V _{LVSD} (OFF)			4.3	4.5	V	
Charge current I _{CL} R = 33 kΩ 30 40 50 μA Discharge current I _{CH} R = 33 kΩ 90 120 150 μA Charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V Discharge start voltage V _{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current ignore time t sm R = 33 kΩ, C = 4700 pF 58 68 78 μs	Hysteresis width			0.4	0.5	0.6	V	
Discharge current I_{CH} $R = 33 \text{ k}\Omega$ 90 120 150 μA Charge start voltage V_{CL} $R = 33 \text{ k}\Omega$ 0.3 0.4 0.5 V Discharge start voltage V_{CH} $R = 33 \text{ k}\Omega$ 1.5 2.0 2.5 V Output current ignore time t sm $R = 33 \text{ k}\Omega$, $C = 4700 \text{ pF}$ 58 68 78 μs	[C pin]							
Charge start voltage V_{CL} R = 33 k Ω 0.3 0.4 0.5 V Discharge start voltage V_{CH} R = 33 k Ω 1.5 2.0 2.5 V Output current ignore time t sm R = 33 k Ω , C = 4700 pF 58 68 78 μ s	Charge current	I _{CL}	$R = 33 \text{ k}\Omega$	30	40	50	μΑ	
Charge start voltage V _{CL} R = 33 kΩ 0.3 0.4 0.5 V Discharge start voltage V _{CH} R = 33 kΩ 1.5 2.0 2.5 V Output current ignore time t sm R = 33 kΩ, C = 4700 pF 58 68 78 μs	Discharge current		$R = 33 \text{ k}\Omega$	90	120	150	μΑ	
Discharge start voltage V_{CH} R = 33 k Ω 1.5 2.0 2.5 V Output current ignore time t sm R = 33 k Ω , C = 4700 pF 58 68 78 μ s	Charge start voltage		$R = 33 \text{ k}\Omega$	0.3	0.4	0.5	V	
Output current ignore time t sm R = 33 k Ω , C = 4700 pF 58 68 78 μ s	Discharge start voltage		$R = 33 \text{ k}\Omega$	1.5	2.0	2.5	V	
Dutput off time t so $R = 33 \text{ k}\Omega$, $C = 4700 \text{ pF}$ 164 193 222 μs	Output current ignore time		R = 33 kΩ, C = 4700 pF	58	68	78	μs	
	Output off time	t so	R = 33 kΩ, C = 4700 pF	164	193	222	μs	

Truth Table

	Input		Input Forward/reverse control Output		FG output								
	IN1	IN2	IN3	F/R	Source -> Sink	FG1	FG2						
4	Н		- 11	L	OUT2 -> OUT1		L						
1	н	L	Н	Н	OUT1 -> OUT2	L							
_				L	OUT3 -> OUT1	,							
2	Н	L	L	Н	OUT1 -> OUT3	L	H						
		Н	Н		L	OUT3 -> OUT2							
3	Н				Н	OUT2 -> OUT3	L						
4		Н	Н	Н	Н	Н	Н	Н		L	OUT1 -> OUT2		Н
4	L								"	L	Н	OUT2 -> OUT1	Н
_	5 L H	н н			- 11	L	OUT1 -> OUT3	Н					
5			П H OUT3 -> О	OUT3 -> OUT1	П								
6			L	OUT2 -> OUT3		Н							
6 L		Н	OUT3 -> OUT2	Н									



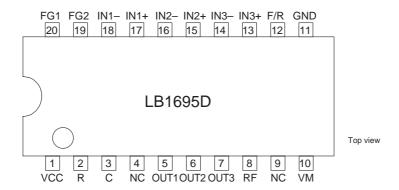
Block Diagram and Peripheral Circuitry

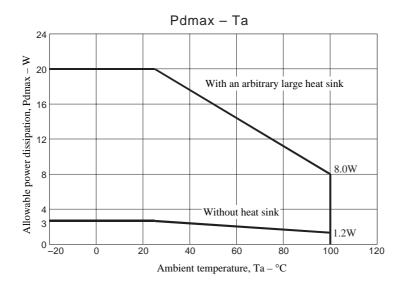


Pin Description

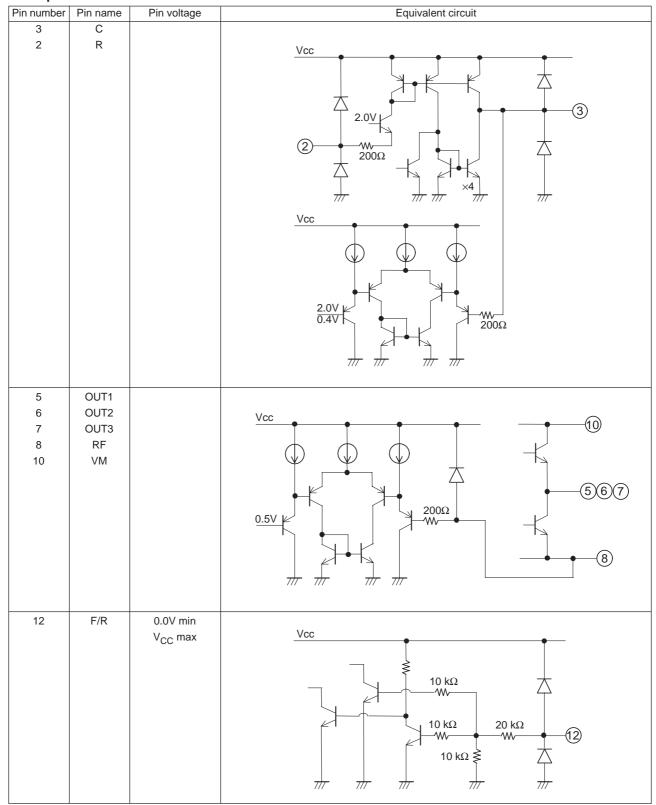
Pin name	Pin number	Function
VCC	1	Power supply pin for blocks except output
R	2	C pin charge/discharge current set pin
С	3	Setting pin for current limiter output off time and output current ignore time
NC	4, 9	May be used for wiring
OUT1	5	Output pin 1
OUT2	6	Output pin 2
OUT3	7	Output pin 3
D.E.	8	Output current detection pin. Insert a resistor (Rf) between this pin and ground.
RF		The output current will be limited to the value determined by VRF/Rf (output current limiter).
VM	10	Power supply pin for output
CNID	44	Ground for blocks except output
GND	11	Lowest electrical potential of output transistors is voltage at RF pin.
F/R	12	Forward/reverse control pin
IN1+, IN1-	17, 18	Hall input pin Logic High refers to IN+ > IN-
IN2+, IN2-	15, 16	Hall input pin Logic High refers to IN+ > IN-
IN3+, IN3-	13, 14	Hall input pin Logic High refers to IN+ > IN-
FG1	20	Speed pulse output pin 1 with built-in pull-up resistor
FG2	19	Speed pulse output pin 2 with built-in pull-up resistor

Pin Assignment





Pin Equivalent Circuit



Pin number	Pin name	Pin voltage	Equivalent circuit
17	IN1+	1.5V min	
18	IN1-	V _{CC} -1.8V max	Vcc
15	IN2+		1.00
16	IN2-		
13	IN3+		
14	IN3-		13 200Ω 14 15 W 16 17 / / / / / / / / / / / / / / / / / / /
20 19	FG1 FG2		Vcc 10kΩ 1920

Description of the LB1695D

1. Hall input circuit

The Hall input circuit is a differential amplifier with a hysteresis of 30 mV (typ.). The operating DC level must be within the common mode input voltage range (1.5V to V_{CC} – 1.8V). To prevent noise and other adverse influences, the input level should be at least 3 times the hysteresis (120 to 160 mVp-p). If noise evaluation at the Hall input shows a problem, a noise-canceling capacitor (about 0.01 μ F) should be connected across the Hall input IN+ and IN– pins.

2. Protection circuits

2-1. Low voltage protection circuit

When the V_{CC} voltage falls below a certain level (V_{LVSD}), the low voltage protection circuit cuts off the sink-side output transistors to prevent malfunction caused by a V_{CC} voltage drop.

2-2. Thermal shutdown circuit

When the junction temperature rises above a certain value (TSD), the thermal shutdown circuit cuts off the sink-side output transistors to prevent IC damage due to overheating. Design the application heat characteristics so that the protection circuit will not be triggered under normal circumstances.

3. FG output circuit

The Hall input signal at IN1, IN2, and IN3 is synthesized and subject to waveform shaping before appearing at this output. The signal at FG1 has the same frequency as the Hall input, and the signal at FG2 has a frequency that is three times higher than the Hall input.

4. Forward/Reverse control circuit

This IC is designed under the assumption that forward/reverse (F/R) switching will not be carried out while the motor is running. If switching is carried out while the motor is running, a feedthrough current flows in the output and a problem will be caused regarding ASO. F/R switching should be carried out while the V_M power supply is off (motor is stopped).

5. V_{CC}, V_M power supply

When the power supply voltage (V_{CC} , VM) rises very quickly at power-on, a feedthrough current may flow in the output and a problem will be caused regarding ASO. The power supply rise speed should be kept below $\Delta V_{CC}/\Delta t = 0.04 V/\mu S$ and $\Delta V_{M}/\Delta t = 0.16 V/\mu S$. For the power-up sequence, V_{CC} should be turned on before V_{M} . The sequence at power-down should be V_{M} first, and then motor stop, and then V_{CC} . With some motors, if V_{CC} is switched off immediately after V_{M} , while the motor is still rotating due to inertia, the V_{M} voltage may rise and exceed the withstand voltage.

6. Power supply stabilizing capacitors

If the V_{CC} line fluctuates drastically, the low-voltage protection circuit may be activated by mistake, or other malfunctions may occur. The V_{CC} line should therefore be stabilized by connecting a capacitor of at least several μF between V_{CC} and ground. Because a large switching current flows in the V_M line, wiring inductance and other factors can lead to VM voltage fluctuations. As the GND line also fluctuates, the V_M line must be stabilized by connecting a capacitor of at least several μF between V_M and ground, to prevent malfunction or exceeding the withstand voltage. Especially when long wiring runs (V_M, V_{CC}, GND) are used, sufficient capacitance should be provided to ensure power supply stability.

7. Current limiter circuit

The current limiter circuit cuts off the sink-side output transistors when the output current reaches a preset value (limiter value). This limits the output current peak value.

For detection of output current, the RF pin is used. By connecting the resistance Rf between the RF pin and ground, the output current can be detected as a voltage. When the RF pin voltage reaches 0.5V (typ.), the current limiter is activated. This limits the output current to the value determined by 0.5/Rf.

7-1. Output off time

When the current limiter circuit was triggered and has switched off the sink-side output transistors, it will turn them on again after a preset interval (power off time). By switching the output in this way, the current limiter circuit of the LB1695D reduces the likelihood of ASO problems as compared to current limiters using the non-saturation output principle.

The output off time is determined by the charge time for the capacitance C connected to the C pin. When the limiter is triggered, C starts to charge, and the time required for the C voltage to reach 2V (typ.) is the output off time. When C was charged to 2V, the sink-side output is turned on again. The charge current for C is constant-current and is determined by the resistance R connected to the R pin. The C charge current I_{CL} and the output off time toff are calculated according to the following equations.

```
\begin{split} I_{CL} &\ \ \  \  \, \stackrel{.}{=} \  \, 1.3/R \quad (R \text{ should be between } 13 \text{ k}\Omega \text{ to } 100 \text{ k}\Omega) \\ toff &\ \  \  \, \stackrel{.}{=} \  \, C/I_{CL} \times 2.0 \\ &\  \  \, \stackrel{.}{=} \  \, 1.53 \times R \times C \end{split}
```

7-2. Output current ignore time

While the sink-side output is turned off by the current limiter, a regenerative current flows in the upper side regenerative current absorption diode connected externally. When the output off time has elapsed and the sink-side output is turned on again, a momentary reverse current flows in the external diode (due to the reverse recovery time of the diode), which causes a limiter-value current to flow momentarily in the output. If this triggers the current limiter again, the output will be turned off, which lowers the average current and causes a reduction in motor torque for example during startup. To prevent this, the circuit is designed not to monitor the output current for a certain period after the sink-side output were turned off and on again. This is called the output current ignore time.

The output current ignore time is determined by the discharge time of the capacitance C connected to the C pin. After the current limiter was triggered and C was charged to 2V, the discharge process starts. The time required to discharge to a voltage of 0.4V (typ.) is the output ignore time. The discharge current for C is constant-current and is about 3 times the charge current (I_{CL}). Therefore the output current ignore time is about 1/3 of the output off time.

The C discharge current I_{CH} and the output current ignore time tsm are calculated according to the following equations.

$$\begin{split} I_{CH} &\ \ \ \ \ ^{:}=\ 1.3/R\times 3\\ tsm &\ \ \ \ ^{:}=\ C/I_{CH}\times 1.6\\ &\ \ \ \ ^{:}=\ 0.41\times R\times C \end{split}$$

Because the current limiter circuit is slanted towards the ON time for turning the sink-side output on again, the reverse current will not be so large even if a rectifying diode (without a short reverse recovery time) is used as regenerative current absorption diode connected externally.

7-3. Output off time setting

The output off time must be optimized for the type of motor that is being controlled. The output off time setting is controlled by the external resistance connected to the R pin and the external capacitance connected to the C pin. Figure 1 shows the current limiter operating waveform.

(1) Short output off time setting

Because the IC is designed internally to give a ratio of about 3:1 for the output off time and output current ignore time, the two values cannot be set independently. If the output off time is set to a very small value, the output current ignore time may be too short. In such a case, the external regenerative current absorption diode acts to limit current flow by its reverse current (see section 7-2). If the output off time is small, the diode reverse current will increase, which can lead to ASO problems.

(2) Long output off time setting

If the output off time is set to a very high value, the average current will be reduced, resulting in lower motor startup torque. Depending on the motor type, the circuit may not change from the current limiter operating state to the normal rotation state.

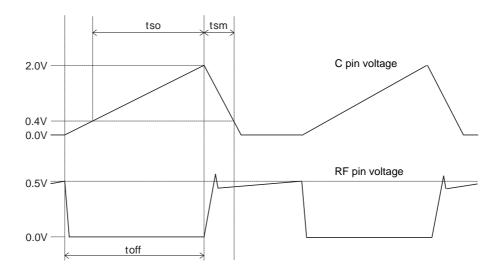


Figure. 1 Current limiter operating waveform

8. Internal power dissipation calculation

 $Pd = (V_{CC} \times I_{CC}) + (V_M \times I_M) - (motor\ coil\ power\ dissipation)$

9. IC temperature rise measurement

Because the chip temperature of the IC cannot be measured directly, measurement should be carried out according to one of the following procedures.

9-1. Thermocouple measurement method

A thermocouple element is mounted to the IC heat dissipation fin. This measurement method is easy to implement, but it will be subject to measurement errors if the temperature is not stable.

9-2. Measurement using internal diode characteristics of IC

This is the recommended measurement method. It makes use of the parasitic diode incorporated in the IC between FG1 and GND. Set FG1 to High (off) and measure the voltage VF of the parasitic diode to calculate the temperature.

(Sanyo data: for $I_F = -1$ mA, V_F temperature characteristics are about -2 mV/°C)

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