

LB1810M**SANYO****FDD Spindle Motor Driver****Overview**

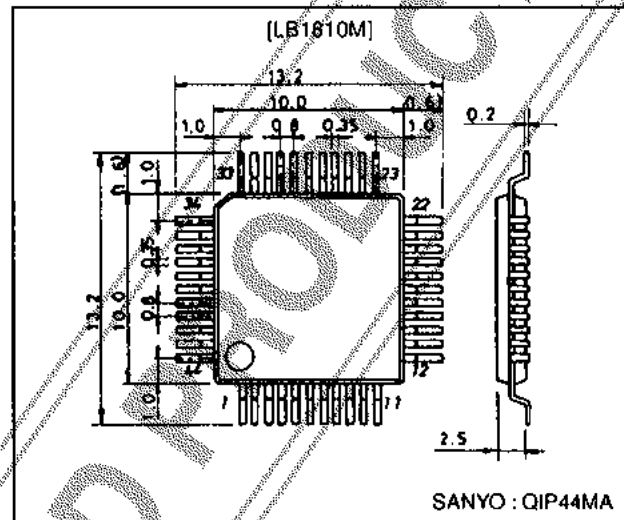
The LB1810M is a 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

Functions and Features

- Three phase total wave linear driver.
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply)
- On-chip digital speed control : $f_{OSC} = (1024 \times f_{FG}) / D$
When SL1=high D=5/8,
SL1=low D=6/8
- Start/Stop circuit. S/S1 : high active, S/S2 : low active.
- Rotation speed switching.
- Current limiter circuit.
- On-chip index comparator (single HYS).
- On-chip index delay circuit.
- AGC circuit.
- Thermal protection circuit.

Package Dimensions

unit:mm

3148-QFP44MA**Specifications****Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$**

Parameter	Symbol	Conditions	Rating	Unit
Maximum supply voltage	$V_{CC\ max}$		14.5	V
Maximum output current	$I_{O\ max1}$	$t \leq 0.5s$	1.0	A
Steady maximum output current	$I_{O\ max2}$		0.7	A
Allowable power dissipation	$P_d\ max$	Independent IC	1	W
Operating temperature	T_{opr}		-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

Allowable Operating Conditions at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{CC}		4.2 to 6.5	V

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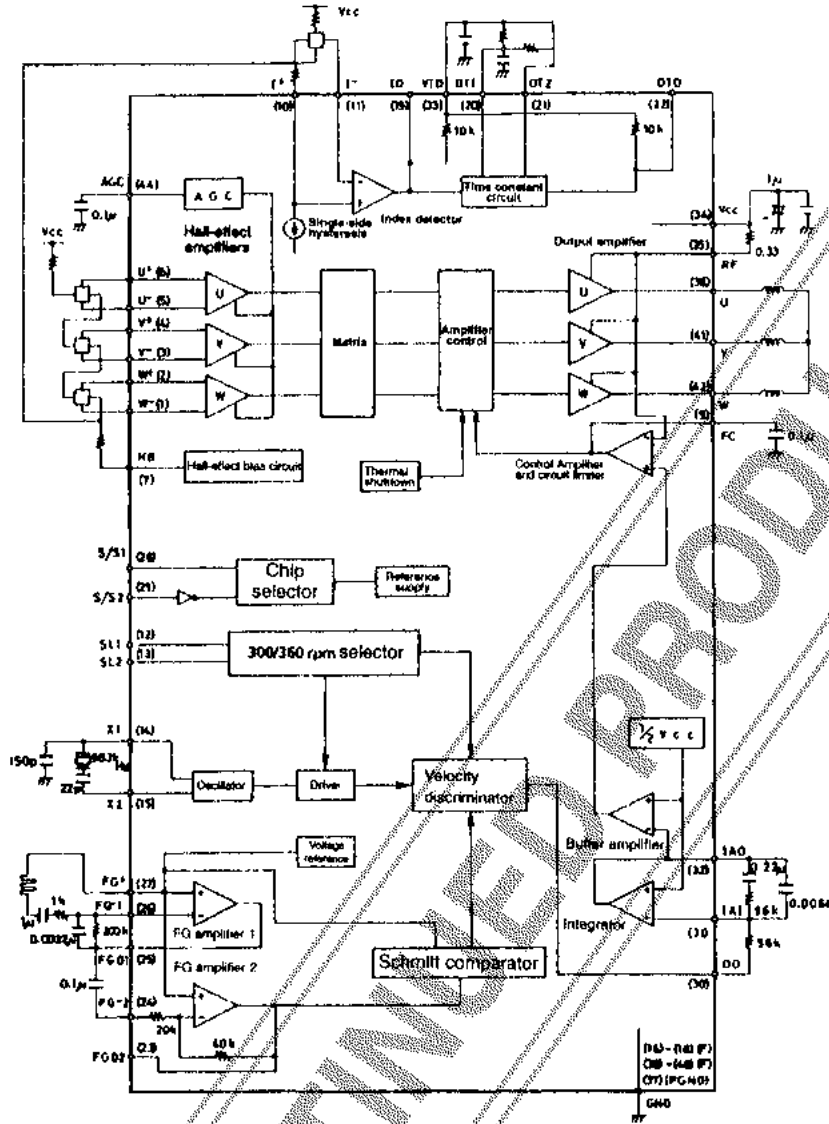
Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Current drain	I _{CC1}	V _{CC} =5.0V (Stop)			0.2	mA	
	I _{CC2}	V _{CC} =12V (Stop)			0.5	mA	
	I _{CC1}	V _{CC} =5.0V (Steady)		20	30	mA	
	I _{CC2}	V _{CC} =12V (Steady)		22	33	mA	
Time changeover bias current	I _{SL}				0.4	mA	
Time changeover input voltage 1	V _{SLL}		0		0.8	V	
Time changeover input voltage 2	V _{SLH}		2.0		V _{CC}	V	
S/S1 bias current	I _{S/S1}				0.4	mA	
S/S1 start voltage	V _{S/S1}		2.0		V _{CC}	V	
S/S1 stop voltage	V _{S/S1}		0		0.8	V	
S/S2 bias current	I _{S/S2}				0.1	mA	
S/S2 start voltage	V _{S/S2}		0		0.8	V	
S/S2 stop voltage	V _{S/S2}		2.0		V _{CC}	V	
Hall-effect bias amplifier input current	I _{HB}				20	μA	
In-phase input voltage range	V _H		2.2		V _{CC} -0.7	V	
Differential input voltage range	V _{dif}		70		200	mVp-p	
Input offset voltage	V _{HO}				±1.0	mV	
Hall-Effect output voltage	V _H	I _H =5mA		1.5	1.8	V	
Leak current	I _{HL}	Stop			±10	μA	
Output saturation voltage (sink plus source)	V _{sat1}	I _O =0.35A, V _{CC} =4.2V		1.2	1.4	V	
	V _{sat2}	I _O =0.70A, V _{CC} =4.2V		1.5	2.0	V	
Output leak current	I _{OL}				±1.0	mA	
Current limiter	V _{ref1}		0.27	0.30	0.33	V	
Control amplifier voltage gain	G _C			-6		dB	
Voltage gain phase differential	ΔG _C				±1	dB	
Integrated amplifier internal reference voltage	V _{ref2}			V _{CC} /2		V	
Integrated amplifier bias current	I _b				±1	μA	
Integrated output voltage amplitude	V _{r*}	I _b =-0.5mA with reference of V _{ref2}		0.75		V	
	V _{r*}	I _b =0.5mA with reference of V _{ref2}		-1.4		V	
Gain band width				1000		KHz	
FG amplifier1 input voltage	V _{FG1}		2		40	mVp-p	
FG amplifier1 voltage gain	G _{FG1}	Open loop		60		dB	
FG amplifier1 input offset	V _{FG10}				±10	mV	
FG amplifier2 input voltage range	V _{FG2}		1		V _{CC} -1	V	
FG amplifier2 voltage gain	G _{FG2}			6.0		dB	
FG amplifier2 input offset	V _{FG20}				±10	mV	
FG amplifier internal reference voltage	V _{FGB}		5.30	5.90	6.50	V	
			(2.20)	(2.50)	(2.60)	V	
Schmitt hysteresis width	ΔV _{sh1}	High→Low			25	mV	
	ΔV _{sh2}	Low→High			25	mV	
Schmitt input operation level	V _{sh}		1		V _{CC} -1	V	
Speed disk recount number	N			1024			
Disk recount out, low level voltage	V _{DL}	I _D =-0.5mA			0.3	V	
Disk recount out, high level voltage	V _{DH}	I _D =0.5mA		V _{CC} -0.4		V	
Disk recount out leak current	I _{D1}				±1.0	μA	
Disk recount operation frequency	F _D				1.0	MHz	
Oscillation range	F _{OSC}				1.0	MHz	
Index bias current	I _{IOB}				±10	μA	
In-phase input voltage range	V _{ID}		1.5		V _{CC} -0.5	V	
Hysteresis setting current range	I _{IDO}		5	10	15	μA	
Index output low level voltage	V _{IDL}	V _{ID} =5V			0.4	V	
Index output high level voltage	V _{IDH}	V _{ID} =5V	4.5			V	
Brak-down voltage	V _{DLDC}	V _{ID} =5V		2.50		V	
Delay output low level voltage	V _{DLL}	V _{ID} =5V			0.4	V	
Delay output high level voltage	V _{DLH}	V _{ID} =5V	4.5			V	
Thermal Shutdown operating temperature	TSD		150	180		°C	
Hysteresis width	ΔTSD			40		°C	

Note : *) Marked values are guaranteed by the design itself and therefore do not require measurement.

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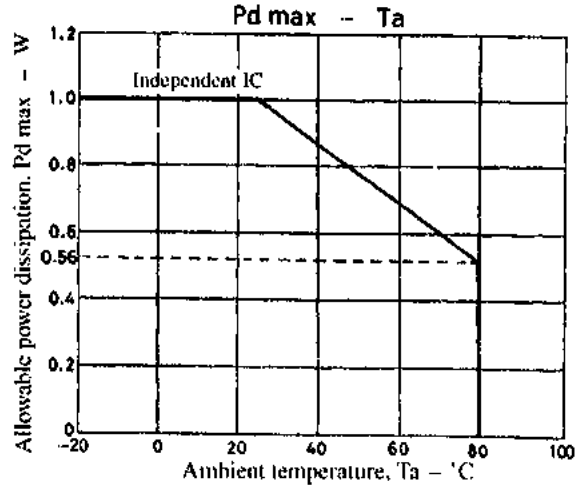
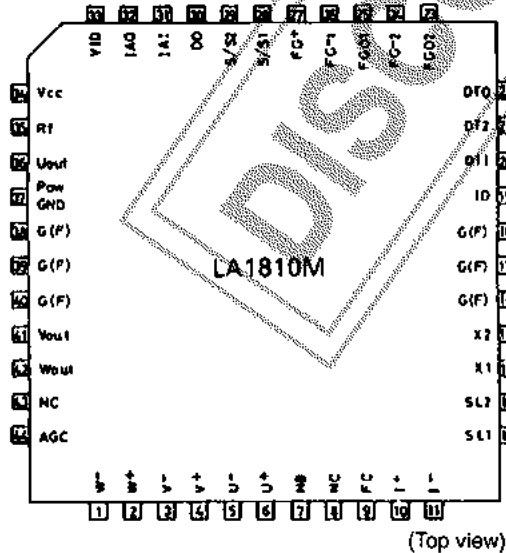
Equivalent Circuit Block Diagram



Unit (resistance : Ω , capacitance : F)

All constants are reference value and integrated constants may vary depending on the motor.

Pin Assignment



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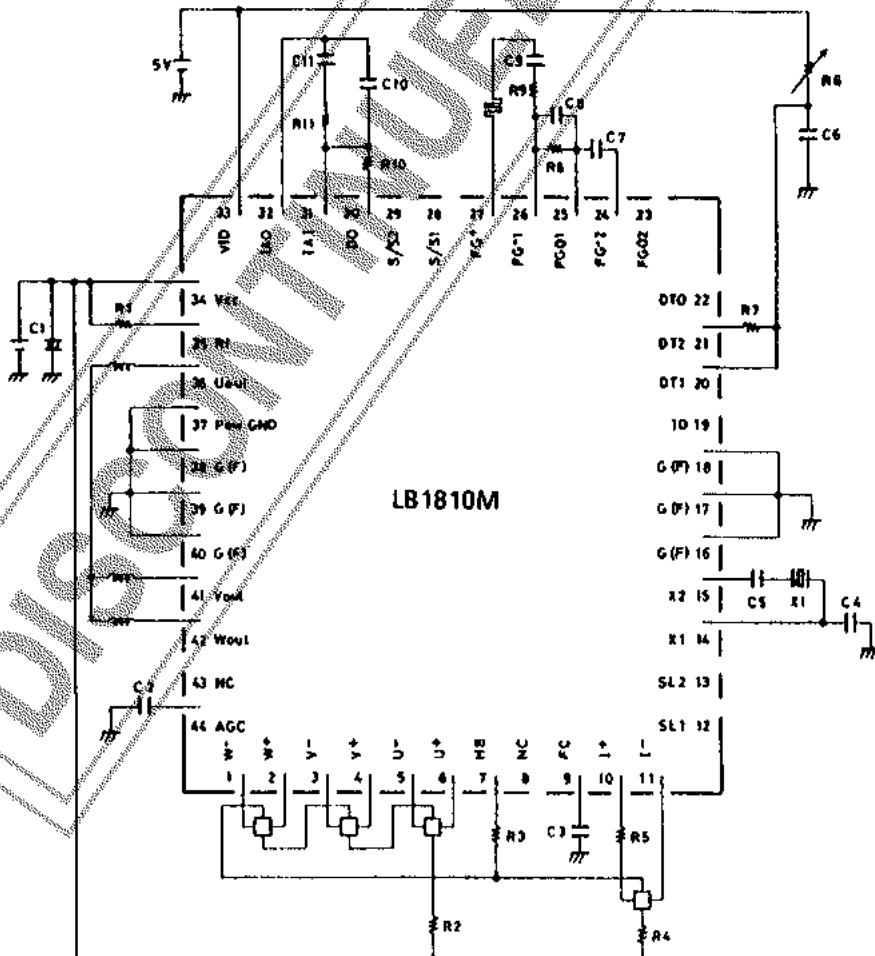
Truth Table

	Source → Sink	Hall-Effect Input		
		U	V	W
1	V-phase → W-phase	H	H	L
2	V-phase → U-phase	L	H	L
3	W-phase → U-phase	L	H	H
4	W-phase → V-phase	L	L	H
5	U-phase → V-phase	H	L	H
6	U-phase → W-phase	H	L	L

When an high level exists for Hall-effect input.

- U' > U
- V' > V
- W' > W

Sample Application Circuit



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Pin Description

Unit (resistance : Ω)

Pin No	Symbol	Pin voltage	Equivalent circuit	Pin function																								
1 2 3 4 5 6	W ⁻ W ⁺ V ⁻ V ⁺ U ⁻ U ⁺	2.2V min V _{CC} -0.7V max		<ul style="list-style-type: none"> W-phase Hall-element input pin W⁺ > W⁻ is established when logic is at a high level. V-phase Hall effect input pin. V⁺ > V⁻ is established when logic is at a high level. U-phase Hall-effect input pin. U⁺ > U⁻ is established when logic is at a high level. 																								
7	HB	1.5V typ (I _H =5mA)		<ul style="list-style-type: none"> Minus pin for Hall-effect bias. When stopped, switches open and Hall-effect bias severs. 																								
9	FC			<ul style="list-style-type: none"> Frequently characteristics revision pin. By installing a capacitor between this pin and GND, close-loop oscillation for the current control system 																								
10 11	I ⁺ I ⁻	1.5V min V _{CC} -0.5V max		<ul style="list-style-type: none"> Index input pin. When the I⁺ pin is at a low level, I1 operates with the fixed current of I1=10μA and when at an high level, I1 does not flow. Hysteresis width is determined by the resistor attached externally to the I⁺ pin. 																								
12	SL1	H : 2.0V min L : 0.8V max		<ul style="list-style-type: none"> Time changeover pin. f_{osc}=993kHz <table border="1"> <tr> <td>SL1</td> <td>SL2</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td></td> <td>600rpm</td> <td>300rpm</td> </tr> <tr> <td>L</td> <td></td> <td>720rpm</td> <td>360rpm</td> </tr> </table> f_{osc}=491kHz <table border="1"> <tr> <td>SL1</td> <td>SL2</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td></td> <td>300rpm</td> <td>-</td> </tr> <tr> <td>L</td> <td></td> <td>360rpm</td> <td>-</td> </tr> </table> FG : 60pulse/round 	SL1	SL2	H	L	H		600rpm	300rpm	L		720rpm	360rpm	SL1	SL2	H	L	H		300rpm	-	L		360rpm	-
SL1	SL2	H	L																									
H		600rpm	300rpm																									
L		720rpm	360rpm																									
SL1	SL2	H	L																									
H		300rpm	-																									
L		360rpm	-																									
13	SL2	H : 2.0V min L : 0.8V max																										

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Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
14	X1			<ul style="list-style-type: none"> Reference clock generating pin.
15	X2			
16 17 18	G(F) G(F) G(F)			<ul style="list-style-type: none"> Frame GND pin. Grounded as with pins 37, 38, 39, 40.
19	ID	H : 4.5V min L : 0.4V max ($V_{ID}=5V$)		<ul style="list-style-type: none"> Index pulse output pin.
20	DT1			<ul style="list-style-type: none"> Pin connecting the external CR for the delay time constant circuit.
21	DT2			<ul style="list-style-type: none"> Break-down current setting pin for the delay time constant circuit.
22	OTO	H : 4.5V min L : 0.4V max ($V_{ID}=5V$)		<ul style="list-style-type: none"> Index delay pulse output pin.

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Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
23	FG02			<ul style="list-style-type: none"> • FG amplifier2 output pin.
24	FG-2			<ul style="list-style-type: none"> • FG amplifier2 negative input pin.
25	FG01			<ul style="list-style-type: none"> • FG amplifier1 output pin.
26	FG-1			<ul style="list-style-type: none"> • FG amplifier1 negative input pin.
27	FG+1	2.48V ($V_{CC}=5V$) 5.8V ($V_{CC}=12V$)		<ul style="list-style-type: none"> • FG amplifier1 positive input pin. Generates reference voltage within IC.
28	S/S1	H : 2.0V min L : 0.8V max		<ul style="list-style-type: none"> • Start/Stop changeover pin. high level active.
29	S/S2	H : 2.0V min L : 0.8V max		<ul style="list-style-type: none"> • Start/Stop changeover pin. low level active.
30	DO			<ul style="list-style-type: none"> • Speed discriminator output pin.

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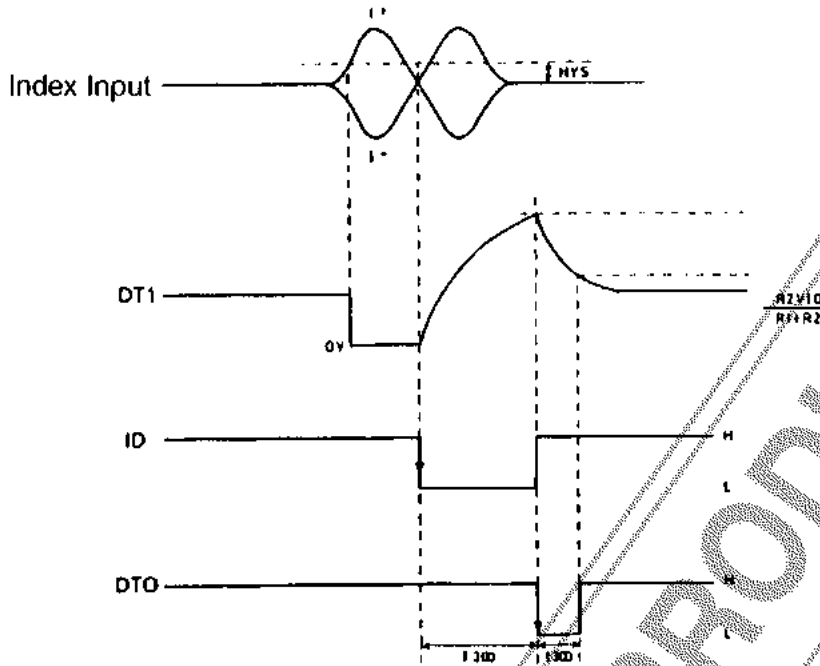
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Unit (resistance : Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
31	IAI			<ul style="list-style-type: none"> Integrated amplifier input pin
32	IAO			<ul style="list-style-type: none"> Integrated amplifier output pin
33	V_{ID}			<ul style="list-style-type: none"> Index pulse output and index delay pulse output power supply pin. For applications when $V_{CC} = 5V$, $V_{CC} = V_{ID} = 5V$ For applications when $V_{CC} = 12V$, $V_{CC} = V_{ID} = 5V$
34	V_{CC}			<ul style="list-style-type: none"> Total power supply voltage pin except for V_{ID}. Voltage must be stable and free of ripple and noise interference.
35	R_I			<ul style="list-style-type: none"> Output current detection pin. By installing an R_I resistor between this pin and V_{CC}, output current is detected as voltage. Voltage detection at this pin actuates the current limiter.
36	U_{OUT}			<ul style="list-style-type: none"> U-phase output pin.
37	Pow GND			<ul style="list-style-type: none"> Output transistor ground pin.
38	G (F)			<ul style="list-style-type: none"> Ground pin.
39	G (F)			<ul style="list-style-type: none"> Grounded as with pins 16, 17, 18, 37
40	G (F)			
41	V_{OUT}			<ul style="list-style-type: none"> V-phase output pin.
42	W_{OUT}			<ul style="list-style-type: none"> W-phase output pin.
44	AGC			<ul style="list-style-type: none"> AGC pin. Controls Hall-effect amplifier gain in response to Hall-effect input frequency.

Index and Timing Chart



When SL1=high level

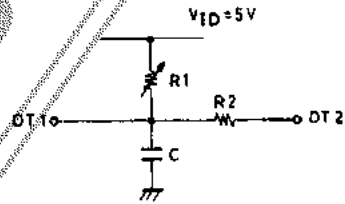
$$T_{300} \approx 0.693CR1$$

$$t_{300} \approx \frac{CR1R2}{R1+R2} \left\{ 0.405 + \ln \left(\frac{R1-R2}{R1-2R2} \right) \right\}$$

When SL1=low level.

$$T_{360} \approx 0.577CR1$$

$$t_{360} \approx \frac{CR1R2}{R1+R2} \left\{ 0.522 + \ln \left(\frac{0.781R1-R2}{R1-2R2} \right) \right\}$$



Using only the ID pulse involves shorting DT1 and DT2.

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No	Reference value	Objection	Note
R1	0.5Ω	Current detection, current limiter	1
R2 R3 R4		Hall bias (Hall element bias current setting)	
R5	2kΩ	Index amplifier Hysteresis width setting	2
R6	10kΩ to 100kΩ	Index output timing setting	3
R7		Index output timing setting	3
R8	200kΩ	FG amplifier feedback resistance	4
R9	1kΩ	FG amplifier input resistance	4
R10 R11		Integrator constant	5
C1	±0.1μF	Supply bypass	6
C2	0.1μF	AGC filter	
C3	0.1μF	Frequency characteristics revision	
C4	150pF	Oscillator stabilization	7
C5	22pF	Oscillator connection	7
C6	0.1μF	Index output timing setting	3
C7	0.1μF	FG amplifier connection	4
C8	0.0022μF	FG amplifier filter	4
C9	1μF	FG amplifier connection	4
C10 C11		Integrator constant	5
X1	983kHz or 491kHz	Oscillator	7

Note : 1. Current limiter

$$I_{LIM} = \frac{V_{REF}}{R1} \text{ [A]}$$

Refer to the electrical characteristic for V_{REF}

2. Index amplifier hysteresis width

$$\Delta V_{HYS} = I_{DD} \times R5$$

Refer to the electrical characteristics for I_{DD}

3. Refer to the timing chart of index block.

4. If the input amplifier is large enough that no noise problem will occur.

C8 can be deleted and C9 can be shorted.

5. Speed discriminator gain.

$$K_V = 0.025 \text{ [V/\%]}$$

Control amplifier gain.

$$G_C = 0.5 \text{ [V/V]}$$

6. Connect this as close to the IC as possible.

7. Consult oscillator manufacturer to determine the values.