



# LB1813M

## FDD Spindle Motor Driver

### Overview

The LB1813M is 3-phase DD motor driver IC and is an ideal FDD spindle motor driver for 3.5 inch applications.

### Features

- Three phase total wave linear driver.
- Eliminates need for output electrolytic capacitor (however, depending on the motor, this may not apply)
- On-chip digital speed control :  $f_{osc}=(1024 \times f_{FG})/D$   
When SL1=high D=5/8  
SL1=low D=6/8
- Start/Stop circuit.
- Rotation speed switching.
- Current limiter circuit.
- On-chip index comparator (single hysteresis)
- On-chip index delay circuit.
- AGC circuit.
- Thermal protection circuit.

### Specifications

#### Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \max}$		7.0	V
Maximum output current	$I_O \max 1$	$t \leq 0.5s$	1.0	A
Steady maximum output current	$I_O \max 2$		0.7	A
Allowable power dissipation	$P_d \max$	Independent IC	1	W
Operating temperature	$T_{opr}$		-20 to +80	°C
Storage temperature	$T_{stg}$		-40 to +150	°C

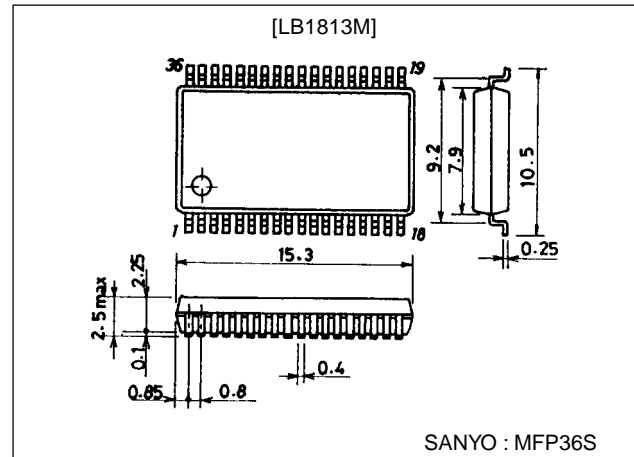
#### Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}$		4.2 to 6.5	V

### Package Dimensions

unit:mm

#### 3129-MFP36S



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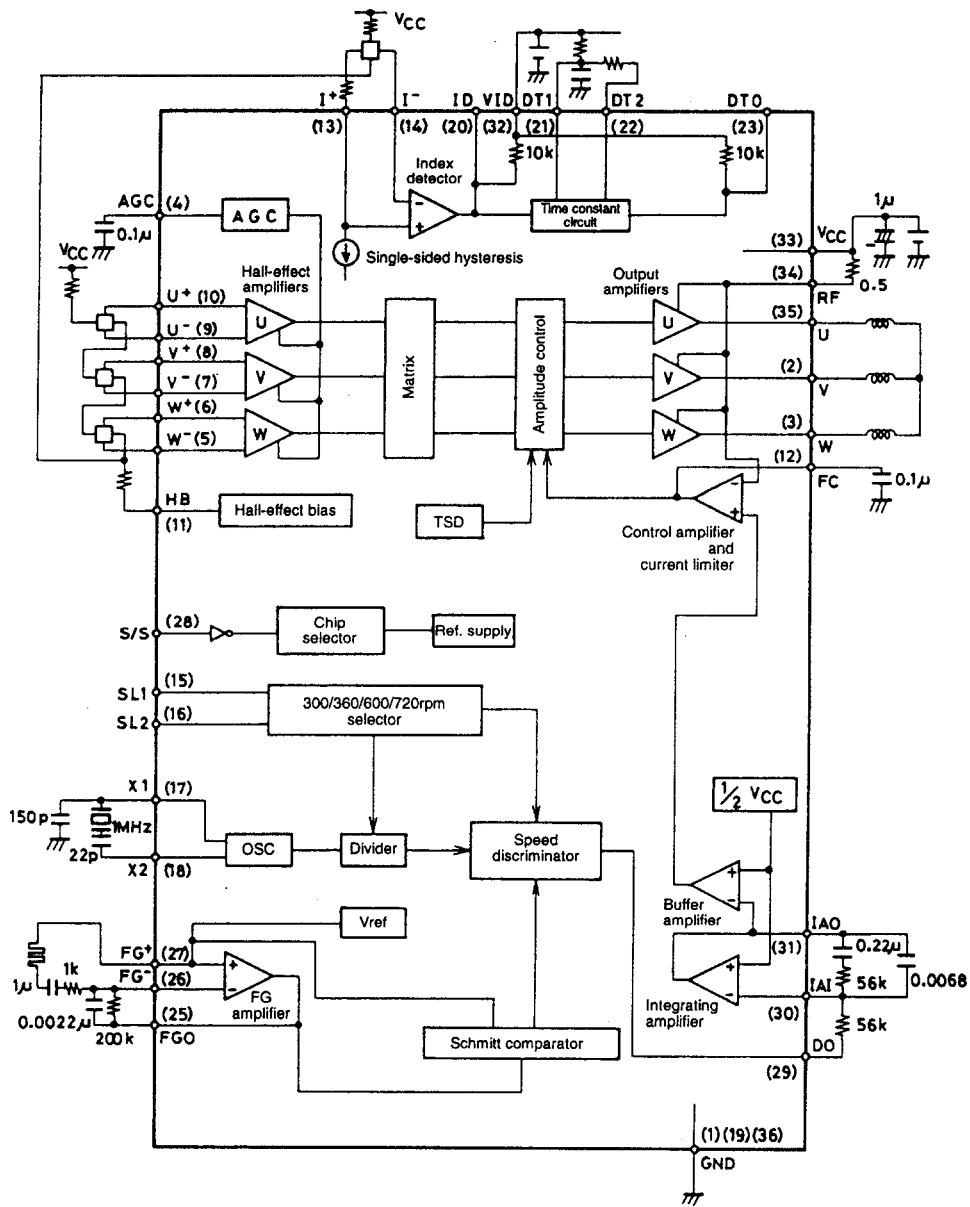
## Electrical Characteristics at Ta = 25°C, VCC=5V

Parameter	Symbol	Conditions	Ratings			Unit	Note
			min	typ	max		
Current drain	I <sub>CCO1</sub>	V <sub>CC</sub> =5.0V (Stop)			0.4	mA	
	I <sub>CC1</sub>	V <sub>CC</sub> =5.0V (Steady)		20	30	mA	
Time changeover bias current	I <sub>SL</sub>				0.4	mA	
Time changeover input voltage1	V <sub>SLL</sub>		0		0.8	V	
Time changeover input voltage2	V <sub>SLH</sub>		2.0		V <sub>CC</sub>	V	
S/S bias current	I <sub>S/S</sub>				0.1	mA	
S/S start voltage	V <sub>S/S</sub>		0		0.8	V	
S/S stop voltage	V <sub>S/S</sub>		2.0		V <sub>CC</sub>	V	
Hall-effect bias amplifier input current	I <sub>HB</sub>				20	μA	
In-phase input voltage range	V <sub>h</sub>		2.2		V <sub>CC</sub> -0.7	V	
Differential input voltage range	V <sub>dif</sub>		70		200	mVp-p	
Input offset voltage	V <sub>ho</sub>				±10	mV	*
Hall-effect output voltage	V <sub>H</sub>	I <sub>H</sub> =5mA		1.5	1.8	V	
Leak current	I <sub>HL</sub>	Stop			±10	μA	
Output saturation voltage (sink plus source)	V <sub>sat1</sub>	I <sub>O</sub> =0.35A, V <sub>CC</sub> =4.2V		1.2	1.4	V	
	V <sub>sat2</sub>	I <sub>O</sub> =0.70A, V <sub>CC</sub> =4.2V		1.5	2.0	V	
Output leak current	I <sub>OL</sub>				±1.0	mA	
Current limiter	V <sub>ref1</sub>		0.27	0.30	0.33	V	
Control amplifier voltage gain	G <sub>C</sub>			-6		dB	
Voltage gain phase differential	ΔG <sub>C</sub>				±1	dB	
Integrated amplifier internal reference voltage	V <sub>ref2</sub>			V <sub>CC</sub> /2		V	
Integrated amplifier bias current	I <sub>ib</sub>				±1	μA	
Integrated output voltage amplitude	V <sub>i+</sub>	I <sub>i</sub> =-0.5mA with reference of V <sub>ref2</sub>		0.75		V	
	V <sub>i-</sub>	I <sub>i</sub> =0.5mA with reference of V <sub>ref2</sub>		-1.4		V	
Gain band width				1000		kHz	*
FG amplifier input voltage range	V <sub>FG</sub>		5		100	mVp-p	
FG amplifier voltage gain	G <sub>FG</sub>	Open loop		60		dB	
FG amplifier input offset	V <sub>FG0</sub>				±10	mV	
FG amplifier internal reference voltage	V <sub>FGB</sub>		2.20	2.50	2.80	V	
Schmitt hysteresis width	ΔV <sub>sh1</sub>	High→Low		25		mV	*
	ΔV <sub>sh2</sub>	Low→High		25		mV	*
Schmitt input operation level	V <sub>sh</sub>		1		V <sub>CC</sub> -1	V	
Speed disk recount number	N			1042			
Disk recount out low level voltage	V <sub>DL</sub>	I <sub>D</sub> =-0.5mA			0.3	V	
Disk recount out high level voltage	V <sub>DH</sub>	I <sub>D</sub> =0.5mA	V <sub>CC</sub> -0.4			V	
Disk recount out leak current	I <sub>D1</sub>				±1.0	μA	
Disk recount operation frequency	F <sub>D</sub>				1.0	MHz	*
Oscillation range	F <sub>OSC</sub>				1.0	MHz	*
Index bias current	I <sub>IDB</sub>				±10	μA	
In-phase input voltage range	V <sub>ID</sub>		1.5		V <sub>CC</sub> -0.5	V	
Hysteresis setting current range	I <sub>IDO</sub>		5	10	15	μA	
Index output low level voltage	V <sub>IDL</sub>	V <sub>ID</sub> =5V			0.4	V	
Index output high level voltage	V <sub>IDH</sub>	V <sub>ID</sub> =5V	4.5			V	
Brak-down voltage	V <sub>DLDC</sub>	V <sub>ID</sub> =5V		2.50		V	
Delay output low level voltage	V <sub>DLL</sub>	V <sub>ID</sub> =5V			0.4	V	
Delay output high level voltage	V <sub>DLH</sub>	V <sub>ID</sub> =5V	4.5			V	
Thermal shutdown operating temperature	TSD		150	180		°C	*
Hysteresis width	ΔTSD			40		°C	*

Note : \*) Marked values are guaranteed by the design itself and therefore do not require measurement.

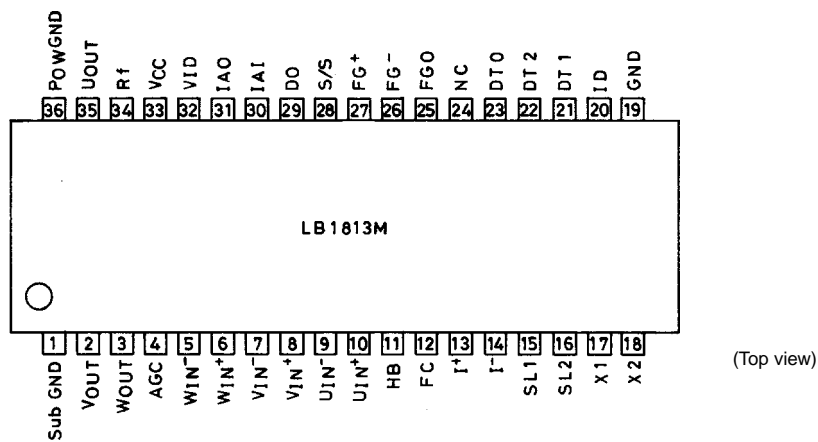
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## Block Diagram



Unit (reissitace : Ω, capacitance : F)

## Pin Assignment



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## Truth Table

	Source→Sink	Hall-Effect Input		
		U	V	W
1	V-phase →W-phase	H	H	L
2	V-phase →U-phase	L	H	L
3	W-phase →U-phase	L	H	H
4	W-phase →V-phase	L	L	H
5	U-phase →V-phase	H	L	H
6	U-phase →W-phase	H	L	L

When an high level exists for Hall-effect input.

U<sup>+</sup>>U<sup>-</sup>  
V<sup>+</sup>>V<sup>-</sup>  
W<sup>+</sup>>W<sup>-</sup>

## Pin Description

Unit (resistance : Ω)

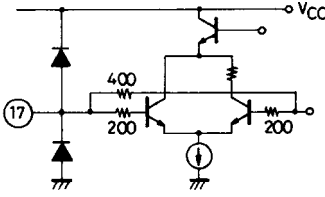
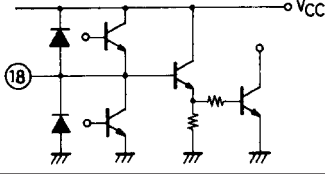
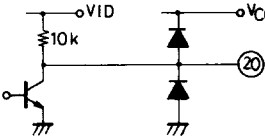
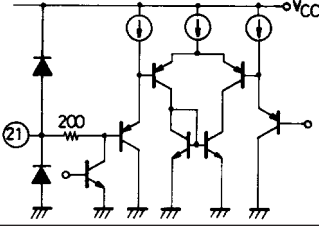
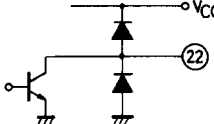
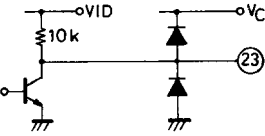
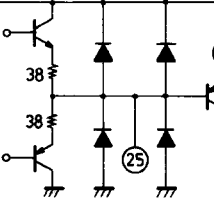
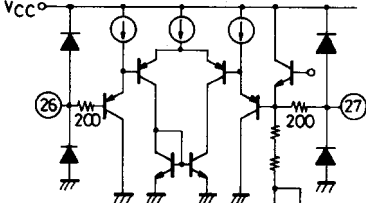
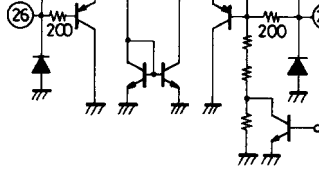
Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function									
5 6 7 8 9 10	W <sup>-</sup> W <sup>+</sup> V <sup>-</sup> V <sup>+</sup> U <sup>-</sup> U <sup>+</sup>	2.2V min V <sub>CC</sub> -0.7V max		<ul style="list-style-type: none"> <li>W-phase Hall-effect input pin. W<sup>+</sup>&gt;W<sup>-</sup> is established when logic is at an high level.</li> <li>V-phase Hall-effect input pin. V<sup>+</sup>&gt;V<sup>-</sup> is established when logic is at an high level.</li> <li>U-phase Hall-effect input pin. U<sup>+</sup>&gt;U<sup>-</sup> is established when logic is at an high level.</li> </ul>									
11	HB	1.5V typ I <sub>H</sub> =5mA		<ul style="list-style-type: none"> <li>Minus pin for Hall-effect bias, When stopped, switches open and Hall-effect bias severs.</li> </ul>									
12	FC			<ul style="list-style-type: none"> <li>Frequency characteristics revision pin. By installing a capacitor between this pin and GND, close-loop oscillation for the current control system halts.</li> </ul>									
13 14	I <sup>+</sup> I <sup>-</sup>	1.5V typ V <sub>CC</sub> -0.5V max		<ul style="list-style-type: none"> <li>Index input pin.</li> <li>When the I<sup>+</sup> pin is at an low level, I1 operates with the fixed current of I1=10μA and when at an high level, I1 does not flow.</li> <li>Hysteresis width is determined by the resistor attached externally to the I<sup>+</sup> pin.</li> </ul>									
15	SL1	High : 2.0V min Low : 0.8V max		<ul style="list-style-type: none"> <li>Time changeover pin.</li> </ul>									
16	SL2	High : 2.0V min Low : 0.8V max		<p>fosc=1MHz</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">SL2 SL1</td> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">600rpm</td> <td style="text-align: center;">300rpm</td> </tr> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">720rpm</td> <td style="text-align: center;">360rpm</td> </tr> </table> <p style="text-align: center;">FG : 60pulse/round</p>	SL2 SL1	H	L	H	600rpm	300rpm	L	720rpm	360rpm
SL2 SL1	H	L											
H	600rpm	300rpm											
L	720rpm	360rpm											

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Unit (resistance :  $\Omega$ )

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
17	X1			• Reference clock generating pin.
18	X2			
19	GND			• Ground pin. Grounded as with pins 1 and 36.
20	ID	High : 4.5V min Low : 0.4V max (When $V_{ID}=5V$ )		• Index pulse output pin.
21	DT1			• Pin Connecting the external CR for the delay time constant circuit.
22	DT2			• Break-down current setting pin for the delay time constant circuit.
23	DTO	High : 4.5V min Low : 0.4V max (When $V_{ID}=5V$ )		• Index delay pulse output pin.
25	FG0			• FG amplifier output pin.
26	FG <sup>-</sup>			• FG amplifier negative input pin.
27	FG <sup>+</sup>	2.48V (When $V_{ID}=5V$ )		• FG amplifier positive input pin. Generates reference voltage within IC.

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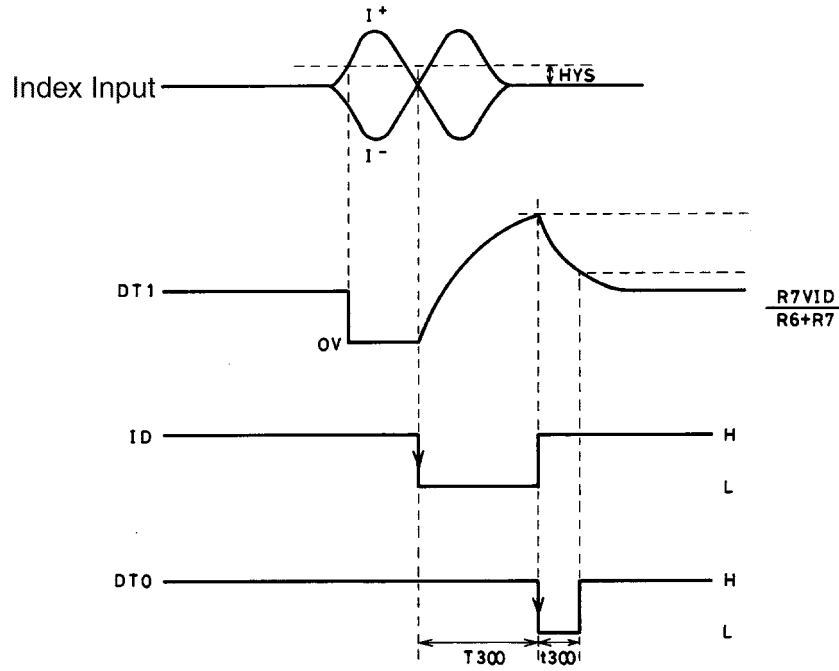
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Unit (resistance :  $\Omega$ )

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
28	S/S	High : 2.0V min Low : 0.8V max		<ul style="list-style-type: none"> <li>Start/Stop changeover pin. Low level active.</li> </ul>
29	DO			<ul style="list-style-type: none"> <li>Speed discriminator output pin.</li> </ul>
30	IAI			<ul style="list-style-type: none"> <li>Integrated amplifier input pin.</li> </ul>
31	IAO			<ul style="list-style-type: none"> <li>Integrated amplifier output pin.</li> </ul>
32	VID			<ul style="list-style-type: none"> <li>Index pulse output and index delay pulse output power supply pin.</li> </ul> <p>For applications when <math>V_{CC}</math> equals 5V, <math>V_{CC}=V_{ID}=5V</math>.</p>
33	$V_{CC}$			<ul style="list-style-type: none"> <li>Total power supply voltage pin except for <math>V_{ID}</math>. Voltage must be stable and free of ripple and noise interference.</li> </ul>
34	$R_f$			<ul style="list-style-type: none"> <li>Output current detection pin.</li> </ul> <p>By installing an <math>R_f</math> resistor between this pin and <math>V_{CC}</math>, output current is detected as voltage. Voltage detection at this pin activates the current limiter.</p>
35	$U_{OUT}$			<ul style="list-style-type: none"> <li>U-phase output pin.</li> </ul>
36	Pow GND			<ul style="list-style-type: none"> <li>Output transistor ground pin.</li> </ul>
1	Sub GND			<ul style="list-style-type: none"> <li>Ground pin. Ground as with pins 19 and 36.</li> </ul>
2	$V_{OUT}$			<ul style="list-style-type: none"> <li>V-phase output pin.</li> </ul>
3	$W_{OUT}$			<ul style="list-style-type: none"> <li>W-phase output pin.</li> </ul>
4	AGC			<ul style="list-style-type: none"> <li>AGC (Automatic gain control) pin. Controls Hall-effect amplifier gain in response to Hall-effect input-frequency.</li> </ul>

Index and Timing Chart



When SL1=high level

$$\cdot T300 \approx 0.693CR6$$

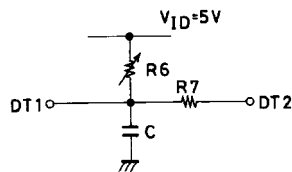
$$\cdot t300 \approx \frac{CR6R7}{R6+R7} \left\{ 0.405 + 1n \left( \frac{R6-R7}{R6-2R7} \right) \right\}$$

When SL1=low level.

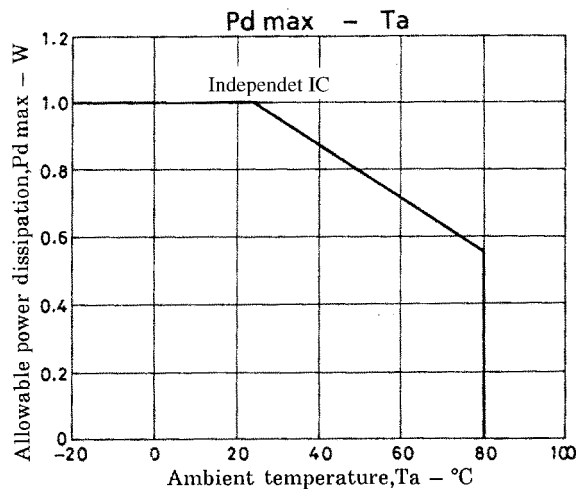
$$\cdot T360 \approx 0.577CR6$$

$$\cdot t360 \approx \frac{CR6R7}{R6+R7} \left\{ 0.522 + 1n \left( \frac{0.781R6-R7}{R6-2R7} \right) \right\}$$

Using only the ID pulse involves shorting DT1 and DT2.



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