Ordering number: EN3302A

Monolithic Digital IC

LB1820

Office Automation-Use 3-Phase Brushless Motor Driver

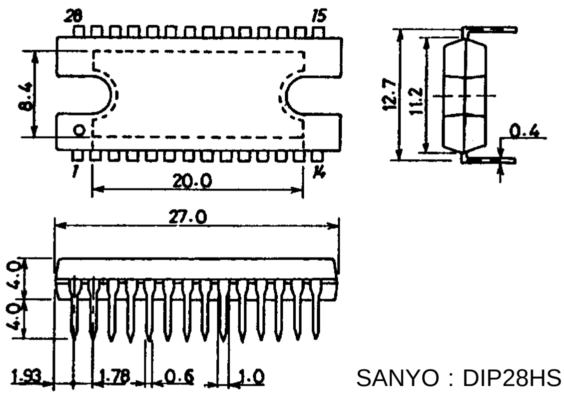
Overview

The LB1820 is a three-phase brushless motor with a digital speed control circuit built in.
The LB1820 is ideally suited for use in office automation applications such as laser beam printers and drum motor drivers.

Package Dimensions

unit : mm

3147-DIP28HS



Features

- Three-phase brushless motor driver with digital speed control function
- 30 V withstand voltage and 2.5 A output current
- Current limiter built in
- Low-voltage protection circuit built in
- Thermal shutdown circuit built in
- Hall amp with hysteresis
- Start/stop pin built in
- Crystal oscillator and divider built in
- Digital speed control circuit built in
- Lock detector built in

Specifications

Absolute Maximum Ratings at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_{CC}		30	V
Maximum supply voltage 2	V_M		30	V
Output current	I_O	t ≦ 100 ms	2.5	A
Allowable power dissipation 1	Pd max 1	Independent IC	3	W
Allowable power dissipation 2	Pd max 2	With arbitrarily large heat sink	20	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25 °C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1	V_{CC}		9.5 to 28	V
Supply voltage range 2	V_M		5 to 28	V
Voltage regulator output current	I_{VH}		0 to +20	mA
Comparator output current	I_{OSC}		0 to +30	mA
Lock detector output current	I_{LD}		0 to +20	mA

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Electrical Characteristics at Ta = 25 °C, V_{CC} = V_M = 24 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply current 1	I_{CC1}			33	50	mA
Supply current 2	I_{CC2}	Stop mode		3	5	mA
Output saturation voltage	$V_{O\ (sat)}$ 1	I_O = 1 A		2.1	3.0	V
	$V_{O(sat)}$2	I_O = 2 A		3.0	4.2	V
Output leak current	I_O leak				100	µA
Voltage regulator						
Output voltage	V_H	I_{VH} = 10 mA	3.8	4.15	4.5	V
Voltage variation	ΔV_H1	V_{CC} = 9.5 to 28 V		60	150	mV
Load variation	ΔV_H2	I_{VH} = 5 to 20 mA		60	150	mV
Temperature coefficient				–2		mV/ °C
Hall amp						
Input bias current	I_{HB}			1	4	µA
Common-mode input voltage	V_{ICM}		1.5		2.8	V
Hall input sensitivity			100			mVp-p
Hysteresis width	ΔV_{IN}		24	33	42	mV
Low-to-high input voltage	V_{SLH}		8	20	32	mV
High-to-low input voltage	V_{SHL}		–25	–13	–1	mV
Oscillator						
High-level output voltage	$V_{OH(CR)}$		2.9	3.2	3.5	V
Low-level output voltage	$V_{OL(CR)}$		0.9	1.1	1.3	V
Oscillation amplitude			1.8	2.1	2.4	V
Oscillation frequency	f	R = 30 kΩ, C = 1500 pF		18.5		kHz
Temperature coefficient	Δf			0.1		%/ °C
Comparator output voltage	V_{OSC}	I_{OSC} = 20 mA			1.5	V
Current limiter						
Limiter 1	V_{Rf}1		0.42	0.5	0.6	V
Limiter 2	V_{Rf}2		0.4	0.44	0.48	V
Thermal shutdown						
Thermal shutdown temperature	TSD	Design target	150	180		°C
Hysteresis width	ΔTSD			30		°C
Low-voltage protection voltage	V_{LVSD}		7.5	8.1	8.7	V
Hysteresis width	ΔV_{LVSD}		0.45	0.6	0.75	V
FG amp						
Input offset voltage	$V_{IO(FG)}$		–10		+10	mV
Input bias current	$I_{B(FG)}$		–1		+1	µA
High-level output voltage	$V_{OH(FG)}$	I_{FG} = –2 mA	5.6	6.2	6.8	V
Low-level output voltage	$V_{OL(FG)}$	$I_{(FG)}$ = 2 mA		1	1.5	V
FG input sensitivity		10 × Gain	5			mV
Schmitt width at next stage				16		mV
Operating frequency range					5	kHz
Open-loop voltage gain			60			dB
Speed discriminator						
High-level output voltage	$V_{OH(D)}$			4.7		V
Low-level output voltage	$V_{OL(D)}$			0.3		V
Maximum clock frequency			1.0			MHz
Number of counts			2044	2046	2048	
Integrator						
Input offset voltage	$V_{IO(INT)}$		–10		+10	mV
Input bias current	$I_{B(INT)}$		–0.4		+0.4	µA
High-level output voltage	$V_{OH(INT)}$		3.7	4.3	4.9	V
Low-level output voltage	$V_{OL(INT)}$			0.8	1.2	V
Open-loop gain			60			dB
Gain-bandwidth product				1.6		MHz
Reference voltage			–5%	V5/2	5%	V
5 V supply	V5		4.6	5	5.4	V

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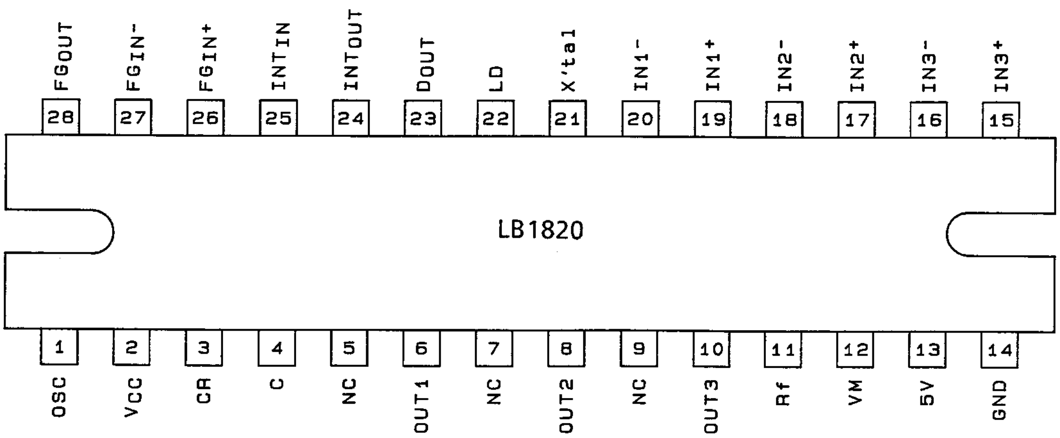
Parameter	Symbol	Conditions	min	typ	max	Unit
Lock detector						
Low-level output voltage	$V_{OL(LD)}$	I_{LD}=10 mA			0.5	V
Lock range				±3.125		%
Start/stop pin						
Start/stop operating voltage			0.4	0.5	0.6	V
Crystal Oscillator						
Precision of oscillating frequency		Referenced to indicated frequency	–500		+500	ppm
Temperature coefficient				–3		ppm/ °C
Drift in rotational speed				±0.01		%

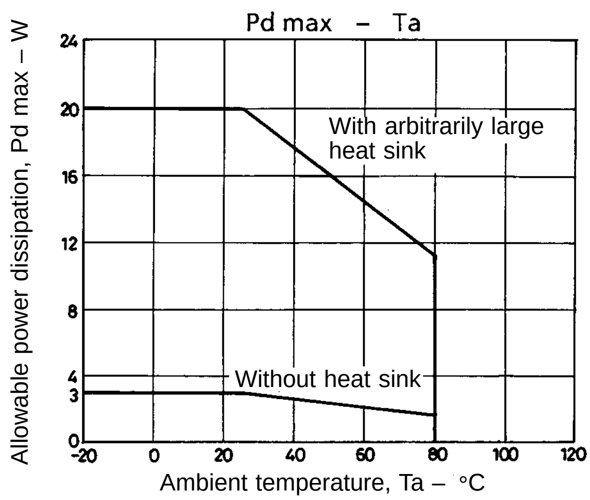
Truth Table

	Source → Sink	Input		
		IN1	IN2	IN3
1	OUT 3 → OUT 2	H	H	L
2	OUT 3 → OUT 1	H	L	L
3	OUT 2 → OUT 1	H	L	H
4	OUT 2 → OUT 3	L	L	H
5	OUT 1 → OUT 3	L	H	H
6	OUT 1 → OUT 2	L	H	L

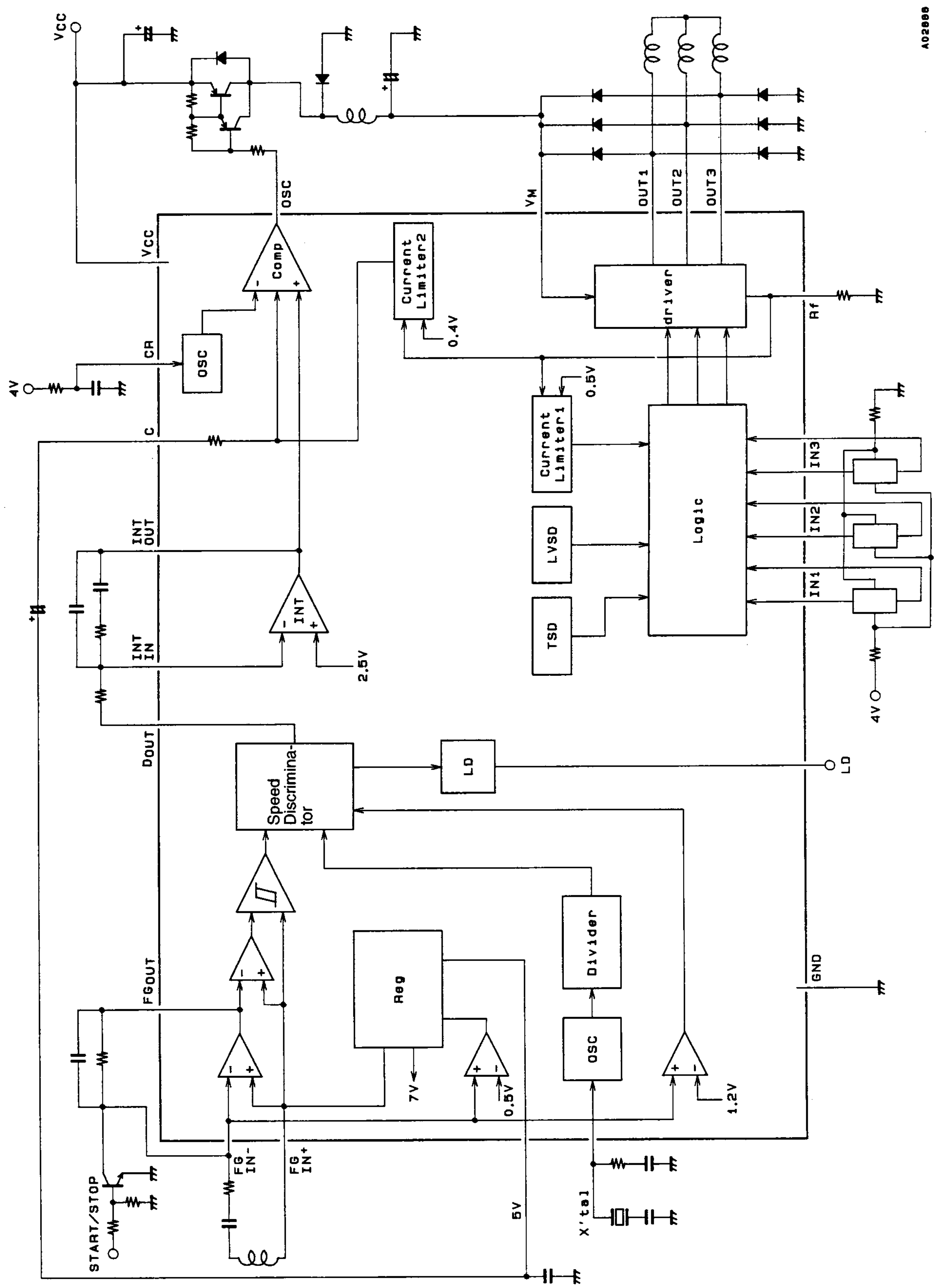
Pin Assignment



Top view



Internal Equivalent Circuit Block Diagram



Pin Description

Pin No.	Pin Name	Functions
19, 20 17, 18 15, 16	IN^+1, IN^-1 IN^+2, IN^-2 IN^+3, IN^-3	OUT 1: Hall element input pins for Phase 1. "H" logic is the state when $IN^+ > IN^-$. OUT 2: Hall element input pins for Phase 2. "H" logic is the state when $IN^+ > IN^-$. OUT 3: Hall element input pins for Phase 3. "H" logic is the state when $IN^+ > IN^-$.
6 8 10	OUT 1 OUT 2 OUT 3	Output pin 1. Output pin 2. Output pin 3.
2	V_{CC}	Power supply for other than output blocks.
12	V_M	Power supply for output blocks.
11	R_f	Output current detection pin. R_f is connected across this pin and GND to detect the output current as voltage.
14	GND	Ground for other than output blocks. The lowest potential of output transistor is the voltage at R_f pin.
3	CR	Sets the oscillating frequency of the switching regulator.
1	OSC	Outputs duty-controlled pulses. Open-collector output.
24	INT_{OUT}	Integrator output pin (speed control pin). Varies the switching regulator output voltage.
25	INT_{IN}	Integrator input pin.
23	D_{OUT}	Speed discriminator output pin. Goes LOW when the specified speed is exceeded.
4	C	Suppresses ripples in the motor current during operation of current limiter 2.
22	LD	Lock detection pin. Goes HIGH when the motor rotation speed is within the locking range.
27 26	FG_{IN}^- FG_{IN}^+	FG pulse input (Start/Stop control) pin. FG pulse input (4 V supply) pin.
28	FG_{OUT}	FG amp output pin.
21	Xtal	Crystal oscillator connecting pin.
13	5 V	5 V supply pin.

Operation Notes

Speed Control Circuit

This IC uses a speed discrimination circuit to perform speed control. The rotation accuracy of the speed discrimination method depends on the counter count. The counter count in this IC is 2046. On the FG1 cycle, a speed error signal with a resolution of 1/2046 is output from the D_{OUT} pin (charge pump method).
The D_{OUT} output shifts among three states: high, high impedance, and low:

High	: Output S (acceleration signal)
High impedance	: When neither output S nor output F is output
Low	: Output F (deceleration signal)

The relationship between the FG frequency (f_{FG}) and the quartz oscillation frequency (f_{OSC}) can be calculated as follows:

$f_{FG} = f_{OSC} \div (\text{ECL division ratio} \times \text{count})$
$f_{OSC} \div (8 \times 2046)$
$f_{OSC} \div 16368$

PAM Drive System

This IC controls motor rotations by configuring an external switching regulator, and controlling the voltage (V_M) of the regulator. Select a switching regulator diode with a short reverse recovery time such as an FRD (First Recovery Diode). Because even a smooth coil can become a noise source, attention must be paid to the arrangement of components on the board (especially avoiding the effects of FG signal lines and integrated amplifiers).
Select a normal rectifier diode for the upper and lower motor drive pin section (OUT1 to 3).

Current Limiter Circuit

The current limiter circuit consists of two limiter circuits.

① Limiter 1
Detection voltage $V_{Rf}1$ = 0.5 V typ. Current is limited by putting the lower output transistor in the nonsaturated state and then dropping the voltage applied to the motor.

② Limiter 2
Detection voltage $V_{Rf}2$ = 0.44 V typ. The V_M voltage is limited by limiting the OSC pin "on duty" ratio.

Normally, if an excessive load is put on the motor, limiter 1 operates first, and after a delay in the switching regulator, limiter 2 operates.
Sometimes, after startup, the ASO of the output transistor is very severe. In such a case, it is necessary to perform a soft start (in which V_M is increased gradually). When using soft starts, connect a capacitor between the pin (V_M, 5 V, etc.) on which the voltage is to be increased during startup and the C pin. If soft starts are not to be used, connect a capacitor between the C pin and ground.

Speed Lock Range

The speed lock signal is output from the LD pin. The speed lock range is within ±3.13%; if the motor rotations fall within the lock range the LD pin goes low (open collector output).

Start/stop Operation

The FG_{IN}^- pin also serves as the start/stop pin. When the FG_{IN}^- pin is connected to a transistor, etc., and the voltage is 0.5 V typ. or less, the stop state goes into effect. In the stopped state, in addition to the drive outputs being turned off, the FG_{IN}^+, 5 V, and other regulator outputs are also turned off.
When it is necessary to drive the motor at high speed, improvement is possible by adding a resistor (of approximately 1 MΩ) between FG_{OUT} and V_{CC}. (The time from when the transistor is turned off until FG_{IN}^- goes to 0.5V is reduced.)

Initial Reset Operation

At startup, it is possible to apply an initial reset to the logic circuits by delaying the increase in voltage on FG_{IN}^-. If an initial reset is not applied, the LD pin may go low from start until the FG pulse is input to the logic circuits (until output of approximately 16 mVp-p is generated on FG_{OUT}).
When an FG reset is applied, the capacitor between the FG_{IN}^+ and GND should be 4.7 μF or more (in order to delay the rise in FG_{IN}^-). Caution is required, because if the FG amplifier input capacitor is too small and the feedback capacitor is too large, the reset time will be shorter. At start, a delay of about 5 μs or more from the rising edge of the 5 V regulator output until the FG_{IN}^- voltage goes to 1.2 V is desirable.

PWM Frequency Setting

The PWM frequency is determined by the resistor and capacitor connected to the CR pin. When a resistor is connected to the FG_{IN+} pin, the PWM frequency can be roughly calculated by the following formula:

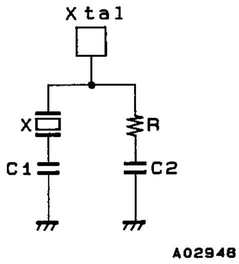
$f_{PWM} \fallingdotseq 1 \div (1.2 \times C \times R)$

The resistor must not be less than 30 kΩ. It is desirable for the PWM frequency to be about 15 kHz.

Quartz Oscillator

An oscillator, capacitor and resistor are to be connected to the quartz oscillator. When selecting the oscillator and the external capacitor and resistor, always obtain approval from the manufacturer of the oscillator in order to avoid problems.

(Circuit with external quartz oscillator)



External constants (reference values)

Xtal (MHz)	C1 (pF)	C2 (pF)	R (kΩ)
3 to 4	39	82	0.82
4 to 5	39	82	1.0
5 to 7	39	47	1.5
7 to 10	39	27	2.0

However, use a crystal such that the base wave f_O impedance : $3f_O$ impedance = 1 : 5 or more

When inputting external signals (of several MHz) to the quartz oscillator, connect external components as shown in the diagram below.

f_{IN} = 1 to 8 MHz

Input signal level High level voltage: 4.0 V min.

Low level voltage: 1.5 V max.

Ra = 2 kΩ, Rb = 1 kΩ (reference values)