



# LB1854M

## Three-Phase Brushless Motor Driver IC

### Overview

The LB1854M is a three-phase brushless motor driver IC and is optimal, in particular, for driving VCR capstan and drum motors.

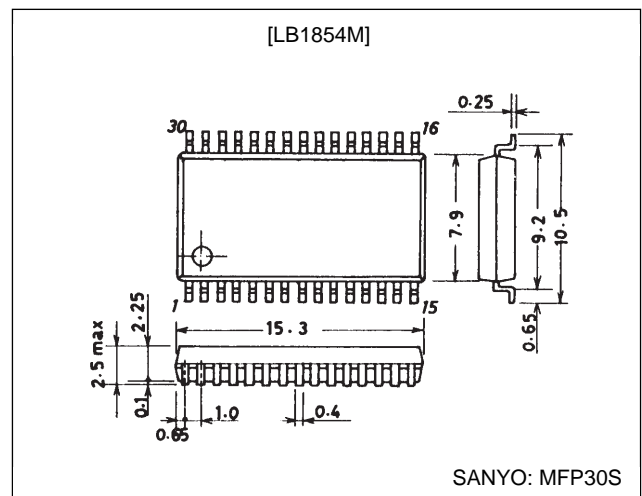
### Features

- 120° voltage linear drive technique
- The LB1854M soft switching scheme allows smaller external capacitors to be used (e.g., chip capacitors).
- Built-in thermal-shutdown function
- Built-in overcurrent protection circuit
- Built-in FG amplifiers (operational amplifier and Schmitt amplifier)
- Control start voltage set by an external voltage
- The output current feedback level can be changed by changing the control gain to one of two levels.

### Package Dimensions

unit: mm

#### 3073A-MFP30S



### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter                   | Symbol                | Conditions | Ratings     | Unit             |
|-----------------------------|-----------------------|------------|-------------|------------------|
| Maximum supply voltage      | $V_{CC1 \text{ max}}$ |            | 20          | V                |
|                             | $V_{CC2 \text{ max}}$ |            | 7.0         | V                |
| Applied output voltage      | $V_{OU, v, w}$        |            | 22          | V                |
| Maximum output current      | $I_{OUT \text{ max}}$ |            | 1.5         | A                |
| Allowable power dissipation | $P_d \text{ max}$     |            | 1.05        | W                |
| Operating temperature       | $T_{opr}$             |            | -20 to +75  | $^\circ\text{C}$ |
| Storage temperature         | $T_{stg}$             |            | -55 to +150 | $^\circ\text{C}$ |

#### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter      | Symbol    | Conditions | Ratings    | Unit |
|----------------|-----------|------------|------------|------|
| Supply voltage | $V_{CC1}$ |            | 5 to 18    | V    |
|                | $V_{CC2}$ |            | 4.3 to 6.5 | V    |

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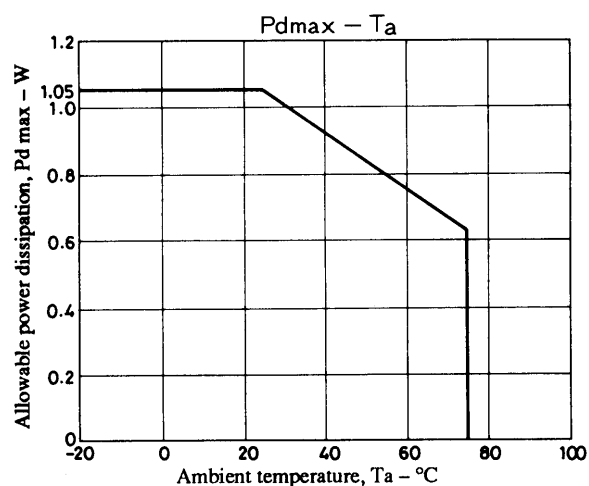
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## LB1854M

### Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC1} = 12\text{ V}$ , $V_{CC2} = 5\text{ V}$

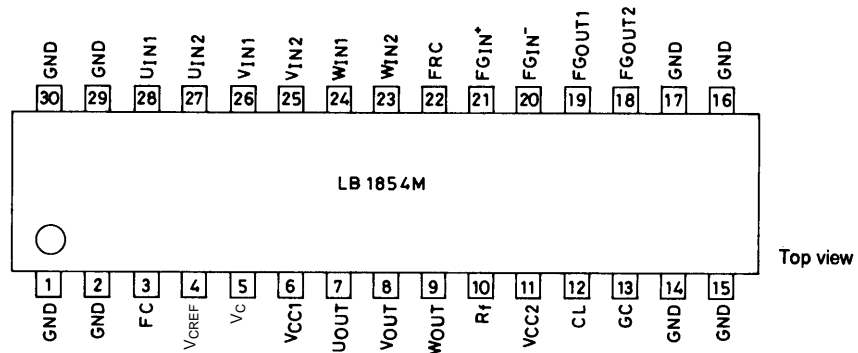
| Parameter                                      | Symbol              | Conditions                               | min | typ | max | Unit             |
|--|---------------------|--|-----|-----|-----|------------------|
| Current drain                                  | $I_{CC1}$           | $V_C = 0\text{ V}$ , $R_L = \infty$      |     | 17  | 30  | mA               |
|  | $I_{CC2}$           | $V_C = 0\text{ V}$                       |     | 6.5 | 9.5 | mA               |
| [Drive Block]                                  |                     |  |     |     |     |                  |
| Output saturation voltage                      | $V_O(\text{sat}) 1$ | $I_{OUT} = 0.5\text{ A}$ , sink + source |     | 1.6 | 2.2 | V                |
|  | $V_O(\text{sat}) 2$ | $I_{OUT} = 1.0\text{ A}$ , sink + source |     | 2.0 | 3.0 | V                |
| Output TRS breakdown voltage                   | $V_O(\text{sus})$   | $I_{OUT} = 20\text{ mA}^*$               | 20  |     |     | V                |
| Output resting potential                       | $V_{OQ}$            | $V_C = 0\text{ V}$                       | 5.7 | 6.0 | 6.3 | V                |
| Hall amplifier input offset voltage            | $V_H$ offset        |  | -5  |     | +5  | mV               |
| Hall amplifier input bias current              | $I_H$ bias          |  |     | 1   | 5   | $\mu\text{A}$    |
| Hall amplifier common mode input voltage range | $V_H$ ch            |  | 1.3 |     | 2.2 | V                |
| Hall input/output voltage gain                 | $GV_{HO}$           |  | 43  | 46  | 49  | dB               |
| [Control Block]                                |                     |  |     |     |     |                  |
| Control output drive gain                      | $GV_{CO1}$          | High gain                                | 37  | 40  | 43  | dB               |
|  | $GV_{CO2}$          | Low gain                                 | 31  | 34  | 37  | dB               |
| Control output CH difference                   | $\Delta GV_{CO}$    |  | -2  |     | +2  | dB               |
| Control start voltage                          | $V_{CTH}$           | When $V_{OUTP-p} = 2\text{ V}$           |     | 2.5 |     | V                |
| Gain control switching high level              |                     |  | 4   |     | 5   | V                |
| Gain control switching middle level            |                     | Middle level when the input is open      | 2   |     | 3   | V                |
| Gain control switching low level               |                     |  | 0   |     | 1   | V                |
| [FG Amplifier]                                 |                     |  |     |     |     |                  |
| FG amplifier input offset voltage              | $V_{FG}$ offset     |  | -8  |     | +8  | mV               |
| Open-loop voltage gain                         | $GV_{FG}$           | $f = 1\text{ kHz}$                       |     | 60  |     | dB               |
| Source output saturation voltage               | $V_{FG\text{ OU}}$  | $I_O = 2\text{ mA}$                      | 37  |     |     | V                |
| Sink output saturation voltage                 | $V_{FG\text{ OD}}$  | $I_O = -2\text{ mA}$                     |     |     | 1.3 | V                |
| Common-mode signal rejection ratio             | CHR                 | *  |     | 80  |     | dB               |
| FG amplifier common-mode input voltage range   | $V_{FG\text{ CH}}$  |  | 0   |     | 3.5 | V                |
| Phase margin                                   |                     | *  |     | 20  |     | Deg              |
| Schmitt hysteresis                             | $\Delta V_{sh1}$    | $FG_{OUT2}$ : High to low                |     | 22  |     | mV               |
|  | $\Delta V_{sh2}$    | $FG_{OUT2}$ : Low to high                |     | 22  |     | mV               |
| Schmitt input voltage range                    | $V_{shCH}$          |  | 0.7 |     | 3.5 | V                |
| [Thermal Shutdown]                             |                     |  |     |     |     |                  |
| Operating temperature                          | TSD                 | *  | 150 | 180 | 210 | $^\circ\text{C}$ |
| Hysteresis                                     | $\Delta TSD$        | *  |     | 15  |     | $^\circ\text{C}$ |

Note: \* Items marked with an asterisk are design target values and are not measured.

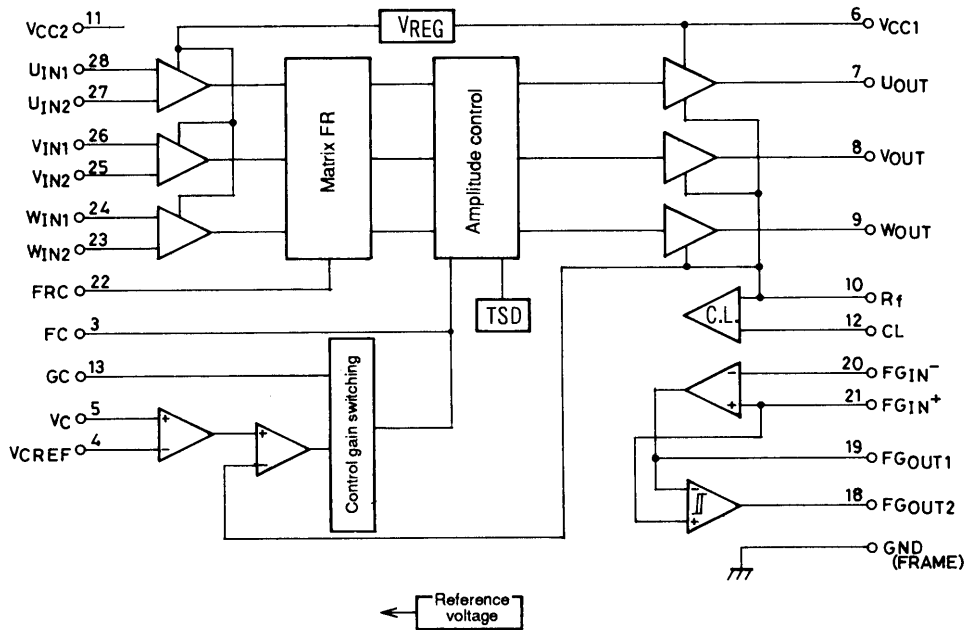


# LB1854M

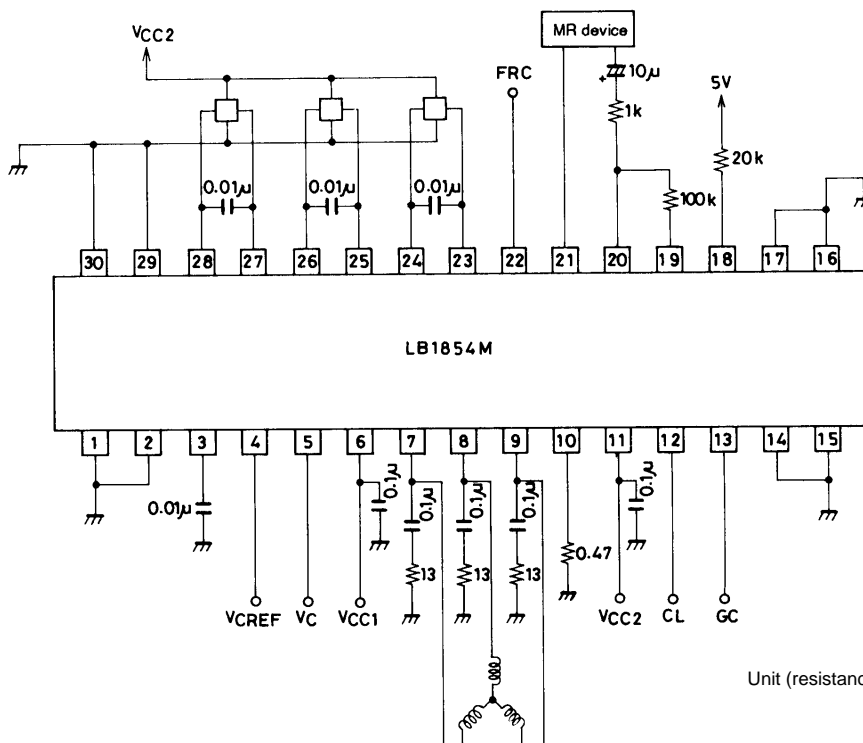
## Pin Assignment



## Block Diagram



## Sample Application Circuit



Unit (resistance: Ω, capacitance: F)

## LB1854M

### Truth Table

|   | Source<br>Sink    | Input |   |   | Forward and reverse control<br>F/RC |
|---|-------------------|-------|---|---|-------------------------------------|
|   |                   | U     | V | W |                                     |
| 1 | W phase → V phase | H     | H | L | L                                   |
|   | V phase → W phase |       |   |   | H                                   |
| 2 | W phase → U phase | H     | L | L | L                                   |
|   | U phase → W phase |       |   |   | H                                   |
| 3 | V phase → W phase | L     | L | H | L                                   |
|   | W phase → V phase |       |   |   | H                                   |
| 4 | U phase → V phase | L     | H | L | L                                   |
|   | V phase → U phase |       |   |   | H                                   |
| 5 | V phase → U phase | H     | L | H | L                                   |
|   | U phase → V phase |       |   |   | H                                   |
| 6 | U phase → W phase | L     | H | H | L                                   |
|   | W phase → U phase |       |   |   | H                                   |

Input high: Phase 1 is 0.2 V or more higher than the corresponding phase 2 for each phase input.

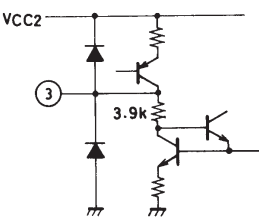
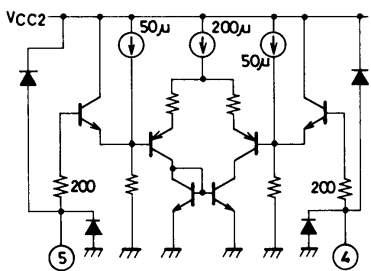
Low: Phase 1 is 0.2 V or more lower than the corresponding phase 2 for each phase input.

Forward and reverse control high: 2.3 V to  $V_{CC1}$

Low: 0 V to 0.7 V

### Pin Functions

Unit (resistance:  $\Omega$ )

| Pin No.                               | Symbol               | Pin voltage  | Equivalent circuit  | Function   |
|---------------------------------------|----------------------|--|---|--|
| 1, 2, 14,<br>15, 16,<br>17, 29,<br>30 | FRAME<br>(GND)       |  |   | Ground for all circuits except the outputs   |
| 3                                     | FC                   |  |  | The gain frequency characteristics can be lowered by connecting a capacitor between this pin and ground to prevent oscillation.  |
| 4<br>5                                | $V_{C REF}$<br>$V_C$ | 1.5 V min<br>$V_{CC2}$ max<br>0 V min<br>$V_{CC2}$ max |  | Speed control<br>The LB1854M implements a voltage control scheme in which the output voltage is controlled by the pin 5 voltage. The pin 4 voltage determines the control start voltage. |
| 6                                     | $V_{CC1}$            | 5 to 18 V  |   | Power supply that provides the drive outputs   |

## LB1854M

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Unit (resistance:  $\Omega$ )

| Pin No.     | Symbol                              | Pin voltage              | Equivalent circuit | Function   |
|-------------|-------------------------------------|--------------------------|--------------------|--|
| 7<br>8<br>9 | $U_{OUT}$<br>$V_{OUT}$<br>$W_{OUT}$ |                          |                    | Output pins  |
| 10          | $R_f$                               |                          |                    | Output transistor ground<br>Feedback can be applied to the control amplifier by inserting resistor between this pin and GND and detecting the output current as a voltage. The overcurrent protection circuit (current limiter) operates by detecting the voltage on this pin. |
| 11          | $V_{CC2}$                           | 4.3 to 6.5 V             |                    | Power supply provided to all blocks other than the output block<br>This voltage must be stabilized so that no ripple or other noise is present.  |
| 12          | CL                                  | 0 V min<br>$V_{CC2}$ max |                    | The current limiter operates when the $R_f$ pin reaches the same potential as pin 12. The pin 12 potential is set up externally.   |
| 13          | GC                                  | 0 V min<br>$V_{CC2}$ max |                    | Control input to output gain switching pin<br>High level (4 to 5 V): 34 dB<br>Middle level (2 to 3 V) or open: 40 dB (low speed): 34 dB (high speed)<br>Low level (0 to 1 V): 40 dB<br>However, note that this applies when $V_{CC2}$ is 5 V.                                  |
| 18          | $FG_{OUT2}$                         |                          |                    | FG Schmitt amplifier output  |
| 19          | $FG_{OUT1}$                         |                          |                    | FG amplifier output  |

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## LB1854M

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Unit (resistance:  $\Omega$ )

| Pin No.                          | Symbol   | Pin voltage  | Equivalent circuit | Function  |
|----------------------------------|--|--|--------------------|---|
| 20<br>21                         | FG <sub>IN-</sub><br>FG <sub>IN+</sub>   | 0 V min<br>3.5 V max<br>(when V <sub>CC2</sub> is 5 V) |                    | FG signal input   |
| 22                               | FRC  | High: 2.3 V min<br>Low: 0.7 V max                      |                    | Motor forward/reverse control pin<br>Low level (0.7 V or lower): forward<br>High level (2.3 V or higher): reverse   |
| 23<br>24<br>25<br>26<br>27<br>28 | W <sub>IN2</sub><br>W <sub>IN1</sub><br>V <sub>IN2</sub><br>V <sub>IN1</sub><br>U <sub>IN2</sub><br>U <sub>IN1</sub> | 1.4 V min<br>2.0 V max                                 |                    | W phase Hall sensor input<br>Logic high is the W <sub>IN1</sub> > W <sub>IN2</sub> state.<br>V phase Hall sensor input<br>Logic high is the V <sub>IN1</sub> > V <sub>IN2</sub> state.<br>U phase Hall sensor input<br>Logic high is the U <sub>IN1</sub> > U <sub>IN2</sub> state. |

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