



Three-Phase Brushless Motor Driver IC

Overview

The LB1857M is a three-phase brushless motor driver IC designed for use as a camcorder capstan or drum motor driver, or as a digital audio tape player/recorder motor driver.

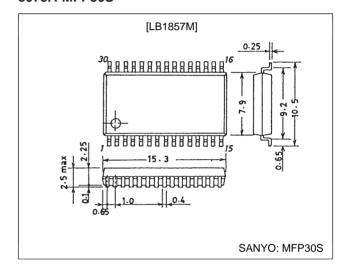
Features

- 120° voltage linear system
- Appropriate for portable applications, since the LB1857M reduces system power requirements by using motor voltage control for speed control.
- Built-in torque ripple compensation circuit
- Small external capacitances due to the adoption of a soft switching technique (chip capacitor).
- Built-in thermal shutdown circuit
- Built-in FG amplifier

Package Dimensions

unit: mm

3073A-MFP30S



Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
	V _{CC} 1 max		7	V
Supply voltage	V _{CC} 2 max		16	V
	V _S max		V _{CC} 2	V
Output applied voltage	V _O max		V _S + 2	V
Output current	I _O max		1.5	A
Allowable power dissipation	Pd max		1.0	W
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
	V _{CC} 1	V _{CC} 1 ≤ V _{CC} 2	4.0 to 6.0	V
Supply voltage	V _{CC} 2		4 to 14	V
	Vs		Up to V _{CC} 2	V

LB1857M

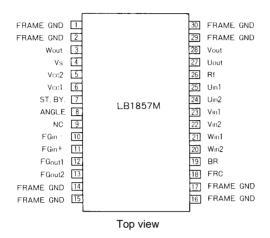
Electrical Characteristics at $Ta=25^{\circ}C,\,V_{CC}1=5~V,\,V_{CC}2=7~V,\,V_{S}=3~V$

		0 1111	Ratings			11.5
Parameter	Symbol	Conditions	min	typ	max	Unit
	I _{CC} 1	V _{BR} = 5 V		4.5	6.5	mA
Supply current	I _{CC} 2	V _{BR} = 5 V		13	20	mA
	I _S	$V_{BR} = 5 \text{ V}, R_L = \infty$		6.5	9.0	mA
Output quiescent current	Iccoq	V _{STBY} = 0 V			180	μA
Output quiescent current	I _{SOQ}	$V_{STBY} = 0 \text{ V}, R_L = \infty$			150	μA
Output saturation voltage	V _{O(sat)}	I _{OUT} = 0.6 A, sink + source			2.3	V
Output TRS withstand voltage	V _{O(sus)}	I _{OUT} = 20 mA*1	16			V
Output quiescent voltage	V _{OQ}	$V_{BR} = 5 V$	1.4	1.5	1.6	V
Hall amplifier input offset voltage	V _{HOFFSET}	*1	-5		+5	mV
Hall amplifier common mode input voltage range	V _{НСОМ}		1.4		2.8	V
Hall I/O voltage gain	GV _{HO}	Rangle = 8.2 kΩ	32.0	35.0	38.0	dB
Brake pin high level voltage	V _{BRH}		2.0			V
Brake pin low level voltage	V _{BRL}				0.8	V
Brake pin input current	I _{BRIN}				100	μA
Brake pin leakage current	I _{BRLEAK}				-30	μA
FRC pin high level voltage	V _{FRCH}		2.8			V
FRC pin low level voltage	V _{FRCL}				1.2	V
FRC pin input current	I _{FRCIN}				100	μA
FRC pin leakage current	I _{FRCLEAK}				-30	μA
Upper side residual voltage	V _{XH}	$I_{OUT} = 100 \text{ mA}, V_{CC}2 = 6 \text{ V}, V_{S} = 2 \text{ V}$	0.32		0.49	V
Lower side residual voltage	V _{XL}	$I_{OUT} = 100 \text{ mA}, V_{CC}2 = 6 \text{ V}, V_{S} = 2 \text{ V}$	0.39		0.48	V
Overlap level	OL	V _{CC} 2 = 6 V, V _S = 3 V	60	70	80	%
Standby on voltage	V _{STBYL}	*2	-0.2		+0.1	V
Standby off voltage	V _{STBYH}		2		5	V
Standby pin bias current	I _{STBYIN}				10	μA
Thermal protection circuit operating temperature	T _{TSD}	*1	150	180	210	°C
Thermal protection circuit hysteresis	ΔT_{TSD}	*1		15		°C
[FG amplifier]						
Input offset voltage	V _{FG} OFFSET		-8		+8	mV
Open loop voltage gain	GV _{FG}	f = 1 kHz		60		dB
Source output saturation voltage	V _{FG OU}	$I_0 = -2 \text{ mA}$	3.7			V
Sink output saturation voltage	V _{FG OD}	I _O = 2 mA			1.3	V
Common mode signal exclusion ratio	CHR	*1		80		dB
FG amplifier common mode input voltage range	V _{FG CH}		0		3.5	V
Phase margin	φМ	*1		20		deg
Schmitt amplifier threshold voltage	V _{FGS SH}	V_{FGIN}^+ = 2.5 V, when V_{FGOUT}^2 goes from high to low	2.45	2.50	2.55	V
Schmitt amplifier hysteresis width	V _{FGS HIS}	V _{FGIN} + = 2.5 V	20	40	60	mV

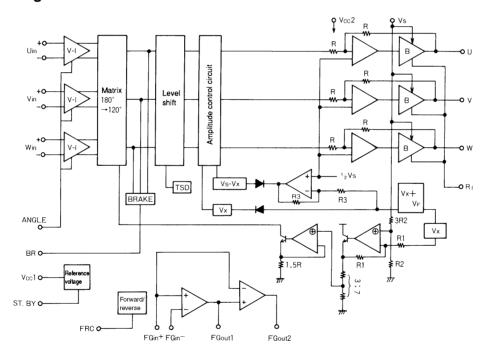
Note: 1. These are target settings, and are not measured. The overlap ratings are taken as test ratings without change.

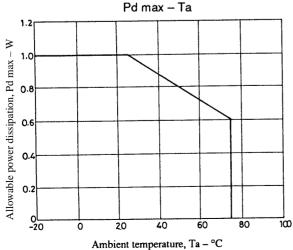
2. When the standby pin is open the IC will be in the standby state.

Pin Assignment



Block Diagram





Pin Functions Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
4	V _S	≤ V _{CC} 2	Equivalent official	Power supply input that determines the output amplitude. It must be set to a voltage equal or lower than $V_{CC}2$.
5	V _{CC} 2	4 to 14 V		Power supply for power amplifier systems other than motor drive transistors. Power supply pin that provides voltage for blocks other than control blocks supplied by V _{CC} 1.
6	V _{CC} 1	4 to 6 V		Power supply that provides voltage for the Hall amplifier, the forward/reverse circuit, the FG amplifier, and the thermal shutdown circuit.
7	ST. BY	(H): 0.1 V max (L): 2.0 V min (When V _{CC} 1 is 5 V)	7 200 7 200	All circuits can be made inoperative either by connecting this pin to GND, or by leaving it open. In that state the supply current will be approximately 100 μA. Hold at 2 V or higher during normal operation.
8	ANGLE		V _{CC} 1	Connect a resistor between this pin and GND. Changing the value of this resistor will change the Hall input-output gain (motor waveform slope).
10 11	FG _{IN} +	0 V min 3.5 V max (When V _{CC} 1 is 5 V)	Vcc1	FG signal input pin
12	FG _{OUT} 1		Vcc1 38 38 12 12	FG amplifier output pin

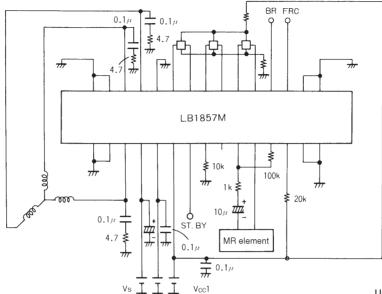
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Unit (resistance: Ω)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Pin function
13	FG _{OUT} 2	Fili voltage	Equivalent circuit	FG Schmitt amplifier output pin
13	1 GOUTZ		Vcc1 13	1 9 Schmitt ampliller output pin
18	FRC	(H): 2.8 V min (L): 1.2 V max (When V _{CC} 1 is 5 V)	Vcc1	Pin for setting the motor to forward or reverse rotation Low level: Forward rotation (under 1.2 V: when V _{CC} 1 is 5 V) High level: Reverse rotation (over 2.8 V: when V _{CC} 1 is 5 V)
19	BR	(H): 2.0 V min (L): 0.8 V max	Vcc2	Motor brake pin Low level: Motor drive (under 0.8 V) High level: Motor brake (over 2.0 V)
20 21 22 23 24 25	W _{IN} 2 W _{IN} 1 V _{IN} 2 V _{IN} 1 U _{IN} 2 U _{IN} 1	1.4 V min 2.8 V max (When V _{CC} 1 is 5 V)	25) 200 24) 200 22) 200 mm	W phase Hall element input pins. Logic high is defined to be states where W _{IN} 1 > W _{IN} 2. V phase Hall element input pins. Logic high is defined to be states where V _{IN} 1 > V _{IN} 2. U phase Hall element input pins. Logic high is defined to be states where U _{IN} 1 > U _{IN} 2.
26	R _f			Output transistor GND
27	U _{OUT}			Output pin
28 3	Vout Wout		28 28 3 77 88	
1, 2, 14, 15, 16, 17, 29, 30	FRAME (GND)			GND for all circuits other than output transistors.

Sample Application Circuit



Units (resistance: Ω , capacitance: F)

Logic Value Table

Source		Input			Forward and reverse control
	Sink	U	V	W	F/RC
1	W phase \rightarrow V phase	Н	Н		L
_ '	$V \text{ phase} \to W \text{ phase}$		П	L	Н
2	W phase \rightarrow U phase	Н			L
	$\text{U phase} \rightarrow \text{W phase}$			-	Н
3	$V \text{ phase} \to W \text{ phase}$			Н	L
3	W phase \rightarrow V phase	-	L		Н
4	$\mbox{U phase} \rightarrow \mbox{V phase}$		Н		L
4	$V \text{ phase} \to U \text{ phase}$	-		L	Н
5	$V \text{ phase} \to U \text{ phase}$	Н		Н	L
5	U phase \rightarrow V phase	"	L	П	Н
6	$U\;phase\toW\;phase$		Н	Н	L
6	W phase → U phase	-			Н

Inputs:

High: For each phase, the input 1 potential is at least 0.2 V higher than the input 2 potential. Low: For each phase, the input 1 potential is at least 0.2 V lower than the input 2 potential.

Forward/reverse control: High: 2.8 V to V_{CC}1 Low: 0 to 1.2 V

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