



LB1889, 1889M, 1889D

3-phase Brushless Motor Driver for VTR Capstans

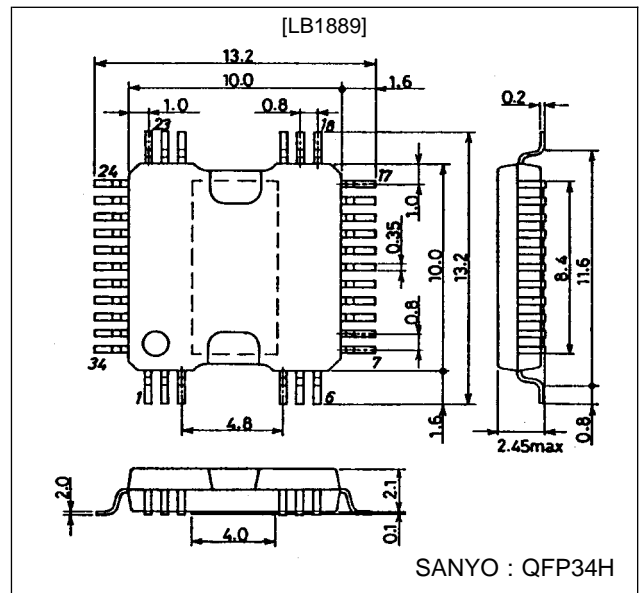
Functions

- 3-phase full-wave current linear drive system
- Torque ripple correction circuit built in (variable compensation ratio)
- Current limiting circuit built in/with control characteristic gain switch
- Output stage upper/lower oversaturation prevention circuit built in (no external capacitor required)
- FG amplifier built in
- Thermal shutdown circuit built in

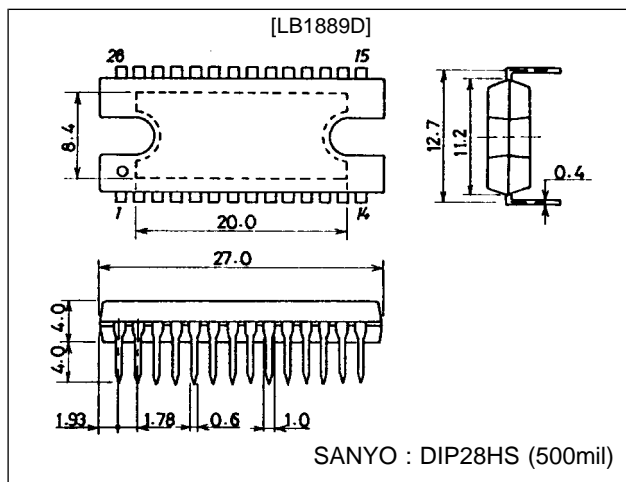
Package Dimensions

unit : mm

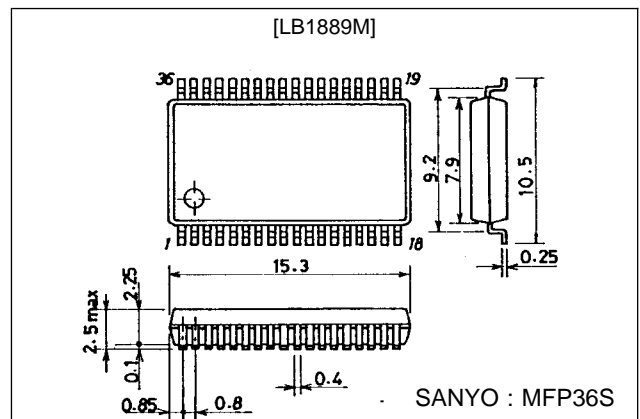
3206-QFP34H



3147A-DIP28HS



3129-MFP36S



Specifications

Absolute Maximum Ratings at $T_a = 25\text{ }^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|--------------|-------------------------------------|-------------|------------------|
| Maximum supply voltage | V_{CC} max | | 7 | V |
| | V_S max | | 24 | V |
| Maximum output current | I_O max | | 1.3 | A |
| Allowable power dissipation | Pd max | Arbitrarily large heat sink LB1889 | 12.5 | W |
| | | Arbitrarily large heat sink LB1889D | 15.0 | W |
| | | Independent IC LB1889 | 0.77 | W |
| | | Independent IC LB1889M | 0.95 | W |
| | | Independent IC LB1889D | 3.0 | W |
| Operating temperature | Topr | | -20 to +75 | $^\circ\text{C}$ |
| Storage temperature | Tstg | | -55 to +150 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = 25\text{ }^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|----------------------|--------------|--------------------------------|----------------------|------------|
| Supply voltage | V_S | | 5 to 22 | V |
| | V_{CC} | | 4.5 to 5.5 | V |
| Hall input amplitude | V_{HALL} | Between Hall inputs | ± 30 to ± 80 | mV_{0-P} |
| GSENSE input range | V_{GSENSE} | Relative to control system GND | -0.20 to +0.20 | V |

Electrical Characteristics at $T_a = 25\text{ }^\circ\text{C}$, $V_{CC} = 5\text{ V}$, $V_S = 15\text{ V}$

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| V_{CC} supply current | I_{CC} | $R_L = \infty$ (when stopped), $V_{CTL} = 0\text{ V}$, $V_{LIM} = 0\text{ V}$ | | 12 | 18 | mA |
| [Output] | | | | | | |
| Output saturation voltage | V_{Osat1} | $I_O = 500\text{ mA}$, $R_f = 0.5\ \Omega$, Sink + Source $V_{CTL} = V_{LIM} = 5\text{ V}$ (with saturation prevention) | | 2.1 | 2.6 | V |
| | V_{Osat2} | $I_O = 1.0\text{ A}$, $R_f = 0.5\ \Omega$, Sink + Source $V_{CTL} = V_{LIM} = 5\text{ V}$ (with saturation prevention) | | 2.6 | 3.5 | V |
| Output leakage current | I_{leak} | | | | 1.0 | mA |
| [FR] | | | | | | |
| FR pin input threshold voltage | V_{FSR} | | 2.25 | 2.50 | 2.75 | V |
| FR pin input bias current | I_b (FSR) | | -5.0 | | | μA |
| [Control] | | | | | | |
| CTLREF pin voltage | V_{CREF} | | 2.37 | 2.50 | 2.63 | V |
| CTLREF pin input range | V_{CREFIN} | | 1.70 | | 3.50 | V |
| CTL pin input bias current | I_b (CTL) | $V_{CTL} = 5\text{ V}$, CTLREF : Open | | | 8.0 | μA |
| CTL pin control start voltage | V_{CTL} (ST) | With $R_f = 0.5\ \Omega$, $V_{LIM} = 5\text{ V}$, $I_O \geq 10\text{ mA}$, Hall input logic fixed, (u, v, w = H, H, L) | 2.20 | 2.35 | 2.50 | V |
| CTL pin control switch voltage | V_{CTL} (ST2) | $R_f = 0.5\ \Omega$, $V_{LIM} = 5\text{ V}$ | 3.00 | 3.15 | 3.30 | V |
| CTL pin control Gm1 | Gm1 (CTL) | With $R_f = 0.5\ \Omega$, $\Delta I_O = 200\text{ mA}$, Hall input logic fixed, (u, v, w = H, H, L) | 0.52 | 0.65 | 0.78 | A/V |
| CTL pin control Gm2 | Gm2 (CTL) | With $R_f = 0.5\ \Omega$, $\Delta V_{CTL} = 200\text{ mV}$, Hall input logic fixed, (u, v, w = H, H, L) | 1.20 | 1.50 | 1.80 | A/V |
| [Current Limit] | | | | | | |
| LIM current limit offset voltage | V_{off} (LIM) | With $R_f = 0.5\ \Omega$, $V_{CTL} = 5\text{ V}$, $I_O \geq 10\text{ mA}$, Hall input logic fixed, (u, v, w = H, H, L) | 140 | 200 | 260 | mV |
| LIM pin input bias current | I_b (LIM) | With $V_{CTL} = 5\text{ V}$, CTLREF : Open, $V_{LIM} = 0\text{ V}$ | -2.5 | | | μA |
| LIM pin current limit level | I_{lim} | With $R_f = 0.5\ \Omega$, $V_{CTL} = 5\text{ V}$, $V_{LIM} = 2.06\text{ V}$, Hall input logic fixed, (u, v, w = H, H, L) | 830 | 900 | 970 | mA |
| [Hall Amplifier] | | | | | | |
| Hall amplifier input offset voltage | V_{off} (HALL) | | -6 | | +6 | mV |
| Hall amplifier input bias current | I_b (HALL) | | | 1.0 | 3.0 | μA |
| Hall amplifier common-mode input voltage | V_{cm} (HALL) | | 1.3 | | 3.3 | V |

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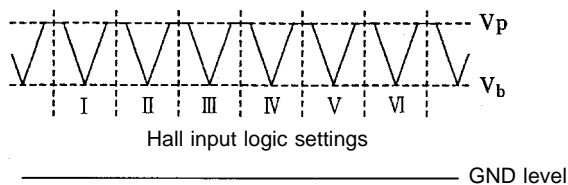
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Continued from preceding page.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|-------------------------------------------------|------------------|-------------------------------------------------------------------------------------------------|-------|------|-------|--------------|
| [TRC] | | | | | | |
| Torque ripple correction factor | T_{RC} | At bottom and peak in Rf waveform at $I_O = 200$ mA (RF = 0.5 Ω , ADJ-OPEN) Note 2 | | 9 | | % |
| ADJ pin voltage | V_{adj} | | 2.37 | 2.50 | 2.63 | V |
| [FG Amplifier] | | | | | | |
| FG amplifier input offset voltage | V_{off} (FG) | | -8 | | +8 | mV |
| FG amplifier input bias current | I_b (FG) | | -100 | | | nA |
| FG amplifier output saturation voltage | V_{Osat} (FG) | At internal pull-up resistor load on sink side | | | 0.5 | V |
| FG amplifier common-mode input voltage | V_{CM} (FG) | | 0.5 | | 4.0 | V |
| [Saturation] | | | | | | |
| Saturation prevention circuit lower set voltage | V_{Osat} (DET) | Voltage between each OUT and Rf at $I_O = 10$ mA, Rf = 0.5 Ω , $V_{CTL} = V_{LIM} = 5$ V | 0.175 | 0.25 | 0.325 | V |
| [TSD] | | | | | | |
| TSD operation temperature | T-TSD | (Design target) Note 1 | | 180 | | $^{\circ}$ C |
| TSD temperature hysteresis width | Δ TSD | (Design target) Note 1 | | 20 | | $^{\circ}$ C |

Note 1: No measurements are performed for any values listed in the conditions column as design targets.

Note 2: The torque ripple correction factor is calculated using the Rf voltage waveform as follows.



$$\text{Correction factor} = \frac{2 \times (V_p - V_b)}{V_p + V_b} \times 100 (\%)$$

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Truth Table & Control Function

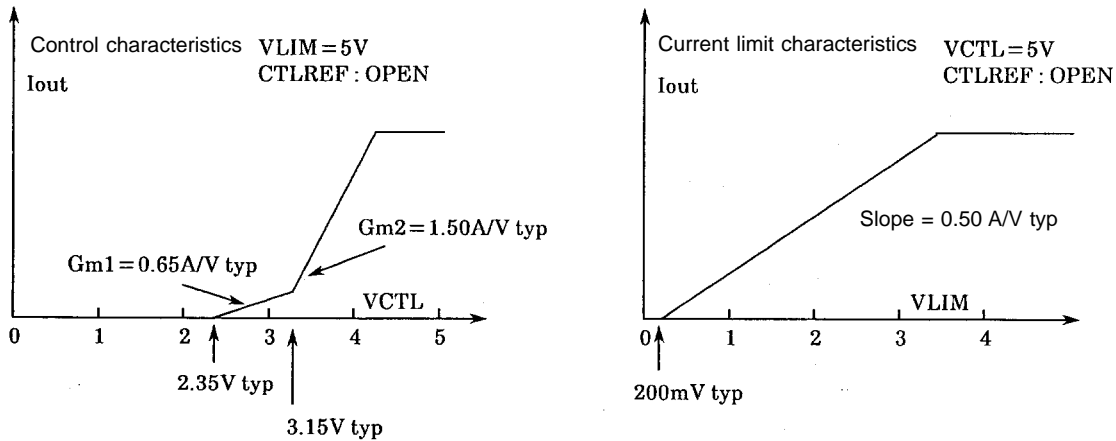
| | Source \rightarrow Sink | Hall input | | | FR |
|---|---------------------------|------------|---|---|----|
| | | U | V | W | |
| 1 | V \rightarrow W | H | H | L | H |
| | W \rightarrow V | | | | L |
| 2 | U \rightarrow W | H | L | L | H |
| | W \rightarrow U | | | | L |
| 3 | U \rightarrow V | H | L | H | H |
| | V \rightarrow U | | | | L |
| 4 | W \rightarrow V | L | L | H | H |
| | V \rightarrow W | | | | L |
| 5 | W \rightarrow U | L | H | H | H |
| | U \rightarrow W | | | | L |
| 6 | V \rightarrow U | L | H | L | H |
| | U \rightarrow V | | | | L |

Note: "H" in the FR column represents a voltage of 2.75 V or more; "L" represents a voltage of 2.25 V or less. (At $V_{CC} = 5$ V)

Note: "H" in the Hall input columns represents a state in which "+" has a potential which is higher by 0.01 V or more than that of the "-" phase inputs. Conversely, "L" represents a state in which "+" has a potential which is lower by 0.01 V or more than that of the "-" phase input.

Note: Since 180 $^{\circ}$ energized system is used as the drive system, other phases than the sink and source phases are turned off.

Control Function & Current Limit Function

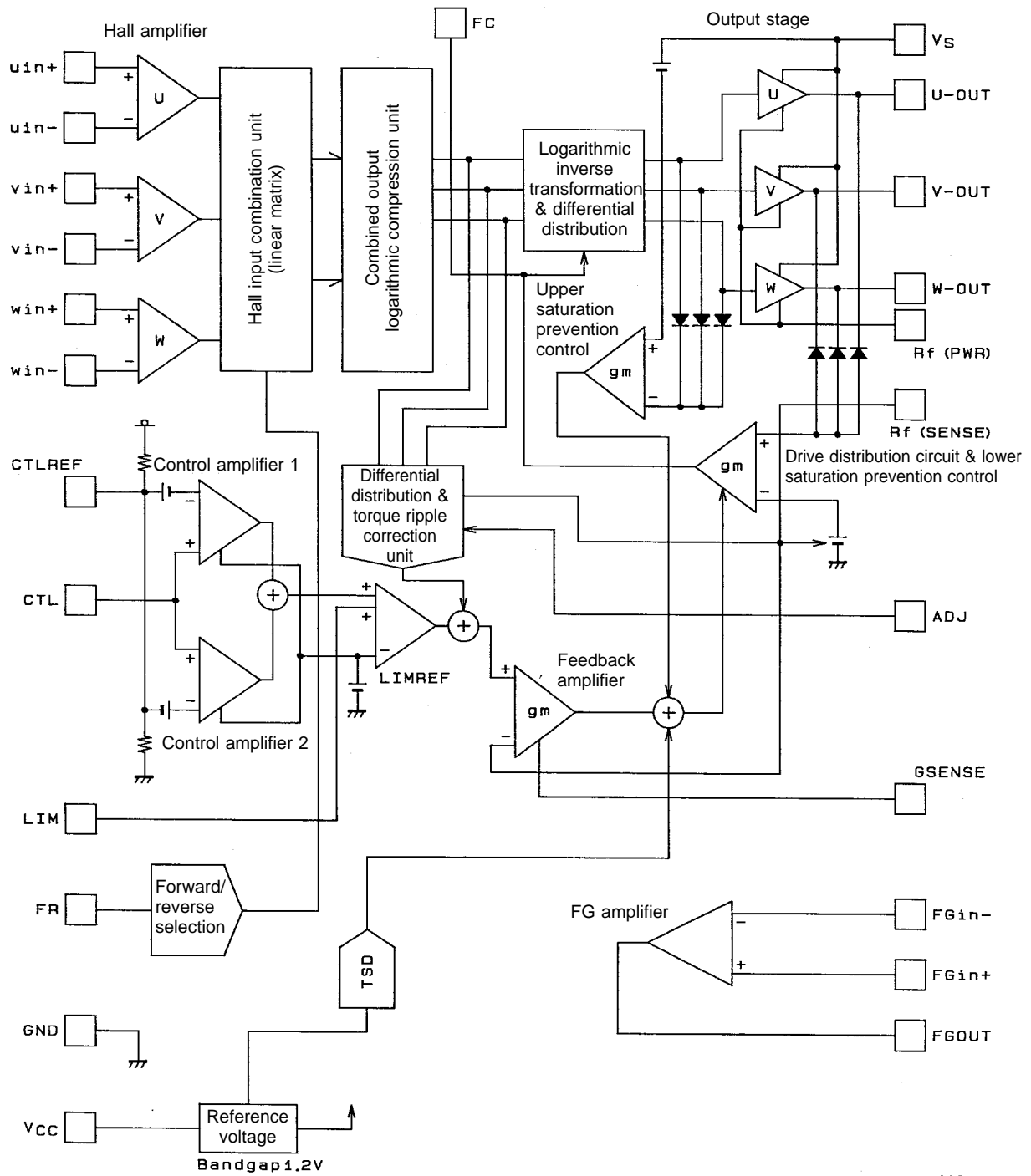


Pin Functions

The pin number in () is for MFP, that in < > is for DIP, and other than these is for QFP.

| Pin name | Pin No. | Function |
|----------------------------------------|--------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| FR | 1 (33) <26> | Forward/reverse select pin. The pin voltage selects forward/reverse. ($V_{th} = 2.5 \text{ V typ}$ at $V_{CC} = 5 \text{ V}$) |
| GND | 2 (34) <27> | GND for other than output transistor. Minimum potential of output transistor is at Rf pin. |
| FGin (-) | 5 (3) <28> | Input pin when FG amplifier is used with inverted input. Feedback resistor is connected between this pin and FG-OUT. |
| FGin (+) | 6 (4) <1> | Noninverting input pin when FG amplifier is used with differential input. Internal bias is not applied. |
| FG-OUT | 8 (5) <3> | FG amplifier output pin. Resistive load provided internally. |
| CTL | 9 (6) <4> | Speed control pin. Control is exercised by constant-current drive with current feedback applied from Rf. $G_m = 0.65 \text{ A/V}$ & 1.50 A/V typ at $R_f = 0.5 \Omega$ |
| CTLREF | 10 (7) <5> | Control reference voltage pin. The voltage is set internally to approx. $V_{CC}/2$ but this can be varied by applying voltage through a low impedance (input impedance = approx. $2.5 \text{ k}\Omega$). |
| LIM | 11 (8) <6> | Current limiting function control pin. The output current is varied linearly by this pin voltage; slope = 0.5 A/V typ at $R_f = 0.5 \Omega$. |
| FC | 12 (9) <7> | Speed control loop frequency characteristic correction pin |
| Uin+, Uin- Vin+, Vin- Win+, Win- | 13, 14 (10, 11) <8, 9> 15, 16 (12, 13) <10, 11> 17, 18 (14, 15) <12, 13> | U-phase Hall device input pin; logic "H" represents $IN+ > IN-$. V-phase Hall device input pin; logic "H" represents $IN+ > IN-$. W-phase Hall device input pin; logic "H" represents $IN+ > IN-$. |
| VCC | 19 (16) <14> | Power supply pin for supplying power to all circuits except output section in IC; this voltage must be stabilized so as to eliminate ripple and noise. |
| Vs | 22 (21) <15> | Output selection power supply pin |
| ADJ | 23 (22) <16> | Pin for external adjustment of torque ripple correction factor. When this factor is to be adjusted, a voltage is externally applied to the ADJ pin through a low impedance. If the voltage applied is increased, the factor drops; conversely, if it is reduced, the factor rises. The factor varies between 0 and 2 times that of the open state. (The voltage is set inside to approx. $V_{CC}/2$ internally, and the input impedance is approx. $5 \text{ k}\Omega$.) |
| Rf (PWR) Rf (SNS) | 24 (23) <17> 33 (31) <24> | Output current detection pin. Current feedback is applied to the control section by connecting Rf between this pin and GND. The lower oversaturation prevention circuit and torque ripple correction circuit are activated in accordance with this pin voltage. Since the oversaturation prevention level is set with this voltage, the lower oversaturation prevention effect may deteriorate in the high current range if the Rf value is reduced to an extremely low level. The PWR and SENSE pins must always be connected. |
| Uout Vout Wout | 27 (26) <21> 29 (27) <22> 31 (28) <23> | U-phase output pin V-phase output pin W-phase output pin (Built-in spark killer diode) |
| GSENSE | 34 (32) <25> | GND sensing pin. By connecting this pin to the neighboring GND on the Rf resistor side of the motor GND wire which contains Rf, the effect that GND common impedance exerts on Rf can be eliminated. (This pin must not be left open.) |

Block Diagram

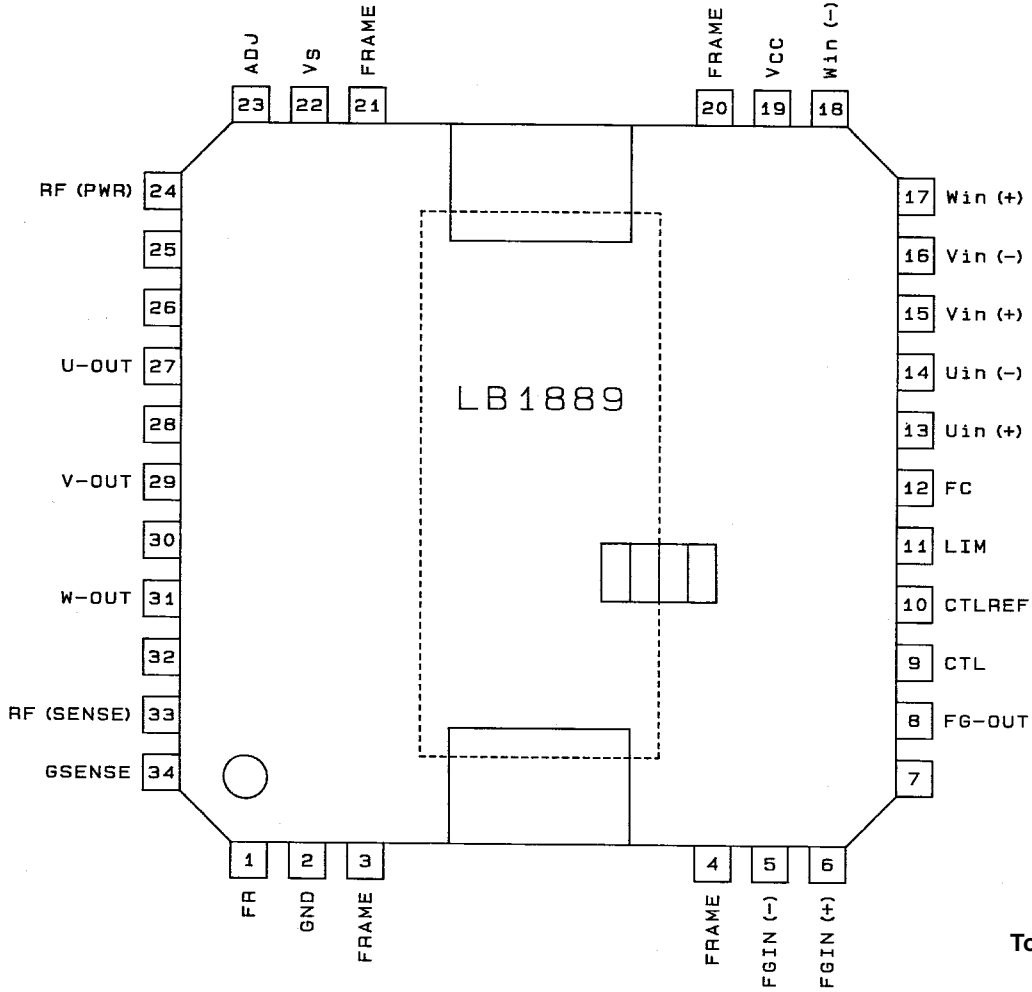


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Pin Assignment [LB1889]

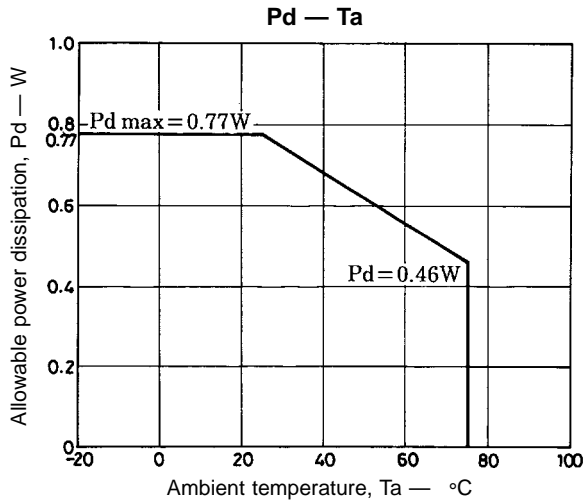
(PACKAGE : QFP-34H-A)



Top view

Note: FRAME must be connected to GND for GND potential stabilization.

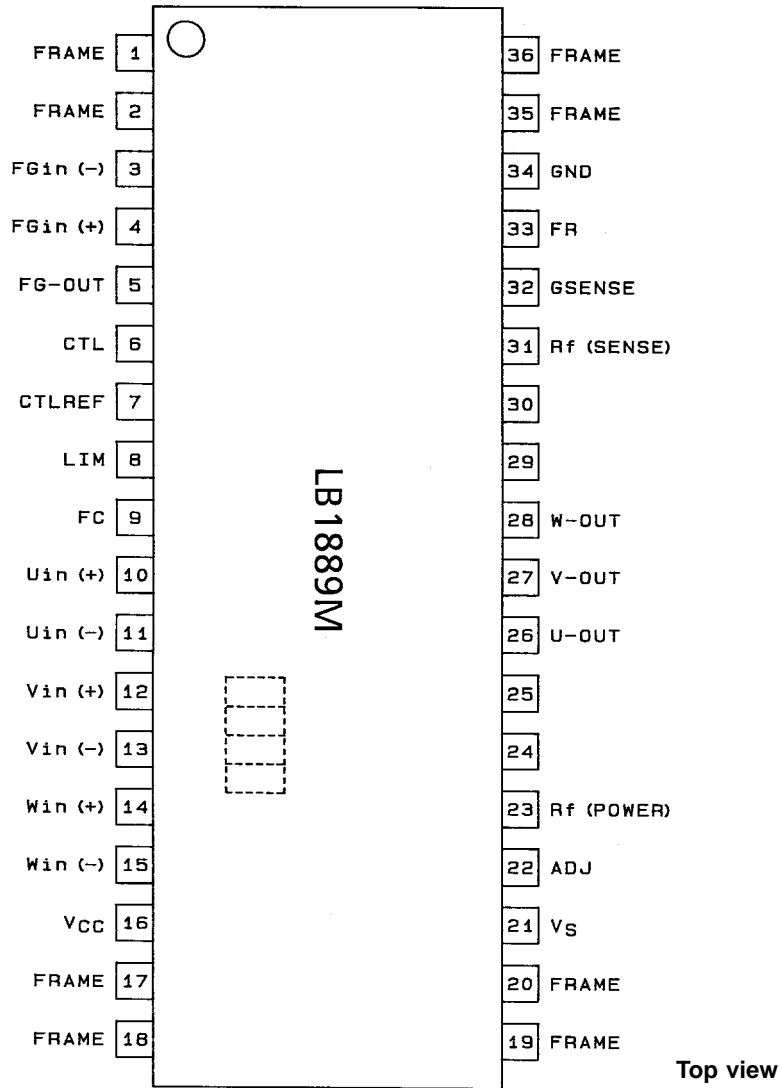
A03960



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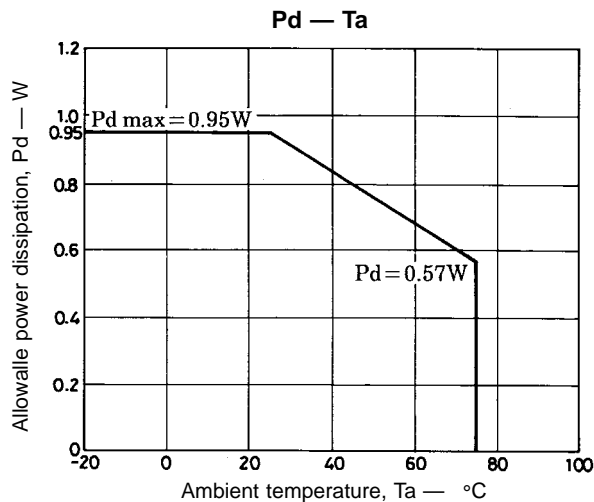
Pin Assignment [LB1889M]

(PACKAGE : MFP-36S-LF)



A03961

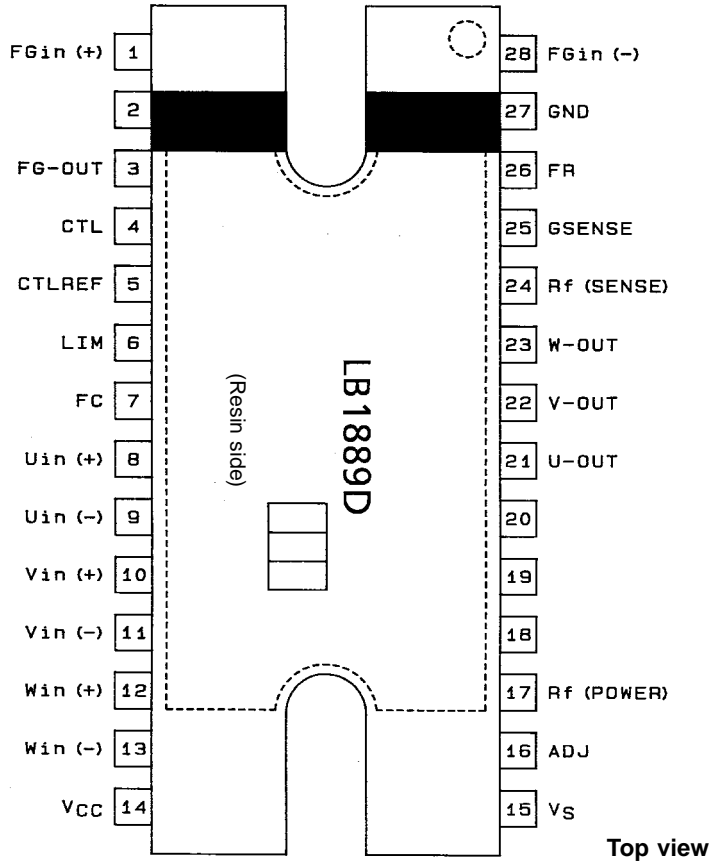
Note: Although there is no internal connection between the FRAME pin and GND, FRAME must be connected to GND externally for GND potential stabilization.



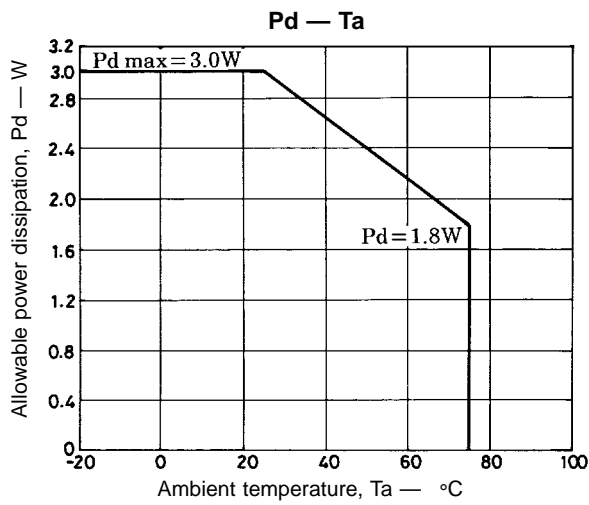
LB1889, 1889M, 1889D

Pin Assignment [LB1889D]

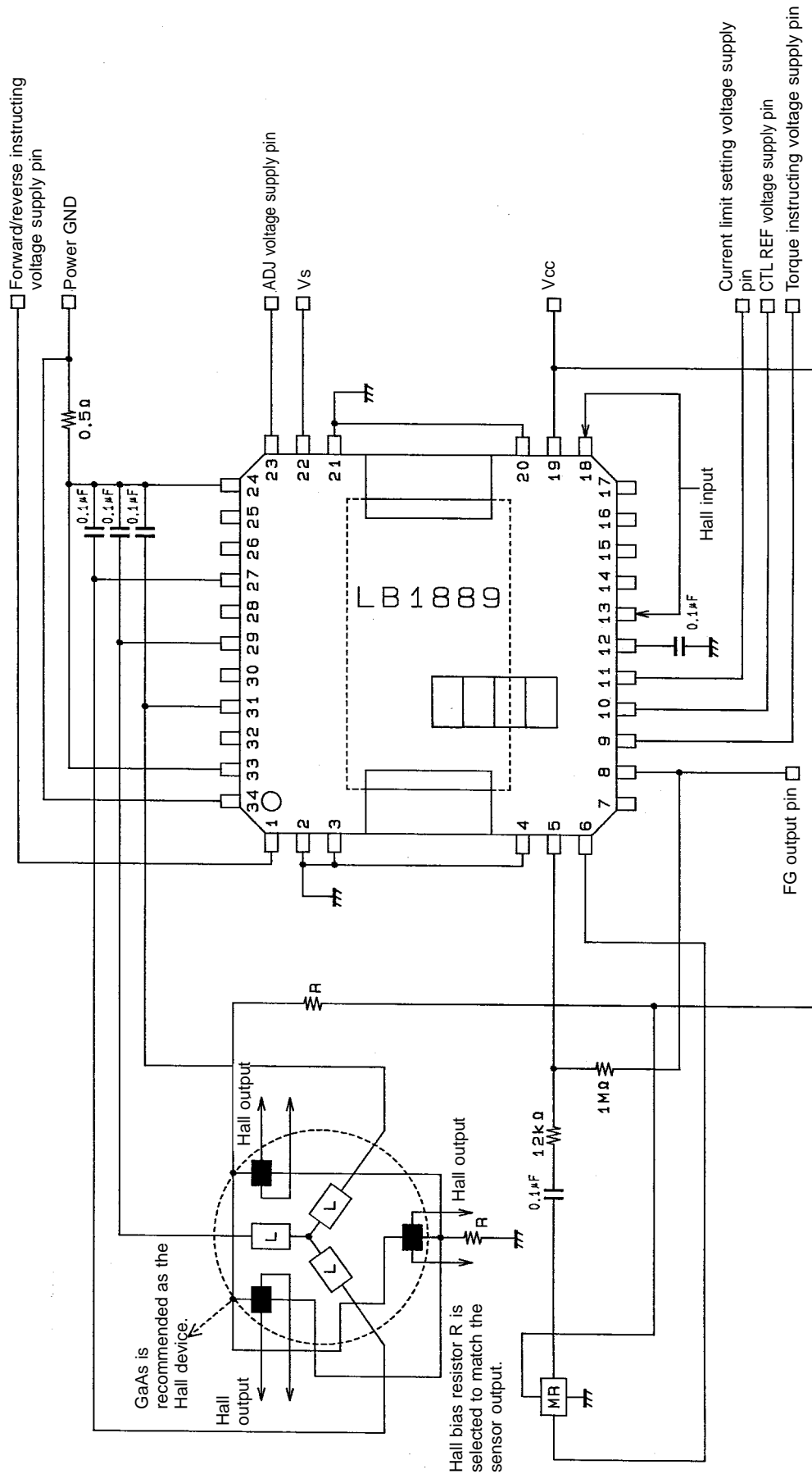
DIP-28HS bent opposite



A03962



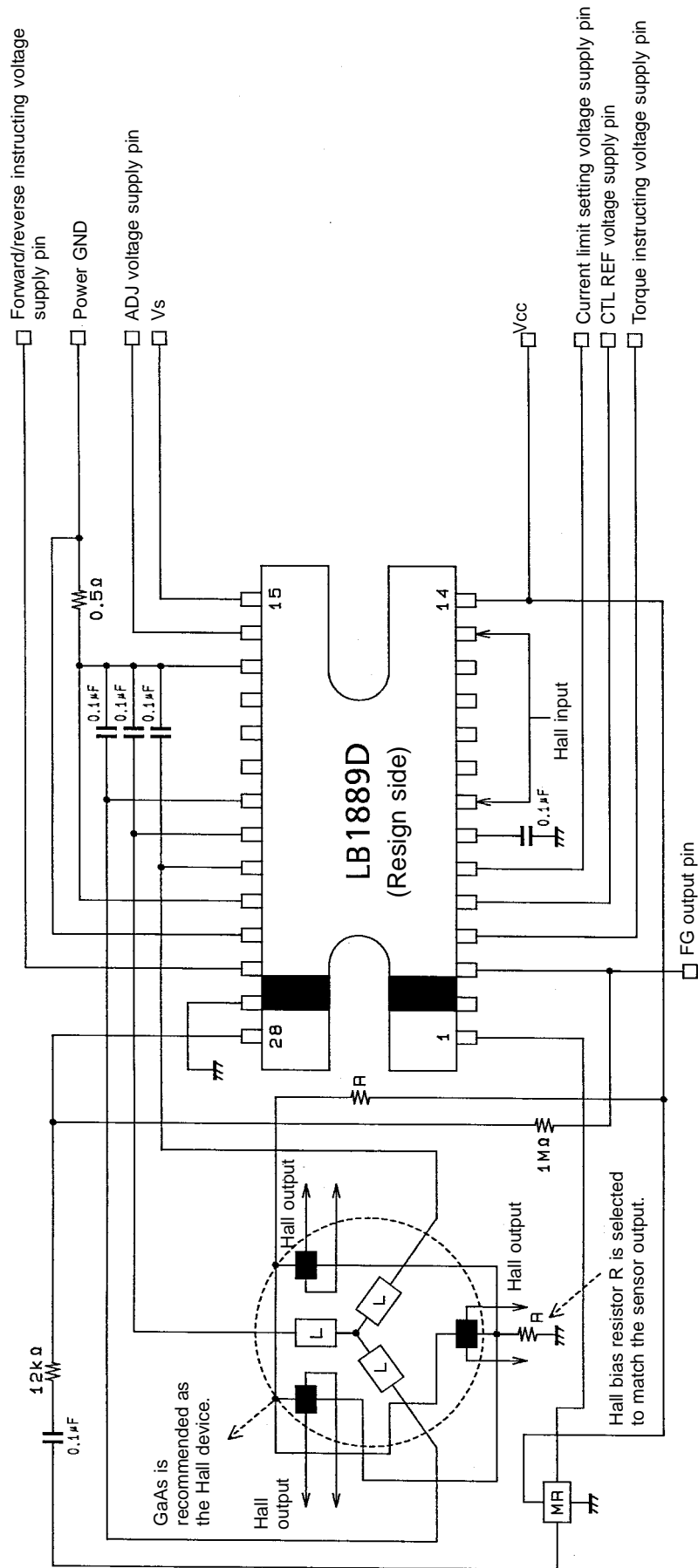
Sample Application Circuit [LB1889]



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Note: The constants provided in this sample application circuit are provided by way of example and are not intended to guarantee the characteristics.

Sample Application Circuit [LB1889D]



A03965

Note: The constants provided in this sample application circuit are provided by way of example and are not intended to guarantee the characteristics.

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Pin Input/Output Equivalent Circuit

| Pin name | Input/Output Equivalent Circuit |
|----------------------------------------------------------------|-------------------------------------------|
| Uin (+) Uin (-) Vin (+) Vin (-) Win (+) Win (-) | <p style="text-align: center;">A03966</p> |
| U-OUT V-OUT W-OUT Vs Rf (POWER) Rf (SENSE) | <p style="text-align: center;">A03967</p> |
| CTL LIM CTLREF | <p style="text-align: center;">A03968</p> |
| FR ADJ | <p style="text-align: center;">A03969</p> |

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| Pin name | Input/Output Equivalent Circuit |
|----------------------|------------------------------------------|
| FGin (-) FGin (+) | <p style="text-align: right;">A03970</p> |
| FGOUT FC | <p style="text-align: right;">A03971</p> |

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