



LC321667BJ, BM, BT-70/80

1 MEG (65536 Words × 16 Bits) DRAM EDO Page Mode Byte Write

Preliminary

Overview

The LC321667BJ series is a CMOS dynamic RAM operating on a single 5 V power source and having a 65536 words × 16 bits configuration. Equipped with large capacity capabilities, high speed transfer rates and low power dissipation, this series is suited for a wide variety of applications ranging from computer main memory and expansion memory to commercial equipment.

Address input utilizes a multiplexed address bus which permits it to be enclosed in a compact plastic package of 40-pin SOJ. Refresh rates are within 4 ms with 256 row address (A0 to A7) selection and support Row Address Strobe ($\overline{\text{RAS}}$)-only refresh, Column Address Strobe ($\overline{\text{CAS}}$)-before- $\overline{\text{RAS}}$ refresh and hidden refresh settings. There are functions such as Extended Data Out (EDO) page mode, read-modify-write and byte write.

Features

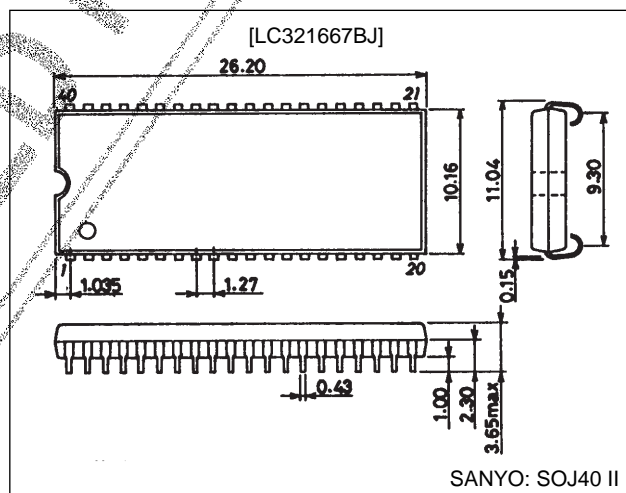
- 65536 words × 16 bits configuration.
- Single 5 V ± 10% power supply.
- All input and output (I/O) TTL compatible.
- Supports EDO page mode, read-modify-write and byte write.
- Supports output buffer control using early write and Output Enable ($\overline{\text{OE}}$) control.

- 4 ms refresh using 256 refresh cycles.
- Supports $\overline{\text{RAS}}$ -only refresh, $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh and hidden refresh.
- Packages
SOJ 40-pin plastic package (400 mil): LC321667BJ
SOP 40-pin plastic package (525 mil): LC321667BM
TSOP 44-pin plastic package (400 mil): LC321667BT
- $\overline{\text{RAS}}$ access time/column address access time/ $\overline{\text{CAS}}$ access time/cycle time/power dissipation.

Package Dimensions

unit: mm.

3200-SOJ40 II



| Parameter | | LC321667BJ, BM, BT-70 | LC321667BJ, BM, BT-80 |
|-------------------------------------|------------------|---------------------------------------|-----------------------|
| $\overline{\text{RAS}}$ access time | | 70 ns | 80 ns |
| Column address access time | | 40 ns | 45 ns |
| $\overline{\text{CAS}}$ access time | | 25 ns | 25 ns |
| Cycle time | | 125 ns | 135 ns |
| Power consumption (max) | During operation | 688 mW | 633 mW |
| | During standby | 5.5 mW (CMOS level)/11 mW (TTL level) | |

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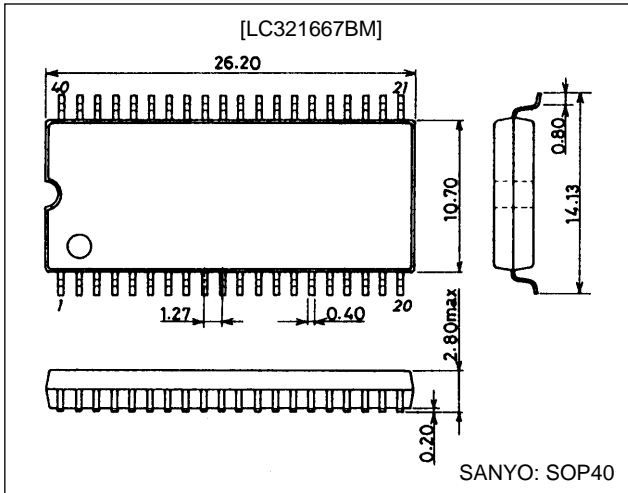
SANYO Electric Co., Ltd. Semiconductor Business Headquarters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Package Dimensions

unit: mm

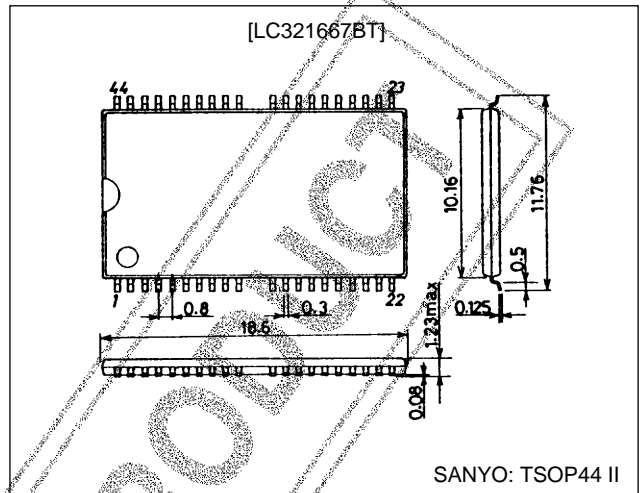
3195-SOP40



Package Dimensions

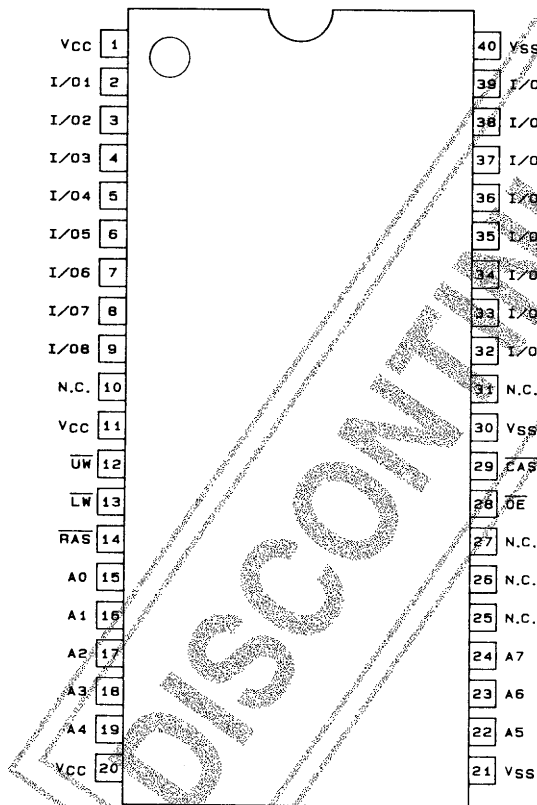
unit: mm

3207-TSOP44 II



Pin AssignmentS

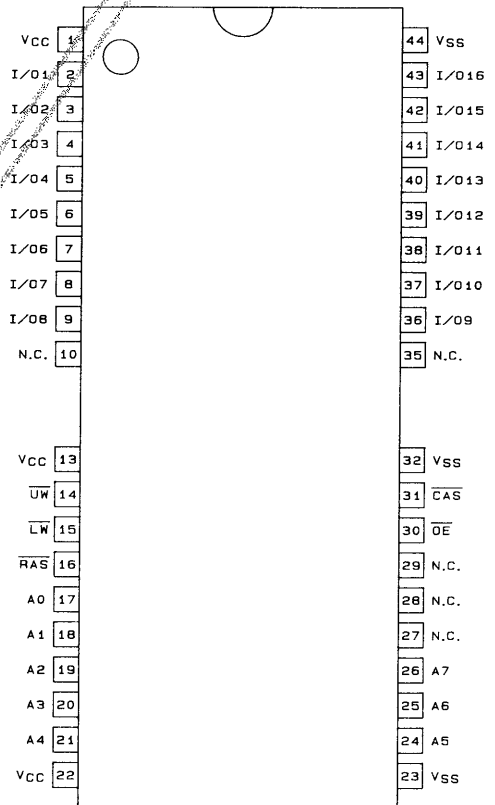
SOJ40, SOP40



Top view

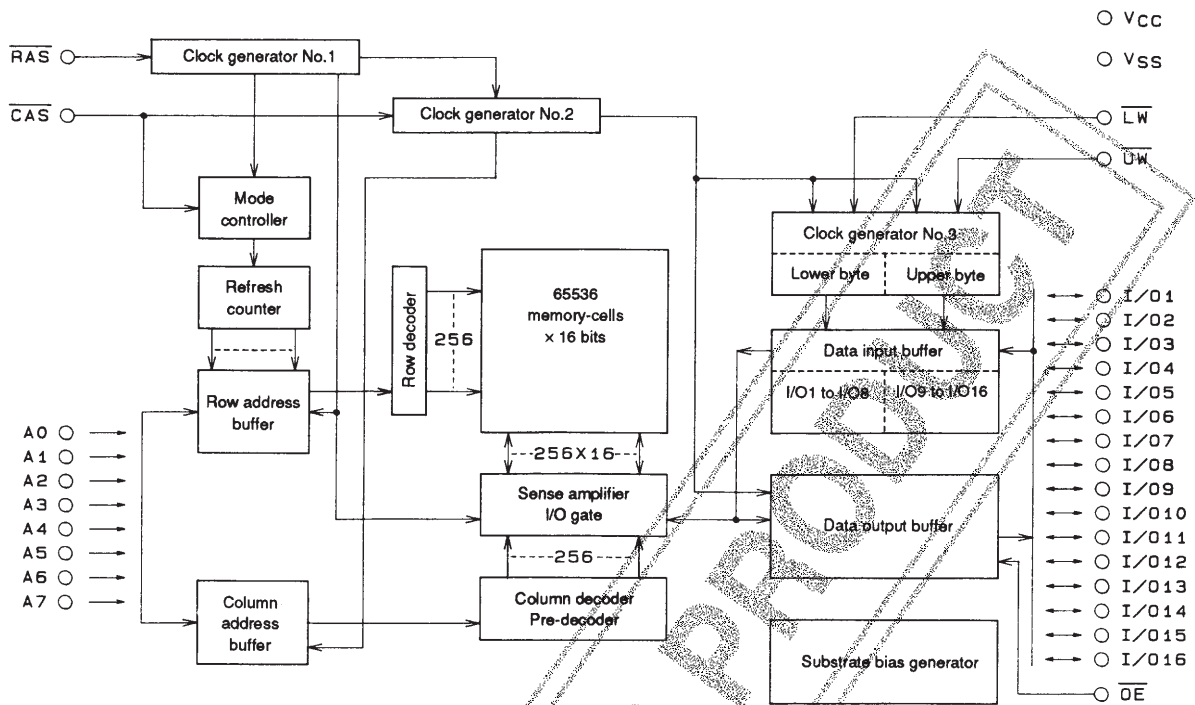
A02123

TSOP44



A02943

Block Diagram



A02125

Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Unit | Note | |
|------------------------------|---------------|----------------------|------|------|---|
| Maximum supply voltage | $V_{CC\ max}$ | -1.0 to +7.0 | V | 1 | |
| Input voltage | V_{IN} | -1.0 to +7.0 | V | 1 | |
| Output voltage | V_{OUT} | -1.0 to +7.0 | V | 1 | |
| Operating temperature range | T_{opr} | 0 to +70 | °C | 1 | |
| Storage temperature range | T_{stg} | -55 to +150 | °C | 1 | |
| Allowable power dissipation | $P_d\ max$ | LC321667BJ, BM-70/80 | 800 | mW | 1 |
| | | LC321667BT-70/80 | 700 | | |
| Output short-circuit current | I_{OUT} | 50 | mA | 1 | |

Note: 1. Stresses greater than the above listed maximum values may result in damage to the device.

DC Recommended Operating Ranges at $T_a = 0$ to $+70^\circ C$

| Parameter | Symbol | min | typ | max | Unit | Note |
|---|----------|--------|-----|------|------|------|
| Power supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V | 2 |
| Input high level voltage | V_{IH} | 2.4 | | 6.5 | V | 2 |
| Input low level voltage (A0 to A7, RAS, CAS, UW, LW, OE) | V_{IL} | -1.0*1 | | +0.8 | V | 2 |
| Input low level voltage (I/O1 to I/O16) | V_{IL} | -0.5*1 | | +0.8 | V | 2 |

Note: 2. All voltages are referenced to V_{SS} .

A bypass capacitor of about 0.1 μF should be connected between V_{CC} and V_{SS} of the device.

*1: -2.0 V when pulse width is less than 20 ns.

LC321667BJ, BM, BT-70/80

DC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10%

| Parameter | Symbol | Conditions | LC321667 BJ, BM, BT-70 | | LC321667 BJ, BM, BT-80 | | Unit | Note |
|--|------------------|---|---------------------------|-----|---------------------------|-----|------|---------|
| | | | min | max | min | max | | |
| Operating current (Average current during operation) | I _{CC1} | $\overline{RAS}, \overline{CAS}$, address cycling: t _{RC} = t _{RC} min | | 125 | | 115 | mA | 3, 4, 5 |
| Standby current | I _{CC2} | $\overline{RAS} = \overline{CAS} = V_{IH}$ | | 2 | | 2 | mA | |
| \overline{RAS} -only refresh current | I _{CC3} | \overline{RAS} cycling, $\overline{CAS} = V_{IH}$: t _{RC} = t _{RC} min | | 125 | | 115 | mA | 3, 5 |
| EDO page mode current | I _{CC4} | $\overline{RAS} = V_{IL}$, \overline{CAS} , address cycling: t _{PC} = t _{PC} min | | 110 | | 100 | mA | 3, 4, 5 |
| Standby current | I _{CC5} | $\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 V$ | | 1 | | 1 | mA | |
| \overline{CAS} -before- \overline{RAS} refresh current | I _{CC6} | $\overline{RAS}, \overline{CAS}$ cycling: t _{RC} = t _{RC} min | | 125 | | 115 | mA | 3 |
| Input leakage current | I _{IL} | 0 V ≤ V _{IN} ≤ 6.5 V, pins other than test pin = 0 V | -10 | +10 | -10 | +10 | μA | |
| Output leakage current | I _{OL} | D _{OUT} disable, 0 V ≤ V _{OUT} ≤ 5.5 V | -10 | +10 | -10 | +10 | μA | |
| Output high level voltage | V _{OH} | I _{OUT} = -2.5 mA | 2.4 | | 2.4 | | V | |
| Output low level voltage | V _{OL} | I _{OUT} = 2.1 mA | | 0.4 | | 0.4 | V | |

Note: 3. All current values are measured at minimum cycle rate. Since current flows immoderately, if cycle time is longer than shown here, current value becomes smaller.

4. I_{CC1} and I_{CC4} are dependent on output loads. Maximum values for I_{CC1} and I_{CC4} represent values with output open.

5. Address change is less than or equal to one time during $\overline{RAS} = V_{IL}$. Concerning I_{CC4}, it is less than or equal to one time during 1 cycle (t_{PC}).

AC Electrical Characteristics at Ta = 0 to +70°C, V_{CC} = 5 V ± 10% (note 6, 7 and 8)

| Parameter | Symbol | LC321667BJ, BM, BT-70 | | LC321667BJ, BM, BT-80 | | Unit | Note |
|---|-------------------|-----------------------|--------|-----------------------|--------|------|-----------|
| | | min | max | min | max | | |
| Random read or write cycle time | t _{RC} | 125 | | 135 | | ns | |
| Read-write/read-modify-write cycle time | t _{RWC} | 170 | | 180 | | ns | |
| EDO page mode cycle time | t _{PC} | 35 | | 40 | | ns | |
| EDO page mode read-write/read-modify-write cycle time | t _{PRWC} | 85 | | 90 | | ns | |
| \overline{RAS} access time | t _{RAC} | | 70 | | 80 | ns | 9, 14, 15 |
| \overline{CAS} access time | t _{CAC} | | 25 | | 25 | ns | 9, 14 |
| Column address access time | t _{AA} | | 40 | | 45 | ns | 9, 15 |
| \overline{CAS} precharge access time | t _{CPA} | | 45 | | 50 | ns | 9 |
| Output low-impedance time from \overline{CAS} low | t _{CLZ} | 0 | | 0 | | ns | 9 |
| Output buffer turn-off delay time from \overline{RAS} or \overline{CAS} | t _{OFF} | 0 | 20 | 0 | 20 | ns | 10, 17 |
| Rise and fall time | t _T | 2.5 | 50 | 2.5 | 50 | ns | |
| \overline{RAS} precharge time | t _{RP} | 45 | | 45 | | ns | |
| \overline{RAS} pulse width | t _{RAS} | 70 | 10000 | 80 | 10000 | ns | |
| \overline{RAS} pulse width for EDO page mode cycle only | t _{RASP} | 70 | 100000 | 80 | 100000 | ns | |
| \overline{RAS} hold time | t _{RSH} | 20 | | 25 | | ns | |
| \overline{CAS} hold time | t _{CSH} | 60 | | 70 | | ns | |
| \overline{CAS} pulse width | t _{CAS} | 20 | 10000 | 25 | 10000 | ns | |
| \overline{RAS} to \overline{CAS} delay time | t _{RCD} | 20 | 45 | 20 | 55 | ns | 14 |
| \overline{RAS} to column address delay time | t _{RAD} | 15 | 30 | 15 | 35 | ns | 15 |
| \overline{CAS} to \overline{RAS} precharge time | t _{CRP} | 10 | | 10 | | ns | |
| \overline{CAS} precharge time | t _{CP} | 10 | | 10 | | ns | |
| Row address setup time | t _{ASR} | 0 | | 0 | | ns | |
| Row address hold time | t _{RAH} | 10 | | 10 | | ns | |
| Column address setup time | t _{ASC} | 0 | | 0 | | ns | |
| Column address hold time | t _{CAH} | 15 | | 15 | | ns | |
| Column address hold time referenced to \overline{RAS} | t _{AR} | 50 | | 55 | | ns | |
| Column address to \overline{RAS} lead time | t _{RAL} | 25 | | 30 | | ns | |
| Read command setup time | t _{RCS} | 0 | | 0 | | ns | |
| Read command hold time referenced to \overline{CAS} | t _{RCH} | 0 | | 0 | | ns | 11 |
| Read command hold time referenced to \overline{RAS} | t _{RRH} | 0 | | 0 | | ns | 11 |
| Write command hold time | t _{WCH} | 15 | | 15 | | ns | |
| Write command hold time referenced to \overline{RAS} | t _{WCR} | 50 | | 55 | | ns | |
| Write command pulse width | t _{WP} | 15 | | 15 | | ns | |

Continued on next page.

LC321667BJ, BM, BT-70/80

Continued from preceding page.

| Parameter | Symbol | LC321667BJ, BM, BT-70 | | LC321667BJ, BM, BT-80 | | Unit | Note |
|---|-------------------|-----------------------|-----|-----------------------|-----|------|------|
| | | min | max | min | max | | |
| Write command to $\overline{\text{RAS}}$ lead time | t_{RWL} | 20 | | 20 | | ns | |
| Write command to $\overline{\text{CAS}}$ lead time | t_{CWL} | 20 | | 20 | | ns | |
| Data input setup time | t_{DS} | 0 | | 0 | | ns | 12 |
| Data input hold time | t_{DH} | 15 | | 15 | | ns | 12 |
| Data input hold time referenced to $\overline{\text{RAS}}$ | t_{DHR} | 50 | | 55 | | ns | |
| Refresh time | t_{REF} | | 4 | | 4 | ms | |
| Write command setup time | t_{WCS} | 0 | | 0 | | ns | 13 |
| $\overline{\text{CAS}}$ to $\overline{\text{UW}}$ or $\overline{\text{LW}}$ delay time | t_{CWD} | 45 | | 45 | | ns | 13 |
| $\overline{\text{RAS}}$ to $\overline{\text{UW}}$ or $\overline{\text{LW}}$ delay time | t_{RWD} | 90 | | 100 | | ns | 13 |
| Column address to $\overline{\text{UW}}$ or $\overline{\text{LW}}$ delay time | t_{AWD} | 60 | | 65 | | ns | 13 |
| CAS precharge $\overline{\text{UW}}$ or $\overline{\text{LW}}$ delay time for 70 EDO page mode cycle only | t_{CPWD} | 65 | | 70 | | ns | 13 |
| CAS setup time for CAS-before-RAS | t_{CSR} | 10 | | 10 | | ns | |
| CAS hold time for CAS-before-RAS | t_{CHR} | 10 | | 10 | | ns | |
| $\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ active time | t_{RPC} | 10 | | 10 | | ns | |
| CAS precharge time for $\overline{\text{CAS}}$ -before-RAS counter test | t_{CPT} | 40 | | 40 | | ns | |
| RAS hold time referenced to $\overline{\text{OE}}$ | t_{ROH} | 15 | | 15 | | ns | |
| $\overline{\text{OE}}$ access time | t_{OEA} | | 25 | | 25 | ns | 9 |
| $\overline{\text{OE}}$ delay time | t_{OED} | 15 | | 15 | | ns | |
| $\overline{\text{OE}}$ output buffer turn-off delay time | t_{OEZ} | 0 | 15 | 0 | 15 | ns | 10 |
| $\overline{\text{OE}}$ command hold time | t_{OEH} | 20 | | 20 | | ns | |
| $\overline{\text{OE}}$ setup time to $\overline{\text{CAS}}$ high | t_{OCH} | 5 | | 5 | | ns | 16 |
| $\overline{\text{OE}}$ hold time from $\overline{\text{CAS}}$ high | t_{CHO} | 10 | | 10 | | ns | 16 |
| $\overline{\text{OE}}$ command pulse width | t_{OEP} | 10 | | 10 | | ns | |
| Data output hold time | t_{DOH} | 5 | | 5 | | ns | |
| $\overline{\text{WE}}$ output buffer turn-off delay time | t_{WEZ} | 0 | 15 | 0 | 15 | ns | |
| Data input to $\overline{\text{CAS}}$ delay time | t_{DZC} | 0 | | 0 | | ns | 16 |
| Data input to $\overline{\text{OE}}$ delay time | t_{DZO} | 0 | | 0 | | ns | 16 |
| Masked write setup time | t_{MCS} | 0 | | 0 | | ns | |
| Masked write hold time referenced to $\overline{\text{RAS}}$ | t_{MRH} | 0 | | 0 | | ns | |
| Masked write hold time referenced to $\overline{\text{CAS}}$ | t_{MCH} | 0 | | 0 | | ns | |

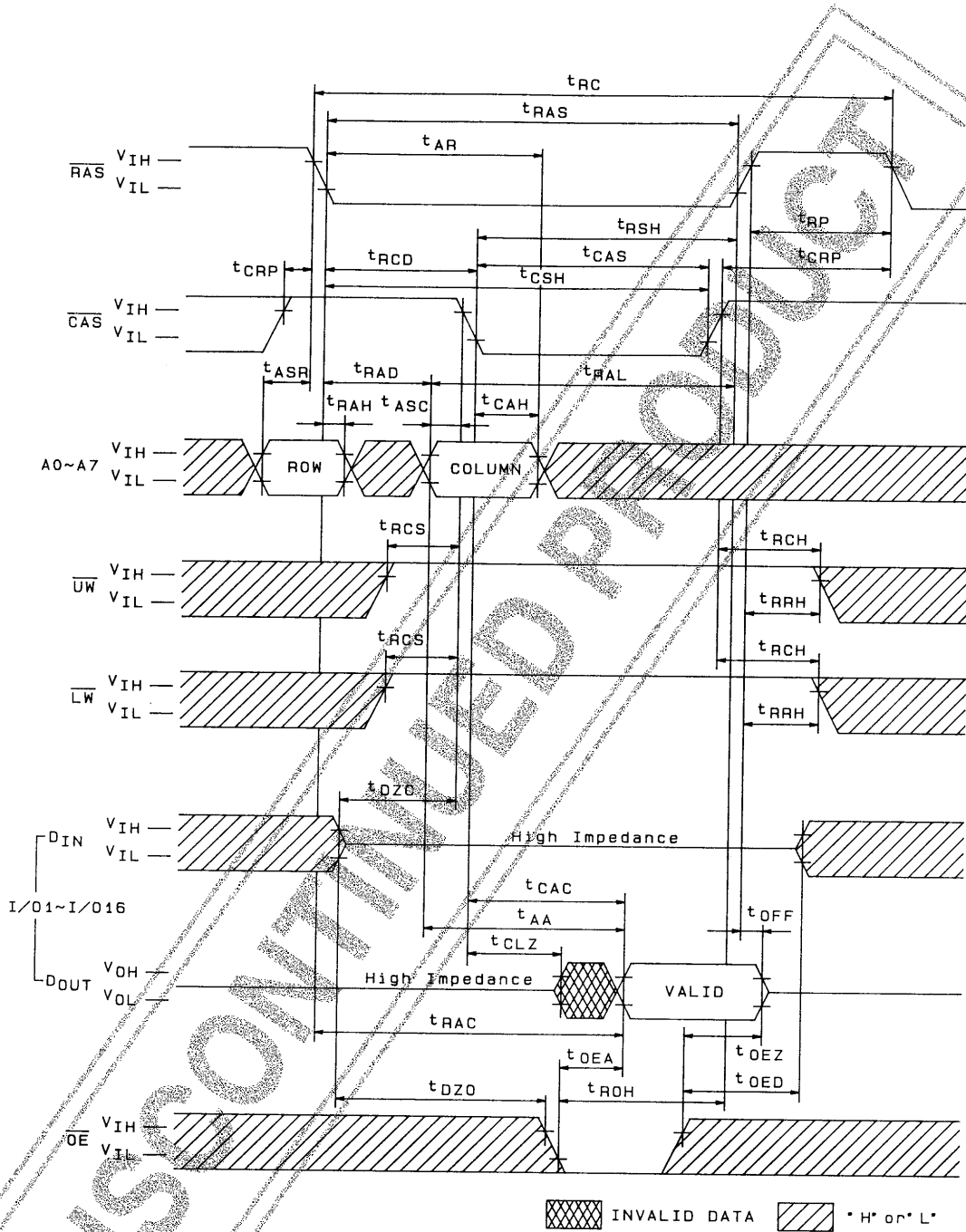
Input/Output Capacitance at $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{\text{CC}} = 5\text{ V} \pm 10\%$

| Parameter | Symbol | min | max | Unit | Note |
|---|-----------------|-----|-----|------|------|
| Input capacitance (A0 to A7, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{UW}}$, $\overline{\text{LW}}$, $\overline{\text{OE}}$) | C_{IN} | | 7 | pF | |
| Input/Output capacitance (I/O1 to I/O16) | C_{IO} | | 7 | pF | |

- Note: 6. An initial pause of 200 μs is required after power-up followed by eight $\overline{\text{RAS}}$ -only refresh cycles before proper device operation is achieved. In case of using refresh counter, a minimum of eight $\overline{\text{CAS}}$ -before-RAS refresh cycles instead of eight $\overline{\text{RAS}}$ -only refresh cycles are required.
7. Measured at $t_T = 2.5\text{ ns}$.
8. When measuring input signal timing, V_{IH} (min) and V_{IL} (max) are used for reference points. In addition, rise and fall time are defined between V_{IH} and V_{IL} .
9. Measured using an equivalent of 50 pF and one standard TTL loads.
10. t_{OFF} (max) and t_{OZ} (max) are defined as the time until output voltage can no longer be measured when output switches to a high impedance condition.
11. Operation is guaranteed if either t_{RRH} or t_{RCH} is satisfied.
12. These parameters are measured from the falling edge of $\overline{\text{CAS}}$ for an early-write cycle, and from the falling edge of $\overline{\text{UW}}$ and $\overline{\text{LW}}$ for a read-write/read-modify-write cycle.
13. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters for memory in that they specify the operating mode. If $t_{\text{WCS}} \geq t_{\text{WCS}}$ (min), the cycle switches to an early-write cycle and output pins switch to high impedance throughout the cycle. If $t_{\text{CWD}} \geq t_{\text{CWD}}$ (min), $t_{\text{RWD}} \geq t_{\text{RWD}}$ (min), $t_{\text{AWD}} \geq t_{\text{AWD}}$ (min) and $t_{\text{CPWD}} \geq t_{\text{CPWD}}$ (min) for fast page mode cycle only, the cycle switches to a read-write/read-modify-write cycle and data output equal information in the selected cells. If neither of the above timings are satisfied, output pins are in an undefined state.
14. t_{RCD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{RCD}} \geq t_{\text{RCD}}$ (max), access time is determined according to t_{CAC} .
15. t_{RAD} (max) is not a restrictive operating parameter but instead represents the point at which the access time t_{RAC} (max) is guaranteed. If $t_{\text{RAD}} \geq t_{\text{RAD}}$ (max), access time is determined according to t_{AA} .
16. Operation is guaranteed if either t_{DZC} or t_{DZO} is satisfied.
17. t_{OFF} is referenced from the rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

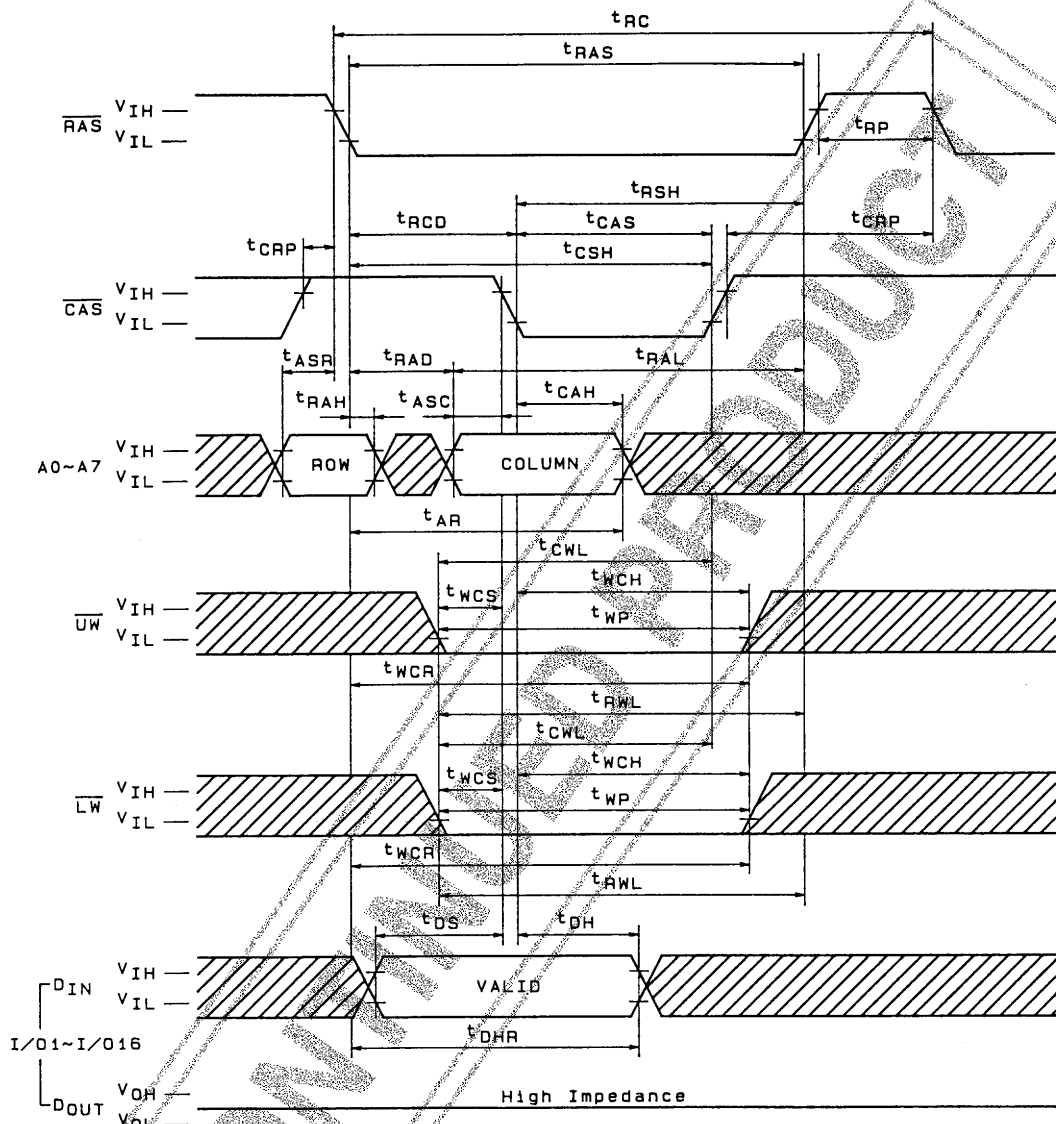
Timing Chart


Read Cycle



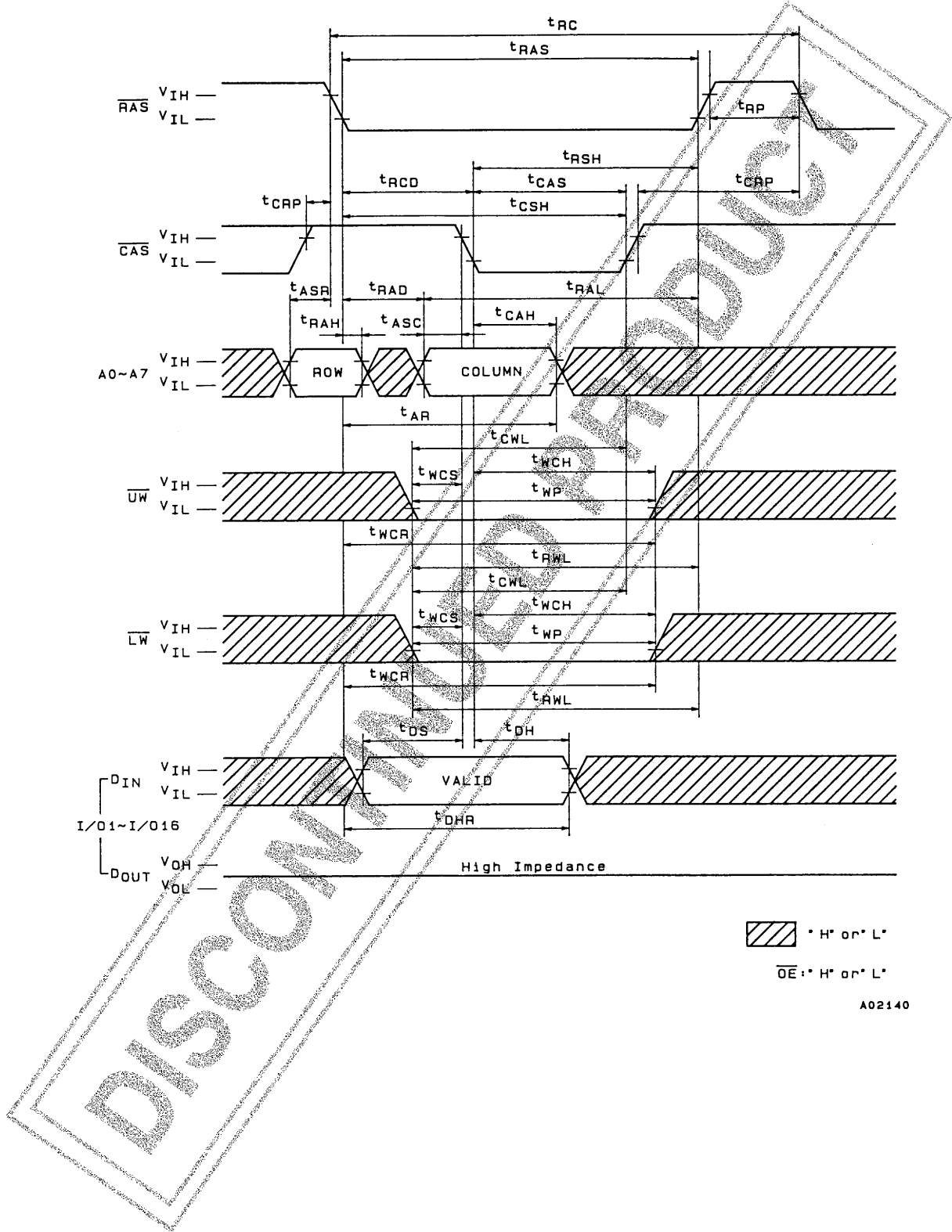
A03721

Early Write Cycle

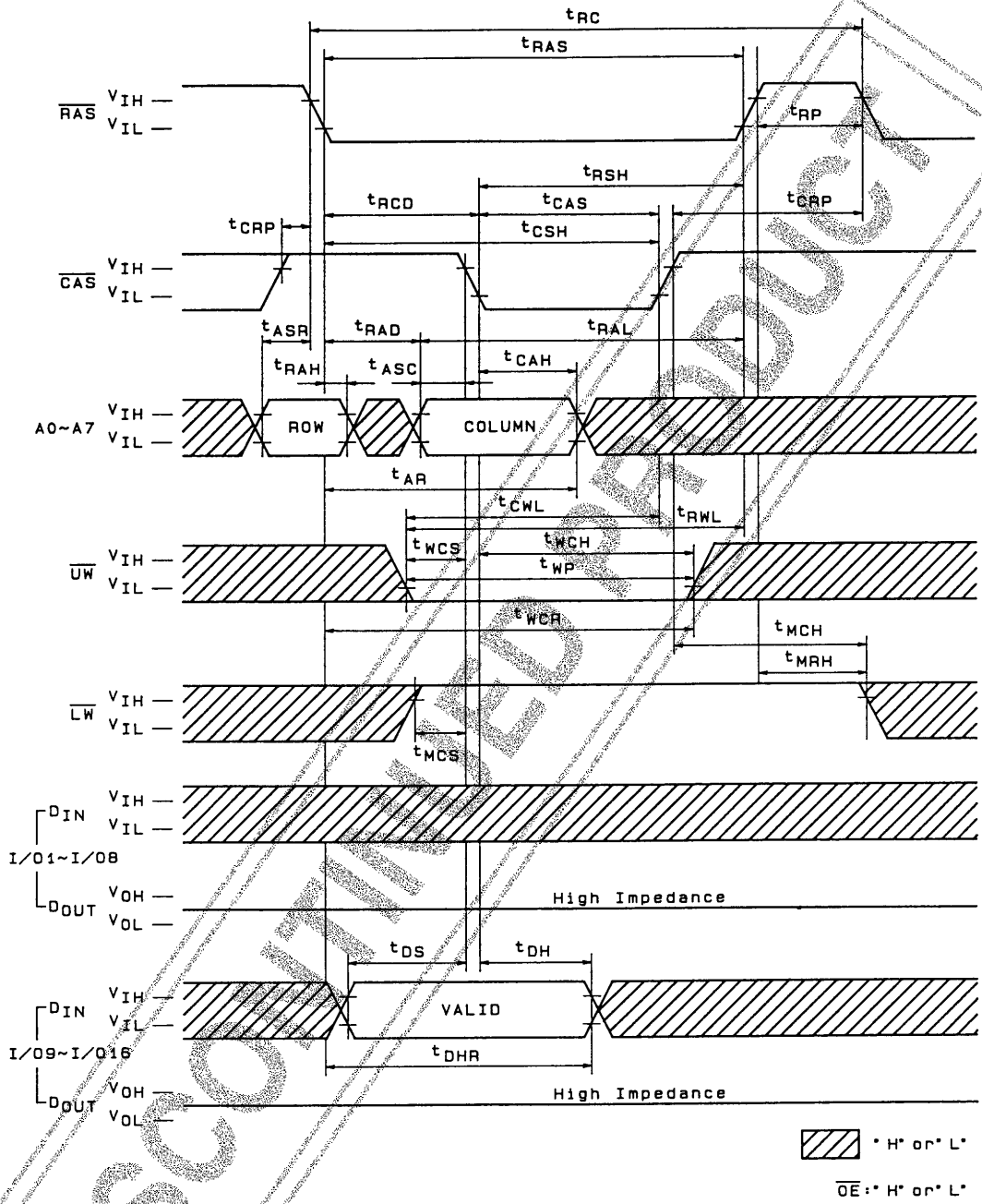


 * H* or* L*
 $\overline{\text{OE}}$: * H* or* L*

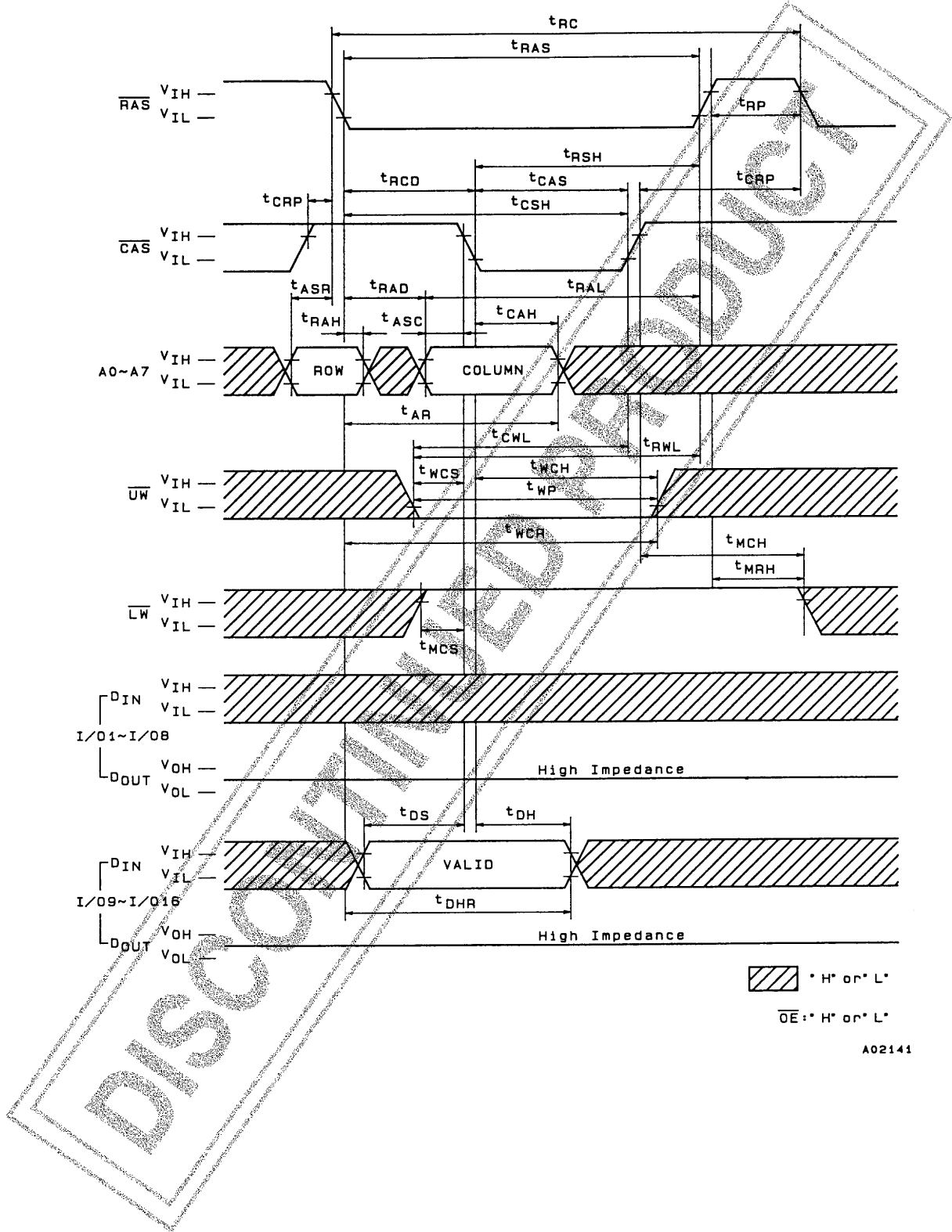
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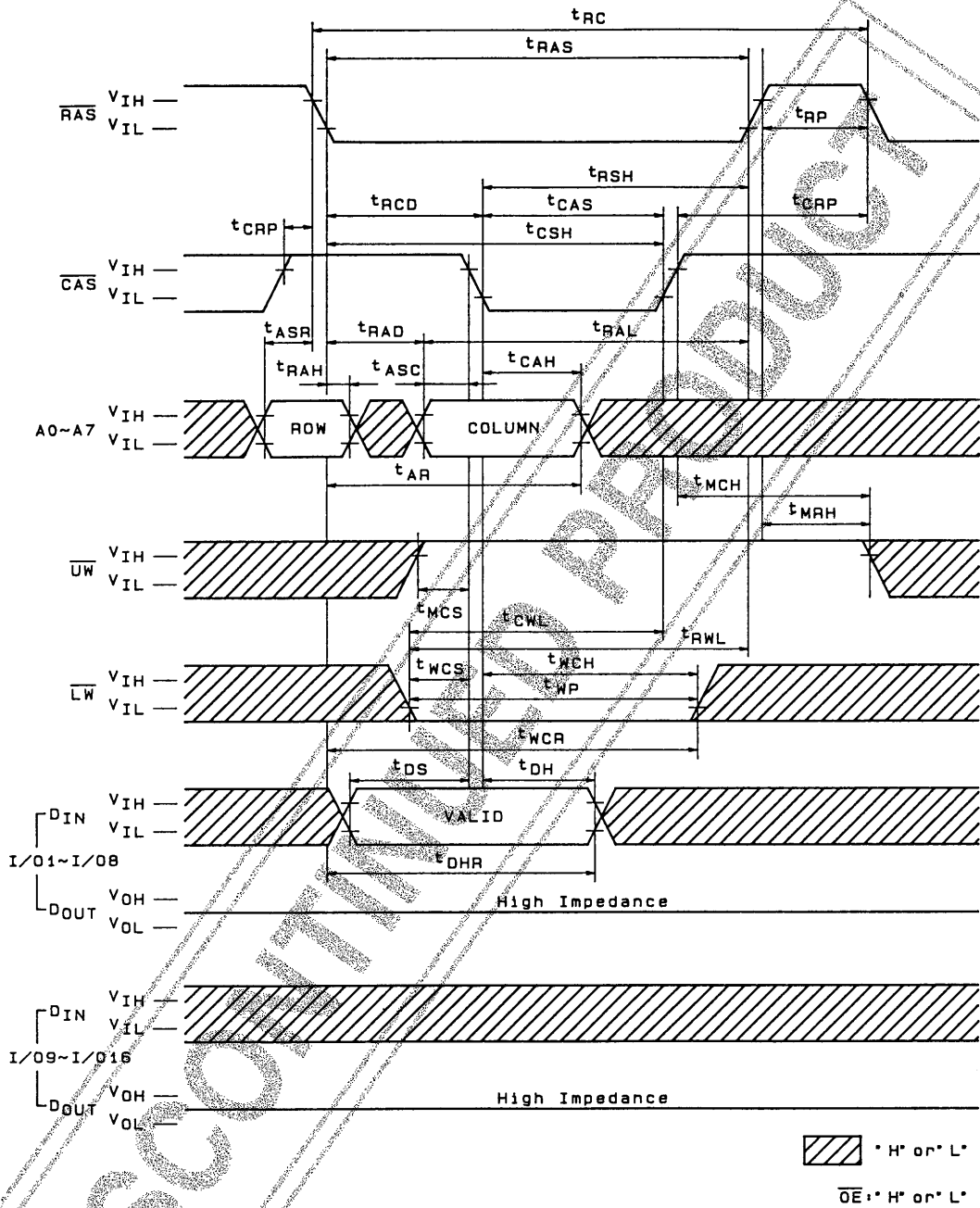
Upper Byte Early Write Cycle



A02141

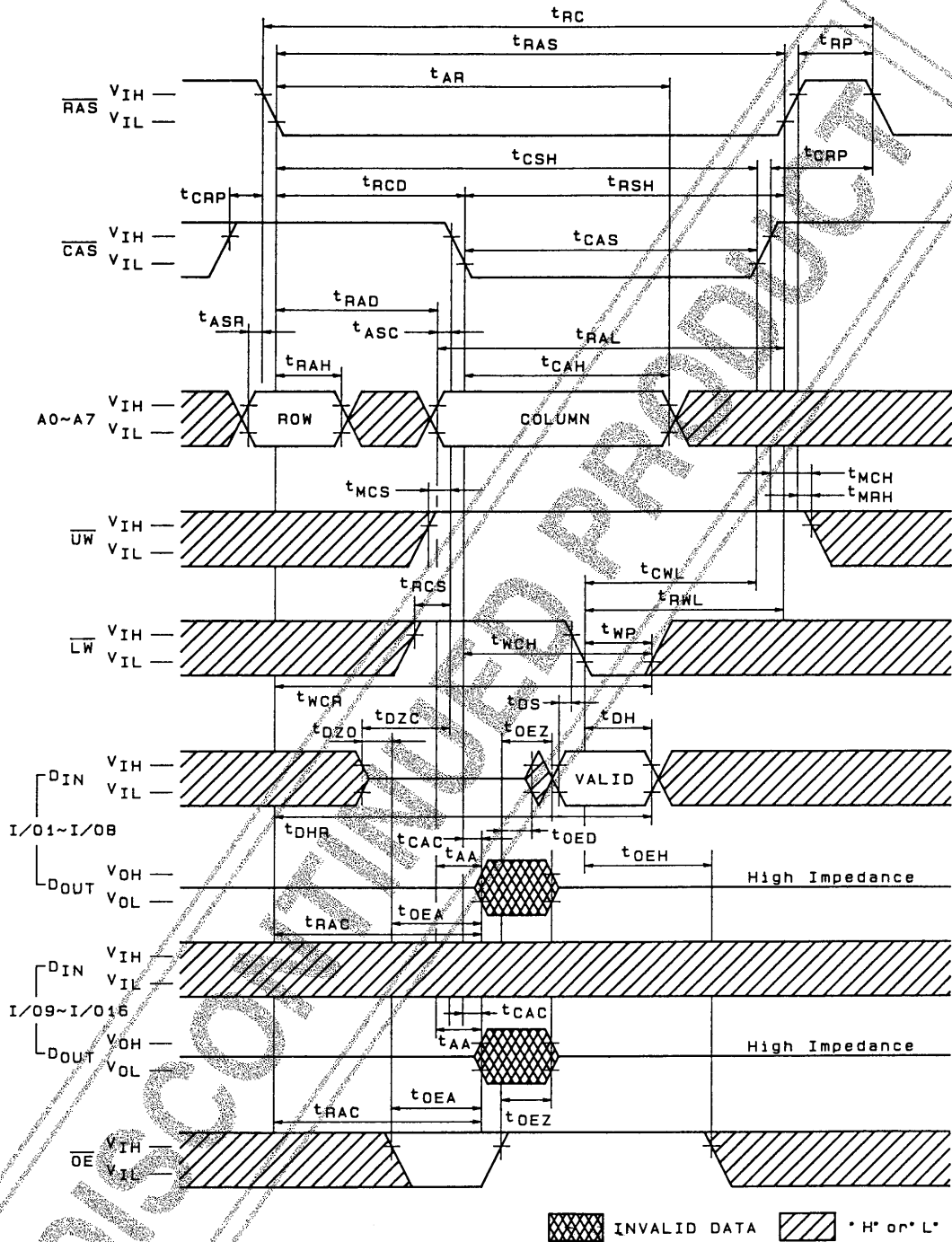


Lower Byte Early Write Cycle



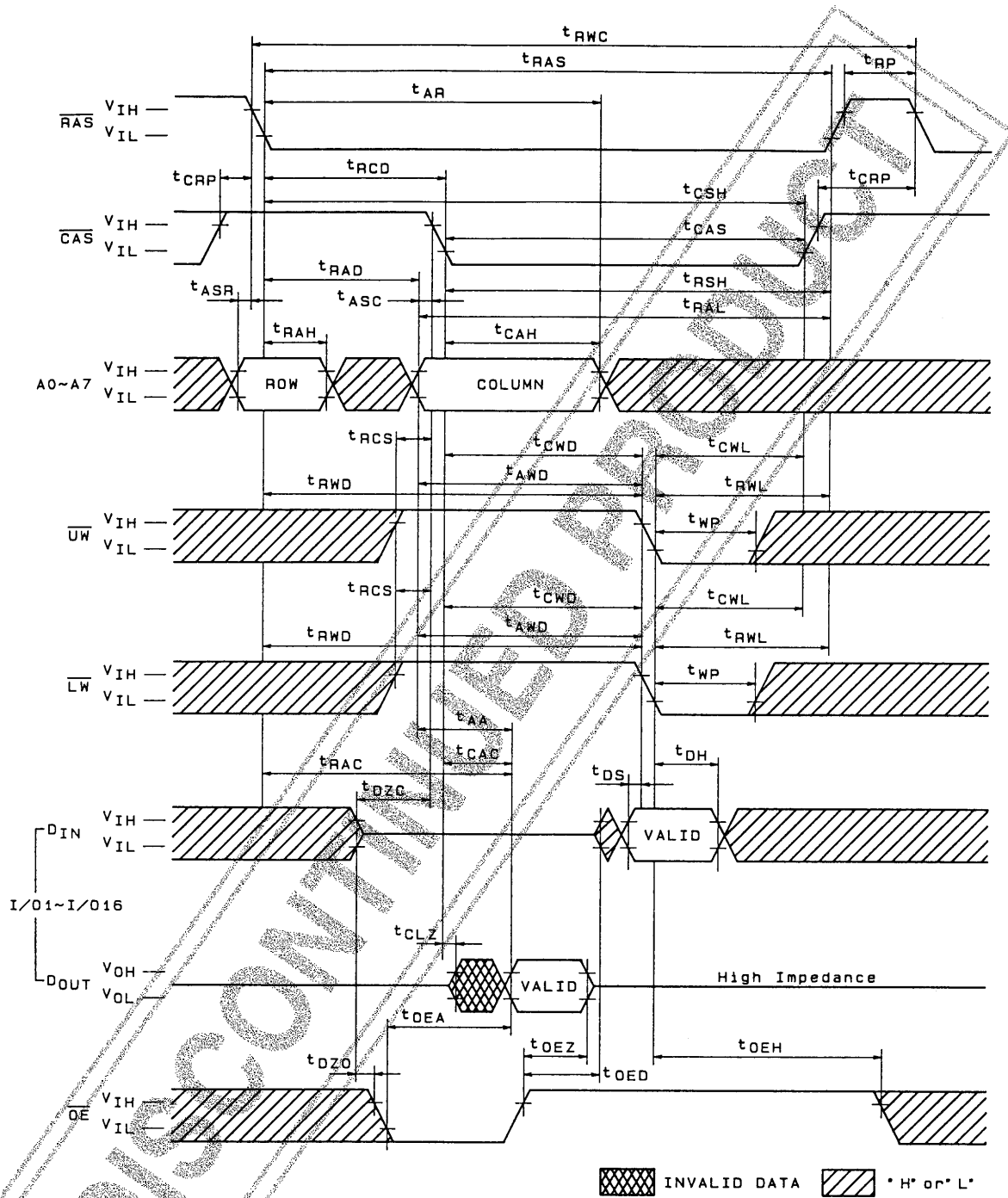
A02142

Lower Byte Write Cycle (\overline{OE} Control)



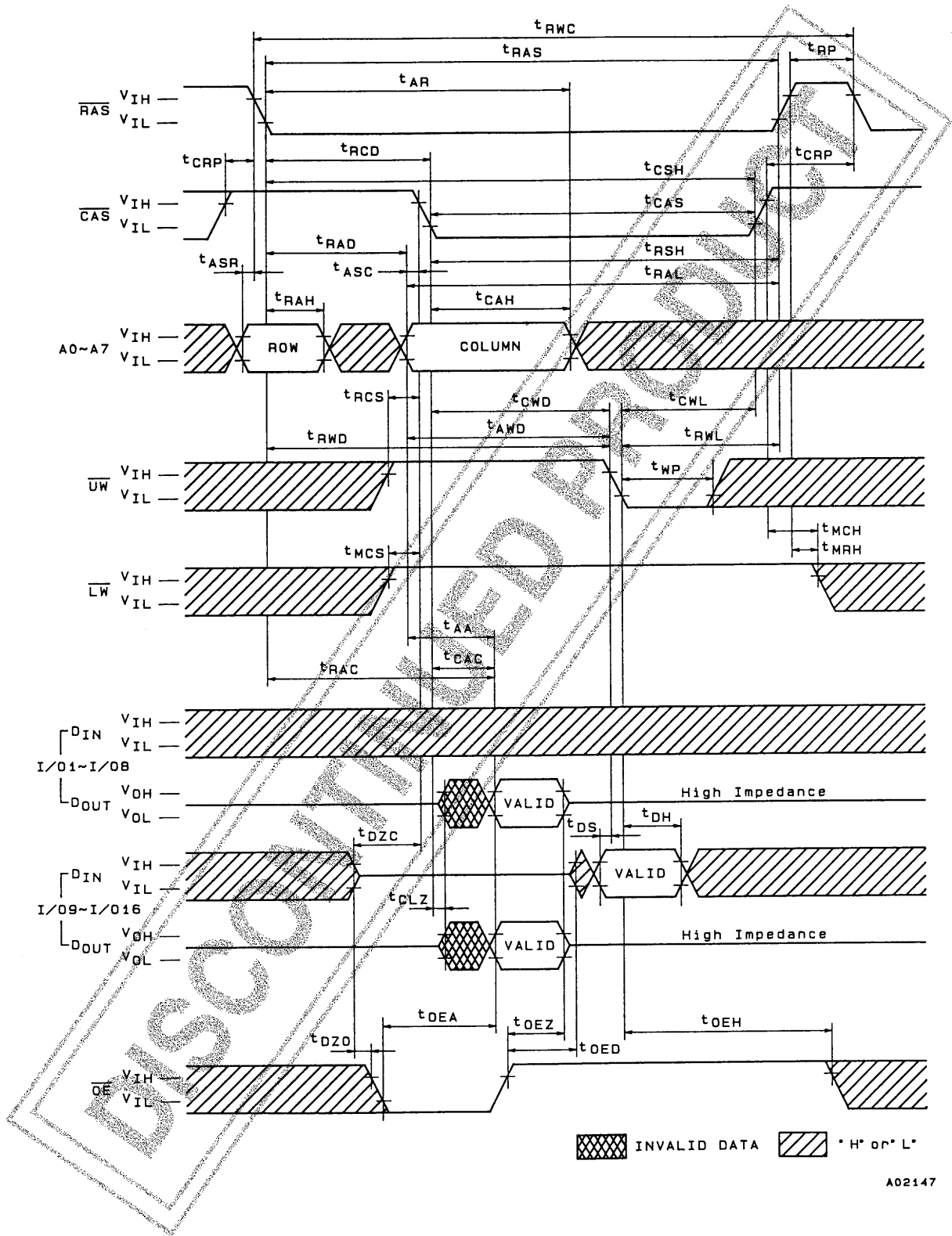
A02145

Read-Modify Write Cycle



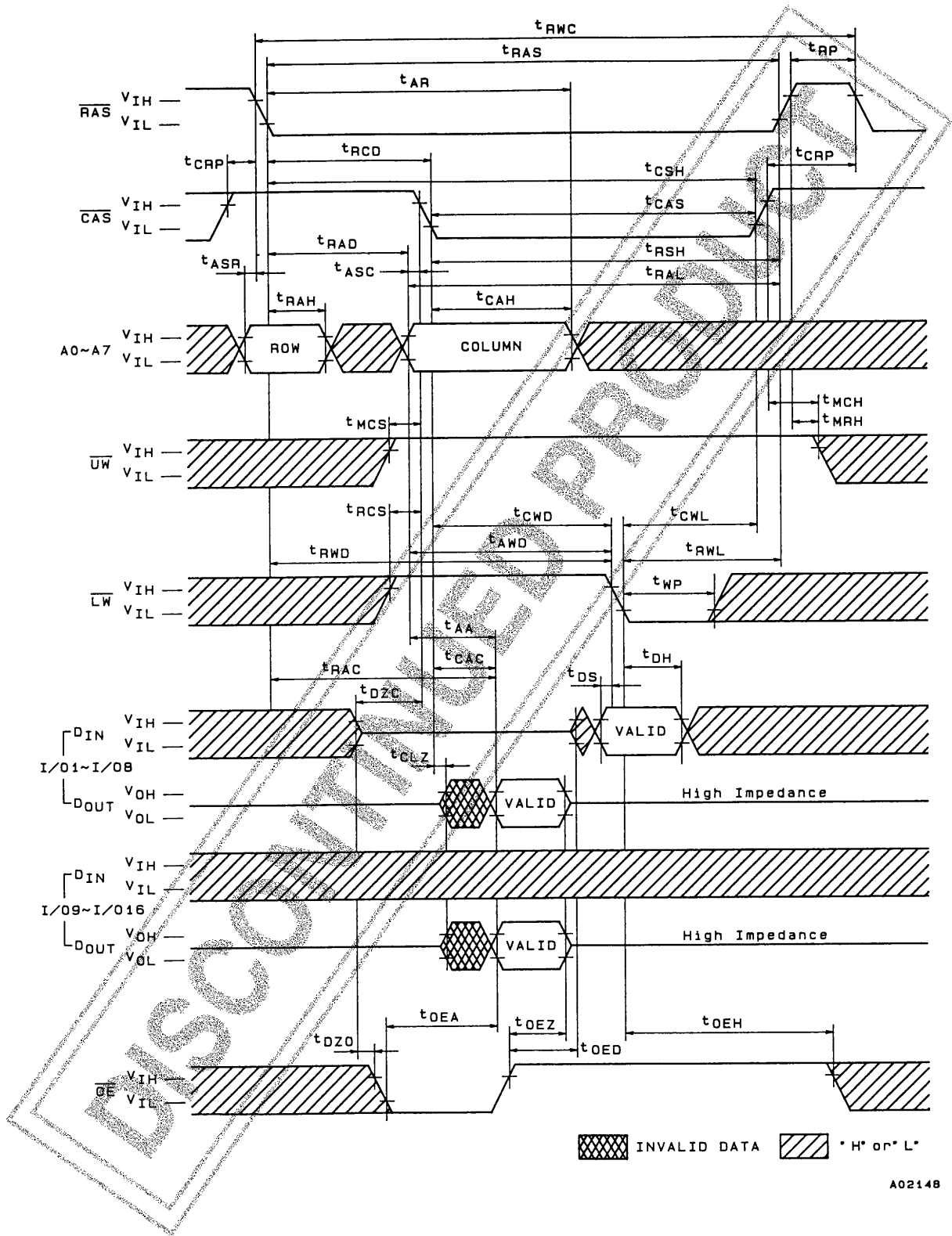
A02146

Read-Modify Upper Byte Write Cycle



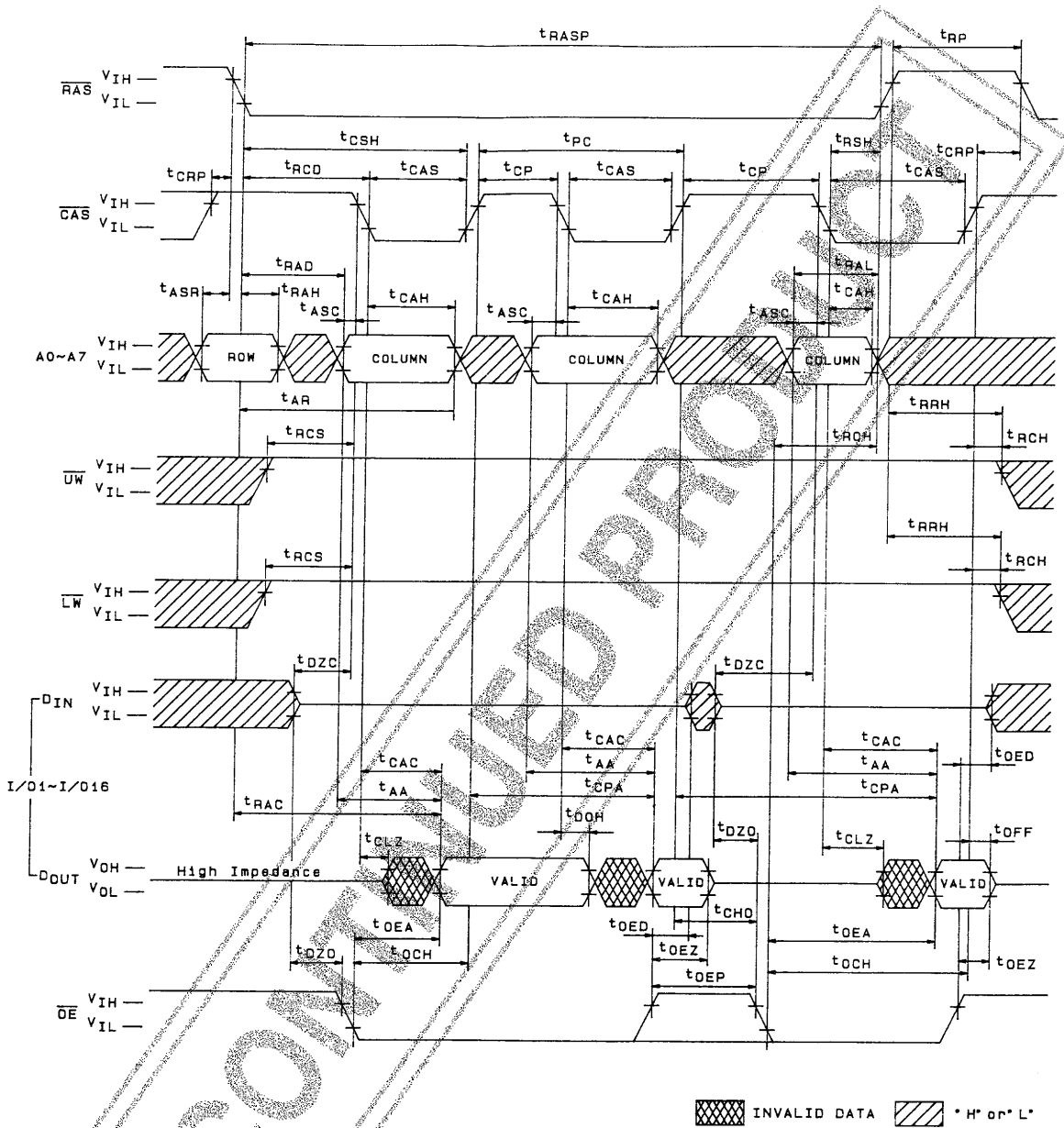
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Read-Modify Lower Byte Write Cycle

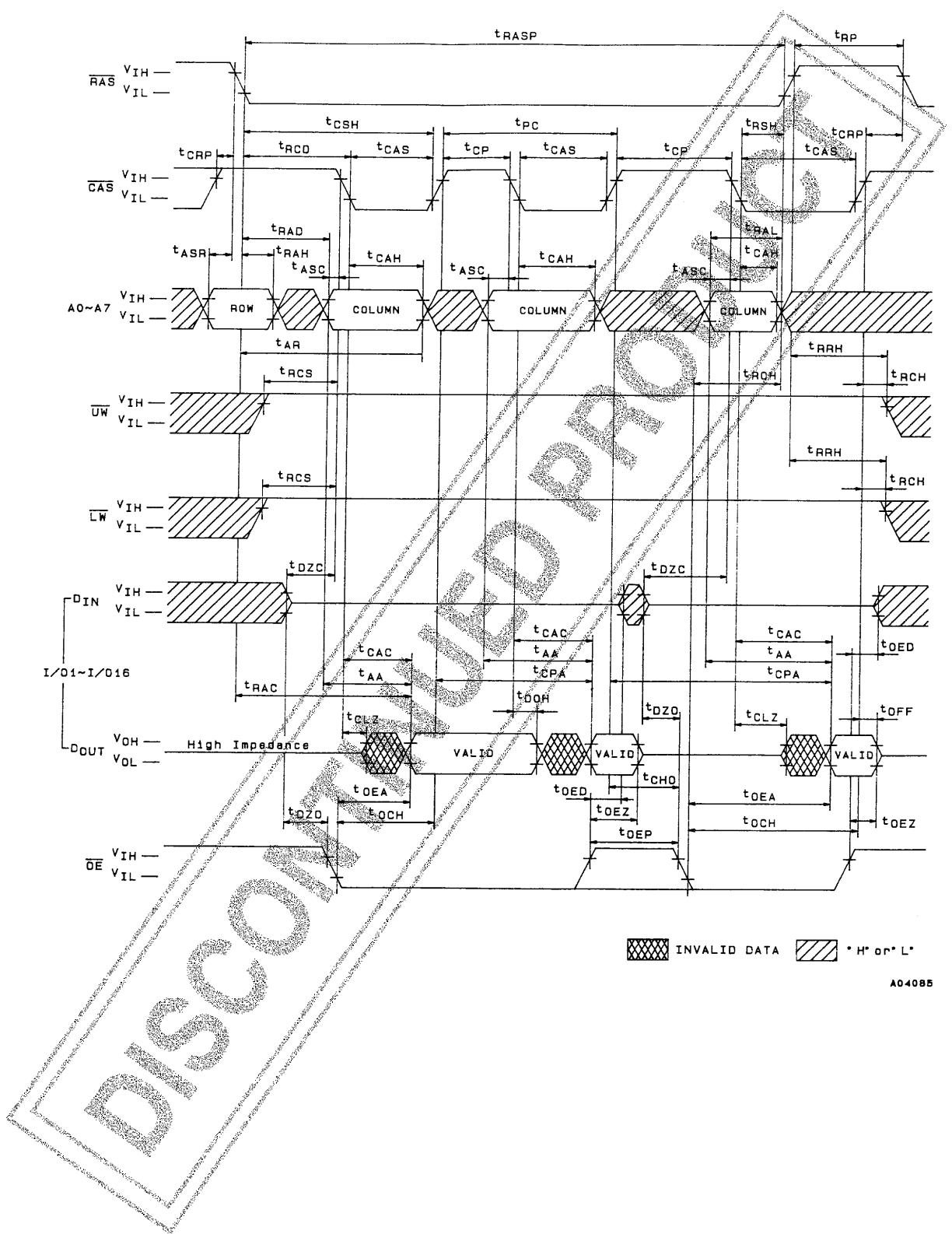


A02148

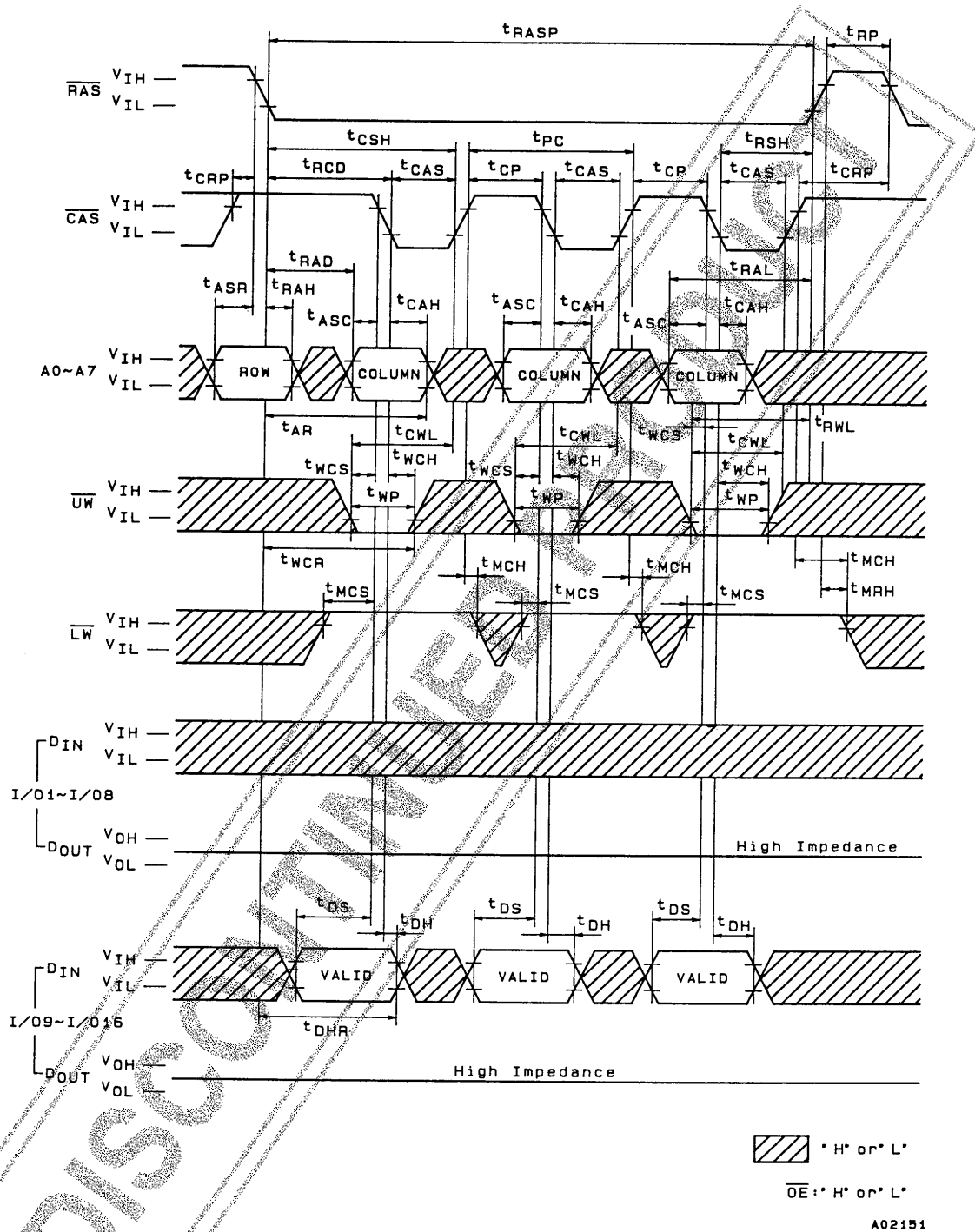
EDO Page Mode Read Cycle



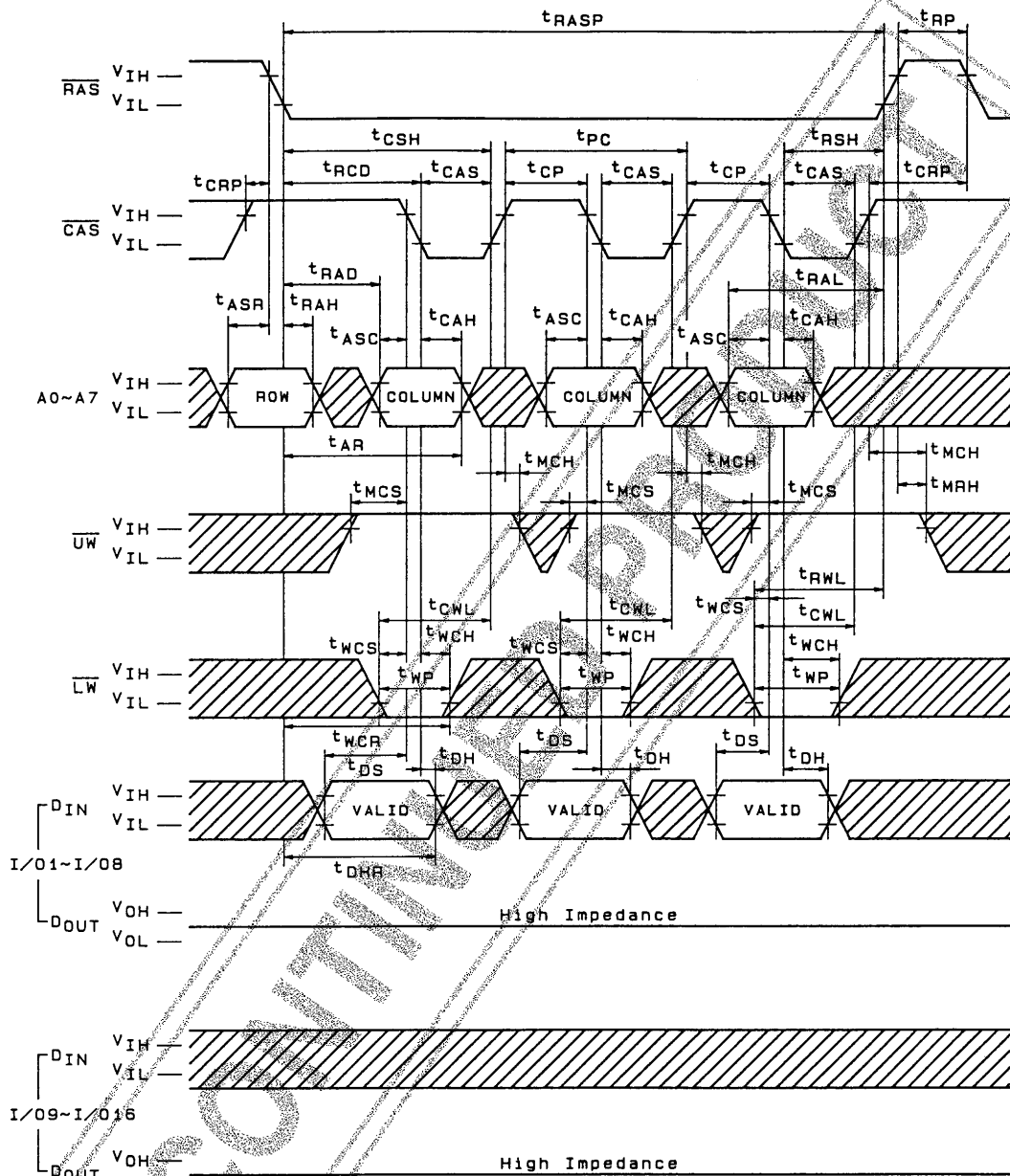
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


EDO Page Mode Upper Byte Early Write Cycle



EDO Page Mode Lower Byte Early Write Cycle

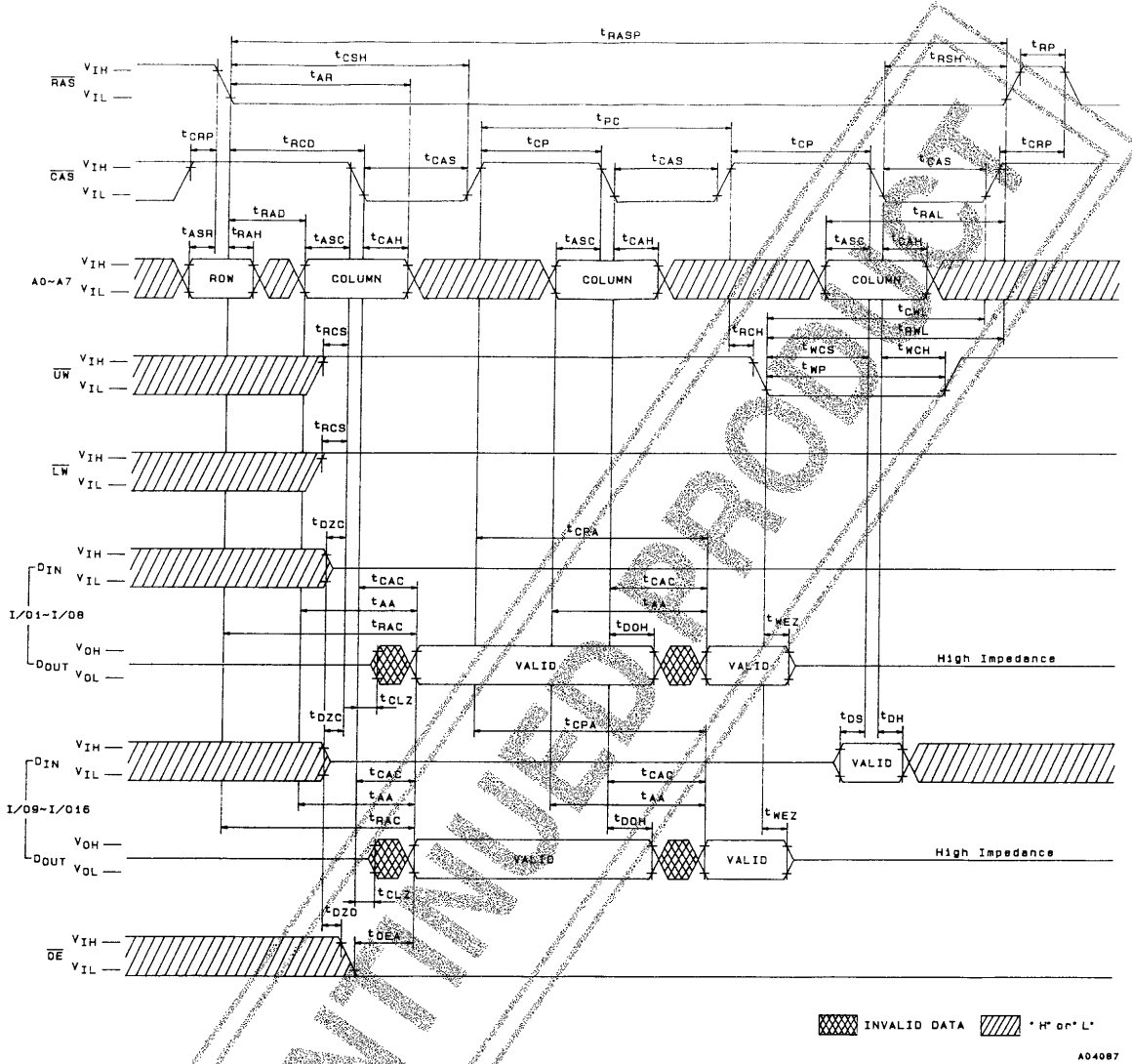


 * H* or * L*
 * H* or * L*

A02152

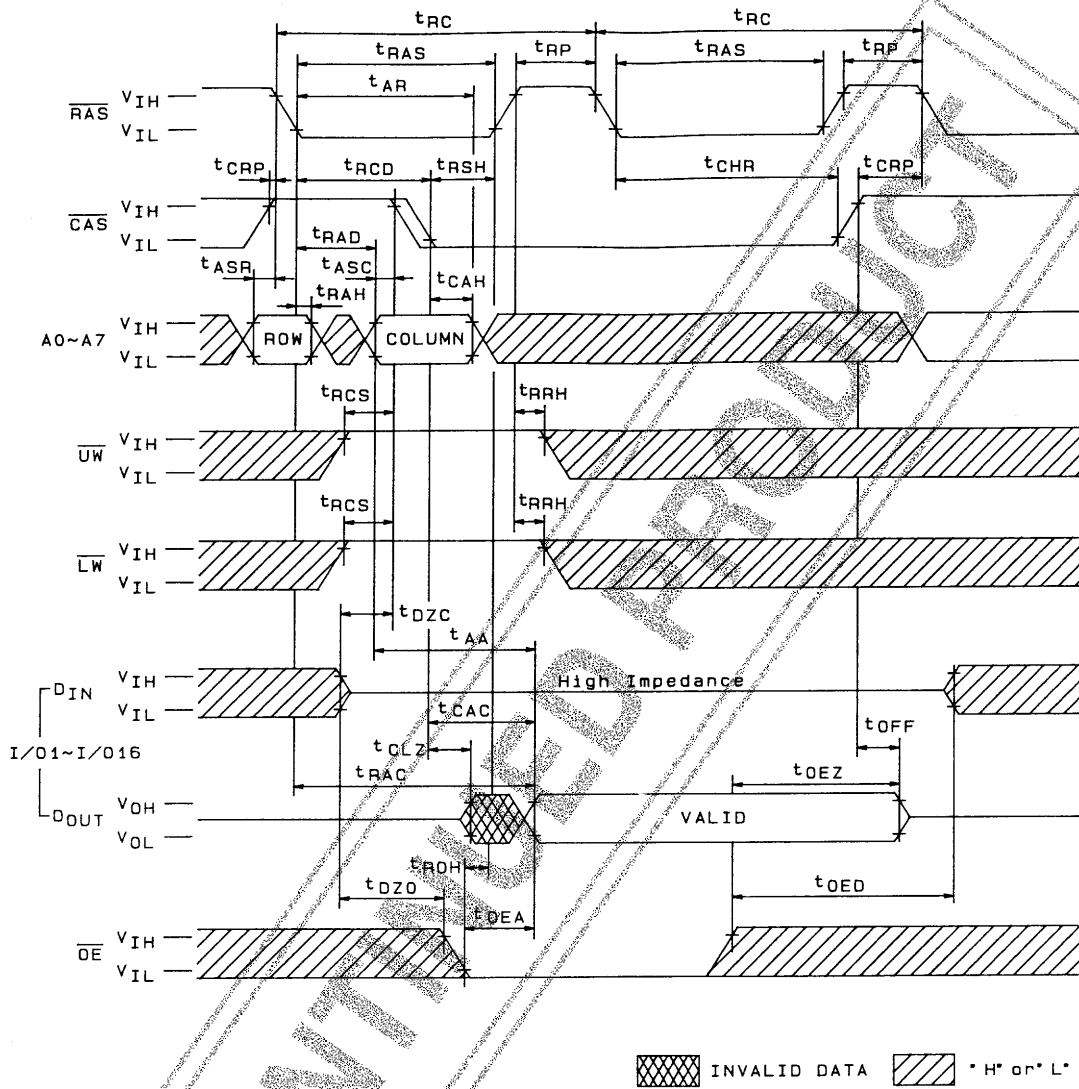
DISCONTINUED

EDO Page Mode Read Upper Byte Early Write Cycle



DISCONTINUED PRODUCT

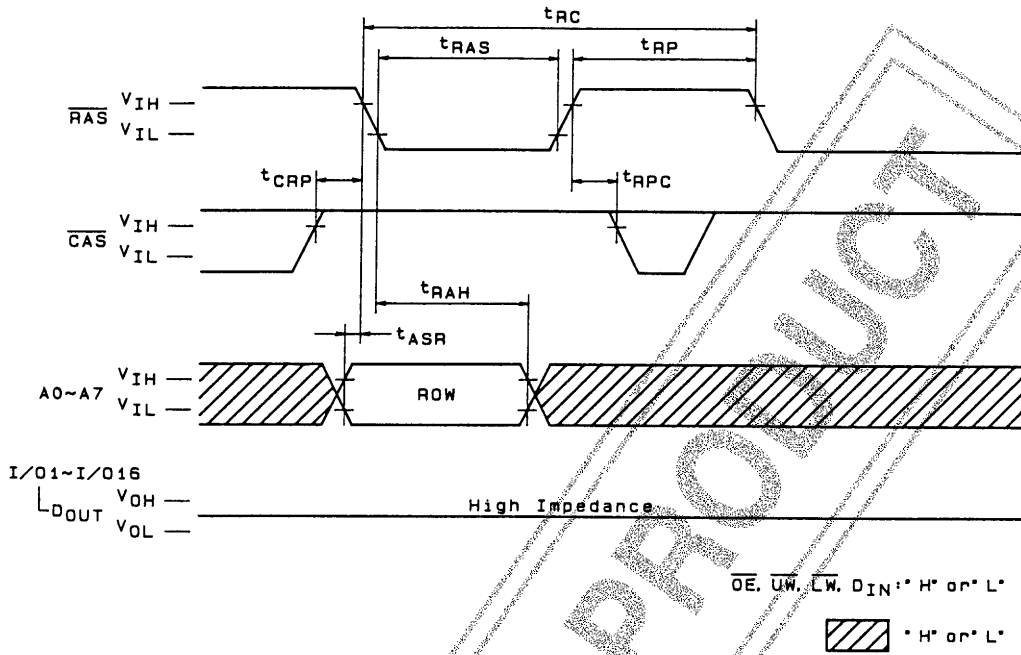
Hidden Refresh Cycle



A03723

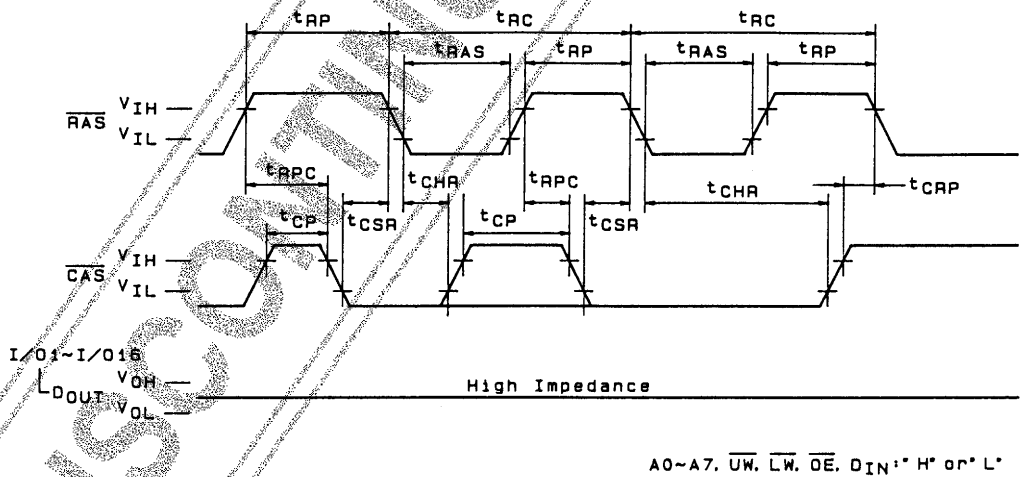
DISCONTINUED PRODUCT

RAS-Only Refresh Cycle



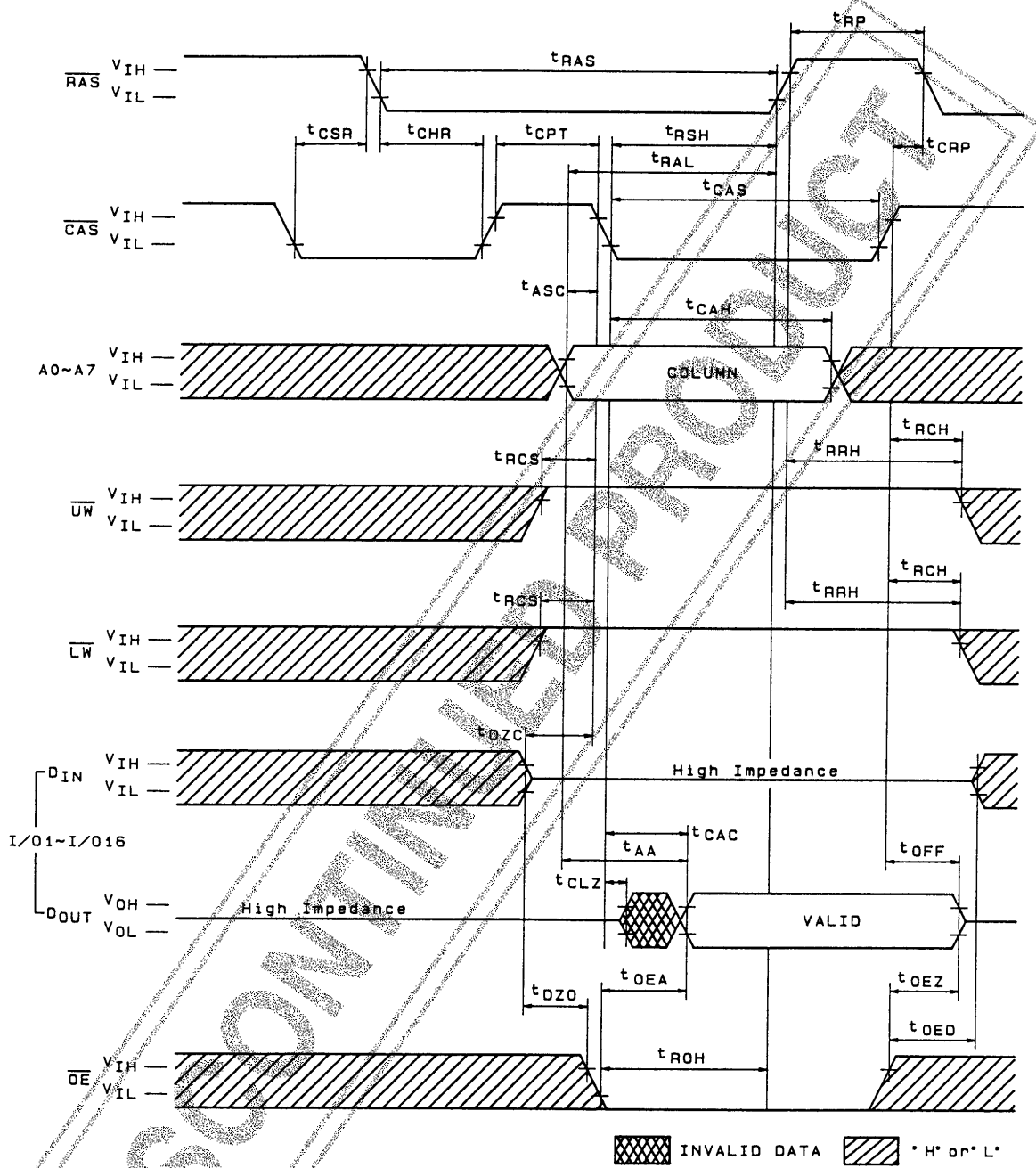
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CAS-Before-RAS Refresh Cycle



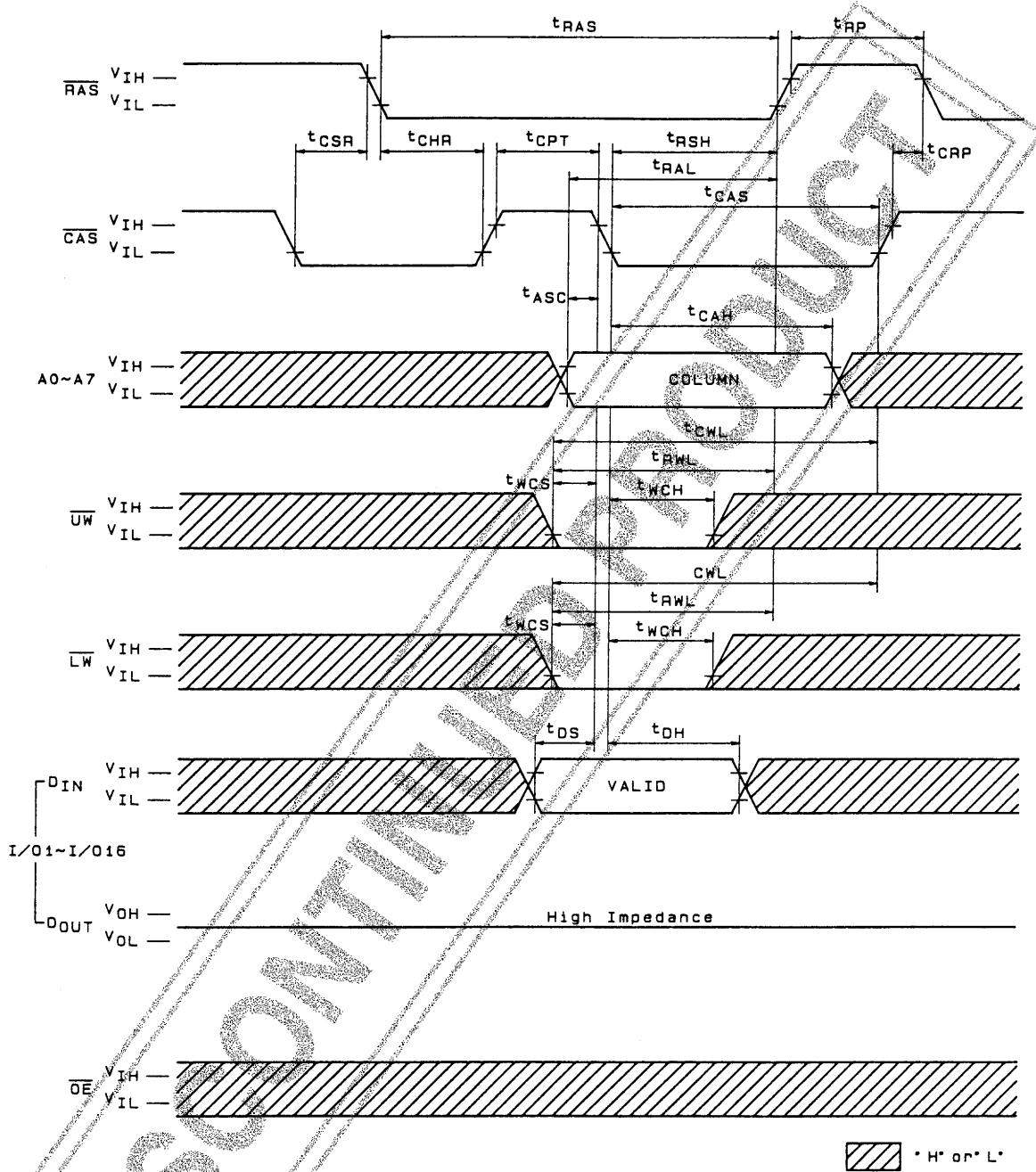
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CAS-Before-RAS Refresh Counter Test Cycle (Read)



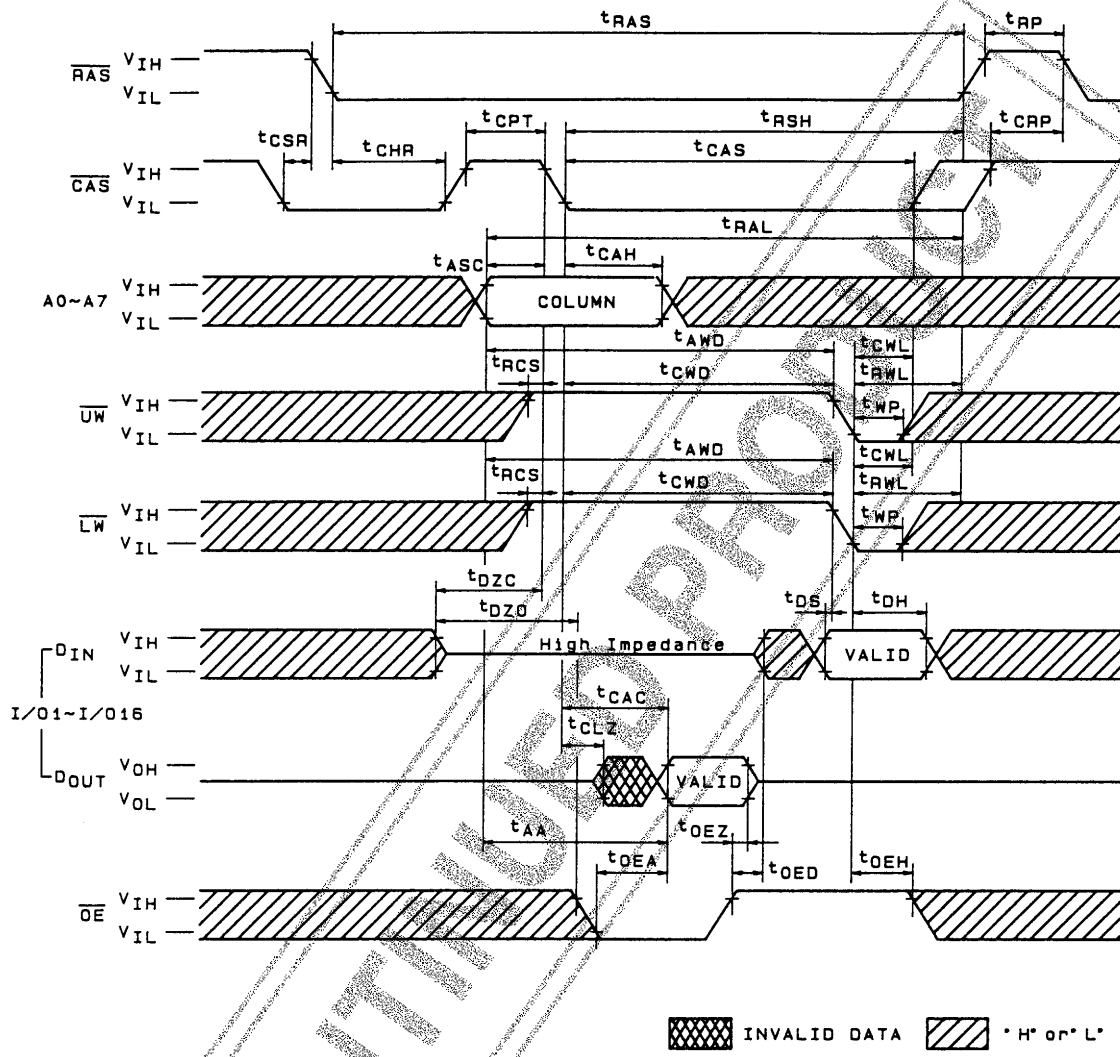
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CAS-Before-RAS Refresh Counter Test Cycle (Write)



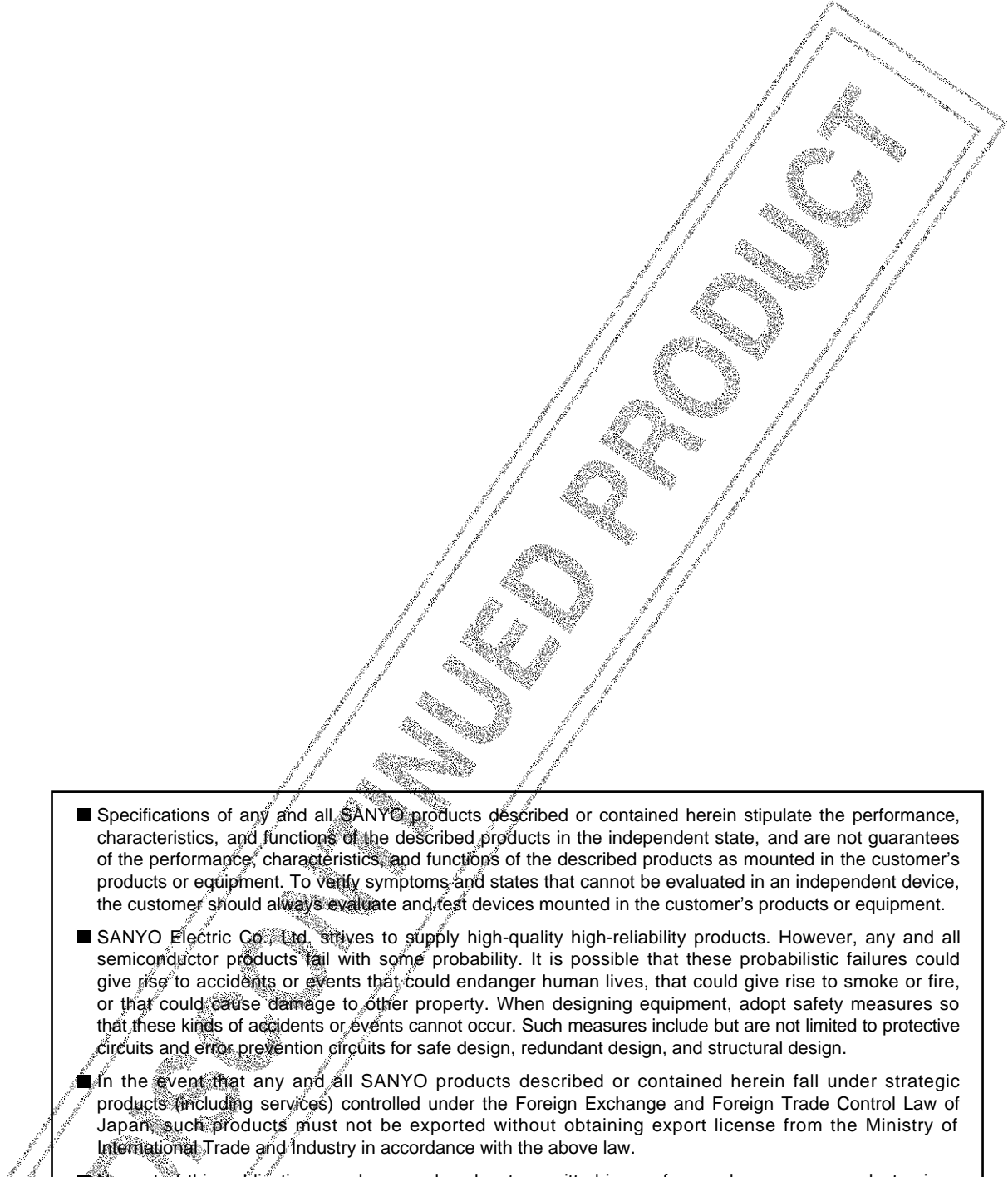
A02160

CAS-Before-RAS Refresh Counter Test Cycle (Read-Modify-Write)



A02181

DISCONTINUED

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