Ordering number : ENN6303

CMOS IC

LC35V256EM, ET-70W

256K (32K words × 8 bits) SRAM
Control pins: $\overline{OE}$ and $\overline{CE}$

Overview

The LC35V256EM-70W and LC35V256ET-70W are asynchronous silicon-gate CMOS SRAMs with a 32768-word by 8-bit structure. These are full-CMOS devices with 6 transistors per memory cell, and feature ultralow-voltage operation, a low operating current drain, and an ultralow standby current. Control inputs include $\overline{OE}$ for fast memory access and $\overline{CE}$ for power saving and device selection. This makes these devices optimal for systems that require low power or battery backup, and makes memory expansion easy. The ultralow standby current allows these devices to be used with capacitor backup as well.

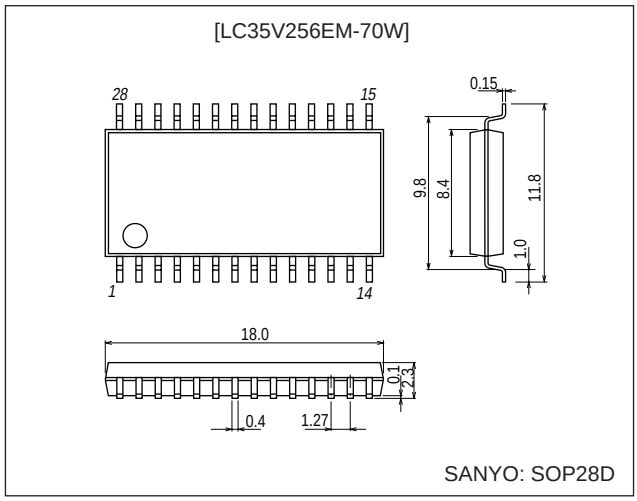
Features

- Supply voltage range: 3.0 to 3.6 V
- Access time: 70 ns (maximum)
- Standby current: 0.8 µA (Ta ≤ 60°C)
  4.0 µA (Ta ≤ 70°C)
- Operating temperature: –10 to +70°C
- Data retention voltage: 2.0 to 3.6 V
- All I/O levels: CMOS compatible (0.8 V_{CC}, 0.2 V_{CC})
- Input/output shared function pins, 3-state output pins
- No clock required (fully static circuits)
- Package
  28-pin SOP (450 mil) plastic package:
  LC35V256EM-70W
  28-pin TSOP (8 × 13.4 mm) plastic package:
  LC35V256ET-70W

Package Dimensions

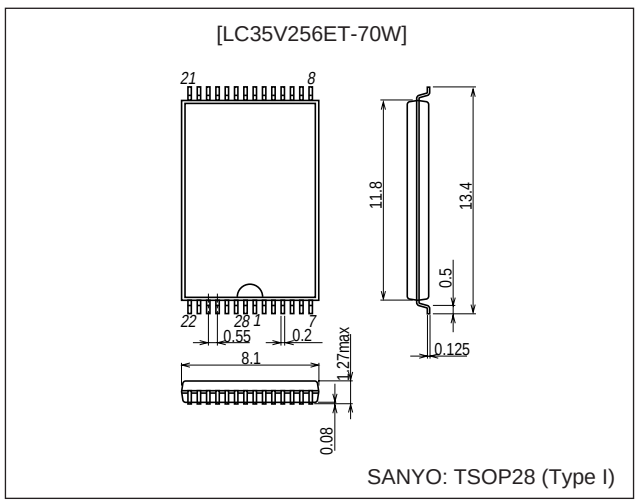
unit: mm

3187A-SOP28D



unit: mm

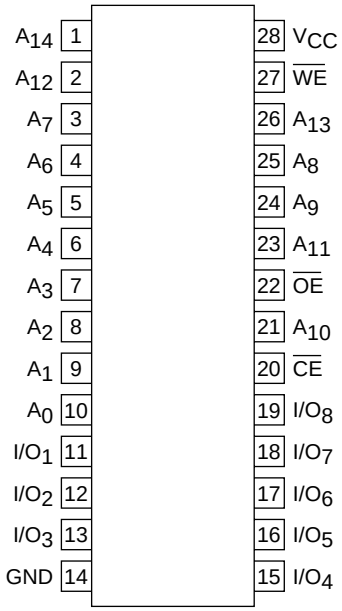
3221-TSOP28 (Type I)



SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Pin Assignment (Top view)

SOP28

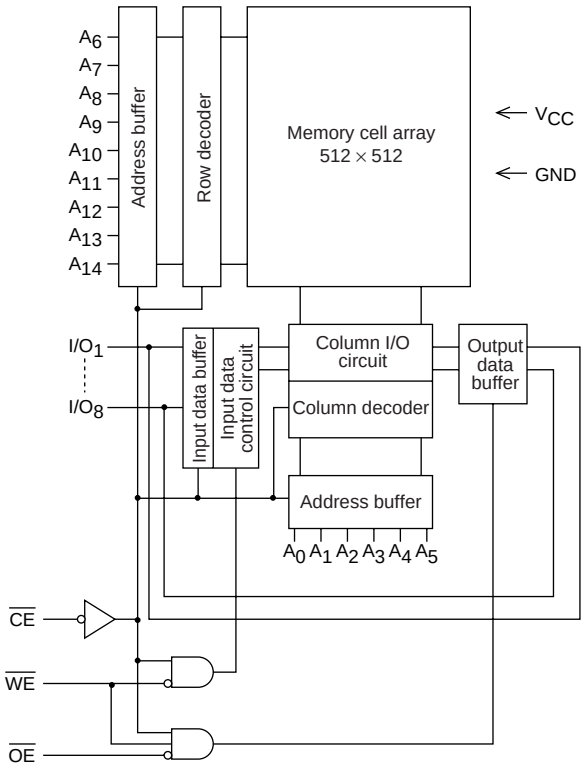


LC35V256EM-70W

TSOP28

LC35V256ET-70W

Block Diagram



Pin Functions

A0 to A14	Address input
$\overline{WE}$	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE}$	Chip enable input
I/O1 to I/O8	Data I/O
V_{CC}, GND	Power supply, ground

Function Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High impedance	I_{CCA}
Unselected	H	X	X	High impedance	I_{CCS}

Note: X indicates H or L.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		4.6	V
Input pin voltage	V_{IN}		–0.3* to V_{CC} + 0.3	V
I/O pin voltage	$V_{I/O}$		–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr		–10 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Note: * The minimum value is –2.0 V for pulse widths under 30 ns.

I/O Capacitances at Ta = 25°C, f = 1 MHz

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		6	10	pF
Input pin capacitance	C_I	V_{IN} = 0 V		6	10	pF

Note: All units are not tested; only samples are tested.

DC Allowable Operating Ranges at Ta = –10 to +70°C, V_{CC} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		3.0	3.3	3.6	V
Input voltage	V_{IH}		0.8V_{CC}		V_{CC} + 0.3	V
	V_{IL}		–0.3*		0.2V_{CC}	V

Note: * The minimum value is –2.0 V for pulse widths under 30 ns.

DC Electrical Characteristics at Ta = –10 to +70°C, V_{CC} = 3.0 to 3.6 V

Parameter		Symbol	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Input leakage current		I_{LI}	V_{IN} = 0 to V_{CC}		–1.0		+1.0	µA
Output leakage current		I_{LO}	$V_{\overline{CE}} = V_{IH}$ or $V_{\overline{OE}} = V_{IH}$ or $V_{\overline{WE}} = V_{IL}$ $V_{I/O}$ = 0 to V_{CC}		–1.0		+1.0	µA
Output high-level voltage		V_{OH1}	I_{OH1} = –2.0 mA		V_{CC} – 0.4			V
		V_{OH2}	I_{OH2} = –100 µA		V_{CC} – 0.1			V
Output low-level voltage		V_{OL1}	I_{OL1} = 2.0 mA				0.4	V
		V_{OL2}	I_{OL2} = 100 µA				0.4	V
Operating current drain	CMOS inputs	I_{CCA2}	$V_{\overline{CE}} = V_{IL}$, $I_{I/O}$ = 0 mA, $V_{IN} = V_{IH}$ or V_{IL}				1.2	mA
		I_{CCA3}	$V_{\overline{CE}} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL} $I_{I/O}$ = 0 mA, DUTY 100 %	min cycle		20	25	mA
				1 µs cycle		1.5	2.5	mA
Standby mode current drain	V_{CC} – 0.2 V/ 0.2 V inputs	I_{CCS1}	$V_{\overline{CE}} \geq V_{CC}$ – 0.2 V, V_{IN} = 0 to V_{CC}	Ta ≤ 25°C		0.01		µA
				Ta ≤ 60°C			0.8	µA
				Ta ≤ 70°C			4.0	µA
	CMOS inputs	I_{CCS2}	$V_{\overline{CE}} = V_{IH}$, V_{IN} = 0 to V_{CC}				0.4	mA

Note: * Reference values when V_{CC} = 3.3 V and Ta = 25°C.

AC Electrical Characteristics at Ta = –10 to +70°C, V_{CC} = 3.0 to 3.6 V

AC test conditions
Input pulse voltage levels: 0.2 V_{CC} to 0.8 V_{CC}
Input rise and fall times: 5 ns
Input and output timing levels: 1/2 V_{CC}
Output load: 30 pF (including the jig capacitance)

Read Cycle

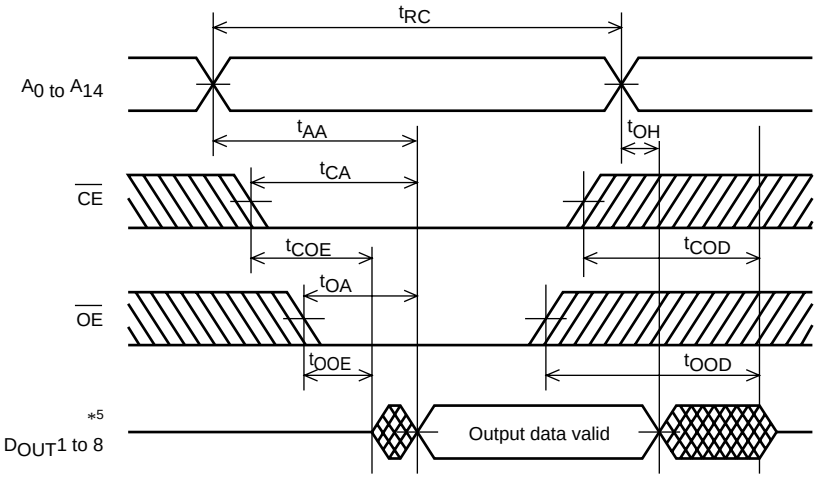
Parameter	Symbol	min	max	Unit
Read cycle time	t_{RC}	70		ns
Address access time	t_{AA}		70	ns
$\overline{CE}$ access time	t_{CA}		70	ns
$\overline{OE}$ access time	t_{OA}		50	ns
Output hold time	t_{OH}	10		ns
$\overline{CE}$ output enable time	t_{COE}	10		ns
$\overline{OE}$ output enable time	t_{OOE}	5		ns
$\overline{CE}$ output disable time	t_{COD}		35	ns
$\overline{OE}$ output disable time	t_{OOD}		30	ns

Write Cycle

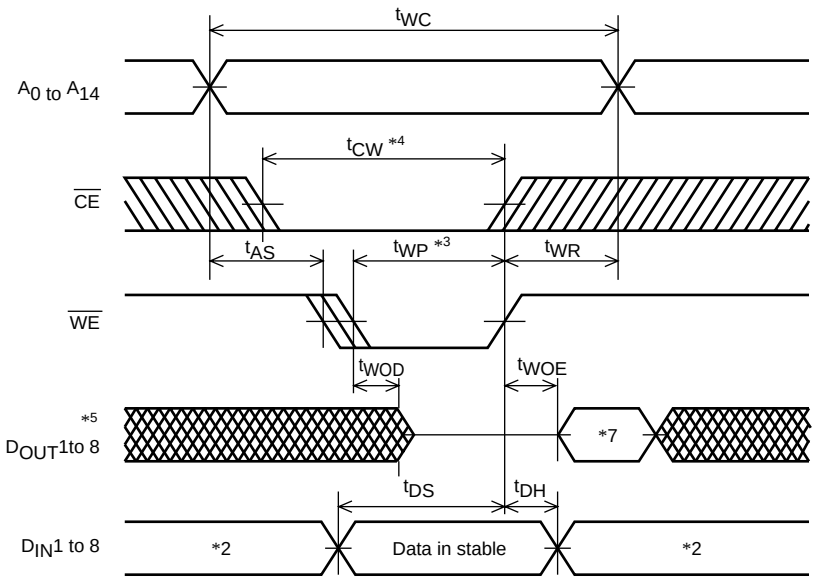
Parameter	Symbol	min	max	Unit
Write cycle time	t_{WC}	70		ns
Address setup time	t_{AS}	0		ns
Write pulse width	t_{WP}	55		ns
$\overline{CE}$ setup time	t_{CW}	60		ns
Write recovery time	t_{WR}	0		ns
$\overline{CE}$ write recovery time	t_{WR1}	0		ns
Data setup time	t_{DS}	50		ns
Data hold time	t_{DH}	0		ns
$\overline{CE}$ data hold time	t_{DH1}	0		ns
$\overline{WE}$ output enable time	t_{WOE}	5		ns
$\overline{WE}$ output disable time	t_{WOD}		35	ns

Timing Charts

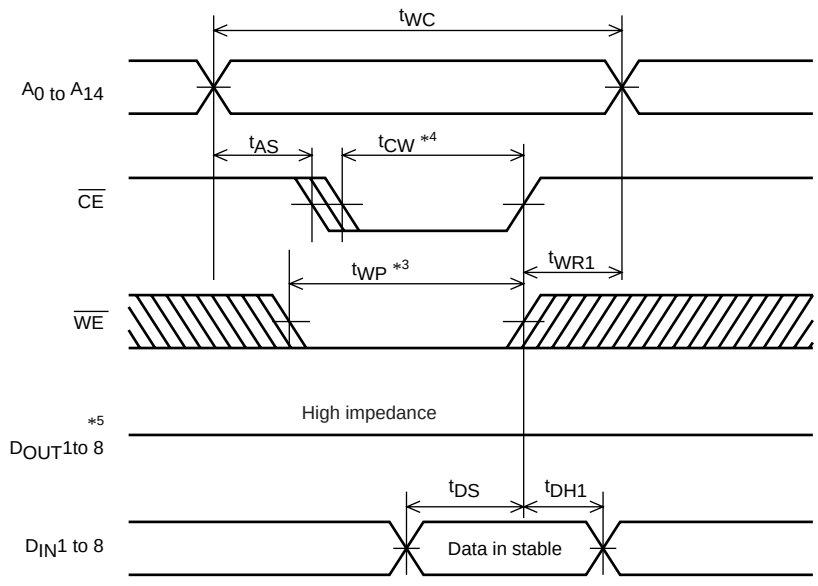
[Read cycle] *1



[Write cycle 1] ($\overline{WE}$ write) *6



[Write cycle 2] ($\overline{CE}$ write) *6



Notes: 1. $\overline{WE}$ must be held at the high level during the read cycle.
2. Do not apply reverse phase signals to the DOUT pins when those pins are in the output state.
3. The time t_{WP} is the period when both $\overline{CE}$ and $\overline{WE}$ are low. It is defined as the time from the fall of $\overline{WE}$ to the rise of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
4. The time t_{CW} is the period when both $\overline{CE}$ and $\overline{WE}$ are low. It is defined as the time from the fall of $\overline{CE}$ to the rise of $\overline{CE}$ or $\overline{WE}$, whichever occurs first.
5. The D_{OUT} pins will be in the high-impedance state if any one of the following is held: $\overline{OE}$ is at the high level, $\overline{CE}$ is at the high level, or $\overline{WE}$ is at the low level.
6. The $\overline{OE}$ pin must be either held high or held low during the write cycle.
7. D_{OUT} has the same phase as the write data during this write cycle.

Data Retention Characteristics at Ta = –10 to +70°C

Parameter	Symbol	Conditions	min	max	Unit
Data retention supply voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC} - 0.2$ V	2.0	3.6	V
Chip enable setup time	t_{CDR}		0		ns
Chip enable hold time	t_R		t_{RC}*		ns

Note: * t_{RC}: Read cycle time

Data Retention Waveforms ($\overline{CE}$ control)