



LC35V256EM, ET-70W

256K (32K words × 8 bits) SRAM
Control pins: \overline{OE} and \overline{CE}

Overview

The LC35V256EM-70W and LC35V256ET-70W are asynchronous silicon-gate CMOS SRAMs with a 32768-word by 8-bit structure. These are full-CMOS devices with 6 transistors per memory cell, and feature ultralow-voltage operation, a low operating current drain, and an ultralow standby current. Control inputs include \overline{OE} for fast memory access and \overline{CE} for power saving and device selection. This makes these devices optimal for systems that require low power or battery backup, and makes memory expansion easy. The ultralow standby current allows these devices to be used with capacitor backup as well.

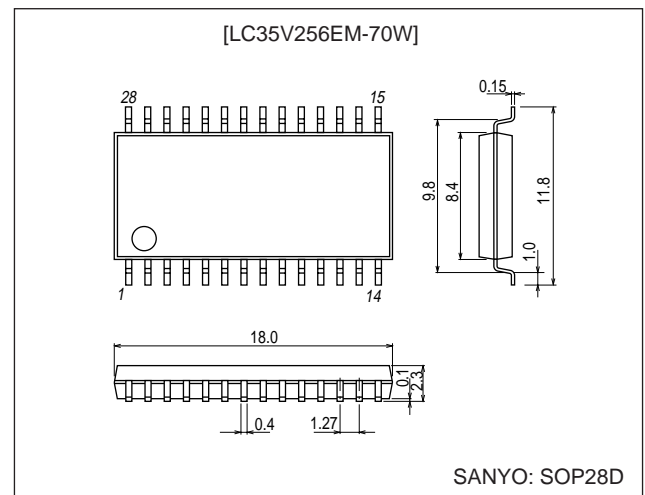
Features

- Supply voltage range: 3.0 to 3.6 V
- Access time: 70 ns (maximum)
- Standby current: 0.8 μ A ($T_a \leq 60^\circ\text{C}$)
4.0 μ A ($T_a \leq 70^\circ\text{C}$)
- Operating temperature: -10 to $+70^\circ\text{C}$
- Data retention voltage: 2.0 to 3.6 V
- All I/O levels: CMOS compatible (0.8 V_{CC} , 0.2 V_{CC})
- Input/output shared function pins, 3-state output pins
- No clock required (fully static circuits)
- Package
 - 28-pin SOP (450 mil) plastic package:
LC35V256EM-70W
 - 28-pin TSOP (8 × 13.4 mm) plastic package:
LC35V256ET-70W

Package Dimensions

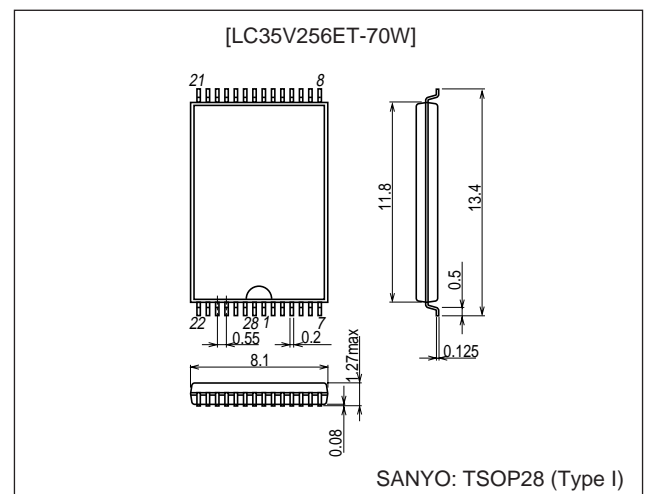
unit: mm

3187A-SOP28D



unit: mm

3221-TSOP28 (Type I)



■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

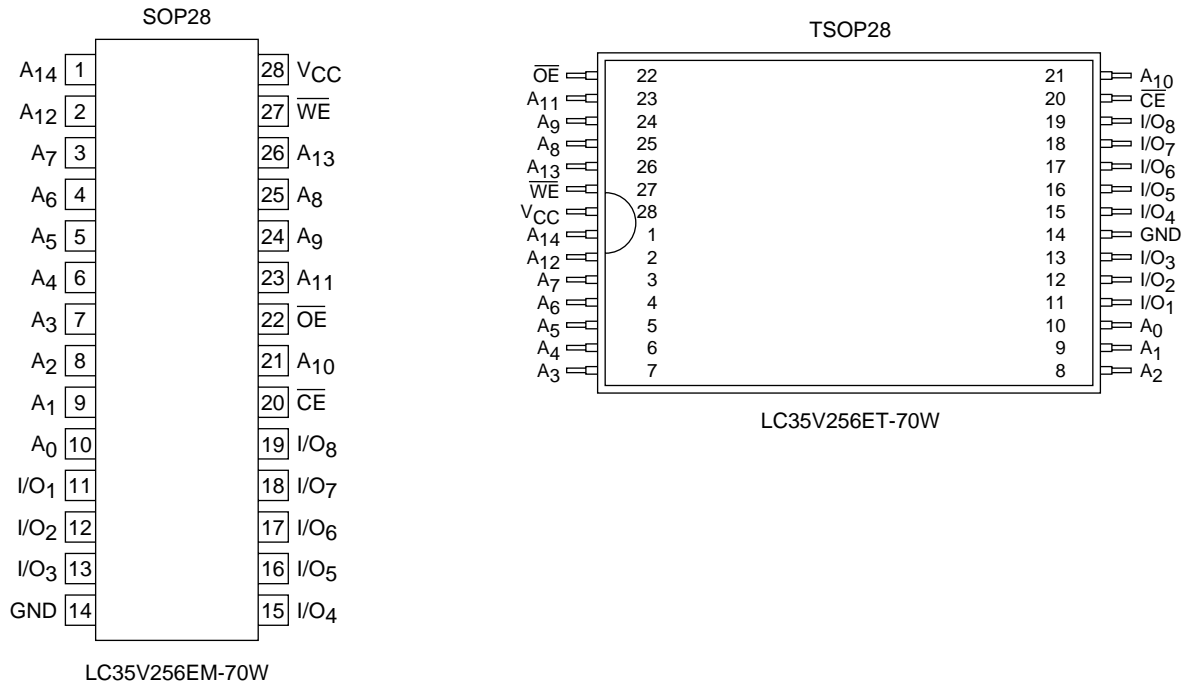
■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co., Ltd. Semiconductor Company

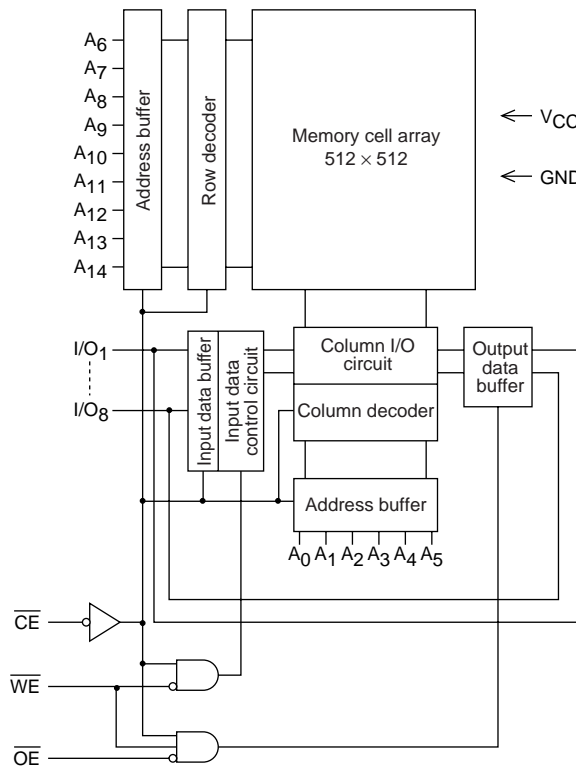
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC35V256EM, ET70W

Pin Assignment (Top view)



Block Diagram



LC35V256EM, ET70W

Pin Functions

A0 to A14	Address input
\overline{WE}	Read/write control input
\overline{OE}	Output enable input
\overline{CE}	Chip enable input
I/O1 to I/O8	Data I/O
V_{CC} , GND	Power supply, ground

Function Table

Mode	\overline{CE}	\overline{OE}	\overline{WE}	I/O	Supply current
Read cycle	L	L	H	Data output	I_{CCA}
Write cycle	L	X	L	Data input	I_{CCA}
Output disable	L	H	H	High impedance	I_{CCA}
Unselected	H	X	X	High impedance	I_{CCS}

Note: X indicates H or L.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\ max}$		4.6	V
Input pin voltage	V_{IN}		-0.3* to $V_{CC} + 0.3$	V
I/O pin voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$	V
Operating temperature	T_{opr}		-10 to +70	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note: * The minimum value is -2.0 V for pulse widths under 30 ns.

I/O Capacitances at $T_a = 25^\circ\text{C}$, $f = 1\ \text{MHz}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
I/O pin capacitance	$C_{I/O}$	$V_{I/O} = 0\ \text{V}$		6	10	pF
Input pin capacitance	C_I	$V_{IN} = 0\ \text{V}$		6	10	pF

Note: All units are not tested; only samples are tested.

DC Allowable Operating Ranges at $T_a = -10\ \text{to}\ +70^\circ\text{C}$, $V_{CC} = 3.0\ \text{to}\ 3.6\ \text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{CC}		3.0	3.3	3.6	V
Input voltage	V_{IH}		$0.8V_{CC}$		$V_{CC} + 0.3$	V
	V_{IL}		-0.3*		$0.2V_{CC}$	V

Note: * The minimum value is -2.0 V for pulse widths under 30 ns.

LC35V256EM, ET70W

DC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 3.0 to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit		
			min	typ	max			
Input leakage current	I _{LI}	V _{IN} = 0 to V _{CC}	-1.0		+1.0	μA		
Output leakage current	I _{LO}	V _{CE} = V _{IH} or V _{OE} = V _{IH} or V _{WE} = V _{IL} V _{I/O} = 0 to V _{CC}	-1.0		+1.0	μA		
Output high-level voltage	V _{OH1}	I _{OH1} = -2.0 mA	V _{CC} - 0.4			V		
	V _{OH2}	I _{OH2} = -100 μA	V _{CC} - 0.1			V		
Output low-level voltage	V _{OL1}	I _{OL1} = 2.0 mA			0.4	V		
	V _{OL2}	I _{OL2} = 100 μA			0.4	V		
Operating current drain	CMOS inputs	I _{CCA2}	V _{CE} = V _{IL} , I _{I/O} = 0 mA, V _{IN} = V _{IH} or V _{IL}		1.2	mA		
		I _{CCA3}	V _{CE} = V _{IL} , V _{IN} = V _{IH} or V _{IL} I _{I/O} = 0 mA, DUTY 100 %	min cycle 1 μs cycle	20 1.5	25 2.5	mA mA	
Standby mode current drain	V _{CC} - 0.2 V/ 0.2 V inputs	I _{CCS1}	V _{CE} ≥ V _{CC} - 0.2 V, V _{IN} = 0 to V _{CC}	Ta ≤ 25°C	0.01		μA	
				Ta ≤ 60°C			0.8	μA
				Ta ≤ 70°C			4.0	μA
	CMOS inputs	I _{CCS2}	V _{CE} = V _{IH} , V _{IN} = 0 to V _{CC}			0.4	mA	

Note: * Reference values when V_{CC} = 3.3 V and Ta = 25°C.

AC Electrical Characteristics at Ta = -10 to +70°C, V_{CC} = 3.0 to 3.6 V

AC test conditions

Input pulse voltage levels: 0.2 V_{CC} to 0.8 V_{CC}

Input rise and fall times: 5 ns

Input and output timing levels: 1/2 V_{CC}

Output load: 30 pF (including the jig capacitance)

Read Cycle

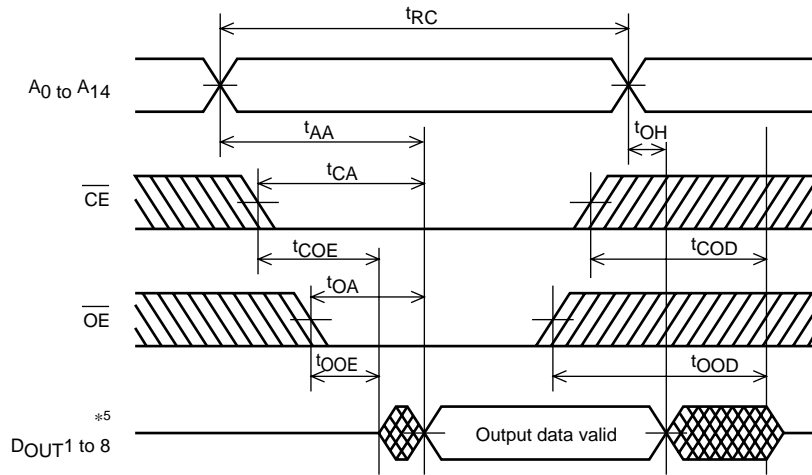
Parameter	Symbol	min	max	Unit
Read cycle time	t _{RC}	70		ns
Address access time	t _{AA}		70	ns
$\overline{\text{CE}}$ access time	t _{CA}		70	ns
$\overline{\text{OE}}$ access time	t _{OA}		50	ns
Output hold time	t _{OH}	10		ns
$\overline{\text{CE}}$ output enable time	t _{COE}	10		ns
$\overline{\text{OE}}$ output enable time	t _{OOE}	5		ns
$\overline{\text{CE}}$ output disable time	t _{COD}		35	ns
$\overline{\text{OE}}$ output disable time	t _{OOD}		30	ns

Write Cycle

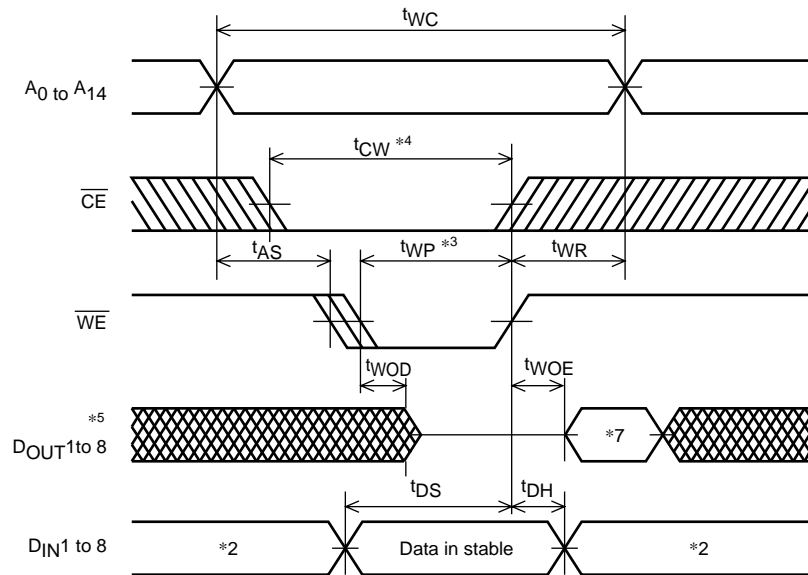
Parameter	Symbol	min	max	Unit
Write cycle time	t _{WC}	70		ns
Address setup time	t _{AS}	0		ns
Write pulse width	t _{WP}	55		ns
$\overline{\text{CE}}$ setup time	t _{CW}	60		ns
Write recovery time	t _{WR}	0		ns
$\overline{\text{CE}}$ write recovery time	t _{WR1}	0		ns
Data setup time	t _{DS}	50		ns
Data hold time	t _{DH}	0		ns
$\overline{\text{CE}}$ data hold time	t _{DH1}	0		ns
$\overline{\text{WE}}$ output enable time	t _{WOE}	5		ns
$\overline{\text{WE}}$ output disable time	t _{WOD}		35	ns

Timing Charts

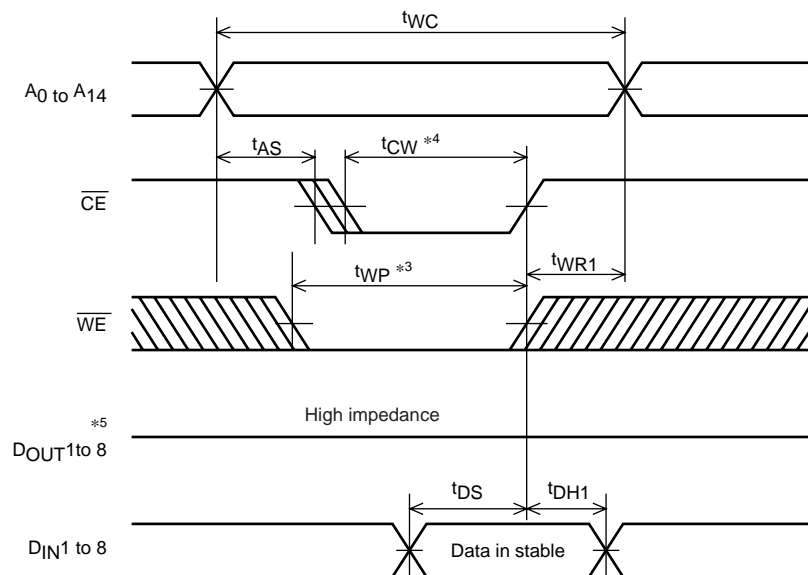
[Read cycle] *1



[Write cycle 1] ($\overline{\text{WE}}$ write) *6



[Write cycle 2] ($\overline{\text{CE}}$ write) *6



LC35V256EM, ET-70W

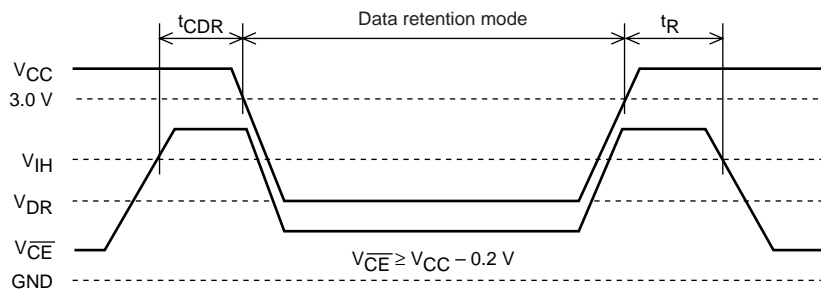
- Notes:
1. \overline{WE} must be held at the high level during the read cycle.
 2. Do not apply reverse phase signals to the DOUT pins when those pins are in the output state.
 3. The time t_{WP} is the period when both \overline{CE} and \overline{WE} are low. It is defined as the time from the fall of \overline{WE} to the rise of \overline{CE} or \overline{WE} , whichever occurs first.
 4. The time t_{CW} is the period when both \overline{CE} and \overline{WE} are low. It is defined as the time from the fall of \overline{CE} to the rise of \overline{CE} or \overline{WE} , whichever occurs first.
 5. The DOUT pins will be in the high-impedance state if any one of the following is held: \overline{OE} is at the high level, \overline{CE} is at the high level, or \overline{WE} is at the low level.
 6. The \overline{OE} pin must be either held high or held low during the write cycle.
 7. DOUT has the same phase as the write data during this write cycle.

Data Retention Characteristics at $T_a = -10$ to $+70^\circ\text{C}$

Parameter	Symbol	Conditions	min	max	Unit
Data retention supply voltage	V_{DR}	$V_{\overline{CE}} \geq V_{CC} - 0.2\text{ V}$	2.0	3.6	V
Chip enable setup time	t_{CDR}		0		ns
Chip enable hold time	t_R		t_{RC}^*		ns

Note: * t_{RC} : Read cycle time

Data Retention Waveforms (\overline{CE} control)



- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of January, 2000. Specifications and information herein are subject to change without notice.