Ordering number:ENN1802C

CMOS IC

LC6514B

Single-Chip 4-bit Microcontroller (Low-Threshold Input, On-Chip FLT Driver)

Overview

The LC6514B is a microcontroller with FLT drivers. It is identical with the LC6510C in the internal architecture and instruction set. Since the normal/low-threshold level of input port A can be selected by option and the on-chip pull-down resistor can be bitwise connected to the FLT driver by option, the number of external parts used in the user equipment can be minimized, reducing the cost considerably.

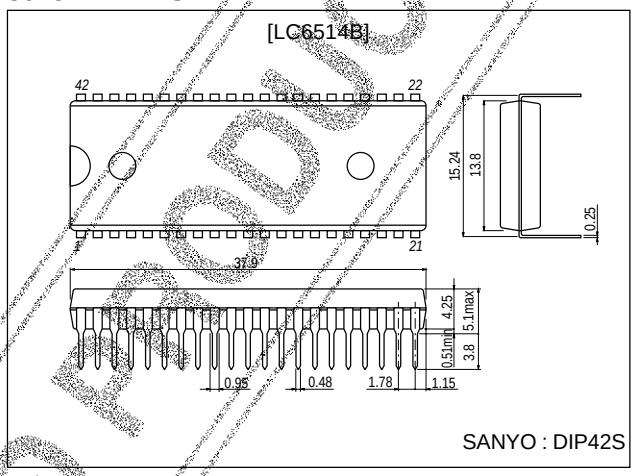
Features

- Low power dissipation.
- ROM capacity : 4096×8 bits.
- RAM capacity : 256×4 bits.
- Subroutine stack : 8 levels (common with interrupt).
- On-chip OSC circuit
  CR OSC : 800kHz typ.
  Ceramic OSC : 400kHz, 800kHz, 1000kHz
  External iuput : 1290kHz max.
- Power-down by 2 standby modes
  HALT mode : Power dissipation saving by program stadby during normal operation
  HOLD mode : Power supply backup during power failure.
- Input/output ports
  Input : 4 bits × 1 port
  3 bits × 1 port
  Input/output : 4 bits × 2 ports
  Output : 4 bits × 4 ports
  2 bits × 1 port
- Interrupt.
  External interrupt : 1
  Internal timer interrupt : 1
- On-chip 4-bit prescaler and 8-bit program timer.
- Instruction cycle time : 3.1μs (at 1290kHz)
- Supply voltage
  Normal operation : 4.0 to 6.0 V
  Memory hold : 1.8 to 6.0 V
- Instruction set common to the LC6502, LC6505 (BANK instruction added)

Package Dimensions

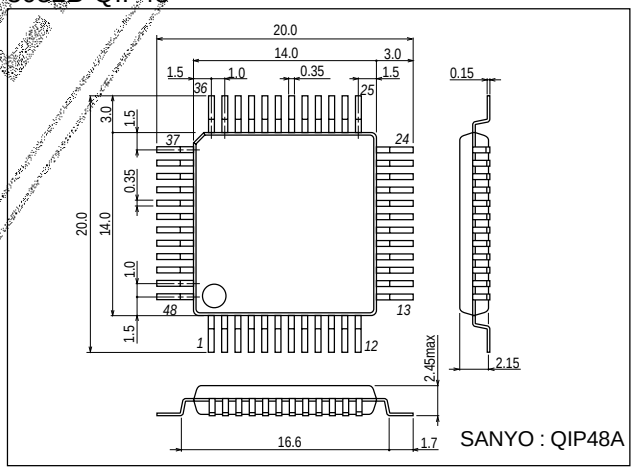
unit:mm

3025B-DIP42S



unit:mm

3052B-QIP48



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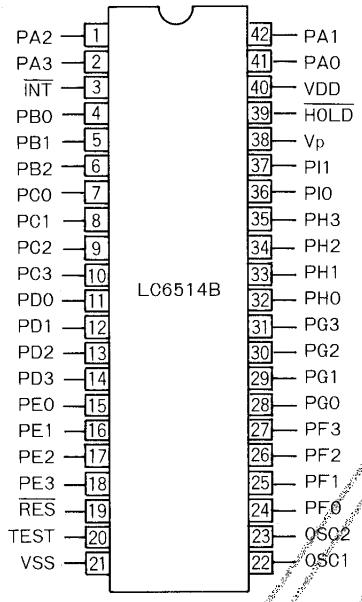
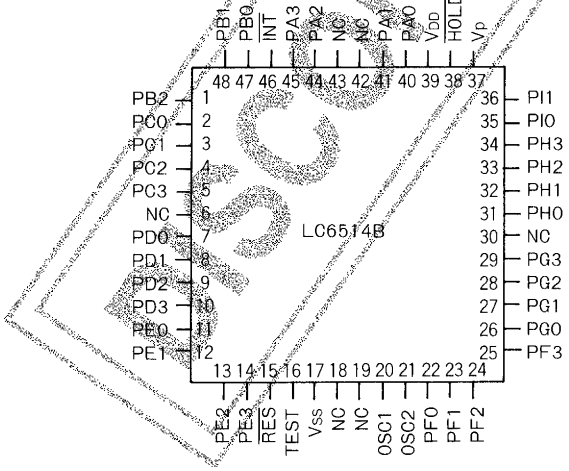
Note
The LC6514B heretofore in use has been improved by changing the value of the pull-down resistor to be contained in FLT drivers as shown below. When using the LC6514B, fully check that the new resistor value meets your application specifications.

Parameter		New resistor value			Old resistor value			Unit
		min	typ	max	min	typ	max	
L-level output current (Output pull-down resistance)	I_{OL} (R_{PD})	0.190 (200)	0.362 (105)	0.760 (50)	0.108 (350)	0.304 (125)	0.543 (70)	mA (kΩ)

Pin Assignment





Pin name

OSC1, OSC2 : C, R or ceramic resonator for system OSC
$\overline{INT}$: Interrupt
$\overline{RES}$: Reset
$\overline{HOLD}$: Hold
$PA_{0\ to\ 3}$: Input port $A_{0\ to\ 3}$
$PB_{0\ to\ 2}$: Input port $B_{0\ to\ 2}$
$PC_{0\ to\ 3}$: Input/output common port $C_{0\ to\ 3}$
$PD_{0\ to\ 3}$: Input/output common port $D_{0\ to\ 3}$
$PE_{0\ to\ 3}$: Output port $E_{0\ to\ 3}$
$PF_{0\ to\ 3}$: Output port $F_{0\ to\ 3}$
$PG_{0\ to\ 3}$: Output port $G_{0\ to\ 3}$
$PH_{0\ to\ 3}$: Output port $H_{0\ to\ 3}$
(With High-voltage driver)
$PI_{0, 1}$: Output port $I_{0, 1}$
TEST : TEST
V_P : Power supply for high-voltage port pull-down resistor

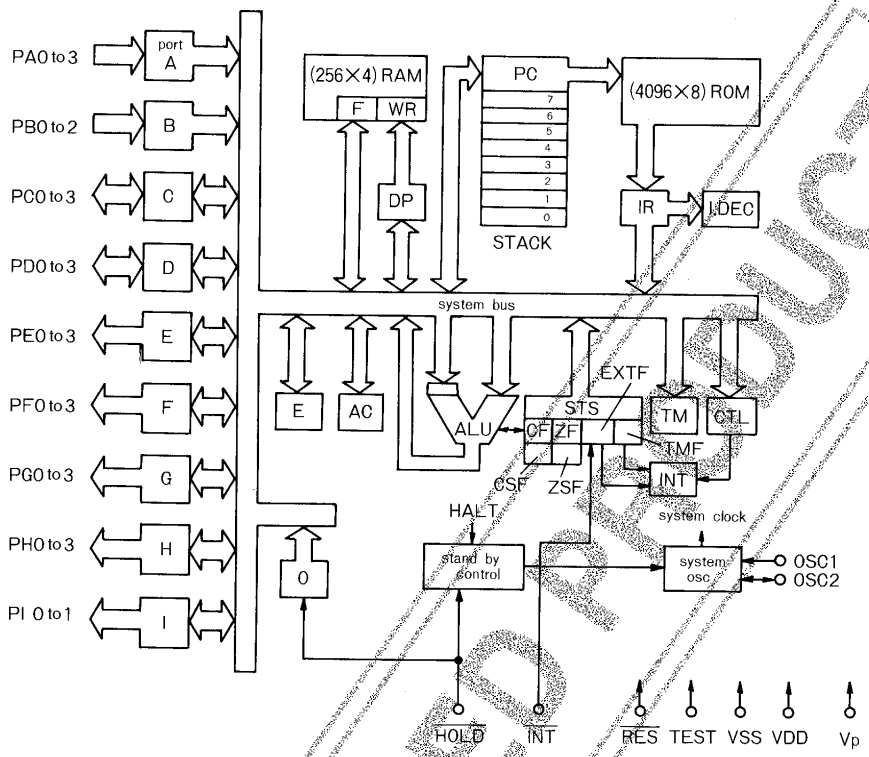
When mounting the QIP package version on the board, do not dip it in solder.

NC pin : No connection

Pin Function

Pin Name	Input/ Output	Function
$\overline{INT}$	Input	Interrupt request input pin.
$\overline{HOLD}$	Input	HOLD mode request input pin (Differs from the LC6502/05 in function.) Capable of being used as general-purpose single-bit input port unless the standby mode is used.
$\overline{RES}$	Input	Reset input pin.
$PA_{0 \text{ to } 3}$	Input	Input port A_0 to A_3 (Normal voltage). Capable of 4-bit input and single-bit decision for branch. Used also for HALT mode release request input. LOW threshold input for 4 bits selectable by option.
$PB_{0 \text{ to } 2}$	Input	Input port B_0 to B_2 (Normal voltage). Capable of 3-bit input and single-bit decision for branch.
$PC_{0 \text{ to } 3}$	Input/ Output	Input/output common port C_0 to C_3 (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
$PD_{0 \text{ to } 3}$	Input/ Output	Input/output common port D_0 to D_3 (Normal voltage). Capable of 4-bit input and single-bit decision for branch during input. Capable of 4-bit output and single-bit set/reset during output.
$PE_{0 \text{ to } 3}$	Output	Output port E_0 to E_3 (with high-voltage segment driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
$PF_{0 \text{ to } 3}$	Output	Output port F_0 to F_3 (with high-voltage segment driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
$PG_{0 \text{ to } 3}$	Output	Output port G_0 to G_3 (with high-voltage digit driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
$PH_{0 \text{ to } 3}$	Output	Output port H_0 to H_3 (with high-voltage digit driver). Capable of 4-bit output and single-bit set/reset. Capable of 4-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
$PI_{0, 1}$	Output	Output port I_0,I_1 (with high-voltage digit driver). Capable of 2-bit output and single-bit set/reset. Capable of 2-bit input of output latch contents and single-bit decision of output latch for branch. Use/nonuse of pull-down resistor bitwise selectable by option.
OSC1	Input	Pin for supplying external clock. If the internal clock mode is used, C, R or a ceramic resonator is connected to this pin and pin OSC2.
OSC2	Output	Pin for externally connecting a resonance circuit for the internal clock mode.
V_{DD}	Input	Power supply pin. Normally connected to +5V.
V_{SS}	–	Connected to 0V power supply.
VP	Input	Power supply for high-voltage port pull-down resistor.
TEST	Input	IC test pin. Normally connected V_{SS}(0V).

System Block Diagram



RAM :	Data memory	ROM :	Program memory
F :	Flag	PC :	Program counter
WR :	Working register	INT :	Interrupt control
AC :	Accumulator	IR :	Instruction resister
ALU :	Arithmetic and logic unit	I.DEC :	Instruction decoder
DP :	Data pointer	CF, CSF :	Carry flag Carry save flag
E :	E register		
CTL :	Control register	ZF, ZSF :	Zero flag Zero save flag
OSC :	Oscillator		
TM :	Timer	EXTF :	External interrupt request flag
STS :	Status register	TMF :	Internal interrupt request flag

Absolute Maximum Ratings at Ta = 25˚C, V_{SS}=0V (V_{DD}=5V±20% unless otherwise specified)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input voltage	V_{IN1}	Inputs other than Vp (Note 1)	–0.3 to V_{DD}+0.3	V
	V_{IN2}	V_P	V_{DD}–45 to V_{DD}+0.3	V
Output voltage	V_{OUT1}	Outputs other than ports E, F, G, H, I	–0.3 to V_{DD}+0.3	V
	V_{OUT2}	Ports E, F, G, H, I	V_{DD}–45 to V_{DD}+0.3	V
Peak output current	I_{O1}	Each pin of ports C, D	–2.0 to +2.0	mA
	I_{O2}	Each pin of ports E, F	–10 to 0	mA
	I_{O3}	Each pin of ports G, H, I	–15 to 0	mA
	I_{O4}	All pins of ports C to I	–90 to +16	mA
Allowable power dissopation	Pd max1	Dip package, Ta=–30 to +70°C	600	mW
	Pd max2	Flat package, Ta=–30 to +70°C	400	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C

Note 1: For pin OSC1, up to oscillation amplitude generated when internaly oscillated under the recommended oscillation conditions in Fig. 3 is allowable.

Recommended Operating Conditions at Ta = –30˚C to +70˚C, V_{SS} = 0V(V_{DD} = 4.0V to 6.0V unless otherwise specified)

Parameter	Symbol	Conditions	Rating			Unit
			min	typ	max	
Operating supply voltage	V_{DD}		4.0	5.0	6.0	V
Power-down supply voltage	V_{DD}MR	$\overline{HOLD}$=V_{IL4}, HOLD mode	1.8		6.0	V
H-level input votage	V_{IH1}	Ports A to D, port A : "normal threshold input"	0.7V_{DD}		V_{DD}	V
	V_{IH2}	V_{DD}=4.5 to 5.5V, port A : "low threshold input"	1.9		V_{DD}	V
	V_{IH3}	$\overline{INT}$, $\overline{RES}$, $\overline{HOLD}$, OSC1 pins	0.8V_{DD}		V_{DD}	V
L-level input votage	V_{IL1}	Ports A to D, port A : "normal threshold input"	V_{SS}		0.3V_{DD}	V
	V_{IL2}	V_{DD}=4.5 to 5.5V, port A : "low threshold input"	V_{SS}		0.5	V
	V_{IL3}	$\overline{INT}$, $\overline{RES}$, OSC1 pins	V_{SS}		0.2V_{DD}	V
	V_{IL4}	V_{DD}=1.8 to 6.0V, $\overline{HOLD}$, TEST pins	V_{SS}		0.2V_{DD}	V
Operating clock frequency	f_{extosc}	At external clock input, See Fig.1	222		1290	kHz
H-level clock pulse width	$t_{w\phi H}$		0.3			µs
L-level clock pulse width	$t_{w\phi L}$		0.3			µs
Clock input rise time	$t_{osc}R$				0.2	µs
Clock input fall time	$t_{osc}F$				0.2	µs
External capacitance for CR OSC	Cext	See Fig. 8			220±5%	pF
External resistance for CR OSC	Rext				6.8±1%	kΩ
External circuit constants for ceramic OSC	R1, R2 C1, C2	See Fig. 3				
Standby timing	t_{VDDR}	See Fig. 6, V_{DD}=1.8 to 6.0V	0			µs
	t_{VDDF}		0			µs
Allowable delay in	t_{DL}	See Fig. 9, 10.			(n-3)· Tc	µs
Key scan circuit	t_{DH}				(n-3)· Tc	µs

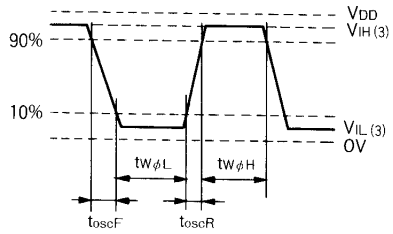


Fig. 1 OSC1 Pin input waveform

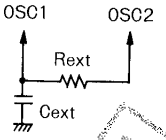
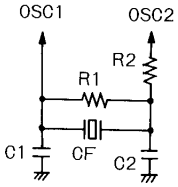


Fig. 2 Recommended Oscillator for CR OSC



CF : Ceramic resonator

CSB400P (Murata)
KBR400B (Kyocera)
CSB800K (Murata)
KBR800H (Kyocera)
CSB1000K (Murata)

Center Frequency	CF	C1(pF)	C2(pF)	R1(kΩ)	R2(kΩ)
400kHz	CSB400P(Murata)	470	470	1000	1.5
	KBR400B(Kyocera)	470	470	1000	1.5
800kHz	CSB800K(Murata)	220	220	1000	1.0
	KBR800H(Kyocera)	220	220	1000	1.0
		150	150	1000	1.5
1000kHz	CSB1000K(Murata)	100	100	1000	1.5

C1, C2 : Tolerance ±10%
R1, R2 : Tolerance ±5%

Fig. 3 Recommended Oscillator for Ceramic OSC

Electrical Characteristics at Ta = –30 to +70˚C, V_{DD}=5V±20%, V_{SS}=0V

Parameter	Symbol	Conditions	Rating min	Rating typ	Rating max	Unit
H-level iuput current	I_{IH}	All input pins except V_P, $V_{IN}=V_{DD}$			1	µA
L-level iuput current	I_{IL}	All input pins except V_P, $V_{IN}=V_{SS}$	–1			µA
H-level output votage	V_{OH1}	Ports C, D : I_{OH}=–1mA	V_{DD}–2.0			V
	V_{OH2}	Ports C, D : I_{OH}=–100µA	V_{DD}–0.5			V
	V_{OH3}	Ports E, F : I_{OH}=–2mA	V_{DD}–1.0			V
	V_{OH4}	Ports E, F : I_{OH}=–1mA, all ports I_{OH}=–1mA	V_{DD}–0.5			V
	V_{OH5}	Ports G, H, I : I_{OH}=–10mA	V_{DD}–1.8			V
	V_{OH6}	Ports G, H, I : I_{OH}=–2mA	V_{DD}–1.0			V
	V_{OH7}	Ports G, H, I : I_{OH}=–1mA, all ports I_{OH}=–1mA	V_{DD}–0.5			V
L-level output votage	V_{OL1}	Ports C, D: I_{OL}=1mA			0.4	V
	V_{OL2}	Ports E, F, G, H, I : V_P=–35V, output Tr OFF, output open, with pull-down resistor			–33	V
L-leve output current (Output pull-down resistor)	I_{OL} (R_{PD})	Ports E, F, G, H, I : V_P=–35V, V_{OL}=3V, V_{DD}=5V, with pull-down resistor	0.190 (200)	0.362 (105)	0.760 (20)	mA (kΩ)
Output OFF leak current	I_{OFF1}	Ports C, D : $V_{OUT}=V_{DD}$			1.0	µA
	I_{OFF2}	Ports C, D : $V_{OUT}=V_{SS}$	–1.0			µA
	I_{OFF3}	Ports E to I : $V_{OUT}=V_{DD}$, OD output			30	µA
	I_{OFF4}	Ports E to I : $V_{OUT}=V_{DD}$–40V, OD output	–30			µA
Clock OSC frequency for ceramic OSC	f_{CFOSC1}	Recommended conditions for ceramic OSC, at OSC circuit in Fig.3(Note 1)	384	400	416	kHz
	f_{CFOSC2}		768	800	832	kHz
	f_{CFOSC3}		960	1000	1040	kHz
Clock OSC frequency for CR OSC	f_{CROSC}	C_{ext}=220pF, R_{ext}=6.8kΩ, at OSC circuit in Fig. 2	600	800	1220	kHz
Current drain	I_{DD1}	At CR OSC, C_{ext}=220pF, R_{ext}=6.8kΩ, output pin open, input pin, $V_{IN}=V_{DD}$		1.0	2.0	mA
	I_{DD2}	At ceramic OSC (800kHz), output pin open, input pin, $V_{IN}=V_{DD}$		1.0	2.0	mA
	I_{DD3}	HALT mode, V_{DD}=4.0 to 6.0V, at test circuit in Fig. 4			10	µA
	I_{DD4}	HOLD mode, V_{DD}=1.8 to 6.0V, at test circuit in Fig. 5			10	µA
Input capacitance	C_{IN}	f=1MHz		5		pF
Output capacitance	C_{OUT}	f=1MHz, output : high impedance		10		pF
Input/output capacitance	C_{IO}			10		pF

(Note 1) f_{CFOSC} : Oscillatable frequency.

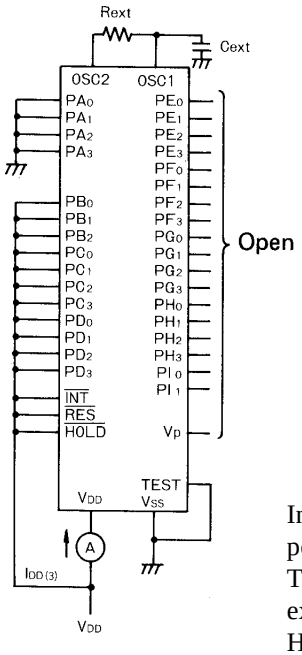


Fig. 4 I_{DD3} Test Circuit

Input/output common port C, D : Output inhibit
The HALT instruction is executed to csuse the HALT mode to be entered.

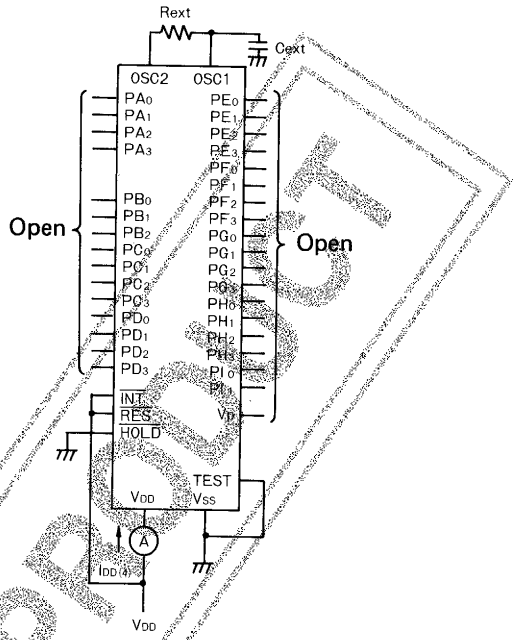


Fig. 5 I_{DD4} Test Circuit

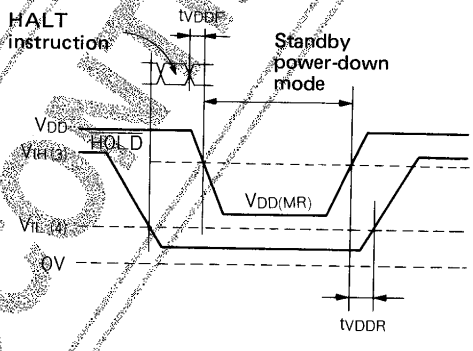
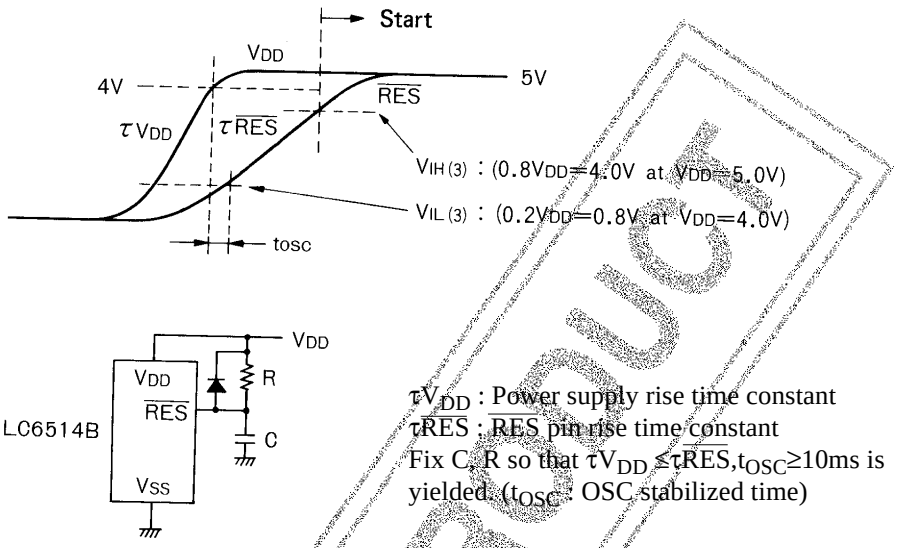


Fig. 6 Standby Mode Timing

(Note)
During the HALT instruction execution cycle, no chattering must be applied to the $\overline{\text{HOLD}}$ pin and $PA_{0\text{ to }3}$ pins.



τV_{DD} : Power supply rise time constant
$\tau\overline{RES}$: $\overline{RES}$ pin rise time constant
Fix C, R so that $\tau V_{DD} \leq \tau\overline{RES}, t_{OSC} \geq 10ms$ is yielded. (t_{OSC} : OSC stabilized time)

Fig. 7 Initial Reset Timing

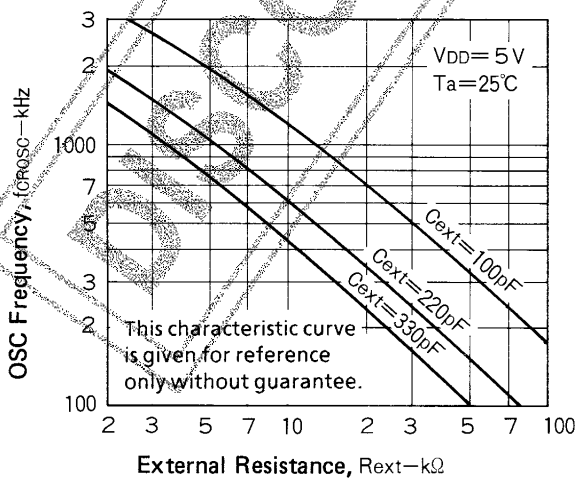
CR OSC characteristic of LC6514B

Fig. 8 shows the CR OSC characteristic of the LC6514B. For the variation range of CR OSC frequency of the LC6514B, the following is guaranteed at external consatants of Cext=220pF, Rext=6.8kΩ only. The outgoing inspection is performed under this condition only.

$$600kHz \leq f_{CROSC} \leq 1220kHz \quad \begin{pmatrix} Ta=-30°C \text{ to } +70°C \\ V_{DD}=4 \text{ to } 6V \end{pmatrix}$$

If any other constants than specified above are used, the range of Rext=5k to 50kΩ, Cext=100p to 300pF must be observed. (See Fig. 8.)

Fig. 8 $f_{CROSC.}$ – Rext



Note 1. The OSC frequency at V_{DD}=5V, Ta=25°C must be 800KHz or less.
Note 2. The OSC frequency at V_{DD}=4 to 6V, Ta=–30 to +70°C must be within the operation clock frequency range (222KHz to 1290 kHz).

Proper Cares in using the IC

[Digit drive signal-used key scan]

When key-scanning with the FLT digit drive signal in Fig. 9 and inputting the return signal to port A, the following must be observed.

(a) Estimate voltage drop (V_{ON}) in the output transistor using the current flowing in an FLT used and the V-1 characteristic of the output port of the LC6514B.
(b) Estimate voltage drop (V_{SW}) in the switch circuit.
(c) Check to see that ($V_{ON} + V_{SW}$) meets the V_{IH}/V_{IL} requirement of the input port.

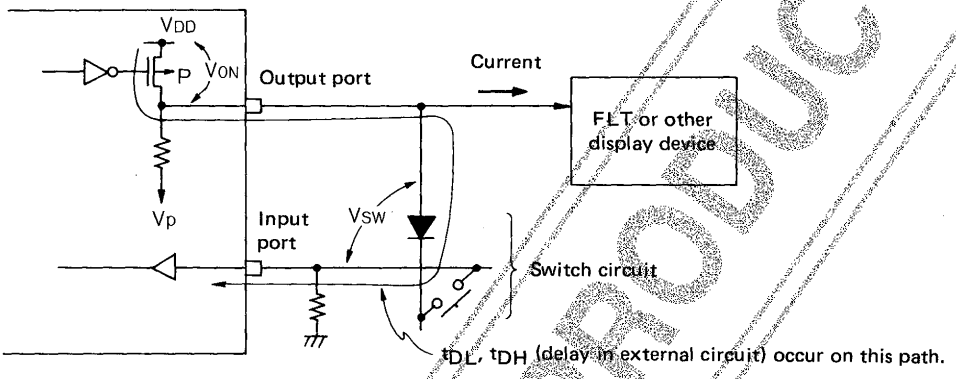
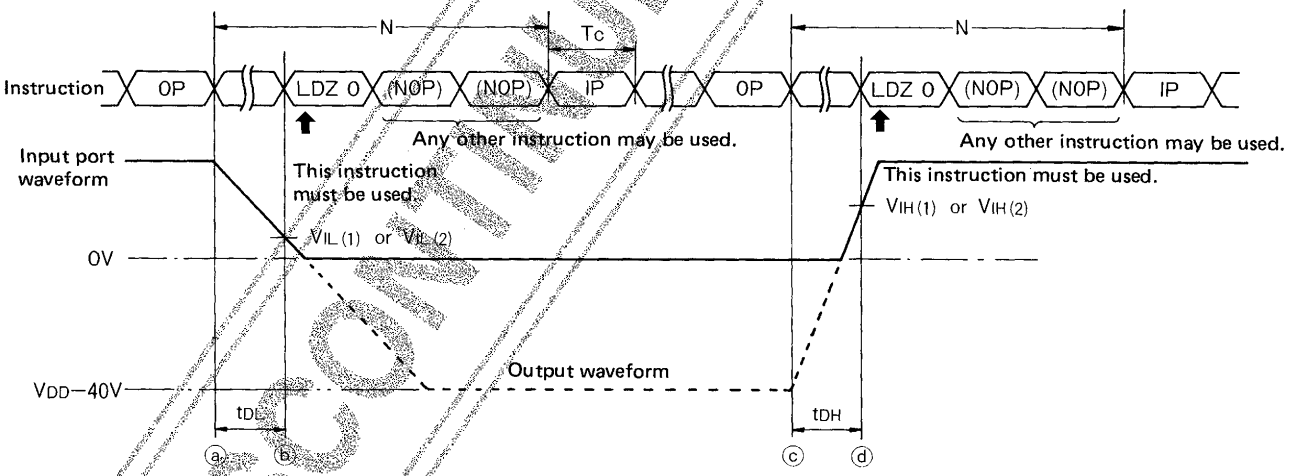


Fig. 9 Sample Key Scan Application

For the key scan application in Fig. 9, make the program considering the deley in the external circuit and the input delay shown below.



N : Number of instruction cycles existing between instruction (OP, SPB, RPB) used to output data to output port and insutruction (IP, BP, BNP) used to input data from input port. (Number of instruction cycles to be programmed according to the length of t_{DL}, t_{DH})

t_{DL}, t_{DH} : Delay in external circuit from output port to input port.

When the IP instruction is used to input the return signal as shown in Fig. 10, the input delay must be considered and three instructions are placed between the IP instruction and the crossing of input port waveform and V_{IL1} or V_{IL2}, VI_{H1} or V_{IH2}, respectively.

Some instructions must be placed additionally according to the length of delay (t_{DL}, t_{DH}) in the external circuit after the digit drive signal is delivered with the execution of the OP instruction (ⓐ and ⓒ).

<Notes for Standby Fuction Application>

[Proper cares in using standby function]

The LC6514B provides the standby function called HALT, HOLD mode to minimize the current drain when the program is in the wait state. The standby function is controlled by the HALT instruction, the $\overline{\text{HOLD}}$ pin, $\overline{\text{RES}}$ pin. A peripheral circuit and program must be so designed as to provide precise control of the standby function. In most applications where the standby function is performed, voltage regulation, instantaneous break of power, and external noise are not negligible. When designing an application circuit and program, whether or not to take some measures must be considered according to the extent to which these factors are allowed.

This section mainly describes power failure backup for which the satndby function is mostly used. A sample application circuit where the standby function is performed precisely is shown below and notes for circuit design and program design are also given below. When using the standby function, the application circuit shown below must be used and the notes must be also fully observed. If any other method than shown in this section is applied, it is necessary to fully check the environmental conditions such as power failure and the actual operation of an application equipment.

[Sample application and notes]

When using the HOLD mode, an appliacation circuit and program must be designed with the following in mind.

(1) The supply voltage at the standby state must not be less than specified.
(2) Input timing of each control signal ($\overline{\text{HOLD}}$, $\overline{\text{RES}}$ port A, $\overline{\text{INT}}$, etc.) at the standby initiate/release state.
(3) Release operation must not be overlapped at the time of execution of the HALT instruction.

A sample application where the standby function is used for power failure backup is shown below as a concrete method to observe these notes. A sample application circuit, its operation, and notes for program design are given below.

1. Sample application where the standby function is used for power failure backup.
   Power failure backup is an application where power failure of the main power source is detected by the $\overline{\text{HOLD}}$ pin, etc. to cause the HOLD mode to be entered so that the current drain is minimized and a backup capacitor is used to retain the contents of the internal registers even during power failure.

1-1. Sample application circuit (CF OSC)

Fig. 11 shows a CF OSC-applied circuit where the standby function is used for power failure backup.

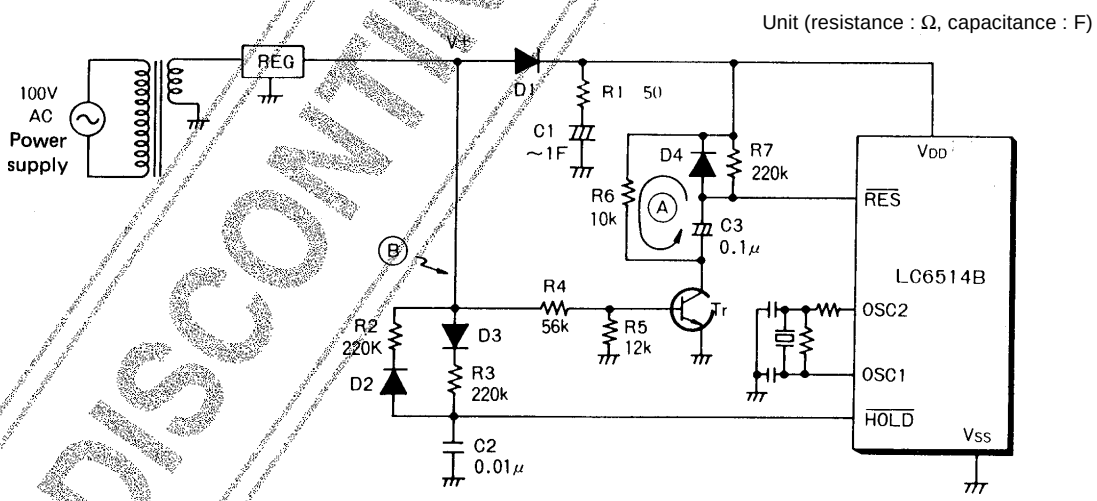
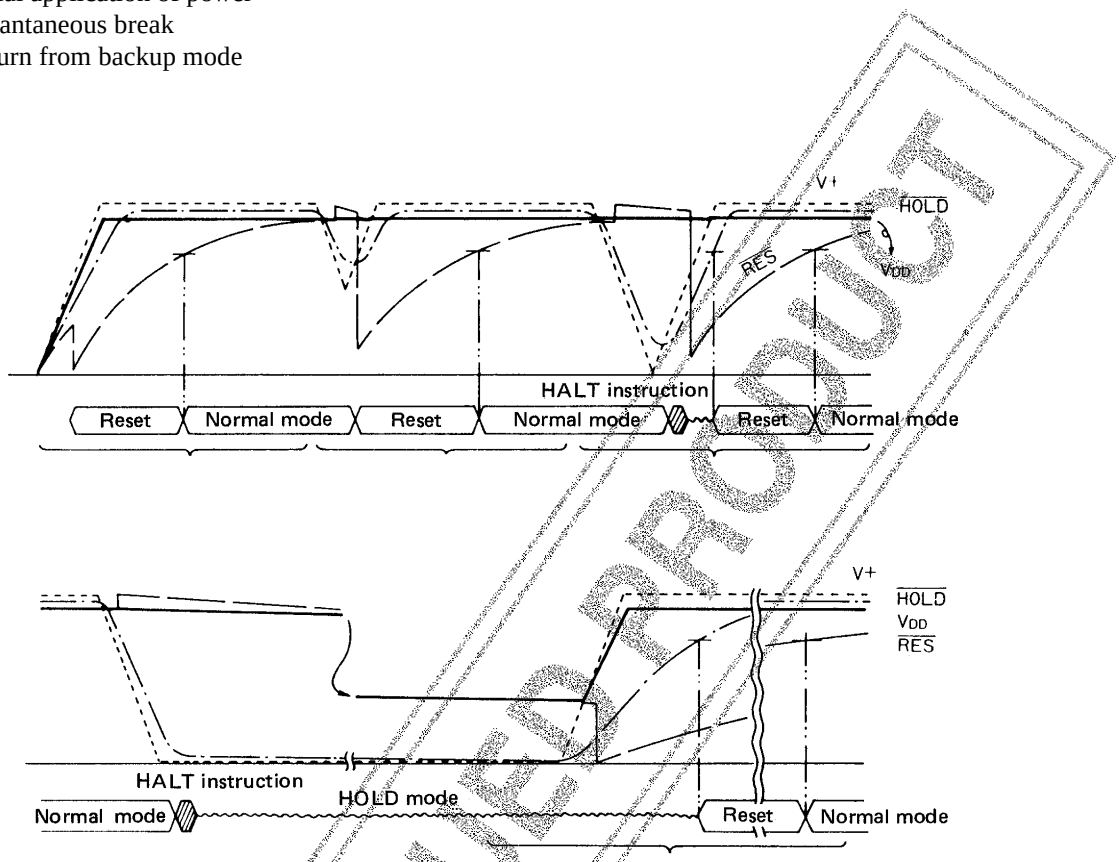


Fig. 11 Sample Application Circuit

1-2. Operating waveform

The operating waveform in the sample application circuit in Fig. 11 is shown below. The mode is roughly divided as follows.

① Initial application of power
② Instantaneous break
③ Return from backup mode



1-3. Operation of sample application circuit

① At the time of initial application of power
A reset occurs and the execution of the program starts at address 000H of the program counter (PC).

② At the time of instantaneous break
(1) At the time of very short instantaneous break
The execution of the program continues.
(2) At the time of instantaneous break being a little longer than (1)
(When the $\overline{RES}$ input voltage meets V_{IL} and $\overline{HOLD}$ input voltage does not meet V_{IL})
A reset occurs during the execution of the program and the execution of the program starts at address 000H of the program counter (PC).
Since the $\overline{HOLD}$ request signal is not applied to the $\overline{HOLD}$ pin, the HOLD mode is not entered.
(3) At the time of long instantaneous break (When both of the $\overline{RES}$ input voltage and $\overline{HOLD}$ input voltage meet V_{IL})
The $\overline{HOLD}$ request signal is applied to the $\overline{HOLD}$ pin and the HOLD mode is entered.
When V+ rises after instantaneous break, a reset occurs to release the HOLD mode and the execution of the program starts at address 000H of the program counter (PC).

③ At the time of return from backup voltage
A reset occurs and the execution of the program starts at address 000H of the program counter (PC).

1-4. Notes for circuit design

① How to fix C3, R6, C2, R2
Fix closed loop Ⓐ discharge time constants C3, R6 and $\overline{HOLD}$ pin charge time constants C2, R2 so that closed loop Ⓐ fully discharges before the $\overline{HOLD}$ input voltage gets lower than V_{IL} at the time of instantaneous break and the $\overline{RES}$ input voltage is sure to get lower than V_{IL} (a reset occurs) when V+ rises after instantaneous break where the $\overline{HOLD}$ input voltage gets lower than V_{IL}.

② How to fix C3, R7
Fix $\overline{RES}$ pin charge time constats C3, R7 so that when power is applied initially or the HOLD mode is released the CF OSC oscillates normally and the $\overline{RES}$ input voltage exceeds V_{IH} and the program starts running.

③ How to fix R4, R5
Fix Tr bias constants R4, R5 so that when V+ rises after instantaneous break the $\overline{RES}$ input voltage gets lower than V_{IL} (brought to L-level) befor the $\overline{HOLD}$ input voltage exceeds V_{IH} (brought to H-level).

④ How to fix C2, R3
Fix $\overline{HOLD}$ pin charge time constants C2, R3 so that when the HOLD mode is released from the backup mode the $\overline{HOLD}$ input voltage does not exceed V_{IH} (not brought to H-level) until the $\overline{RES}$ input voltage gets lower than V_{IL}(brought to L-level).
Fix C3, R7 and C2, R3 so that the time interval from the moment the $\overline{HOLD}$ input voltage exceeds V_{IH} until the $\overline{RES}$ input voltage exceeds V_{IH} is longer than the CF OSC stabilizing time.

⑤ When the load is heavy or the polling interval is long
Since C1 discharges largely, increase the capacity of C1 or separate Ⓑ detection from V+ and use a power supply or signal that rises faster than V+.

1-5. Notes for software design

When the HOLD request signal is detected, the HALT instruction is executed immediately. A concrete example is shown below.

① An interrupt is inhibited before polling the HOLD request pin ($\overline{HOLD}$ pin).
② Polling of the $\overline{HOLD}$ pin and the HALT instruction are programmed consecutively.
[Concrete example]

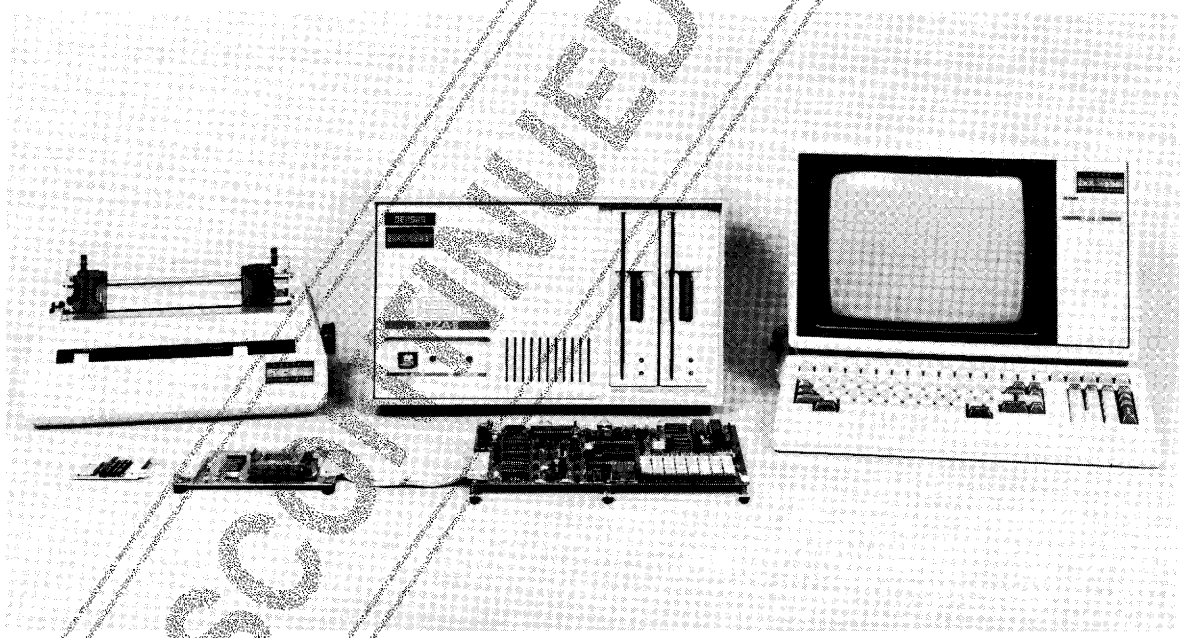
```
            :
            :
            :
        RCTL    3       ; EXTEN, TMEN←0 (External, timer interrupt intibit)
        BPO     AAA     ; Polling of the HOLD pin (If H-level, a branch occurs to AAA.)
        HALT            ; The HOLD mode is entered.
            :
            :
AAA :       :
```

Application development tools

Evaluation chip (LC6597), simulation chip (LC65PG97) and the dedicated equipment called “applicaction development tools” are available to facilitate application development of the LC6514B.

- SDS-410 system
  This is combination of floppy disk-provided CPU, CRT, and priter. This system enables application deveropment programs of microcomputers to be prepared (edited, assembled) very speedily and efficiently in assembly language. By connecting the EVA-410 to the CPU, programs can be debugged and assembled data can be written into the EPROM (using EPROM WRITER function contained in the EVA-410).
- EVA-410
  This is an evaluation kit having EPROM WRITER function, function of parallel/serial data communication with external equipment (SDS-410, etc.). This kit enables application development programs to be corrected or debugged on the machine language level.
- EVA-TB3B
  This is board which is connected with the EVA-410 to develop programs dedicated to the LC6514B.
- EVA-97-14B
  Simulation chip (LC65PG97) is identical with the LC6510C in the I/O port breakdown voltage and pin assignment. Since the LC6514B has high-voltage output ports and differs partially in the pin assignment, conversion board “EVA-97-14B” with high-voltage drivers is used to evaluate the LC6514B.

(Note) The threshold level of input port A of the LC6514B can be selected to be normal/low level by option. However, since port A of the EVA-TB3B, EVA-97-14B is of normal threshold input type, they cannot be used to evaluate the low threshold input version of the LC6514B.



APPENDIX LC6510 Series Instruction Set (by Function)

Symbols	Meaning				
AC :	Accumulator	M :	Memory	ZF :	Zero flag
ACt :	Accmulator bit t	M (DP) :	Memory addressed by DP	( ), [ ] :	Contents
CF :	Carry flag	P (DP_L) :	Input/output port addressed by DP_L	←:	Transfer and direction
CTL :	Control register	PC :	Program counter	+ :	Addition
DP :	Data pointer	STACK :	Stack register	– :	Subtraction
E :	E register	TM :	Timer	∧:	AND
EXTF :	External interrupt request flag	TMF :	Timer (internal) interrupt request flag	∨:	OR
Fn :	Flag bit n	At, Ha, La :	Working resister	⊻:	Exclusive OR

Instructions	Mnemonic		Instuction code $D_7D_6D_5D_4$	Instuction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Accumulator manipulation instructions	CLA	Clear AC	1 1 0 0	0 0 0 0	1	1	AC←0	The AC contents are cleared.	ZF	*1
	CLC	Clear CF	1 1 1 0	0 0 0 1	1	1	CF←0	The CF is reset.	CF	
	STC	Set CF	1 1 1 1	0 0 0 1	1	1	CF←1	The CF is set.	CF	
	CMA	Complement AC	1 1 1 0	1 0 1 1	1	1	AC←$\overline{(AC)}$	The AC contents are complemented (zero bits become 1, one bits become 0).	ZF	
	INC	Increment AC	0 0 0 0	1 1 1 0	1	1	AC←(AC)+1	The AC contents are incremented +1.	ZF CF	
	DEC	Decrement AC	0 0 0 0	1 1 1 1	1	1	AC←(AC)–1	The AC contents are decremented –1.	ZF CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0←(CF), $ACn+1$←(ACn), CF←(AC_3)	The AC contents are shifted left through the CF.	ZF CF	
	TAE	Transfer AC to E	0 0 0 0	0 0 1 1	1	1	E←(AC)	The AC contents are transferred to the E.		
	XAE	Exchange AC with E	0 0 0 0	1 1 0 1	1	1	AC↔(E)	The AC contents and the E contents are exchanged.		
Memory manipulation instructions	INM	Increment M	0 0 1 0	1 1 1 0	1	1	M (DP)←[M (DP)]+1	The M (DP) contents are incremented +1.	ZF CF	
	DEM	Decrement M	0 0 1 0	1 1 1 1	1	1	M (DP)←[M (DP)]–1	The M (DP) contents are decremented –1.	ZF CF	
	SMB bit	Set M data bit	0 0 0 0	1 0 B_1B_0	1	1	M (DP) B_1B_0←1	A single bit of the M (DP) specified by B_1, B_0 is set.		
	RMB bit	Reset M data bit	0 0 1 0	1 0 B_1B_0	1	1	M (DP) B_1B_0←0	A single bit of the M (DP) specified by B_1, B_0 is set.	ZF	
Operation/comparison instructions	AD	Add M to AC	0 1 1 0	0 0 0 0	1	1	AC←(AC)+[M (DP)]	The AC contents and the M (DP) contents are binary-added and the result is placed in the AC.	ZF CF	
	ADC	Add M to AC with CF	0 0 1 0	0 0 0 0	1	1	AC←(AC)+[M (DP)]+(CF)	The AC, CF, M (DP) contents are binary-added and the result is placed in the AC.	ZF CF	
	DAA	Decimal adjust AC in addition	1 1 1 0	0 1 1 0	1	1	AC←(AC)+6	6 is added to the AC contents.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 1 0	1 0 1 0	1	1	AC←(AC)+10	10 is added to the AC contents.	ZF	
	EXL	Exclusive or M to AC	1 1 1 1	0 1 0 1	1	1	AC←(AC) ⊻ [M (DP)]	The AC contents and the M (DP) contents are exelusive-ORed and the result is placed in the AC.	ZF	
	AND	And M to AC	1 1 1 0	0 1 1 1	1	1	AC←(AC)∧[M (DP)]	The AC contents and the M (DP) contents are ANDed and the result is placed in the AC.	ZF	
	OR	Or M to AC	1 1 1 0	0 1 0 1	1	1	AC←(AC) V [M (DP)]	The AC contents and the M (DP) contents are ORed and the result is placed in the AC.	ZF	
	CM	Compare AC with M	1 1 1 1	1 0 1 1	1	1	$\overline{[M (DP)]}$+ (AC)+1	The AC contents and the M (DP) contents are compared and the CF and ZF are set/reset.	ZF CF	
	CI data	Compare AC with immediate data	0 0 1 0 0 1 0 0	1 1 0 0 I_3 I_2 I_1 I_0	2	2	$\overline{I_3\ I_2\ I_1\ I_0}$+ (AC)+1	The AC contents and immediate data I_3 I_2 I_1 I_0 are compared and the ZF and CF are set/reset.	ZF CF	
	CLI data	Compare DP_L with immediate data	0 0 1 0 0 1 0 1	1 1 0 0 I_3 I_2 I_1 I_0	2	2	$(DP_L)\forall I_3\ I_2\ I_1\ I_0$	The DPL contents and immediate data I_3 I_2 I_1 I_0 are compared.	ZF	

Comparison result	CF	ZF
[M(DP)] > (AC)	0	0
[M(DP)] = (AC)	1	1
[M(DP)] < (AC)	1	0

Comparison result	CF	ZF
$I_3I_2I_1I_0$> (AC)	0	0
$I_3I_2I_1I_0$ = (AC)	1	1
$I_3I_2I_1I_0$< (AC)	1	0

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Instructions	Mnemonic		Instuction code $D_7D_6D_5D_4$	Instuction code $D_3D_2D_1D_0$	Bytes	Cycles	Function	Description	Status flag affected	Remarks
Load/store instructions	LI data	Load AC with immediate data	1 1 0 0	I_3 I_2 I_1 I_0	1	1	AC←I_3 I_2 I_1 I_0	Immediate data I_3 I_2 I_1 I_0 is loaded in the AC.	ZF	*1
	S	Store AC to M	0 0 0 0	0 0 1 0	1	1	M (DP)←AC	The AC contents are stored in the M(DP).		
	L	Load AC from M	0 0 1 0	0 0 0 1	1	1	AC←[M (DP)]	The M(DP) contents are loaded in the AC.	ZF	
	XM data	Exchange AC with M. then modify DP_H with immediate data	1 0 1 0	0 M_2 M_1 M_0	1	2	(AC)↔[M (DP)] DP_H←(DP_H) $\forall$ 0 M_2 M_1 M_0	The AC contents and the M(DP) contents are exchanged. Then, the DP_H contents are modified with the contents of (DP_H)$\forall$ 0$M_2M_1M_0$.	ZF	The ZF is set/reset according to the result of (DP_H) $\forall$ 0$M_2M_1M_0$.
	X	Exchange AC with M	1 0 1 0	0 0 0 0	1	2	(AC)↔[M (DP)]	The AC contents and the M(DP) contents are exchanged.	ZF	The ZF is set/reset according to the DP_H contents at the time of instruction execution.
	XI	Exchange AC with M. then increment DP_L	1 1 1 1	1 1 1 0	1	2	(AC)↔[M (DP)] DP_L←(DP_L) +1	The AC contents and the M(DP) contents are exchanged. Then, the DP_L contents are incremented +1.	ZF	The ZF is set/reset according to the result of (DP_L+1).
	XD	Exchange AC with M. then decrement DP_L	1 1 1 1	1 1 1 1	1	2	(AC)↔[M (DP)] DP_L←(DP_L) –1	The AC contents and the M(DP) contents are exchanged. Then, the DP_L contents are decremented –1.	ZF	The ZF is set/reset according to the result of (DP_L–1).
	RTBL	Read table data from program ROM	0 1 1 0	0 0 1 1	1	2	AC, E←ROM (PCh, E, AC)	The contents of ROM addressed by the PC whose low-order 8 bits are replaced with the E and AC contents are loaded in the AC and E.		
Data pointer manipulation instructions	LDZ data	Load DP_H with Zero and DP_L with immediate data respectively	1 0 0 0	I_3 I_2 I_1 I_0	1	1	DP_H←0 DP_L←I_3 I_2 I_1 I_0	The DP_H and DP_L are loaded with 0 and immediate data I_3 I_2 I_1 I_0 respectively.		
	LHI data	Load DP_H with immediate data	0 1 0 0	I_3 I_2 I_1 I_0	1	1	DP_H←I_3 I_2 I_1 I_0	The DP_H is loaded with immediate data I_3 I_2 I_1 I_0.		
	IND	Increment DP_L	1 1 1 0	1 1 1 0	1	1	DP_L←(DP_L) +1	The DP_L contents are incremented +1.	ZF	
	DED	Decrement DP_L	1 1 1 0	1 1 1 1	1	1	DP_L←(DP_L) –1	The DP_L contents are incremented –1.	ZF	
	TAL	Transfer AC to DP_L	1 1 1 1	0 1 1 1	1	1	DP_L←(AC)	The AC contents are transferred to the DP_L.		
	TLA	Transfer DP_L to AC	1 1 1 0	1 0 0 1	1	1	AC←(DP_L)	The DP_L contents are transferred to the AC.	ZF	
	XAH	Exchange AC with DP_H	0 0 1 0	0 0 1 1	1	1	(AC)↔(DP_H)	The AC contents and the DP_H contents are exchanged.		
Working register manipulation instructions	XAt XA0 XA1 XA2 XA3	Exchange AC with working register At	1 1 1 0 1 1 1 0 1 1 1 0 1 1 1 0	t1 t0 0 0 0 1 1 0 1 1	1 1 1 1	1 1 1 1	(AC)↔(A0) (AC)↔(A1) (AC)↔(A2) (AC)↔(A3)	The AC contents and the contents of working register A0, A1, A2, or A3 specified by t1 t0 are exchanged.		
	XHa XH0 XH1	Exchange DP_H with working register Ha	1 1 1 1 1 1 1 1	a 0 1	1 1	1 1	(DP_H)↔(H0) (DP_H)↔(H1)	The DP_H contents and the contents of working register H0 or H1 specified by a are exchanged.		
	XLa XL0 XL1	Exchange DP_L with working register La	1 1 1 1 1 1 1 1	a 0 1	1 1	1 1	(DP_L)↔(L0) (DP_L)↔(L1)	The DP_L contents and the contents of working register L0 or L1 specified by a are exchanged.		
Flag manipulation intructions	SFB flag	Set flag bit	0 1 0 1	$B_3B_2B_1B_0$	1	1	Fn←1	A flag specified by $B_3B_2B_1B_0$ is set.		
	RFB flag	Reset flag bit	0 0 0 1	$B_3B_2B_1B_0$	1	1	Fn←0	A flag specified by $B_3B_2B_1B_0$ is reset.	ZF	The flags are divided into 4 groups of F0 to F3, F4 to F7, F8 to F11, F12 to F15. The ZF is set/reset according to the 4 bits including a single bit specified by immediate data $B_3B_2B_1B_0$.
Jump/subroutine instructions	JMP addr	Jamp in the current bank	0 1 1 0 $P_7P_6P_5P_4$	1 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC←PC_{11}(or $\overline{PC_{11}}$) $P_{10}P_9P_8P_7P_6$ $P_5P_4P_3P_2P_1P_0$	A jump to an address spesified by the PC_{11} (or $\overline{PC_{11}}$) and immediate data P_{10} to P_0 occurs.		If the BANK and JMP instructions are executed consecutively, $\overline{PC_{11}}$→PC_{11}
	JPEA	Jamp in the current page modified by E and AC	1 1 1 1	1 0 1 0	1	1	PC_7 to 0←(E, AC)	A jump to an address spesified by the contents of the PC whose low-order 8bits are replaced with the E and AC contents occurs.		
	CZP addr	Call subroutine in the zero page	1 0 1 1	$P_3P_2P_1P_0$	1	1	STACK←(PC) +1 PC_{11} to 6, PC_1 to 0←0 PC_5 to 2←$P_3P_2P_1P_0$	A subroutine in page 0 of bank 0 is called.		
	CAL addr	Call subroutine in the zero bank	1 0 1 0 $P_7P_6P_5P_4$	1 $P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	STACK←(PC) +2 PC_{11} to 0←0$P_{10}P_9P_8$ $P_7P_6P_4P_3P_2P_1P_0$	A subroutine in bank 0 is called.		
	RT	Return from subroutine	0 1 1 0	0 0 1 0	1	1	PC←(STACK)	A return from a subroutine occurs.		
	RTI	Return from interrrupt routine	0 0 1 0	0 0 1 0	1	1	PC←(STACK) CF ZF←CSF, ZSF	A return from an interrupt servicing routine occurs.	ZF CF	
	BANK	Change bank	1 1 1 1	1 1 0 1	1	1	PC_{11}←($\overline{PC_{11}}$)	The bank is changed.		Effective only when used immediately before the JMP instruction.

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Instructions	Mnemonic		Instuction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Branch instructions	BAt addr	Branch on AC bit	0 1 1 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt =1	If a single bit of the AC specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BA0 to BA3 according to the value of t.
	BNAt addr	Branch on no AC bit	0 0 1 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ACt =0	If a single bit of the AC specified by immediate data t_1t_0 is 0 a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNA0 to BNA3 according to the value of t.
	BMt addr	Branch on M bit	0 1 1 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [M (DP, t_1t_0)]=1	If a single bit of the M(DP) specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BM0 to BM3 according to the value of t.
	BNMt addr	Branch on no M bit	0 0 1 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [M (DP, t_1t_0)]=0	If a single bit of the M(DP) specified by immediate data t_1t_0 is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNM0 to BNM3 according to the value of t.
	BPt addr	Branch on Port bit	0 1 1 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [P (DP_L, t_1t_0)]=1	If a single bit of port P(DP_L) specified by immediate data t_1t_0 is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BP0 to BP3 according to the value of t.
	BNPt addr	Branch on no Port bit	0 0 1 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if [P (DP_L, t_1t_0)]=0	If a single bit of port P(DP_L) specified by immediate data t_1t_0 is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNP0 to BNP3 according to the value of t.
	BTM addr	Branch on timer	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF =1 then TMF←0	If the TMF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The TMF is reset.	TMF	
	BNTM addr	Branch on no timer	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if TMF =0 then TMF←0	If the TMF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The TMF is reset.	TMF	
	BI addr	Branch on interrupt	0 1 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if EXTF =1 then XETF←0	If the EXTF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The EXTF is reset.	EXTF	
	BNI addr	Branch on no interrupt	0 0 1 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if EXTF =0 then XETF←0	If the EXTF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs. The EXTF is reset.	EXTF	
	BC addr	Branch on CF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF =1	If the CF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BNC addr	Branch on no CF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 1 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if CF =0	If the CF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BZ addr	Branch on ZF	0 1 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF =1	If the ZF is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BNZ addr	Branch on no ZF	0 0 1 1 $P_7P_6P_5P_4$	1 1 1 0 $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if ZF =0	If the ZF is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		
	BFn addr	Branch on flag bit	1 1 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if Fn =1	If the flag bit of the 16 flags specified by immediate data $n_3n_2n_1n_0$ is 1, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BF0 to BF15 according to the value of n.
	BNFn addr	Branch on no flag bit	1 0 0 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	$PC_{7\text{ to }0}\leftarrow P_7P_6P_5P_4P_3P_2P_1P_0$ if Fn =0	If the flag bit of the 16 flags specified by immediate data $n_3n_2n_1n_0$ is 0, a branch to an address specified by immediate data P_7 to P_0 within the current page occurs.		Mnemonic is BNF0 to BNF15 according to the value of n.
Input/output instructions	IP	Input port to AC	0 0 0 0	1 1 0 0	1	1	AC←[P(DP_L)]	The contnts of port P (DP_L) are inputted to the AC.	ZF	
	OP	Output AC to port	0 1 1 0	0 0 0 1	1	1	P(DP_L)← AC	The AC contnts are outputted to port P (DP_L).		
	SPB bit	Set port bit	0 0 0 0	0 1 B_1B_0	1	2	P(DP_L, B_1B_0)←1	Immediate data B_1B_0-specified one bit in poirt P(DP_L) is set		Mnemonic is BNF0 to BNF15 according to the value of n.
	RPB bit	Reset port bit	0 0 1 0	0 1 B_1B_0	1	2	P(DP_L, B_1B_0)←0	Immediate data B_1B_0-specified one bit in poirt P(DP_L) is reset	ZF	When this instruction is executed, the E register contents are destroyed.

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Continued from preceding page.

Instructions	Mnemonic		Instuction code		Bytes	Cycles	Function	Description	Status flag affected	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Other instructions	SCTL bit	Set control register bit (S)	0 0 1 0 1 0 0 0	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL←(CTL) V $B_3B_2B_1B_0$	Immediate data $B_3B_2B_1B_0$-specified bits in the control register are set.		
	RCTL bit	Reset control register bit (S)	0 0 1 0 1 0 0 1	1 1 0 0 $B_3B_2B_1B_0$	2	2	CTL←(CTL) ^ $\overline{B_3B_2B_1B_0}$	Immediate data $B_3B_2B_1B_0$-specified bits in the control register are reset.	ZF	
	WTTM	Write timmer	1 1 1 1	1 0 0 1	1	1	TM←(E), (AC) TMF←0	The E and AC contents are loaded in the timer. The TMF is reset.	TMF	
	HALT	Halt	1 1 1 1	0 1 1 0	1	1	Halt	The standby mode is entered.		
	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	No operation is performed, but 1 machine cycle is consumed.		

*1 If the L1 instruction or CLA instruction is used consecutively in such a manner as LI, LI, LI, -----, or CLA, CLA, CLA,-----, the first LI instruction or CLA instruction only is effective and the following LI instructions or CLA instructions are changed to the NOP instructions.