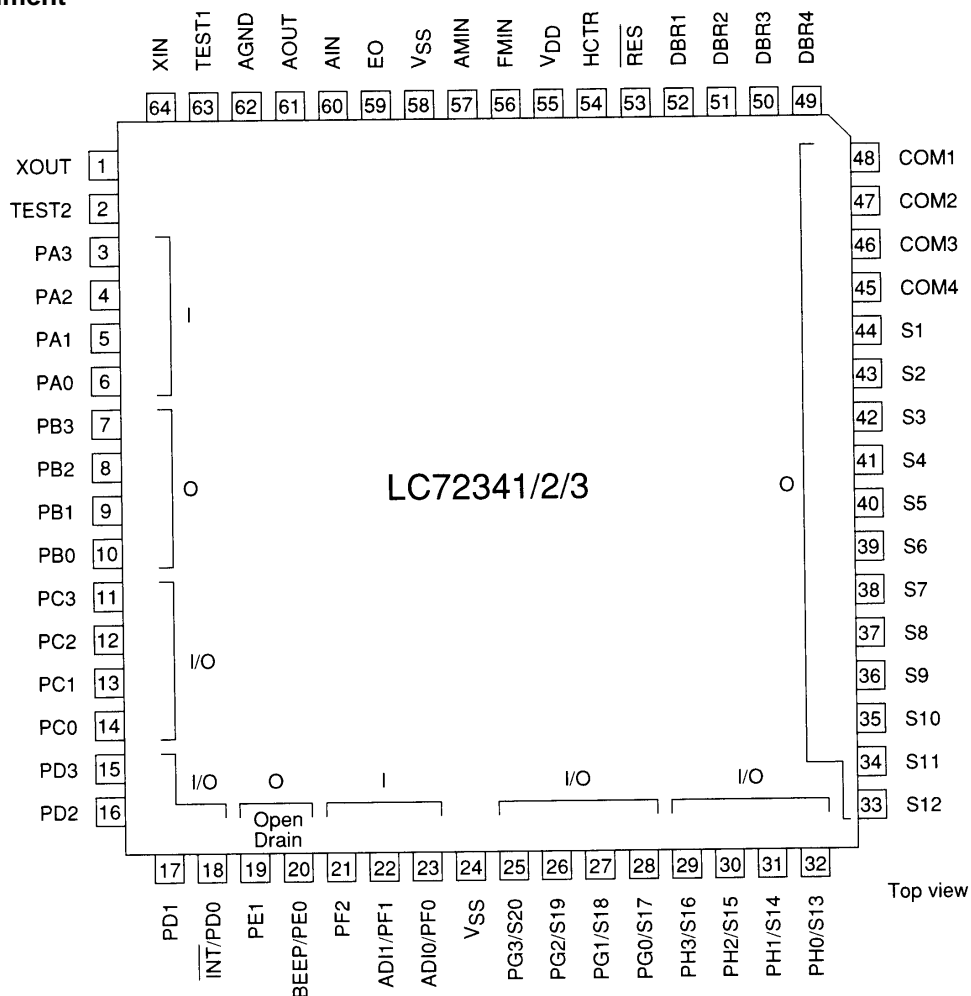


LC72341G/W, 72342G/W, 72343G/W

- IF counter
 - HCTR input pin; 0.4 to 12 MHz
- Voltage detection circuit (VSENSE)
 - Detects the V_{DD} voltage and sets a flag
- External reset pin
 - Restarts execution from location 0 when the CPU and PLL circuits are operating
- Power on reset circuit
 - Starts execution from location 0 at power on.
- Universal counter
 - 20 bits
- Beep tones
 - 3.1 and 1.5 kHz
- Halt mode: The microcontroller operating clock is stopped
- Backup mode: The crystal oscillator is stopped
- An amplifier for a low-pass filter is built in
- CPU and PLL circuit operating voltage
 - 1.8 to 3.6 V
- RAM data retention voltage
 - 1.0 V or higher
- Packages
 - QIP-64G : 0.8-mm lead pitch
 - SQFP-64 : 0.5-mm lead pitch

Pin Assignment



* PE0 and PE1 are open-drain outputs.

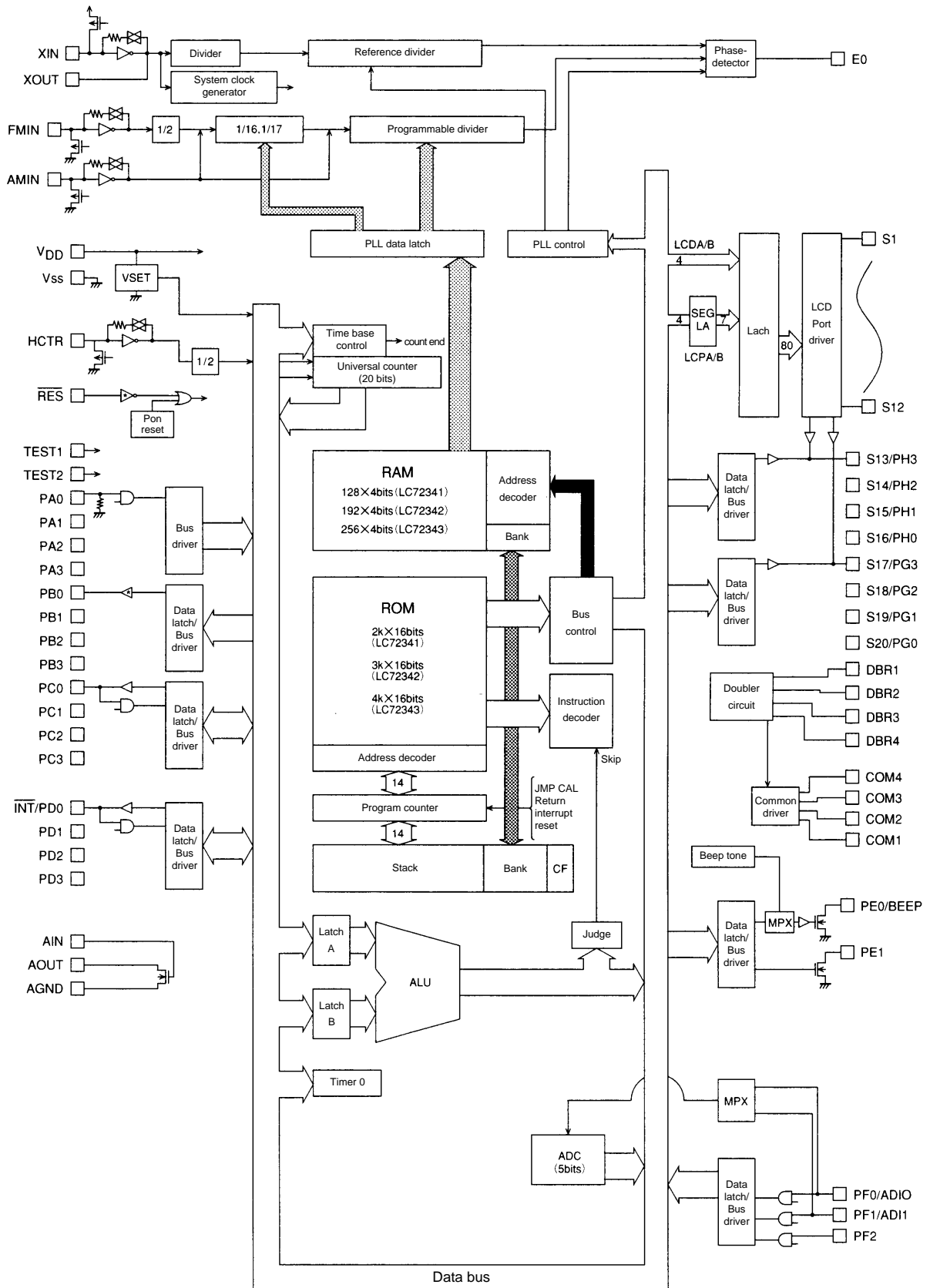
* The I/O ports can be set to input or output individually.

* The functions of the segment/general-purpose ports can be set in bit units.

A09866

LC72341G/W, 72342G/W, 72343G/W

Block Diagram



A09867

LC72341G/W, 72342G/W, 72343G/W

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD\text{ max}}$		-0.3 to +4.0	V
Input voltage	V_{IN}	All input pins	-0.3 to $V_{DD} + 0.3$	V
Output voltage	V_{OUT1}	AOUT, PE	-0.3 to +15	V
	V_{OUT2}	All output pins except V_{OUT1}	-0.3 to V_{DD} to + 0.3	V
Output current	I_{OUT1}	PC, PD, PG, PH, EO	0 to 3	mA
	I_{OUT2}	PB	0 to 1	mA
	I_{OUT3}	AOUT, PE	0 to 2	mA
	I_{OUT4}	S1 to S20	300	μA
	I_{OUT5}	COM1 to COM4	3	mA
Allowable power dissipation	$P_d\text{ max}$	$T_a = -20$ to $+70^\circ\text{C}$	300	mW
Operating temperature	T_{opr}		-20 to +70	$^\circ\text{C}$
Storage temperature	T_{stg}		-45 to +125	$^\circ\text{C}$

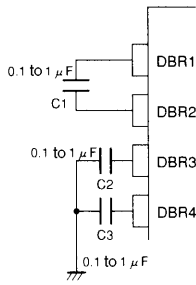
Allowable Operating Ranges at $T_a = -20$ to 70°C , $V_{DD} = 1.8$ to 3.6 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	CPU and PLL operating voltage	1.8	3.0	3.6	V
	V_{DD2}	Memory retention voltage	1.0			V
Input high-level voltage	V_{IH1}	V_{IH2} , V_{IH3} , AMIN, FMIN, Input ports except HCTR and XIN.	$0.7 V_{DD}$		V_{DD}	V
	V_{IH2}	$\overline{\text{RES}}$	$0.8 V_{DD}$		V_{DD}	V
	V_{IH3}	Port PF	$0.6 V_{DD}$		V_{DD}	V
Input low-level voltage	V_{IL1}	V_{IL2} , V_{IL3} , AMIN, FMIN, Input ports except HCTR and XIN.	0		$0.3 V_{DD}$	V
	V_{IL2}	$\overline{\text{RES}}$	0		$0.2 V_{DD}$	V
	V_{IL3}	Port PF	0		$0.2 V_{DD}$	V
Input amplitude	V_{IN1}	XIN	0.5		0.6	Vrms
	V_{IN2}	FMIN, AMIN	0.035		0.35	Vrms
	V_{IN3}	FMIN	0.05		0.35	Vrms
	V_{IN4}	HCTR	0.035		0.35	Vrms
Input voltage range	V_{IN5}	ADIO, ADI1	0		V_{DD}	V
Input frequency	F_{IN1}	XIN : $C_I \leq 35\text{ k}\Omega$	70	75	80	kHz
	F_{IN2}	FMIN : V_{IN2} , V_{DD1}	10		130	MHz
	F_{IN3}	FMIN : V_{IN3} , V_{DD1}	130		250	MHz
	F_{IN4}	AMIN (H) : V_{IN2} , V_{DD1}	2		40	MHz
	F_{IN5}	AMIN (L) : V_{IN2} , V_{DD1}	0.5		10	MHz
	F_{IN6}	HCTR : V_{IN4} , V_{DD1}	0.4		12	MHz

Electrical Characteristics at $T_a = -20$ to 70°C , $V_{DD} = 1.8$ to 3.6 V (in the allowable operating ranges)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I_{IH1}	$X_{IN} : V_I = V_{DD} = 3.0\text{ V}$			3	μA
	I_{IH2}	FMIN, AMIN, HCTR : $V_I = V_{DD} = 3.0\text{ V}$	3	8	20	μA
	I_{IH3}	Ports PA/PF (with no pull-down resistor), PC, PD, PG, and PH. RES: $V_I = V_{DD} = 3.0\text{ V}$			3	μA
Input low-level current	I_{IL1}	XIN : $V_I = V_{DD} = V_{SS}$			-3	μA
	I_{IL2}	FMIN, AMIN, HCTR : $V_I = V_{DD} = V_{SS}$	-3	-8	-20	μA
	I_{IL3}	Ports PA/PF (with no pull-down resistor), PC, PD, PG, and PH. RES: $V_I = V_{DD} = V_{SS}$			-3	μA
Input floating voltage	V_{IF}	PA/PF with pull-down resistors used			$0.05 V_{DD}$	V
Pull-down resistance	R_{PD1}	PA/PF with pull-down resistors used, $V_{DD} = 3\text{ V}$	75	100	200	$\text{k}\Omega$
Hysteresis	V_H	$\overline{\text{RES}}$	$0.1 V_{DD}$	$0.2 V_{DD}$		V
Voltage doubler reference voltage	DBR4	$T_a = 25^\circ\text{C}$, referenced to V_{DD} , $C_3 = 0.47\text{ }\mu\text{F}$	1.3	1.5	1.7	V
Voltage doubler step-up voltage	DBR1, 2, 3	$T_a = 25^\circ\text{C}$, $C_1 = 0.45\text{ }\mu\text{F}$, $C_2 = 0.47\text{ }\mu\text{F}$, no load	2.7	3.0	3.3	V

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Note: C1, C2, and C3 must be provided even if no LCD is used.

Electrical Characteristics at $T_a = -30$ to 70°C , $V_{DD} = 1.8$ to 3.6 V (in the allowable operating ranges)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output high-level voltage	V_{OH1}	PB : $I_O = -1$ mA	$V_{DD} - 0.7 V_{DD}$			V
	V_{OH2}	PC, PD, PG, PH : $I_O = -1$ mA	$V_{DD} - 0.3 V_{DD}$			V
	V_{OH3}	EO : $I_O = -500$ μA	$V_{DD} - 0.3 V_{DD}$			V
	V_{OH4}	XOUT : $I_O = -200$ μA	$V_{DD} - 0.3 V_{DD}$			V
	V_{OH5}	S1 to S20 : $I_O = -20$ μA : *1	2.0			V
	V_{OH6}	COM1, COM2, COM3, COM4 : $I_O = -100$ μA : *1	2.0			V
Output low-level voltage	V_{OL1}	PB : $I_O = -50$ μA			$0.7 V_{DD}$	V
	V_{OL2}	PC, PD, PE, PG, PH : $I_O = -1$ mA			$0.3 V_{DD}$	V
	V_{OL3}	EO : $I_O = -500$ μA			$0.3 V_{DD}$	V
	V_{OL4}	XOUT : $I_O = -200$ μA			$0.3 V_{DD}$	V
	V_{OL5}	S1 to S20 : $I_O = -20$ μA : *1			1.0	V
	V_{OL6}	COM1, COM2, COM3, COM4 : $I_O = -100$ μA : *1			1.0	V
	V_{OL7}	PE : $I_O = 5$ mA			1.0	V
	V_{OL8}	AOUT : $I_O = 1$ mA, AIN = 1.3 V, $V_{DD} = 3$ V			0.5	V
Output off leakage current	I_{OFF1}	Ports PB, PC, PD, PG, PH, and EO	-3		+3	μA
	I_{OFF2}	Ports AOUT and PE	-100		+100	nA
A/D conversion error		ADI0, ADI1, $V_{DD} = V_{DD1}$	-1/2		+1/2	LSB

Note: 1. Capacitors C1, C2, and C3 must be connected to the DBR pins.

Electrical Characteristics at $T_a = -20$ to 70°C , $V_{DD} = 1.8$ to 3.6 V (in the allowable operating ranges)

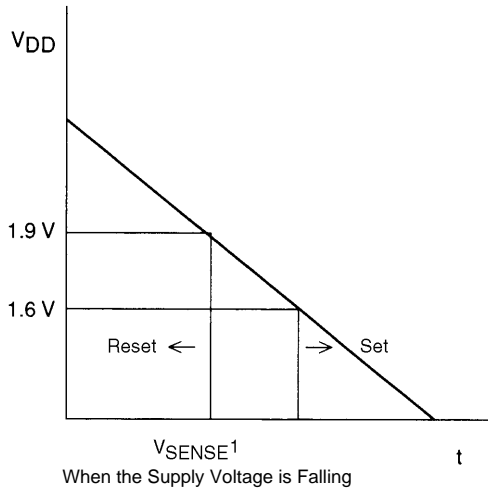
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Falling supply voltage detection voltage	V_{SENSE1}	$T_a = 25^\circ\text{C}$ *2	1.6	1.75	1.9	V
Rising supply voltage detection voltage	V_{SENSE2}	$T_a = 25^\circ\text{C}$ *2	$V_{SENSE1} + 0.1$		$V_{SENSE1} + 0.2$	V
Pull-down resistance	R_{PD2}	TEST1, TEST2		10		$k\Omega$
Supply current	I_{DD1}	V_{DD1} : F_{IN2} 130 MHz, $T_a = 25^\circ\text{C}$		10		mA
	I_{DD2}	V_{DD2} : In halt mode at $T_a = 25^\circ\text{C}$, *3		0.1		mA
	I_{DD3}	$V_{DD} = 3.6$ V, with the oscillator stopped, at $T_a = 25^\circ\text{C}$, *4		1		μA
	I_{DD4}	$V_{DD} = 1.8$ V, with the oscillator stopped, at $T_a = 25^\circ\text{C}$, *4		0.5		μA

Note: The halt mode current is measured with the CPU executing 20 instructions every 125 ms.

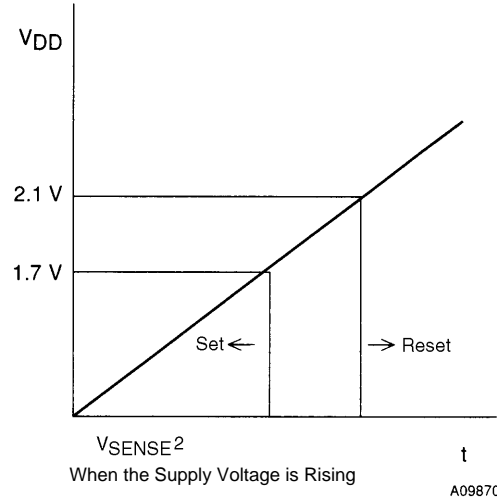
LC72341G/W, 72342G/W, 72343G/W

Note: 2. The V_{SENSE} voltage

When the V_{DD} voltage falls, the V_{SENSE} flag is set at the point that voltage falls under 1.75 V (typical). The TST instruction can be used to read the value of the V_{SENSE} flag. Applications can easily determine when the batteries are exhausted by monitoring this flag. After V_{SENSE} is set when the supply voltage falls, it will not be reset if the supply voltage rises by less than 0.1 V, because the voltages detected by the V_{SENSE} circuit differ when the supply voltage is falling and when the supply voltage is rising.



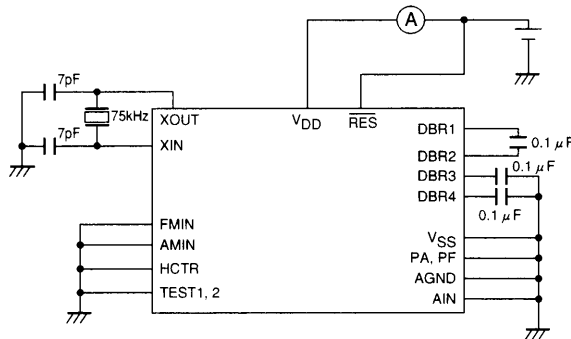
A09869



A09870

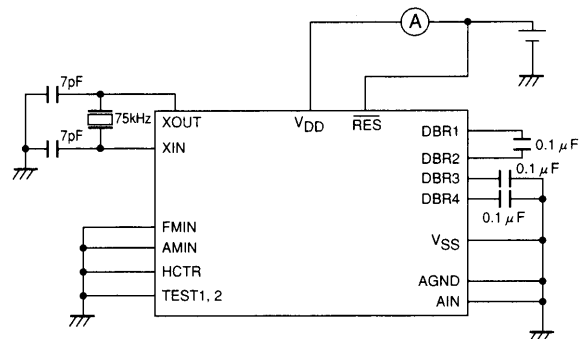
Note: 3. Halt Mode Current Test Circuit

Note: 4. Backup Mode Current Test Circuit



All ports other than those specified in the figure must be left open.
Set ports PC and PD to output.
Select segments S13 to S20.

A09871

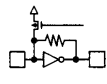
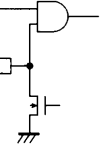
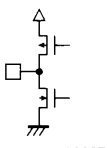
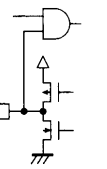
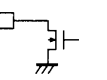
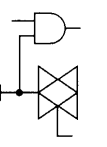


All ports other than those specified in the figure must be left open.
Set ports PC and PD to output.
Select segments S13 to S20.

A09872

LC72341G/W, 72342G/W, 72343G/W

Pin Functions

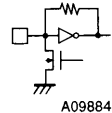
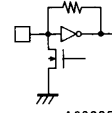
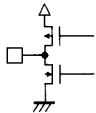
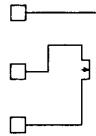
Pin No.	Pin	I/O	Function	I/O circuit
64 1	XIN XOUT	I O	Connections for a 75-kHz crystal oscillator element	 A09873
63 2	TEST1 TEST2	I I	IC test pins. These pins must be tied to ground.	
6 5 4 3	PA0 PA1 PA2 PA3	I	Special-purpose key return signal input ports designed with a low threshold voltage. When used in conjunction with port PB to form a key matrix, up to 3 simultaneous key presses can be detected. The four pull-down resistors are selected together in a single operation using the IOS instruction (PwN = 2, b1); they cannot be specified individually. Input is disabled in backup mode, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor  A09874
10 9 8 7	PB3 PB2 PB1 PB0	O	Special-purpose key source signal output ports. Since unbalanced CMOS output transistor circuits are used, diodes to prevent short-circuits when multiple keys are pressed are not required. These ports go to the output high-impedance state in backup mode. These ports go to the output high-impedance state after a reset and remain in that state until an output instruction (OUT, SPB, or RPB) is executed. Care is required in designing the output loads if these pins are used for functions other than key source outputs.	Unbalanced CMOS push-pull circuit  A09875
14 13 12 11 18 17 16 15	PC0 PC1 PC2 PC3 INT/PD0 PD1 PD2 PD3	I/O	General-purpose I/O ports*. PD0 can be used as an external interrupt port. Input or output mode can be set in a bit unit using the IOS instruction (PwN = 4, 5). A value of 0 specifies input, and 1 specifies output. These ports go to the input disabled high-impedance state in backup mode. They are set to function as general-purpose input ports after a reset.	CMOS push-pull circuit  A09876
20 19	BEEP/PE0 PE1		General-purpose output ports with shared beep tone output function (PE0 only). The BEEP instruction is used to switch PE0 between the general-purpose output port and beep tone output functions. To use PE0 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use PE0 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. When PE0 is set up as the beep tone output, executing an output instruction to PN0 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only the PE0 pin can be switched between the general-purpose output function and the beep tone output function; the PE1 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V _{DD} . These ports are set to their general-purpose output port function after a reset.	N-channel open drain  A09877
23 22 21	PF0/AD10 PF1/AD11 PF2	I	General-purpose input and A/D converter input shared function ports (PF2 is a general-purpose input only port). The IOS instruction (PwN = FH) is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a bit unit, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with PwN set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 5-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (1FH) is (63 · 96)V _{DD} .	CMOS input/analog input  A09878

Note: * Applications must establish the output data in advance with an OUT, SPB, or RPB instruction and then set the pin to output mode with an IOS instruction when using the I/O switchable ports as output pins.

Continued on next page.

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Continued from preceding page.

Pin No.	Pin	I/O	Function	I/O circuit												
56	FMIN	I	<p>FM VCO (local oscillator) input.</p> <p>This pin is selected with the PLL instruction CW1.</p> <p>The input must be capacitor coupled.</p> <p>Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</p>	<p>CMOS amplifier input</p>  <p>A09884</p>												
57	AMIN	I	<p>AM VCO (local oscillator) input.</p> <p>This pin and the bandwidth are selected with the PLL instruction CW1.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>CW1</th> <th>b1</th> <th>b0</th> <th>Bandwidth</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td></td> <td>2 to 40 MHz (SW)</td> </tr> <tr> <td>1</td> <td>1</td> <td></td> <td>0.5 to 10 MHz (MW, LW)</td> </tr> </tbody> </table> <p>The input must be capacitor coupled.</p> <p>Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</p>	CW1	b1	b0	Bandwidth	1	0		2 to 40 MHz (SW)	1	1		0.5 to 10 MHz (MW, LW)	<p>CMOS amplifier input</p>  <p>A09885</p>
CW1	b1	b0	Bandwidth													
1	0		2 to 40 MHz (SW)													
1	1		0.5 to 10 MHz (MW, LW)													
59	EO	O	<p>The main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output, and the pin is set to the high-impedance state when the frequencies match.</p> <p>Output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.</p>	<p>Push-pull CMOS output</p>  <p>A09886</p>												
60 61 62	AIN AOOUT AGND	O	<p>Transistor used for the low-pass filter amplifier.</p> <p>Connect AGND to ground.</p>	 <p>A09887</p>												
24 58 55	V _{SS} V _{SS} V _{DD}	—	<p>Power supply pin. This pin must be connected to ground.</p> <p>Power supply pin. This pin must be connected to ground.</p> <p>Power supply pin. This pin must be connected to V_{DD}.</p>													

Handling of Unused Pins

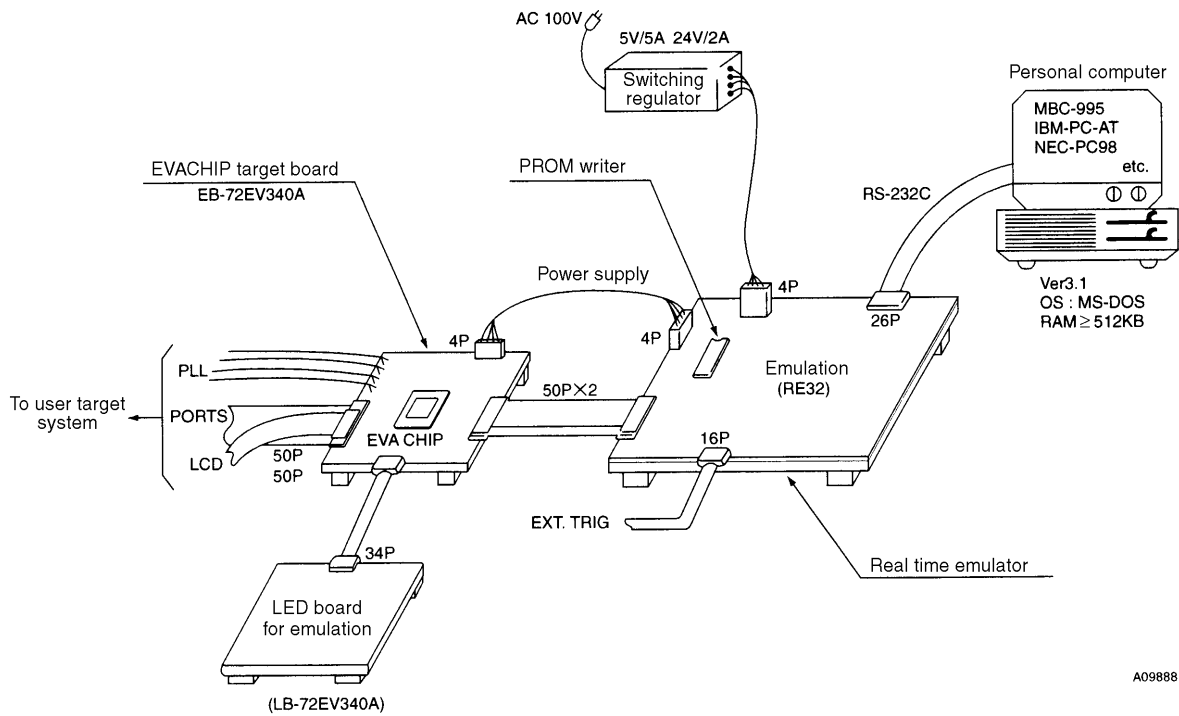
Pin No.	Pin	I/O type	Pin handling
3 to 6	PA port	I	Connect to V _{DD} or V _{SS} . May be left open if the pull-up resistor is selected with the IOS instruction.
7 to 10	PB port	O	Open
11 to 14	PC port	I/O	Connect to V _{DD} or V _{SS} when input is selected. Leave open if output is selected.
15 to 18	PD port	I/O	Connect to V _{DD} or V _{SS} when input is selected. Leave open if output is selected.
19, 20	PE port	O	Open
21 to 23	PF port	I	Connect to V _{DD} or V _{SS} . The PF2 pin only may be left open if the pull-up resistor is selected with the IOS instruction.
25 to 28	PG/S ports	I/O/S	Connect to V _{DD} or V _{SS} when input is selected. Leave open if output or LCD operation is selected.
29 to 32	PH/S ports	I/O/S	Connect to V _{DD} or V _{SS} when input is selected. Leave open if output or LCD operation is selected.
33 to 41	S port	O	Open
45 to 48	COM	O	Open
49	DBR1	—	Connect to DBR2 through a capacitor.
50	DBR2	—	Connect to DBR1 through a capacitor.
51	DBR3	—	Connect to V _{SS} through a capacitor.
52	DBR4	—	Connect to V _{SS} through a capacitor.
53	RES	I	V _{DD}
54	HCTR	I	V _{SS} Leave open if FMIN is used.
56	FMIN	I	V _{SS}
57	AMIN	I	V _{SS}
59	EO	O	Open
60	AIN	I	V _{SS}
61	AOOUT	O	Open
63	TEST1	I	Connect to V _{SS} or leave open. Connection to V _{SS} is preferable.
2	TEST2	I	Connect to V _{SS} or leave open. Connection to V _{SS} is preferable.

Mask Options

Port		Selection	
1	PG3/S20	General-purpose port	LCD port
2	PG2/S19	General-purpose port	LCD port
3	PG1/S18	General-purpose port	LCD port
4	PG0/S17	General-purpose port	LCD port
5	PH3/S16	General-purpose port	LCD port
6	PH2/S15	General-purpose port	LCD port
7	PH1/S14	General-purpose port	LCD port
8	PH0/S13	General-purpose port	LCD port

Development Environment and Tools

- The LC72P341 is available as a OTP version.
- The LC72EV340 is available as an evaluation chip.
- A total debugging system is formed by the combination of the TB-72EV32 evaluation chip board, the RE32 multi-function emulator, and a personal computer for system control.



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LC72341G/W, 72342G/W, 72343G/W

Instruction Set

Instruction group	Mnemonic	Opcode		Machine code							Operation	
		1st	2nd	15	12	11	8	7	4	3		0
Addition instructions	AD	r	M	0100	00	DH	DL	r				$r \leftarrow (r) + (M)$
	ADS	r	M	0100	01	DH	DL	r				$r \leftarrow (r) + (M)$, skip if carry
	AC	r	M	0100	10	DH	DL	r				$r \leftarrow (r) + (M) + C$
	ACS	r	M	0100	11	DH	DL	r				$r \leftarrow (r) + (M) + C$, skip if carry
	AI	M	I	0101	00	DH	DL	I				$M \leftarrow (M) + I$
	AIS	M	I	0101	01	DH	DL	I				$M \leftarrow (M) + I$, skip if carry
	AIC	M	I	0101	10	DH	DL	I				$M \leftarrow (M) + I + C$
	AICS	M	I	0101	11	DH	DL	I				$M \leftarrow (M) + I + C$, skip if carry
Subtraction instructions	SU	r	M	0110	00	DH	DL	r				$r \leftarrow (r) - (M)$
	SUS	r	M	0110	01	DH	DL	r				$r \leftarrow (r) - (M)$, skip if borrow
	SB	r	M	0110	10	DH	DL	r				$r \leftarrow (r) - (M) - b$
	SBS	r	M	0110	11	DH	DL	r				$r \leftarrow (r) - (M) - b$, skip if borrow
	SI	M	I	0111	00	DH	DL	I				$M \leftarrow (M) - I$
	SIS	M	I	0111	01	DH	DL	I				$M \leftarrow (M) - I$, skip if borrow
	SIB	M	I	0111	10	DH	DL	I				$M \leftarrow (M) - I - b$
	SIBS	M	I	0111	11	DH	DL	I				$M \leftarrow (M) - I - b$, skip if borrow
Comparison instructions	SEQ	r	M	0001	00	DH	DL	r				$(r) \leftarrow (M)$, skip if zero
	SEQI	M	I	0001	10	DH	DL	I				$(M) \leftarrow I$, skip if zero
	SNEI	M	I	0000	01	DH	DL	I				$(M) \leftarrow I$, skip if not zero
	SGE	r	M	0001	10	DH	DL	r				$(r) \leftarrow (M)$, skip if not borrow
	SGEI	M	I	0001	11	DH	DL	I				$(M) \leftarrow I$, skip if not borrow
	SLEI	M	I	0000	11	DH	DL	I				$(M) \leftarrow I$, skip if borrow
Logic and arithmetic instructions	ANDI	M	I	0010	01	DH	DL	I				$M \leftarrow (M) \text{ AND } I$
	ORI	M	I	0010	11	DH	DL	I				$M \leftarrow (M) \text{ OR } I$
	EXLI	M	I	0011	10	DH	DL	I				$M \leftarrow (M) \text{ XOR } I$
	AND	r	M	0010	00	DH	DL	r				$r \leftarrow (r) \text{ AND } M$
	OR	r	M	0010	10	DH	DL	r				$r \leftarrow (r) \text{ OR } M$
	EXL	r	M	0011	00	DH	DL	r				$r \leftarrow (r) \text{ XOR } M$
	SHR	r		0000	00	00	1110	r				Shift r right with carry
	Transfer instructions	LD	r	M	1101	00	DH	DL	r			
ST		M	r	1101	01	DH	DL	r				$M \leftarrow (r)$
MVRD		r	M	1101	10	DH	DL	r				$[DH, r] \leftarrow (M)$
MVRS		M	r	1101	11	DH	DL	r				$M \leftarrow [DH, r]$
MVSR		M1	M2	1110	00	DH	DL1	DL2				$[DH, DL1] \leftarrow [DH, DL2]$
MVI		M	I	1110	01	DH	DL	I				$M \leftarrow I$
Memory test instructions	TMT	M	N	1111	00	DH	DL	N				if M (N) = all 1, then skip
	TMF	M	N	1111	01	DH	DL	N				if M (N) = all 0, then skip
Jump and subroutine call instructions	JMP	ADDR		100	ADDR (13 bits)						$PC \leftarrow ADDR$	
	CAL	ADDR		101	ADDR (13 bits)						$PC \leftarrow ADDR, \text{Stack} \leftarrow (PC) + 1$	
	RT			0000	0000	1000				$PC \leftarrow \text{Stack}$		
	RTI			0000	0000	1001				$PC \leftarrow \text{Stack}, \text{BANK} \leftarrow \text{Stak}, \text{carry} \leftarrow \text{stack}$		
Status register test and flip-flop control instructions	SS	I	N	1111	1111	000I		N				$(\text{Status reg. I})N \leftarrow 1$
	RS	I	N	1111	1111	001I		N				$(\text{Status reg. I})N \leftarrow 0$
	TST	I	N	1111	1111	01I		N				if (Status reg. I)N = all 1, then skip
	TSF	I	N	1111	1111	10I		N				if (Status reg. I)N = all 0, then skip
	TUL	N		0000	0000	1101		N				if Unlock F/F (N) = all 0, then skip

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Instruction group	Mnemonic	Opcode		Machine code						Operation		
		1st	2nd	15	12	11	8	7	4		3	0
Peripheral hardware control instructions	PLL	M	r	1111	10	DH	DL	r				PLL reg. ← PLL data
	TMS	I		0000	0000		1100	I				Timer reg. ← I
	UCS	I		0000	0000		0001	I				UCS reg. ← I
	UCC	I		0000	0000		0010	I				UCC reg. ← I
	BEEP	I		0000	0000		0110	I				BEEP reg. ← I
	DZC	I		0000	0000		1011	I				DZC reg. ← I
	BANK	I		0000	0000		0111	I				BANK ← I
	IOS	Pn	I	1111	1110			Pn	I			
I/O instructions	INR	M	Rn	0011	10	DH	DL	r				M ← (Rn reg.)
	IN	M	Pn	1110	10	DH	DL	Pn				M ← (Pn)
	OUT	M	Ph	1110	11	DH	DL	Pn				Pn ← M
	SPB	Pn	N	0000	0010			Pn	N			(Pn) N ← 1
	RPB	Pn	N	0000	0011			Pn	N			(Pn) N ← 0
	TPT	Pn	N	1111	1100			Pn	N			if (Pn) N = all 1, then skip
	TPF	Pn	N	1111	1101			Pn	N			if (Pn) N = all 0, then skip
LCD control instructions	LCDA	M	I	1100	00	DH	DL	DIGIT				LCD (DIGIT) ← M
	LCDB	M	I	1100	01	DH	DL	DIGIT				
	LCPA	M	I	1100	10	DH	DL	DIGIT				LCD (DIGIT) ← Logic
	LCPB	M	I	1100	11	DH	DL	DIGIT				Array ← M
Other instructions	HALT	I		0000	0000		0100	I				HALT reg. ← I, then CPU Stop
	CKSTP			0000	0000		0101					Stop Xtal OSC
	NOP			0000	0000		0000					No operation

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