Ordering number : ENN6171

CMOS IC

LC72344W, 72345W

Low-Voltage ETR Controller with On-Chip DC-DC Converter

Overview

The LC72344W and LC72345W are low-voltage electronic tuning microcontrollers that include a DC-DC converter, a PLL that operates up to 230 MHz, a 1/4 duty 1/2 bias LCD driver and other functions on chip. The built-in DC-DC converter provided by these ICs can easily implement a tuning system voltage generator circuit, and furthermore, since the transistor required for the low-pass filter is built in, these ICs can contribute to further end product cost reductions. Additionally, the DC-DC converter output voltage can be provided to other external ICs, making these products optimal for low-voltage portable audio equipment that includes a radio receiver.

Functions

- Program memory (ROM): 3072 × 16 bits (6 KB) LC72344W
  4096 × 16 bits (8 KB) LC72345W
- Data memory (RAM): 192 × 4 bits LC72344W
  256 × 4 bits LC72345W
- Cycle time: 40 µs (all 1-word instructions)
- Stack: 8 levels
- LCD driver: 48 to 76 segments (1/4 duty, 1/2 bias drive)
- Interrupts: One external interrupt
  Timer interrupts (1, 5, 10, and 50 ms)
- A/D converter: Two input channels (5-bit successive approximation conversion)
- Input ports: 6 ports (of which 2 can be switched for use as A/D converter inputs)
- Output ports: 6 ports (of which 1 can be switched for use as the beep tone output and 2 are open-drain ports)
- I/O ports: 16 ports (of which 8 can be switched for use as LCD ports as mask options)

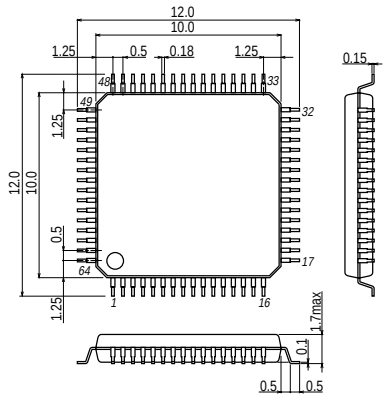
(Continued on next page.)

Package Dimensions

unit: mm

3190-SQFP64

[LC72344W, 72345W]



SANYO: SQFP64

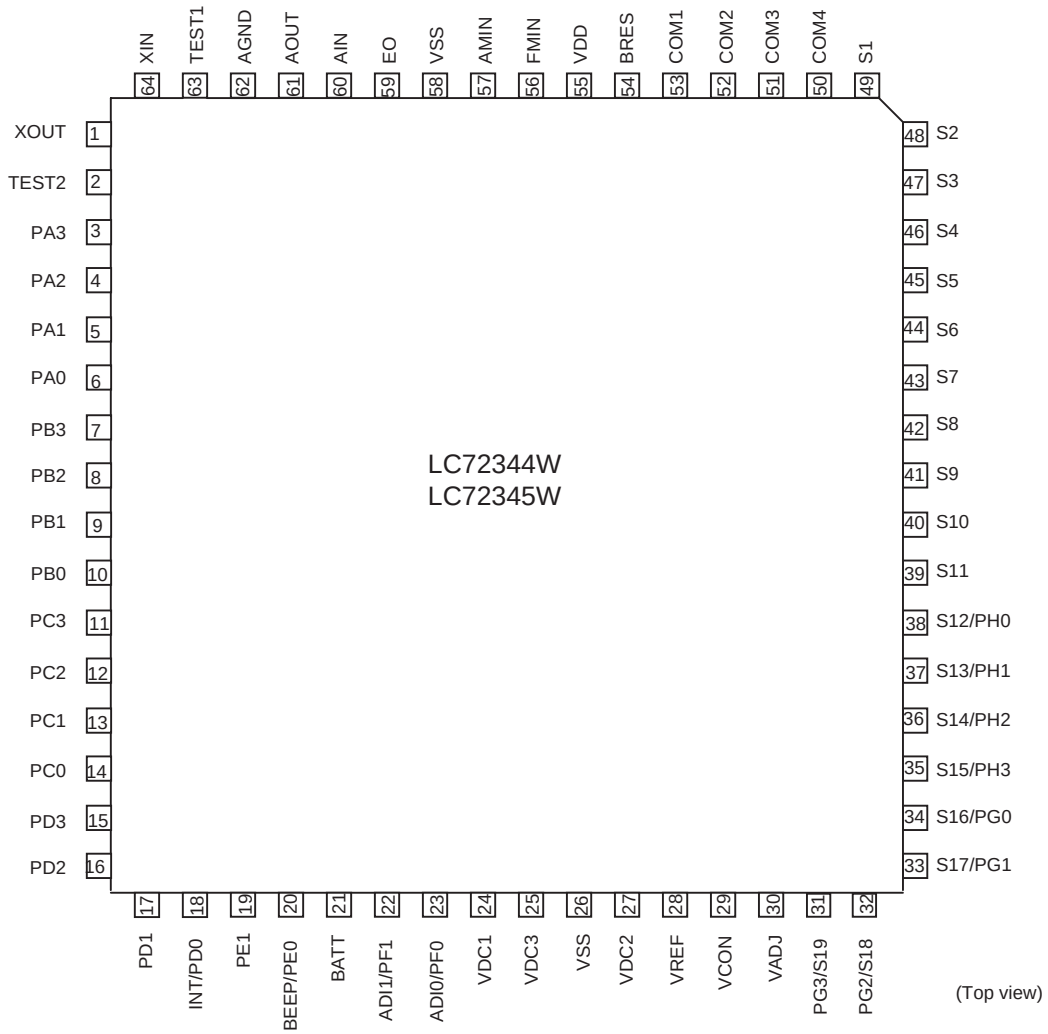
SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

31000RM (OT) No. 6171-1/13

(Continued from preceding page.)

- PLL: Supports dead band control (two types)
  Reference frequencies: 1, 3, 5, 6.25, 12.5, and 25 kHz
- Input frequencies: FM band: 10 to 230 MHz
  AM band: 0.5 to 10 MHz
- Input sensitivity: FM band: 35 mV rms (50 mV rms at 130 MHz or higher frequency)
  AM band: 35 mV rms
- External reset input: During CPU and PLL operation, instruction execution is started from location 0.
- Built-in power-on reset circuit:
  The CPU starts executing from location 0 when power is first applied.
- Static power-on function: Backup state clear function using the BATT pin.
- Halt mode: The controller operating clock is stopped.
- Backup mode: The crystal oscillator is stopped.
- Beep tone: 1.5 and 3.1 kHz
- Built-in DC-DC converter: Two systems (One system can be used as an external circuit power supply by providing an external transistor.)
- Built-in low-pass filter amplifier: An external low-pass filter amplifier circuit is no longer required in end products.
- Remaining power check function: The battery voltage can be directly converted to a digital value by the A/D converter.
- Memory retention voltage: 0.9 V or higher.
- V_{DD} voltage: 0.9 to 1.8 V
- Package: SQFP-64 (0.5 mm lead pitch)

Pin Assignment



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD}(1)max	VDD	–0.3 to +0.3	V
	V_{DD}(2)max	VDC1	–0.3 to +4.0	V
	V_{DD}(3)max	VDC2	–0.3 to +4.0	V
	V_{DD}(4)max	VDC3	–0.3 to +4.0	V
Input voltage	V_{IN}(1)	PF, FMIN, AMIN, AIN, BATT, and BRES	–0.3 to V_{DD}(3) to +0.3	V
	V_{IN}(2)	PA, PC, PD, PG, and PH	–0.3 to V_{DD}(1) to +0.3	V
Output voltage	V_{OUT}(1)	AOUT, and PE	–0.3 to +15	V
	V_{OUT}(2)	PB, PC, PD, PG, and PH	–0.3 to V_{DD}(1) +0.3	V
	V_{OUT}(3)	VREF, and EO	–0.3 to V_{DD}(3) +0.3	V
	V_{OUT}(4)	COM1 to COM4, S1 to S19	–0.3 to V_{DD}(4) +0.3	V
Output current	I_{OUT}(1)	PC, PD, PG, PH, and EO	0 to 3	mA
	I_{OUT}(2)	PB	0 to 1	mA
	I_{OUT}(3)	AOUT, and PE	0 to 2	mA
	I_{OUT}(4)	S1 to S20	300	µA
	I_{OUT}(5)	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –20 to +70°C	200	mW
Operating temperature	Topr		–20 to +70	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –20 to +70°C, V_{DD} = 0.9 to 1.8 V

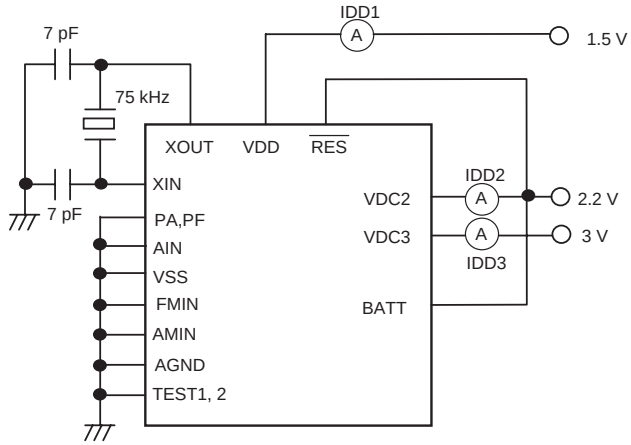
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}(1)	The voltage applied to the VDD pin	0.9	1.5	1.8	V
	V_{DD}(2)	The voltage applied to the VDC1 pin	0.9	1.5	1.8	V
	V_{DD}(3)	The voltage applied to the VDC2 pin	1.8	2.1	2.4	V
	V_{DD}(4)	The voltage applied to the VDC3 pin	2.6	3.0	3.4	V
	V_{DD}(5)	Memory retention voltage	0.9			V
Input high-level voltage	V_{IH}(1)	Ports PC, PD, PG, and PH	0.7 V_{DD}(1)		V_{DD}(1)	V
	V_{IH}(2)	Port PA	0.8 V_{DD}(1)		V_{DD}(1)	V
	V_{IH}(3)	Port PF	0.8 V_{DD}(1)		V_{DD}(3)	V
	V_{IH}(4)	Ports BRES and BATT	0.6 V_{DD}(1)		V_{DD}(3)	V
Input low-level voltage	V_{IL}(1)	Ports PC, PD, PG, and PH	0		0.3 V_{DD}(1)	V
	V_{IL}(2)	Port PA	0		0.2 V_{DD}(1)	V
	V_{IL}(3)	Port PF	0		0.2 V_{DD}(1)	V
	V_{IL}(4)	Ports BRES and BATT	0		0.2 V_{DD}(1)	V
Input amplitude	V_{IN}(1)	XIN	0.5		0.6	Vrms
	V_{IN}(2)	FMIN, AMIN: V_{DD}(3) = 2.1 V	0.035		0.35	Vrms
	V_{IN}(3)	FMIN: V_{DD}(3) = 2.1 V	0.05		0.35	Vrms
Input voltage range	V_{IN}(4)	ADI0, ADI1, and V_{DD}	0		V_{DD}(4)	V
Input frequency	F_{IN}(1)	XIN: CI ≤ 35 kΩ	70	75	80	kHz
	F_{IN}(2)	FMIN: V_{IN}(2), V_{DD}(3) = 2.1 V	10		130	MHz
	F_{IN}(3)	FMIN: V_{IN}(3), V_{DD}(3) = 2.1 V	130		230	MHz
	F_{IN}(4)	AMIN(L): V_{IN}(2), V_{DD}(3) = 2.1 V	0.5		10	MHz

Electrical Characteristics under allowable operating conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	$I_{IH}(1)$	XIN: $V_{DD}(1)$ = 1.8 V, $V_{DD}(2)$ = 1.8 V, $V_{DD}(3)$ = 2.1 V			3	µA
	$I_{IH}(2)$	FMIN, and AMIN: $V_{DD}(3)$ = 2.1 V	3	8	20	µA
	$I_{IH}(3)$	Ports BRES, BATT, and PF: $V_{DD}(3)$ = 2.1 V			4	µA
	$I_{IH}(4)$	Ports PA (no pull-down resistor), PC, PD, PG, and PH: $V_{DD}(1)$ = 1.8 V			3	µA
Input low-level voltage	$I_{IL}(1)$	XIN: $V_{DD}(1) = V_{DD}(2) = V_{DD}(3) = V_{SS}$			–3	µA
	$I_{IL}(2)$	FMIN, and AMIN: $V_{DD}(3) = V_{SS}$	–3	–8	–20	µA
	$I_{IL}(3)$	Ports BRES, BATT, and PF: $V_{DD}(3) = V_{SS}$			–4	µA
	$I_{IL}(4)$	Ports PA (no pull-down resistor), PC, PD, PG, and PH: $V_{DD}(1) = V_{SS}$			–3	µA
Input floating voltage	V_{IF}	Port PA pull-down resistor present			0.05 $V_{DD}(1)$	V
Pull-down resistor	$R_{PD}(1)$	Port PA pull-down resistor: $V_{DD}(1)$ = 1.3 V	75	100	200	kΩ
	$R_{PD}(2)$	TEST1 and TEST2 pull-down resistors		10		kΩ
Hysteresis	V_H	BRES	0.1 $V_{DD}(3)$	0.2 $V_{DD}(3)$		V
Output high-level voltage	$V_{OH}(1)$	PB: I_O = 1 mA	$V_{DD}(1)$ – 0.7 $V_{DD}(1)$		$V_{DD}(1)$ – 0.3 $V_{DD}(1)$	V
	$V_{OH}(2)$	PC, PD, PG, PH: I_O = 1 mA	$V_{DD}(1)$ – 0.3 $V_{DD}(1)$			V
	$V_{OH}(3)$	EO: I_O = –500 µA	$V_{DD}(3)$ – 0.3 $V_{DD}(3)$			V
	$V_{OH}(4)$	XOUT I_O = 1 µA	$V_{DD}(3)$ – 0.3 $V_{DD}(3)$			V
	$V_{OH}(5)$	S1 to S20: I_O = 20 µA	$V_{DD}(4)$ – 1			V
	$V_{OH}(6)$	COM1, CM2, COM3, and COM4: I_O = 100 µA	$V_{DD}(4)$ – 1			V
	$V_{OH}(7)$	VREF: I_O = 1 mA	$V_{DD}(3)$ – 1			V
Output low-level voltage	$V_{OL}(1)$	PB: I_O = –50 µA	0.3 $V_{DD}(1)$		0.7 $V_{DD}(1)$	V
	$V_{OL}(2)$	PC, PD, PG, and PH: I_O = –1 mA			0.3 $V_{DD}(1)$	V
	$V_{OL}(3)$	EO: I_O = –500 µA			0.3 $V_{DD}(3)$	V
	$V_{OL}(4)$	XOUT: I_O = –1 µA			0.3 $V_{DD}(3)$	V
	$V_{OL}(5)$	S1 to S20: I_O = –20 µA			$V_{DD}(4)$–2	V
	$V_{OL}(6)$	COM1, COM2, COM3, and COM4: I_O = –100 µA			$V_{DD}(4)$–2	V
	$V_{OL}(7)$	PE: I_O = 2 mA			0.6 $V_{DD}(1)$	V
	$V_{OL}(8)$	AOUT: I_O = 1 mA, AIN = 1.3 V: $V_{DD}(4)$ = 3 V			0.5	V
Output off leakage current	$I_{OFF}(1)$	PB, PC, PD, PG, PH, and E0 ports	–3		3	µA
	$I_{OFF}(2)$	AOUT and PE ports	–100		100	nA
A/D converter error		ADI0 and ADI1, V_{DD}	–1/2		+1/2	LSB
Internal clock frequency	fosc(1)	FM, and PLLSTOP: $V_{DD}(3)$ = 2.1 V, Vcon = OPEN	300	600	900	kHz
	fosc(2)	AM	450		1200	kHz
Current drain	$I_{DD1}(1)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: $F_{IN}(2)$ 130 MHz, Ta = 25°C		1		mA
	$I_{DD2}(2)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: $F_{IN}(2)$ 130 MHz, Ta = 25°C		5		mA
	$I_{DD3}(3)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: $F_{IN}(2)$ 130 MHz, Ta = 25°C		1		mA
	$I_{DD1}(4)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: Halt mode, Ta = 25°C *1		0.1		mA
	$I_{DD2}(5)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: Halt mode, Ta = 25°C *1		0.3		mA
	$I_{DD3}(6)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: Halt mode, Ta = 25°C *1		0.1		mA
	$I_{DD1}(7)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: With the oscillator stopped, Ta = 25°C *		100		nA
	$I_{DD2}(8)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: With the oscillator stopped, Ta = 25°C *		500		nA
	$I_{DD3}(9)$	$V_{DD}(1)$ = 1.5 V, $V_{DD}(3)$ = 2.1 V, $V_{DD}(4)$ = 3.0 V: With the oscillator stopped, Ta = 25°C *		100		nA

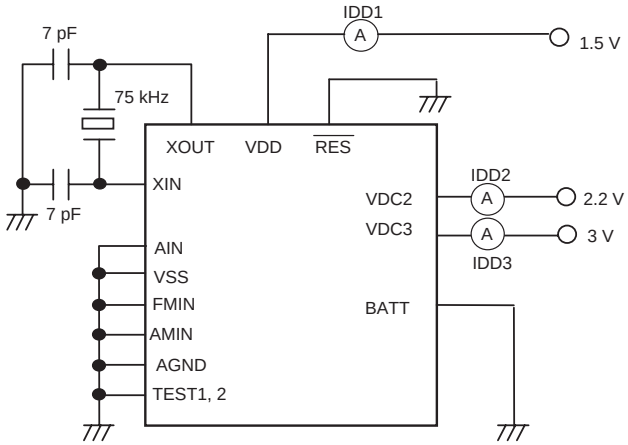
The halt mode current drain is due to 20 instructions being executed every 125 ms.

*1 Halt mode current drain test conditions



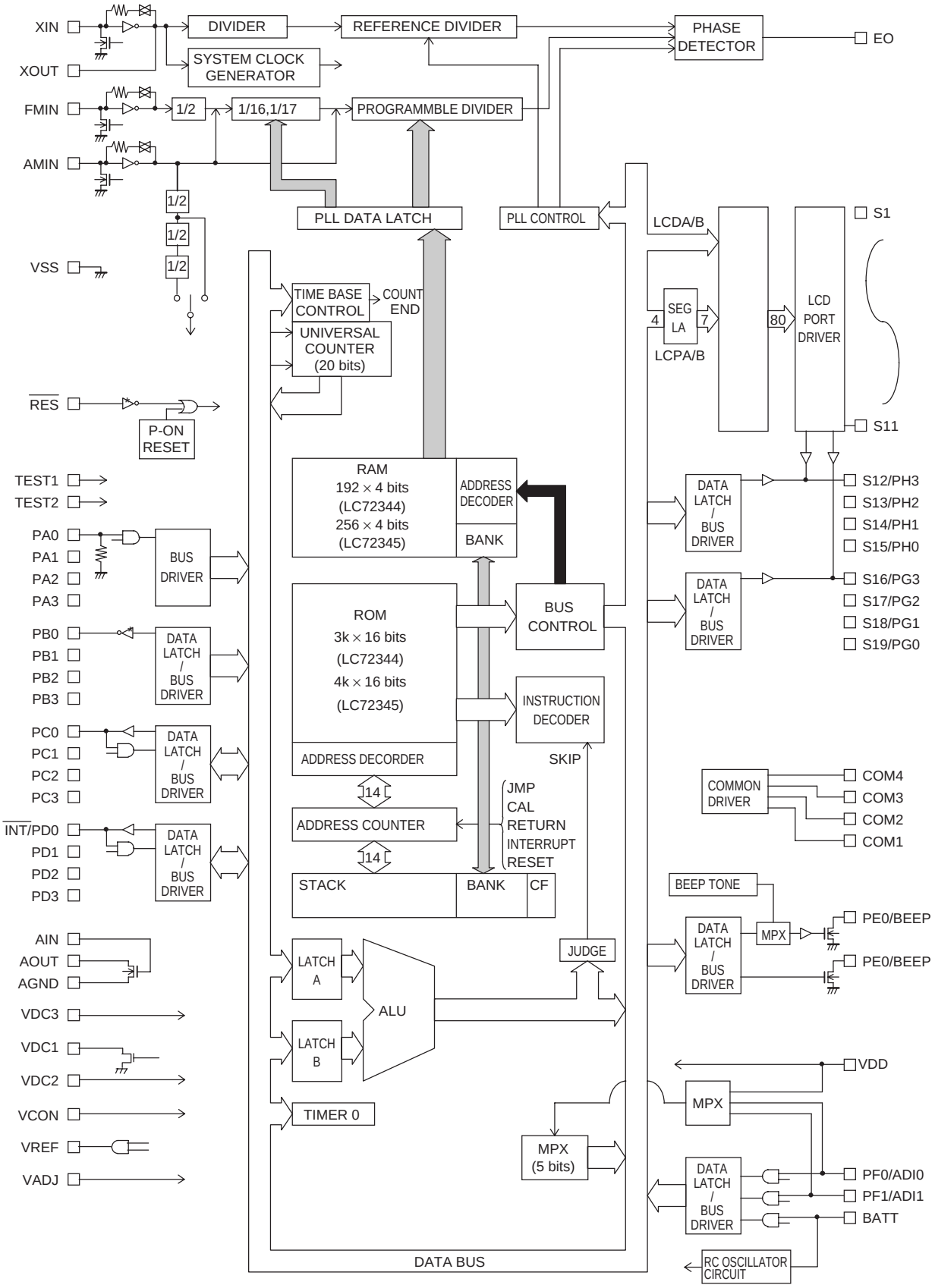
Leave all ports other than those mentioned above open.
Select output mode for PC and PD.
Select the segment function for S12 to S19.

*2 Backup mode current drain test conditions

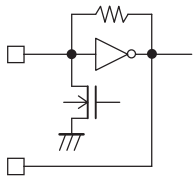
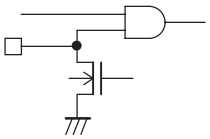
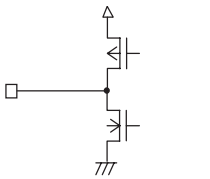
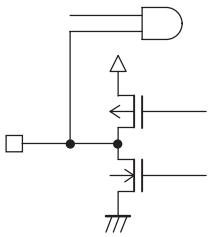
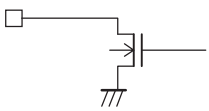


Leave all ports other than those mentioned above open.
Select output mode for PC and PD.
Select the segment function for S12 to S19.

Block Diagram



Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
64 1	XIN XOUT	I O	75 kHz crystal oscillator connections	
63 2	TEST1 TEST2	I I	IC testing. These pins must be connected to ground.	—
6 5 4 3	PA0 PA1 PA2 PA3	I	Special-purpose ports for key return signal input designed with a low threshold voltage. When a key matrix is formed in combination with port PB, simultaneous multiple key presses with up to 3 keys can be detected. The pull-down resistors are set up for all four pins at the same time with the IOS instruction (PWn = 2.b1). This setting cannot be specified for individual pins. In backup mode, these pins go to the input disabled state, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor 
10 9 8 7	PB0 PB1 PB2 PB3	O	Unbalanced CMOS outputs. These outputs are switched with the IOS 0 instruction. Since these outputs are unbalanced, no diodes are required to prevent short circuits due to simultaneous multiple key presses. These outputs go to the high-impedance output state in backup mode. After a reset, they go to the high-impedance output state and remain in that state until an output instruction (OUT, SPB, or RPB) is executed.	Unbalanced CMOS push-pull output 
14 13 12 11 18 17 16 15 (*)	PC0 PC1 PC2 PC3 $\overline{\text{INT}}$/PD0 PD1 PD2 PD3	I/O	General-purpose I/O ports. PD0 can be used as an external interrupt port. The IOS instruction (Pwn = 4, 5) is used for switching the general-purpose I/O port function, and these ports can be set to input or output in 1-bit units. (0: input, 1: output) In backup mode they go to the input disabled high-impedance state. After a reset, they switch to the general-purpose input port function.	CMOS push-pull output 
20 19	BEEP/PE0 PE1		General-purpose output and beep tone output shared function ports (PE0 only). The BEEP instruction is used to switch PE0 between the general-purpose output port and beep tone output functions. To use PE0 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use PE0 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. *: When PE0 is set up as the beep tone output, executing an output instruction to PN0 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only the PE0 pin can be switched between the general-purpose output function and the beep tone output function; the PE1 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V_{DD}. These ports are set to their general-purpose output port function after a reset.	N-channel open-drain output 

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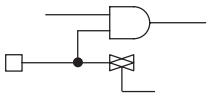
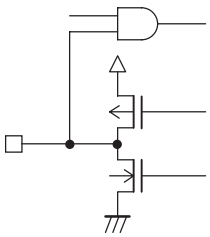
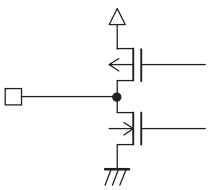
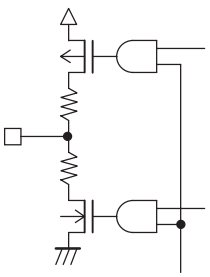
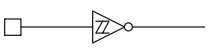
Pin No.	Pin	I/O	Function	I/O circuit
23 22	PF0/ADI0 PF1/ADI1	I	General-purpose input and A/D converter input shared function ports. The IOS instruction (Pwn = FH) is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a bit units, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. *: If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 5-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (1FH) is (63/96) times VDC3.	CMOS input/analog input 
31 32 33 34 35 36 37 38	PG3/S19 PG2/S18 PG1/S17 PG0/S16 PH3/S15 PH2/S14 PH1/S13 PH0/S12 (*)	O	LCD driver segment output and general-purpose I/O shared function ports. The IOS instruction* is used for switching both between the segment output and general-purpose I/O functions and between input and output for the general-purpose I/O port function. • When used as segment output ports The general-purpose I/O port function is selected with the IOS instruction (Pwn = 8). b0 = S16 to 19/PG0 to 3 (0: Segment output, 1: PG0 to 3) The general-purpose I/O port function is selected with the IOS instruction (Pwn = 9). b0 = S12 to 15/PH0 to 3 (0: Segment output, 1: PH0 to 3) • When used as general-purpose I/O ports The IOS instruction (Pwn = 6,7) is used to select input or output. Note that the mode can be set in a bit units. b0 = PG0 b1 = PG1 (0: Input, 1: Output) b2 = PG2 b3 = PG3 b0 = PH0 b1 = PH1 (0: Input, 1: Output) b2 = PH2 b3 = PH3 In backup mode, these pins go to the input disabled high-impedance state if set up as general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset. Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function.	CMOS push-pull output 
39 to 49	S11 to S1	O	LCD driver segment output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	CMOS push-pull output 
50 51 52 53	COM4 COM3 COM2 COM1	O	LCD driver common output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	
54	$\overline{\text{RES}}$	I	System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit.	
21	BATT	I	Battery presence/absence discrimination. The internal clock oscillator starts when a high level is input to this pin. The IN instruction can be used to determine whether or not a battery is present.	

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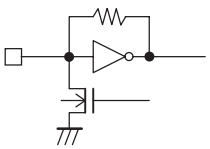
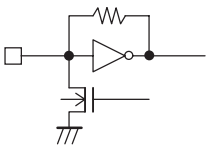
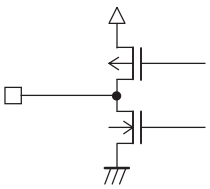
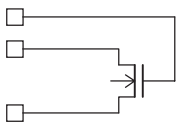
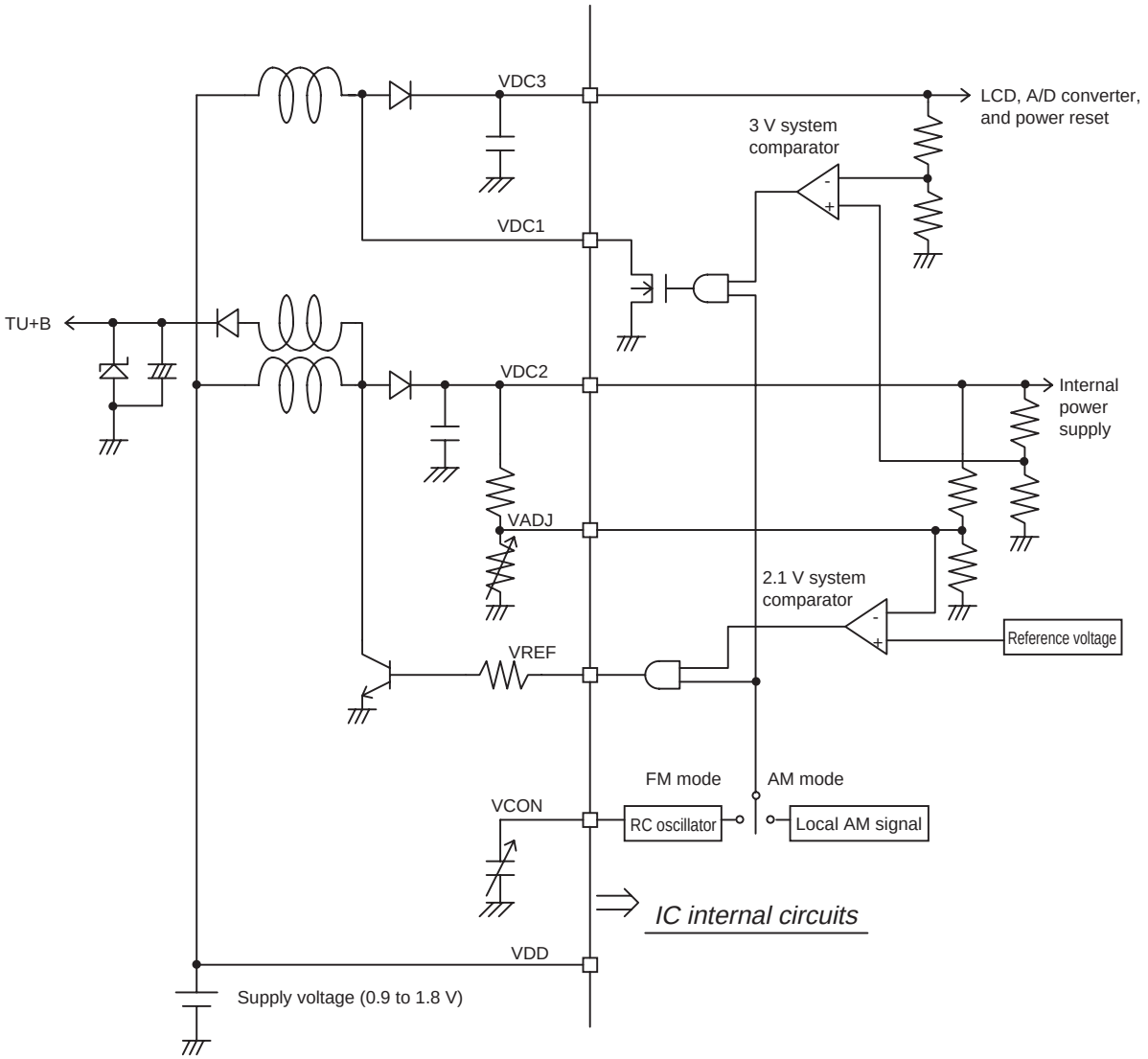
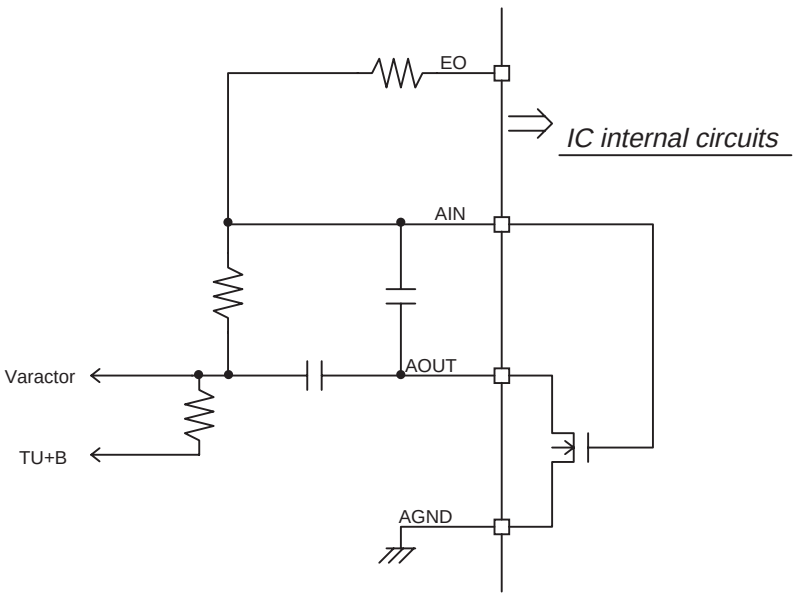
<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>I/O circuit</th></tr>
<tr><td>24</td><td>VDC1</td><td>I</td><td>VDC3 (3 V) step-up control.</td><td></td></tr>
<tr><td>27</td><td>VDC2</td><td>I</td><td>2.1 V power supply. Apply either the voltage stepped-up by the DC-DC converter or an equivalent voltage (2.1 V typical).</td><td></td></tr>
<tr><td>25</td><td>VDC3</td><td>I</td><td>3 V power supply. Apply either the voltage stepped-up by VDC1 or an equivalent voltage (3 V typical).</td><td></td></tr>
<tr><td>28</td><td>VREF</td><td>O</td><td>VDC2 step-up transistor drive.</td><td></td></tr>
<tr><td>29</td><td>VCON</td><td>I</td><td>Frequency adjustment for the internal RC oscillator circuit. The RC oscillator frequency can be lowered by inserting a capacitor between this pin and ground.</td><td></td></tr>
<tr><td>30</td><td>VADJ</td><td>O</td><td>The VDC3 voltage can be adjusted by inserting a resistor between this pin and ground.</td><td></td></tr>
<tr><td>56</td><td>FMIN</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected with the PLL instruction CW1.
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>57</td><td>AMIN</td><td>I</td><td>AM VCO (local oscillator) input.
This pin and the bandwidth are selected with the PLL instruction CW1.
<table><tr><th>CW1 b1, b0</th><th>Bandwidth</th></tr><tr><td>11</td><td>0.5 to 10 MHz (MW, LW)</td></tr></table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>59</td><td>EO</td><td>O</td><td>Main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output, and the pin is set to the high-impedance state when the frequencies match.
This output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS push-pull output
  </td></tr>
<tr><td>60
61
62</td><td>AIN
AOUT
AGND</td><td>O</td><td>Transistor used for the low-pass filter amplifier.
Connect AGND to ground.</td><td>  </td></tr>
<tr><td>26
58
55</td><td>VSS
VSS
VDD</td><td>—</td><td>Power supply pin.
This pin must be connected to ground.
This pin must be connected to ground.
This pin must be connected to VDD. Supports A/D converter.</td><td>—</td></tr>
</table>

Note: *Applications must establish the output data in advance with an OUT, SPB, or RPB instruction and then set the pin to output mode with an IOS instruction when using the I/O switchable ports as output pins.

DC-DC Converter Application Sample



Low-Pass Filter Application Sample



LC72344W and LC72345W Instruction Set

Terminology

ADDR	: Program memory address
b	: Borrow
C	: Carry
DH	: Data memory address High (Row address) [2 bits]
DL	: Data memory address Low (Column address) [4 bits]
I	: Immediate data [4 bits]
M	: Data memory address
N	: Bit position [4 bits]
Rn	: Resister number [4 bits]
Pn	: Port number [4 bits]
PW	: Port control word number [4 bits]
r	: General register (One of the address from 00H to 0FH of BANKO)
( ), [ ]	: Contents of register or memory
M (DH, DL)	: Data memory specified by DH, DL

Instruction group	Mnemonic	Operand		Function	Operational function	Instruction format													
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				r			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M), skip if carry	0	1	0	0	0	1	DH		DL				r			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				r			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I, skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C, skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	DH		DL				r			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M), skip if borrow	0	1	1	0	0	1	DH		DL				r			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b, skip if borrow	0	1	1	0	1	1	DH		DL				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subract I from M, then skip if borrow	M ← (M) – I, skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b, skip if borrow	0	1	1	1	1	1	DH		DL				I			

Continued on next page.

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operational function	Instruction format f e d c b a 9 8 7 6 5 4 3 2 1 0
Comparison instruction	SEQ	r	M	Skip if r equal to M	(r) – (M), skip if zero	0 0 0 1 0 0 DH DL r
	SEQI	M	I	Skip if M equal to I	(M) – I, skip if zero	0 0 0 1 1 0 DH DL I
	SNEI	M	I	Skip if M not equal to I	(M) – I, skip if not zero	0 0 0 0 0 1 DH DL I
	SGE	r	M	Skip if r is greater than or equal to M	(r) – (M), skip if not borrow	0 0 0 1 1 0 DH DL r
	SGEI	M	I	Skip if M is greater than equal to I	(M) – I, skip if not borrow	0 0 0 1 1 1 DH DL I
	SLEI	M	I	Skip if M is less than I	(M) – I, skip if borrow	0 0 0 0 1 1 DH DL I
Logical operation instructions	AND	r	M	AND M with r	r ← (r) AND (M)	0 0 1 0 0 0 DH DL r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0 0 1 DH DL I
	OR	r	M	OR M with r	r ← (r) OR (M)	0 0 1 0 1 0 DH DL r
	ORI	M	I	OR I with M	M ← (M) OR I	0 0 1 0 1 1 DH DL I
	EXL	r	M	Exclusive OR M with r	r ← (r) XOR (M)	0 0 1 1 0 0 DH DL r
	EXLI	M	I	Exclusive OR M with M	M ← (M) XOR I	0 0 1 1 1 0 DH DL I
	SHR	r		Shift r right with carry	carry → (r) → carry	0 0 0 0 0 0 0 0 1 1 1 0 r
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 1 0 1 0 0 DH DL r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1 0 1 DH DL r
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 1 0 1 1 0 DH DL r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 1 0 1 1 1 DH DL r
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 1 1 0 0 0 DH DL1 DL2
	MVI	M	I	Move I to M	M ← I	1 1 1 0 0 1 DH DL I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1s, then skip	1 1 1 1 0 0 DH DL N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0s, then skip	1 1 1 1 0 1 DH DL N
Jump and subroutine instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 0 ADDR (13 bits)
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + 1	1 0 1 ADDR (13 bits)
	RT			Return from subroutine	PC ← Stack	0 0 0 0 0 0 0 0 1 0 0 0
	RTI			Return from interrupt	PC ← Stack, BANK ← Stack, CARRY ← Stack	0 0 0 0 0 0 0 0 1 0 0 1