Ordering number : ENN*7275

CMOS IC

LC723461W, 723462W

Ultralow-Voltage ETR Controller with On-Chip LCD Driver

Preliminary

Overview

The LC723461W and LC723462W are ultralow-voltage electronic tuning microcontrollers that include a PLL that operates up to 250 MHz and a 1/4 duty 1/2 bias LCD driver on chip. This IC includes an on-chip DC-DC converter that can easily create the power supply voltages needed for electronic tuning and contribute to reducing end product costs. This IC is optimal for portable audio equipment that must operate from a single battery.

Function

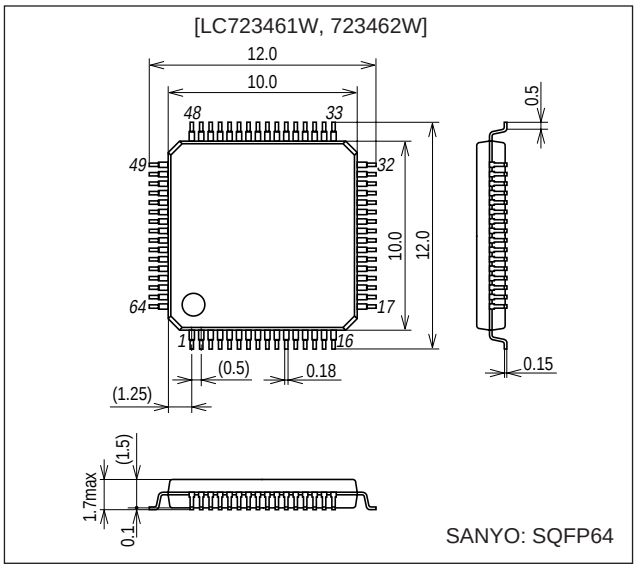
- Program memory (ROM):
  — 4096 × 16 bits (8K bytes) : LC723461
  — 6144 × 16 bits (12K bytes): LC723462
- Data memory (RAM):
  — 256 × 4 bits: LC723461
  — 512 × 4 bits: LC723462
- Cycle time:
  40 µs (all 1-word instructions) at 75kHz crystal oscillation
- Stack: 8 levels
- LCD driver: 48 to 80 segments (1/4 duty, 1/2 bias drive)
- Interrupts: Two external interrupts
  Timer interrupts (1, 5, 10, and 50 ms)
- A/D converter:
  Four input channels (8-bit chopper A/D converter. The reference voltage can be switched using the ADCHG instruction.)
- Input ports: 8 ports (of which three can be switched for use as A/D converter input and one can be switched for use as IF counter input.)
- Output ports: 6 ports (of which 1 can be switched for use as the beep tone output and 2 are open-drain ports)
- I/O ports: 19 ports (of which 8 can be switched for use as LCD ports and as mask options, of which 3 can be switched for use as serial I/O ports) Can be switched for CMOS output/open-drain outputs.
- Serial I/O: One system (LC723462)
- PLL: Reference frequencies:
  1, 3, 3.125, 5, 6.25, 12.5, and 25 kHz
- Input frequencies: FM band: 10 to 250 MHz
  AM band (high): 2 to 20 MHz
  AM band (low): 0.5 to 10 MHz
- Input sensitivity:
  FM band: 35 mVrms (10 mVrms at 130 MHz),
  50 mVrms (130 to 250 MHz)
  AM band (high, low): 35 mVrms
- IF count: HCTR input pin: 0.4 to 12 MHz (HCTR can be switched to function as a general-purpose input port.)

Continued on next page.

Package Dimensions

unit: mm

3190A-SQFP64



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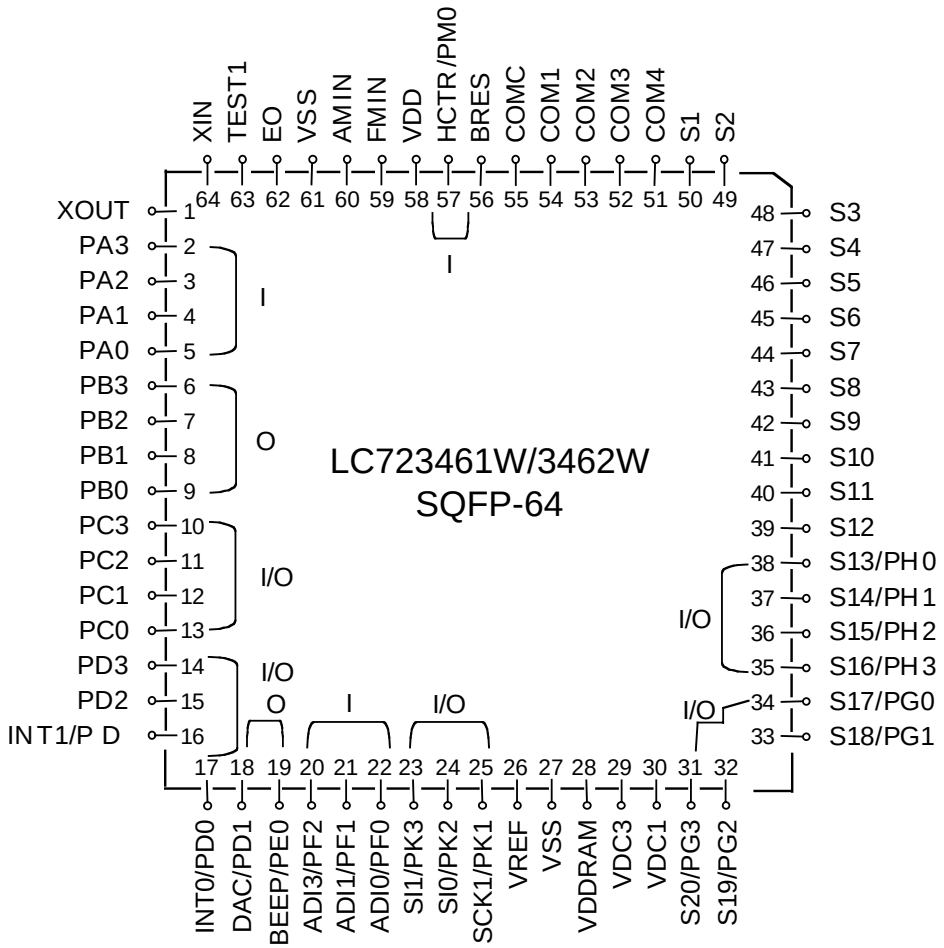
Continued from preceding page.

- External reset input: During CPU and PLL operations, instruction execution is started from location 0.
- Built-in power-on reset circuit:
  The CPU starts execution from location 0 when power is first applied.
- Halt mode: The controller-operating clock is stopped.
- Backup mode: The crystal oscillator is stopped.
- Static power-on function:
  Backup state is cleared with the PF port
- Beep tone: 1.5 and 3.1 kHz
- Built-in DC-DC converter:
  For LCD and A/D converter use (3 V)
  Can also be used for TU + B creation by using a secondary coil. (The DC-DC converter voltage step-up operation can be stopped with the DCDCC instruction.)
- Built-in remaining battery life verification function:
  Converts the V_{DD} pin level through AD converter.
- Memory retention voltage: 0.5 V or higher
- Dedicated memory power supply: The RAM retention time has been increased by the provision of a dedicated memory power supply.
- Package: SQFP-64 (0.5-mm pitch)
- V_{DD} power supply: 0.9 to 1.8 V

Pin Assignment



*: The V_{DD} pin can also function as ADI2 A/D converter input.

Specifications

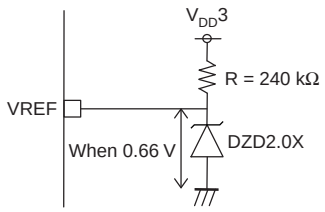
Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD}1$ max	V_{DD}	–0.3 to +3.0	V
	$V_{DD}2$ max	V_{DD}RAM	–0.3 to +4.0	V
	$V_{DD}3$ max	VDC3	–0.3 to +4.0	V
Input voltage	$V_{IN}1$	FMIN, AMIN	–0.3 to $V_{DD}1$ +0.3	V
	$V_{IN}2$	PA, PC, PD, PF, PK, PG, PH, BRES	–0.3 to $V_{DD}1$ +0.3	V
Output voltage	$V_{OUT}1$	PE	–0.3 to +7	V
	$V_{OUT}2$	PB, PC, PD, PG, PH	–0.3 to $V_{DD}1$ +0.3	V
	$V_{OUT}3$	VDC1, EO	–0.3 to $V_{DD}4$ +0.3	V
	$V_{OUT}4$	COM1 to COM4, S1 to S20	–0.3 to $V_{DD}4$ +0.3	V
Output current	$I_{OUT}1$	PC, PD, PG, PH, EO	0 to 3	mA
	$I_{OUT}2$	PB	0 to 1	mA
	$I_{OUT}3$	PE	0 to 2	mA
	$I_{OUT}4$	S1 to S20	300	µA
	$I_{OUT}5$	COM1 to COM4	3	mA
Allowable power dissipation	Pdmax	Ta = –10 to +60°C	100	mW
Operating temperature	Topr		–10 to +60	°C
Storage temperature	Tstg		–45 to +125	°C

Allowable Operating Ranges at Ta = –10 to +60°C, V_{DD} = 0.9 to 1.8 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	Voltage applied to the V_{DD} pin	0.9	1.3	1.8	V
	$V_{DD}2$	Voltage applied to the V_{DD}RAM pin	2.7	3.0	3.3	
	$V_{DD}3$	Voltage applied to the VDC3 pin (See note.)		2.7		
	$V_{DD}4$	Memory retention voltage	0.5			
VREF input voltage	$V_{REF}1$	The voltage input to the VREF pin (See note.)		0.66		V
Input high-level voltage	$V_{IH}1$	Ports PC, PD, PG, PH, and PK	0.7 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}2$	Port PA	0.8 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}3$	Port PF	0.8 $V_{DD}1$		$V_{DD}1$	V
	$V_{IH}4$	Port BRES	0.6 $V_{DD}1$		$V_{DD}1$	V
Input low-level voltage	$V_{IL}1$	Ports PC, PD, PG, PH, and PK	0		0.3 $V_{DD}1$	V
	$V_{IL}2$	Port PA	0		0.2 $V_{DD}1$	V
	$V_{IL}3$	Port PF	0		0.2 $V_{DD}1$	V
	$V_{IL}4$	Port BRES	0		0.2 $V_{DD}1$	V
Input amplitude	$V_{IN}1$	XIN	0.5		0.6	Vrms
	$V_{IN}2$	FMIN, AMIN: $V_{DD}1$ = 0.9 to 1.8 V	0.035		0.35	Vrms
	$V_{IN}3$	FMIN: $V_{DD}1$ = 0.9 to 1.8 V	0.05		0.35	Vrms
	$V_{IN}4$	ADI0, ADI1, V_{DD}, ADI3	0.035		0.35	Vrms
Input voltage range	$V_{IN}4$	ADI0, ADI1, ADI3, $V_{DD}1$	0		$V_{DD}3$	V
Input frequency	$F_{IN}1$	XIN: CI ≤ 35 kΩ	70	75	80	kHz
	$F_{IN}2$	FMIN: $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	10		130	MHz
	$F_{IN}3$	FMIN: $V_{IN}3$, $V_{DD}1$ = 0.9 to 1.8 V	130		250	MHz
	$F_{IN}4$	AMIN(L): $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	2		20	MHz
	$F_{IN}5$	AMIN(H): $V_{IN}2$, $V_{DD}1$ = 0.9 to 1.8 V	0.5		10	MHz
	$F_{IN}6$	HCTR: $V_{IN}4$, $V_{DD}1$ = 0.9 to 1.8 V	0.4		12	MHz

Note:

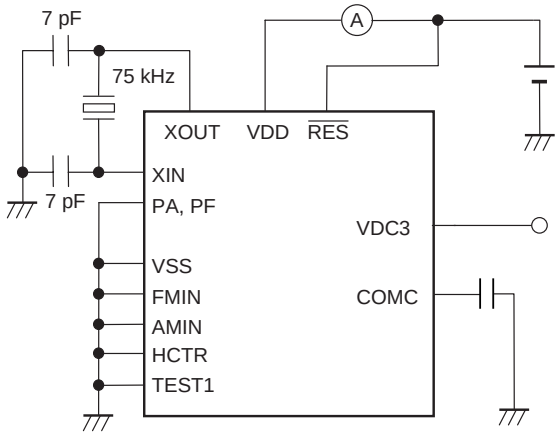


Electrical Characteristics within allowable operating conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	$I_{IH}1$	XIN: $V_{DD}1$ = 1.3 V			3	µA
	$I_{IH}2$	FMIN, AMIN, HCTR: $V_{DD}1$ = 1.3 V	3	8	20	µA
	$I_{IH}3$	Port PF: $V_{DD}1$ = 1.3 V			4	µA
	$I_{IH}4$	PA (without pull-down resistors), the PC, PD, PG, and PH ports, and BRES, PK: $V_{DD}1$ = 1.3 V			3	µA
Input low-level current	$I_{IL}1$	XIN: $V_{DD}1 = V_{SS}$			–3	µA
	$I_{IL}2$	FMIN, AMIN, HCTR: $V_{DD}1 = V_{SS}$	–3	–8	–20	µA
	$I_{IL}3$	Port PF: $V_{DD}1 = V_{SS}$			–4	µA
	$I_{IL}4$	PA (without pull-down resistors), the PC, PD, PG, and PH ports, and BRES, PK: $V_{DD}1 = V_{SS}$			–3	µA
Input floating voltage	V_{IF}	PA (with pull-down resistors)			0.05 $V_{DD}1$	V
Pull-down resistor values	$R_{PD}1$	PA (with pull-down resistors), $V_{DD}1$ = 1.3 V	75	100	200	kΩ
	$R_{PD}2$	TEST1 (with pull-down resistor), $V_{DD}1$ = 1.3 V		10		kΩ
Hysteresis	V_H	BRES	0.1 $V_{DD}1$	0.2 $V_{DD}1$		V
Output high-level voltage	$V_{OH}1$	PB: I_O = 1 mA	$V_{DD}1$ – 0.7 V_{DD}		$V_{DD}1$ – 0.3 V_{DD}	V
	$V_{OH}2$	PC, PD, PG and PH: I_O = 1 mA	$V_{DD}1$ – 0.3 $V_{DD}1$			V
	$V_{OH}3$	EO: I_O = 500 µA	$V_{DD}3$ – 0.3 $V_{DD}3$			V
	$V_{OH}4$	XOUT: I_O = 200 µA	$V_{DD}1$ – 0.3 $V_{DD}1$			V
	$V_{OH}5$	S1 to S20: I_O = 20 µA	$V_{DD}3$ –1			V
	$V_{OH}6$	COM1, COM2, COM3, COM4: I_O = 100 µA	$V_{DD}3$ –1			V
	$V_{OH}7$	VDC1: I_O = 1 mA	$V_{DD}3$ –1			V
Output low-level voltage	$V_{OL}1$	PB: I_O = –50 µA	0.3 $V_{DD}1$		0.7 $V_{DD}1$	V
	$V_{OL}2$	PC, PD, PG, PH: I_O = –1 mA			0.3 $V_{DD}1$	V
	$V_{OL}3$	EO: I_O = –500 µA			0.3 $V_{DD}3$	V
	$V_{OL}4$	XOUT: I_O = –200 µA			0.3 $V_{DD}1$	V
	$V_{OL}5$	S1 to S20: I_O = –20 µA			$V_{DD}3$ –2	V
	$V_{OL}6$	COM1, COM2, COM3, COM4: I_O = –100 µA			$V_{DD}3$ –2	V
	$V_{OL}7$	PE: I_O = 2 mA			0.6 $V_{DD}1$	V
	$V_{OL}8$	VDC1: I_O = 1 mA			1	V
Output off leakage current	$I_{OFF}1$	Ports PB, PC, PD, PG and EO	–3		+3	µA
	$I_{OFF}2$	Port PE	–100		+100	nA
A/D converter error		When the reference voltage is 2.7 V: ADI0, ADI1, $V_{DD}1$, ADI3. Ta = 25°C	–1		+1	LSB
		When the reference voltage is 2.0 V: ADI0, ADI1, $V_{DD}1$, ADI3. Ta = 25°C Note: Linearity is maintained in the converted data.	–1		+1	LSB
Current drain	$I_{DD}1$	$V_{DD}1$ = 1.3 V: $F_{IN}2$ 130 MHz, Ta = 25°C		2		mA
	$I_{DD}3$	$V_{DD}1$ = 1.3 V: In HALT mode, Ta = 25°C *1		0.1		mA
	$I_{DD}4$	$V_{DD}1$ = 1.8 V, with the oscillator stopped, Ta = 25°C *2		1		µA
VDC3 current	$I_{DC3}1$	Vdd3 = 2.7 V: Halt mode, Ta = 25°C		100		µA

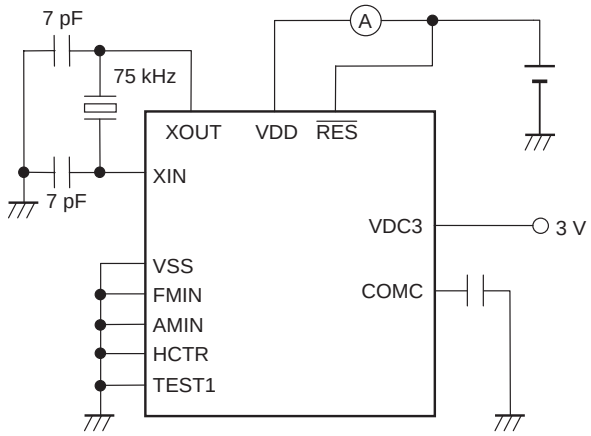
Note*: The halt mode current drain is due to 20 instructions being executed every 125 ms.

*1. Halt and PLL STOP mode current test circuit



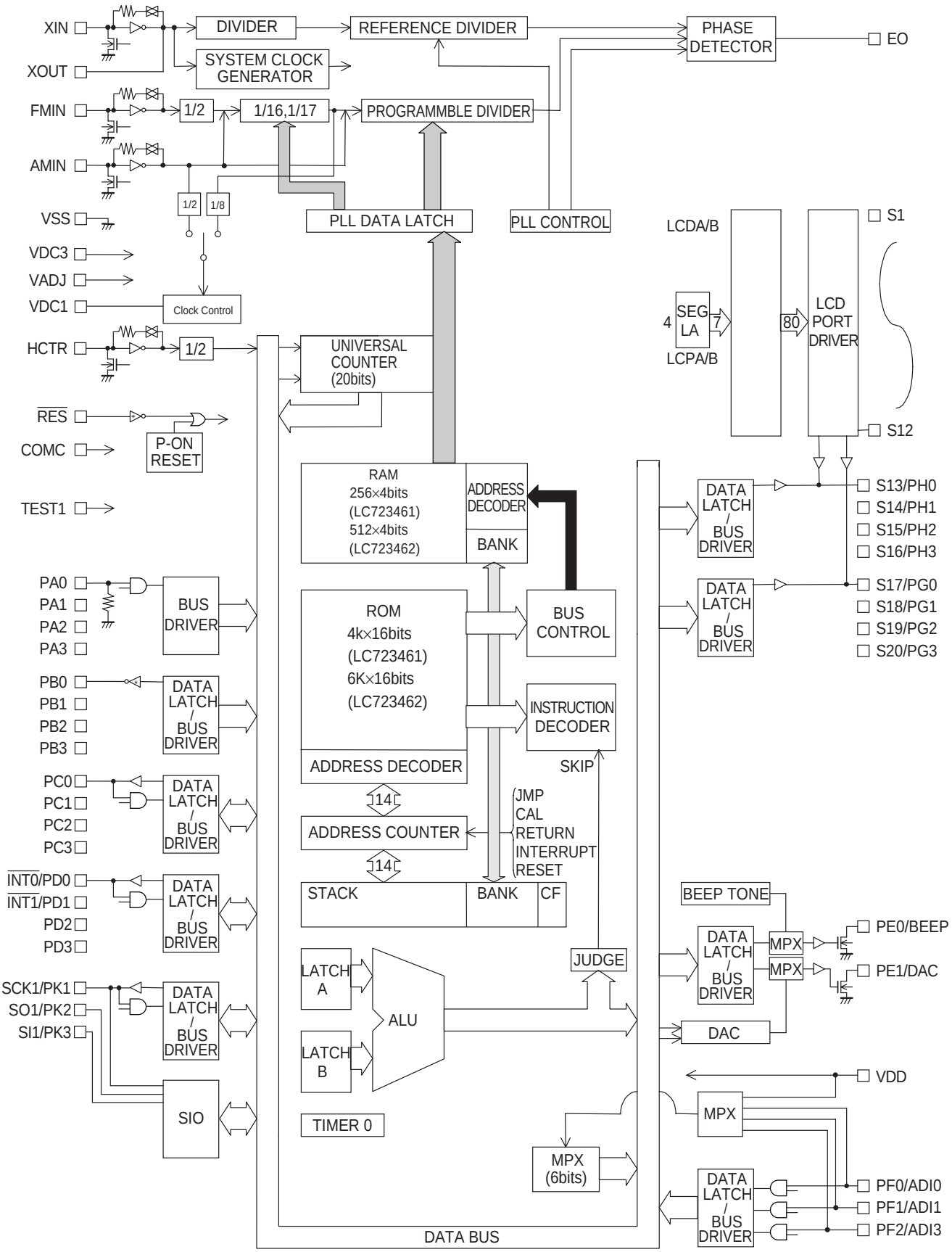
With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S20 selected.
Enter halt mode by software command.
The state where CPU operation is stopped with the crystal oscillator unstopped.

*2. Backup mode current test circuit

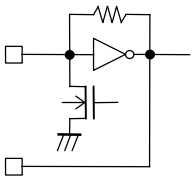
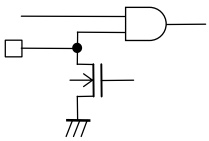
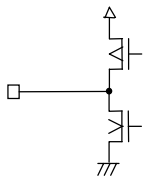
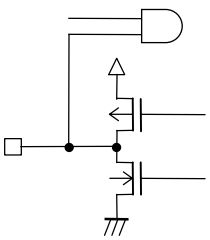
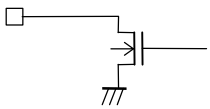
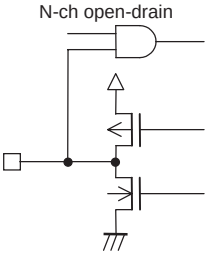


With all ports other than those specified above left open.
With output mode selected for PC and PD.
With segments S13 to S20 selected.
Enter backup mode by software command.
The state where the crystal oscillator is stopped.

Block Diagram



Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
64 1	XIN XOUT	I O	75 kHz oscillator connections	
63	TEST1	I	IC testing. This pin must be connected to ground.	—
5 4 3 2	PA0 PA1 PA2 PA3	I	Special-purpose ports for key return signal input designed with a low threshold voltage. When a key matrix is formed in combination with port PB, simultaneous multiple key presses with up to 3 keys can be detected. The pull-down resistors are set up for all four pins at the same time with the IOS instruction. This setting cannot be specified for individual pins. In backup mode, these pins go to the input disabled state, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor 
9 8 7 6	PB0 PB1 PB2 PB3	O	Unbalanced CMOS outputs. Since these outputs are unbalanced, no diodes are required to prevent short circuits due to simultaneous multiple key presses. These outputs go to the high-impedance output state in backup mode. After a reset, they go to the high-impedance output state and remain in that state until an output instruction (OUT, SPB, or RPB) is executed.	Unbalanced CMOS push-pull 
13 12 11 18 17 16 15 14	PC0 PC1 PC2 PC3 $\overline{\text{INT1}}$/PD0 $\overline{\text{INT0}}$/PD1 PD2 PD3	I/O	General-purpose I/O ports. Note that there is a mask option that allows these pins to be used as n-channel open drain ports. PD0, PD1 can be used as an external interrupt port. The IOS instruction (Pwn = 4, 5) is used for switching the general-purpose I/O port function, and these ports can be set to input or output in 1-bit units. (0: input, 1: output) In backup mode they go to the input disabled high-impedance state. After a reset, they switch to the general-purpose input port function.	CMOS push-pull/ N-ch open-drain 
19 18	BEEP/PE0 DAC/PE1	O	General-purpose output ports. Note that PE0 has a shared function as the BEEP output, and that PE1 has a shared function as a D/A converter output port. Since these ports are open drain ports, a resistor must be inserted between each port and VDD. At reset, they are set to the general-purpose output port function .The BEEP instruction is used to switch the BEEP/PE0 port between the general-purpose output port and the BEEP output functions. A BEEP instruction with b2 = 0 will set the BEEP/PE0 port to function as a general-purpose output port. If b2 is set to 1, the instruction will select the BEEP output function. Bits b0 and b1 switch the frequency of the BEEP output. This IC supports two BEEP frequencies. *: When the PE0 port is set to function as the BEEP output, executing an output instruction for PE0 will only change the value of the internal output latch; it will have no effect on the output. The DAC instruction is used to switch the DAC/PE1 port between the general-purpose output port and DAC output functions. These ports go to the high-impedance state in backup mode. That state is maintained until an output instruction, a BEEP instruction, or a DAC instruction is executed.	N-ch open-drain 
25 24 23	SCK1/PK1 SO1/PK2 SI1/PK3	I/O	Shared function pins used as either general-purpose I/O ports or a serial I/O port. Note that there is a mask option that allows these pins to be used as n-channel open drain ports. When used as general-purpose I/O ports, the I/O direction can be switched in single pin units with the IOS instruction. The IOS instruction is used to switch the function between the general-purpose I/O port and the serial I/O port function. In backup mode, these pins go to the input disabled high-impedance state. After a reset, the general-purpose input port function is selected.	CMOS push-pull/ N-ch open-drain 

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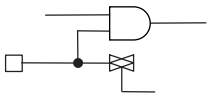
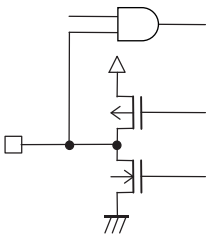
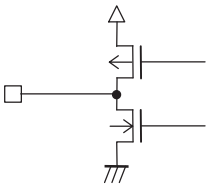
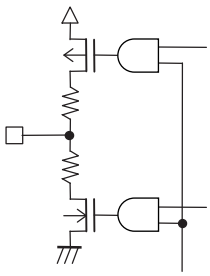
Pin No.	Pin	I/O	Function	I/O circuit
22 21 20	PF0/ADI0 PF1/ADI1 PF2/ADI3	I	General-purpose input and A/D converter input shared function ports. The IOS instruction is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a units, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data. *: If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 8-bit successive approximation type converter, and features a conversion time of 0.64 ms. Note that the full-scale A/D converter voltage (FFH) is VDC3/2.0 V.	CMOS input/analog input 
31 32 33 34 35 36 37 38	PG3/S20 PG2/S19 PG1/S18 PG0/S17 PH3/S16 PH2/S15 PH1/S14 PH0/S13 *2	O	LCD driver segment output and general-purpose I/O shared function ports. The IOS instruction is used for switching between the segment output and general-purpose I/O functions and between input and output for the general-purpose I/O port function. • When used as segment output ports The segment output port is selected with the IOS instruction (Pwn = 8). b0 to b3 = S17 to 20/PG0 to 3 (0: Segment output, 1: PG0 to 3) The segment output port is selected with the IOS instruction (Pwn = 9). b0 to b3 = S13 to 16/PH0 to 3 (0: Segment output, 1: PH0 to 3) • When used as general-purpose I/O ports The IOS instruction is used to select input or output. Note that the mode can be set in a bit units. b0 = PG0 b0 = PH0 b1 = PG1 b1 = PH1 b2 = PG2 b2 = PH2 b3 = PG3 b3 = PH3 0: Input 1: Output Note that there is a mask option that allows these pins to be used as n-channel open drain ports. In backup mode, these pins go to the input disabled high-impedance state if set up as general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset. Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function.	CMOS push-pull 
39 to 50	S12 to S1	O	LCD driver segment output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	CMOS push-pull 
51 52 53 54	COM4 COM3 COM2 COM1	O	LCD driver common output pins. A 1/4-duty 1/2-bias drive technique is used. The frame frequency is 75 Hz. In backup mode, these outputs are fixed at the low level. After a reset, these outputs are fixed at the low level.	

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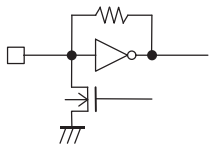
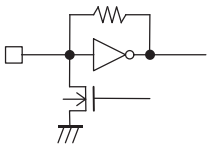
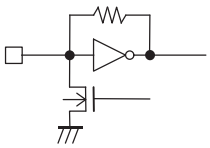
<table>
<tr><th>Pin No.</th><th>Pin</th><th>I/O</th><th>Function</th><th>I/O circuit</th></tr>
<tr><td>56</td><td>$\overline{\text{RES}}$</td><td>I</td><td>System reset input.
In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit.</td><td>  </td></tr>
<tr><td>28</td><td>VDDRAMVADJ</td><td>I</td><td>RAM backup power supply. Connected to the VDC3 voltage through a diode.</td><td></td></tr>
<tr><td>30</td><td>VDC1</td><td>O</td><td>Output for the 3 V step-up circuit clock. Outputs 1/2 the AM local oscillator frequency in AM reception mode, and 1/256 the FM local oscillator or 75 kHz in FM reception mode.</td><td></td></tr>
<tr><td>29</td><td>VDC3</td><td>I</td><td>Voltage stepped up by the DC-DC converter (3 V)
May also be used to input an equivalent voltage.</td><td></td></tr>
<tr><td>26</td><td>VREF</td><td>I</td><td>VDC3 reference voltage input.
When 0.7 V is input, the VDC3 voltage will be 3 V.
The VDC3 sample-to-sample variations can be held to ±3% by attaching an external metal-film resistor and a zener diode.</td><td></td></tr>
<tr><td>55</td><td>COMC</td><td>O</td><td>LCD driver intermediate potential output.
The COM waveform must be stabilized by attaching an external capacitor of about 0.1 µF.</td><td></td></tr>
<tr><td>59</td><td>FMIN</td><td>I</td><td>FM VCO (local oscillator) input.
This pin is selected with the PLL instruction CW1.
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>60</td><td>AMIN</td><td>I</td><td>AM VCO (local oscillator) input.
This pin and the bandwidth are selected with the PLL instruction CW1.
<table>
<tr><th>CW1 b1, b0</th><th>Input pins</th><th>Bandwidth</th></tr>
<tr><td>1 1</td><td>FMIN (L)</td><td>0.5 to 10 MHz (MW, LW)</td></tr>
</table>
The input must be capacitor coupled.
Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.</td><td>CMOS amplifier input
  </td></tr>
<tr><td>57</td><td>HCTR</td><td>I</td><td>General-purpose input and universal counter input shared-function port. The IOS instruction is used to switch between the general-purpose input port and the universal counter input functions.
• When performing frequency measurements, select the HCTR frequency measurement mode and the measurement time with the UCS instruction (b3 = 0, b2 = 0), and start the count with the UCC instruction.
<table>
<tr><th>UCS b3, b2</th><th>Input pins</th><th>Measurement mode</th></tr>
<tr><td>0 0</td><td>HCTR</td><td>Frequency measurement</td></tr>
<tr><td>0 1</td><td>—</td><td></td></tr>
<tr><td>1 0</td><td>—</td><td></td></tr>
</table>
<table>
<tr><th>UCS b1, b0</th><th>Measurement time</th></tr>
<tr><td>0 0</td><td>1 ms</td></tr>
<tr><td>0 1</td><td>4 ms</td></tr>
<tr><td>1 0</td><td>8 ms</td></tr>
<tr><td>1 1</td><td>32 ms</td></tr>
</table>
The CNTEND flag is set when the count completes. Since this circuit operates as an AC amplifier in this mode, the input signal must be capacitor coupled.
When used as a general-purpose input, the input data is acquired with the INR instruction.
Input is disabled in backup mode, halt mode, during a reset, and in PLL stop mode. Note that after a reset, the universal counter input port function will be selected.</td><td>CMOS amplifier input
  </td></tr>
</table>

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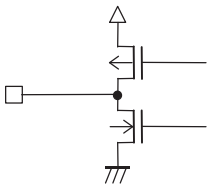
Pin No.	Pin	I/O	Function	I/O circuit
62	EO	O	Main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output,and the pin is set to the high-impedance state when the frequencies match. This output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.	CMOS push-pull 
61 27 58	V_{SS} V_{SS} V_{DD}	—	Power supply pin. This pin must be connected to ground. This pin must be connected to ground. This pin must be connected to V_{DD}. Supports A/D converter.	—

Note*: When a pin in an I/O switching port is used as an output, applications must first set up the data with an OUT, SPB, or RPB instruction and then set up output mode with an IOS instruction.

LC723461W/723462W Series Instruction Set

Terminology

ADDR : Program memory address
b : Borrow
C : Carry
DH : Data memory address High (Row address) [2 bits]
DL : Data memory address Low (Column address) [4 bits]
I : Immediate data [4 bits]
M : Data memory address
N : Bit position [4 bits]
Rn : Resister number [4 bits]
Pn : Port number [4 bits]
PW : Port control word number [4 bits]
r : General register (One of the addresses from 00H to 0FH of BANK0)
( ), [ ] : Contents of register or memory
M (DH, DL) : Data memory specified by DH, DL

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format															
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
Addition instructions	AD	r	M	Add M to r	r ← (r) + (M)	0	1	0	0	0	0	DH		DL				r			
	ADS	r	M	Add M to r, then skip if carry	r ← (r) + (M), skip if carry	0	1	0	0	0	1	DH		DL				r			
	AC	r	M	Add M to r with carry	r ← (r) + (M) + C	0	1	0	0	1	0	DH		DL				r			
	ACS	r	M	Add M to r with carry, then skip if carry	r ← (r) + (M) + C skip if carry	0	1	0	0	1	1	DH		DL				r			
	AI	M	I	Add I to M	M ← (M) + I	0	1	0	1	0	0	DH		DL				I			
	AIS	M	I	Add I to M, then skip if carry	M ← (M) + I, skip if carry	0	1	0	1	0	1	DH		DL				I			
	AIC	M	I	Add I to M with carry	M ← (M) + I + C	0	1	0	1	1	0	DH		DL				I			
	AICS	M	I	Add I to M with carry, then skip if carry	M ← (M) + I + C, skip if carry	0	1	0	1	1	1	DH		DL				I			
Subtraction instructions	SU	r	M	Subtract M from r	r ← (r) – (M)	0	1	1	0	0	0	DH		DL				r			
	SUS	r	M	Subtract M from r, then skip if borrow	r ← (r) – (M), skip if borrow	0	1	1	0	0	1	DH		DL				r			
	SB	r	M	Subtract M from r with borrow	r ← (r) – (M) – b	0	1	1	0	1	0	DH		DL				r			
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	r ← (r) – (M) – b, skip if borrow	0	1	1	0	1	1	DH		DL				r			
	SI	M	I	Subtract I from M	M ← (M) – I	0	1	1	1	0	0	DH		DL				I			
	SIS	M	I	Subtract I from M, then skip if borrow	M ← (M) – I, skip if borrow	0	1	1	1	0	1	DH		DL				I			
	SIB	M	I	Subtract I from M with borrow	M ← (M) – I – b	0	1	1	1	1	0	DH		DL				I			
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	M ← (M) – I – b, skip if borrow	0	1	1	1	1	1	DH		DL				I			
Comparison instructions	SEQ	r	M	Skip if r equal to M	(r) – (M), skip if zero	0	0	0	1	0	0	DH		DL				r			
	SEQI	M	I	Skip if M equal to I	(M) – I, skip if zero	0	0	0	1	1	0	DH		DL				I			
	SNEI	M	I	Skip if M not equal to I	(M) – I, skip if not zero	0	0	0	0	0	1	DH		DL				I			
	SGE	r	M	Skip if r is greater than or equal to M	(r) – (M), skip if not borrow	0	0	0	1	1	0	DH		DL				r			
	SGEI	M	I	Skip if M is greater than equal to I	(M) – I, skip if not borrow	0	0	0	1	1	1	DH		DL				I			
	SLEI	M	I	Skip if M is less than I	(M) – I, skip if borrow	0	0	0	0	1	1	DH		DL				I			

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f e d c b a 9 8 7 6 5 4 3 2 1 0
Logic operation instructions	AND	r	M	AND M with r	r ← (r) AND (M)	0 0 1 0 0 0 DH DL r
	ANDI	M	I	AND I with M	M ← (M) AND I	0 0 1 0 0 1 DH DL I
	OR	r	M	OR M with r	r ← (r) OR (M)	0 0 1 0 1 0 DH DL r
	ORI	M	I	OR I with M	M ← (M) OR I	0 0 1 0 1 1 DH DL I
	EXL	r	M	Exclusive OR M with r	r ← (r) XOR (M)	0 0 1 1 0 0 DH DL r
	EXLI	M	I	Exclusive OR M with M	M ← (M) XOR I	0 0 1 1 1 0 DH DL I
	SHR	r		Shift r right with carry	carry (r)	0 0 0 0 0 0 0 0 1 1 1 0 r
Transfer instructions	LD	r	M	Load M to r	r ← (M)	1 1 0 1 0 0 DH DL r
	ST	M	r	Store r to M	M ← (r)	1 1 0 1 0 1 DH DL r
	MVRD	r	M	Move M to destination M referring to r in the same row	[DH, Rn] ← (M)	1 1 0 1 1 0 DH DL r
	MVRS	M	r	Move source M referring to r to M in the same row	M ← [DH, Rn]	1 1 0 1 1 1 DH DL r
	MVSR	M1	M2	Move M to M in the same row	[DH, DL1] ← [DH, DL2]	1 1 1 0 0 0 DH DL1 DL2
	MVI	M	I	Move I to M	M ← I	1 1 1 0 0 1 DH DL I
Bit test instructions	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1 1 1 1 0 0 DH DL N
	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1 1 1 1 0 1 DH DL N
Jump and subroutine call instructions	JMP	ADDR		Jump to the address	PC ← ADDR	1 0 0 ADDR (13 bits)
	CAL	ADDR		Call subroutine	PC ← ADDR Stack ← (PC) + 1	1 0 1 ADDR (13 bits)
	RT			Return from subroutine	PC ← Stack	0 0 0 0 0 0 0 0 1 0 0 0
	RTI			Return from interrupt	PC ← Stack, BANK ← Stack, CARRY ← Stack	0 0 0 0 0 0 0 0 1 0 0 1
Status register instructions	SS	SWR	N	Set status register	(Status W-reg) N ← 1	1 1 1 1 1 1 1 1 0 0 0 SWR N
	RS	SWR	N	Reset status register	(Status W-reg) N ← 0	1 1 1 1 1 1 1 1 0 0 1 SWR N
	TST	SRR	N	Test status register true	If (Status R-reg) N = all 1, then skip	1 1 1 1 1 1 1 1 0 1 SRR N
	TSF	SRR	N	Test status register false	If (Status R-reg) N = all 0, then skip	1 1 1 1 1 1 1 1 1 0 SRR N
	TUL	N		Test Unlock F/F	If Unlock F/F (N) = All 0, then skip	0 0 0 0 0 0 0 0 1 1 0 1 N
Hardware control instructions	PLL	M		Load M to PLL register	PLL reg ← PLL data	1 1 1 1 1 0 DH DL r
	SIO	I1			SIO reg ← I1, I2	0 0 0 0 0 0 0 1 I1 I2
	UCS	I		Set I to UCCW1	UCCW1 ← I	0 0 0 0 0 0 0 0 0 0 0 1 I
	UCC	I		Set I to UCCW2	UCCW2 ← I	0 0 0 0 0 0 0 0 0 0 1 0 I
	BEEP	I		Beep control	BEEP reg ← I	0 0 0 0 0 0 0 0 0 1 1 0 I
	DZC	I		Dead zone control	DZC reg ← I	0 0 0 0 0 0 0 0 1 0 1 1 I
	TMS	I		Set timer register	Timer reg ← I	0 0 0 0 0 0 0 0 1 1 0 0 I
	IOS	PWn	N	Set port control word	IOS reg PWn ← N	1 1 1 1 1 1 1 0 PWn N
	DAC	I		DA converter control	DAC reg ← DAC data	0 0 0 0 0 0 0 0 0 0 1 1 I
I/O instructions	IN	M	Pn	Input port data to M	M ← (Pn)	1 1 1 0 1 0 DH DL Pn
	OUT	M	Pn	Output contents of M to port	P1n ← M	1 1 1 0 1 1 DH DL Pn
	INR	M	Pn	Input register/port data to M	M ← (Pn)	0 0 1 1 1 0 DH DL Pn
	SPB	P1n	N	Set port1 bits	(Pn)N ← 1	0 0 0 0 0 0 1 0 Pn N
	RPB	P1n	N	Reset port1 bits	(Pn)N ← 0	0 0 0 0 0 0 1 1 Pn N
	TPT	P1n	N	Test port1 bits, then skip if all bits specified are true	If (Pn)N = all 1, then skip	1 1 1 1 1 1 0 0 Pn N
	TPF	P1n	N	Test port1 bits, then skip if all bits specified are false	If (Pn)N = all 0, then skip	1 1 1 1 1 1 0 1 Pn N
Bank switching instructions	BANK	I		Select Bank	BANK ← I	0 0 0 0 0 0 0 0 0 1 1 1 I

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Instruction group	Mnemonic	Operand 1st	Operand 2nd	Function	Operations function	Instruction format f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
LCD instructions	LCDA	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1	1	0	0	0	0	DH		DL				DIGIT			
	LCDB	M	I			1	1	0	0	0	1	DH		DL				DIGIT			
	LCPA	M	I	Output segment pattern to LCD digit through LA	LCD (DIGIT) ← LA ← M	1	1	0	0	1	0	DH		DL				DIGIT			
	LCPB	M	I			1	1	0	0	1	1	DH		DL				DIGIT			
Other instructions	ADCHG	I		AD converter reference voltage change		1	1	1	1	1	1	1	1	1	1	1	0	I			
	DCDCC	I		DC/DC clock control		0	0	0	0	0	0	0	0	1	1	1	1	I			
	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0	0	0	0	0	0	0	0	0	1	0	0	I			
	CKSTP			Clock stop	Stop x'tal OSC	0	0	0	0	0	0	0	0	0	1	0	1				
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0	0				