Ordering number:ENN3725

CMOS IC

LC7470

Character and Pattern Display Control IC

Overview

Character and pattern display control IC for TV screen. A character dot configuration is 12 × 18. The IC has 64 internal character ROMs and displays up to 288 characters (24 characters × 12 lines) on a TV screen. It can be controlled by a microcontroller.

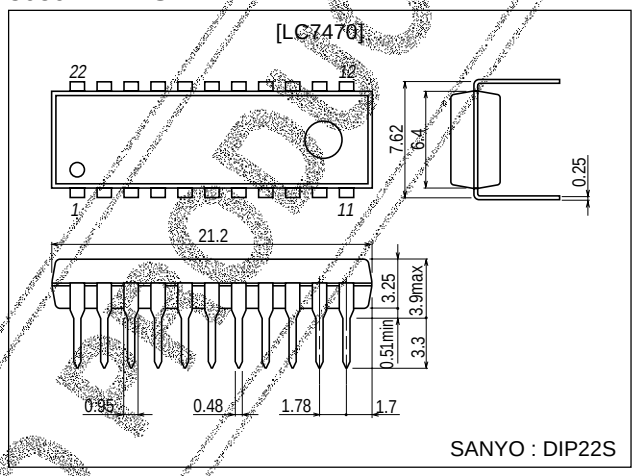
Function and Applications

- Screen Display Mode: 24 characters × 12 lines
- Number of display characters: 288 characters (max.)
- Display control ROM (line ROM):
  64 lines (line control: 24-character line)
- Display RAM:
  176 characters (used for specifying variable characters)
- Character configuration:
  12 (horizontal) × 18 (vertical) dots
- Number of character types: 64 types
- Character size:
  Horizontal direction: 4, Vertical direction: 4
- Display start position:
  Horizontal direction: 64, Vertical direction: 64
- Blinking mode: Character blinking
- Display ON/OFF mode:
  ON/OFF cycle; 1.0 second and 0.5 second. Duty cycle; 25%, 50% and 75%
- Blanking mode: Entire font area (12 × 18 dots)
- Background colors: 4 (at internal SYNC. operation mode)
- External control input: Serial data input
- Synchronous signal: Selectable: Internal and External
- Internal SYNC. separation circuit available.
- Video output: NTSC-format composite output
- Superimpose function:
  Superimposes character output on composite video output

Package Dimensions

unit:mm

3059-DIP22S



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Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings	Unit
Maximum supply voltage	V_{DD}	V_{DD1}, V_{DD2}	$V_{SS}-0.3$ to $V_{SS}+7.0$	V
Maximum input voltage	V_{IN}	All input pins	$V_{SS}-0.3$ to $V_{DD1}+0.3$	V
Maximum output voltage	V_{OUT}		$V_{SS}-0.3$ to $V_{DD1}+0.3$	V
Allowable power dissipation	Pd max	Ta = 25˚C	300	mW
Operating temperature	Topr		–30 to +70	˚C
Storage temperature	Tstg		–40 to +125	˚C

Reommended Operating Conditions at Ta = –30 to +70˚C

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	Pin V_{DD1}	4.5	5.0	5.5	V
	V_{DD2}	Pin V_{DD2}	4.5	5.0	$1.27V_{DD1}$	V
Input high-level voltage	V_{IH2}	Pins $\overline{CS}$, SIN, $\overline{RST}$, SCLK	$0.8V_{DD1}$		$V_{DD1}+0.3$	V
Input low-level voltage	V_{IL2}	Pins $\overline{CS}$, SIN, $\overline{RST}$, SCLK	$V_{SS}-0.3$		$0.2V_{DD1}$	V
Composite video input voltage	V_{IN1}	CV_{IN}		2Vp-p		V
	V_{IN2}	Pin SYNI		2Vp-p	2.5Vp-p	
Oscillation frequency	F_{OSC1}	Xtal oscillation pin (at $4f_{OSC}$)		14.31		MHz
	F_{OSC2}	Xtal oscillation pin (at $2f_{OSC}$)		7.16		MHz
	F_{OSC3}	LC oscillation pin		7		MHz

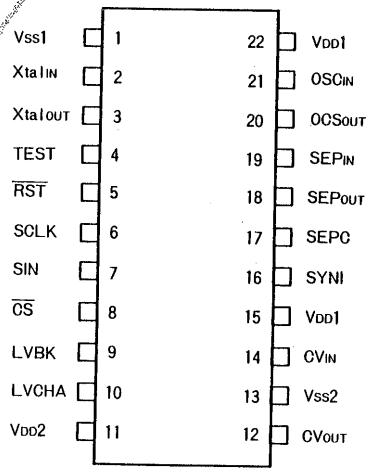
Electrical Characteristics at Ta = –30 C to +70˚C, and V_{DD} = 5V, unless other noted

Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Output-off leakage current	I_{leak}	CV_{OUT}			10	µA
Output high-level voltage	V_{IH1}	SEP_{OUT}, V_{DD}=4.5V, I_{OH}=1.0mA	3.5			V
Output low-level voltage	V_{IL1}	SEP_{OUT}, V_{DD}=4.5V, I_{OL}=1.0mA			1.0	V
Input current	I_{IH}	$\overline{CS}$, SIN, $\overline{RST}$, SCLK,SEPIN, $V_{IN}=V_{DD}$			1	µA
	I_{IL}	OSCIN, $V_{IN}=V_{SS}$	–1			µA
Operating current drain	I_{DD}				15	mA

Timing Characteristics at Ta = –30 to +70˚C, V_{DD} = 5±0.5V

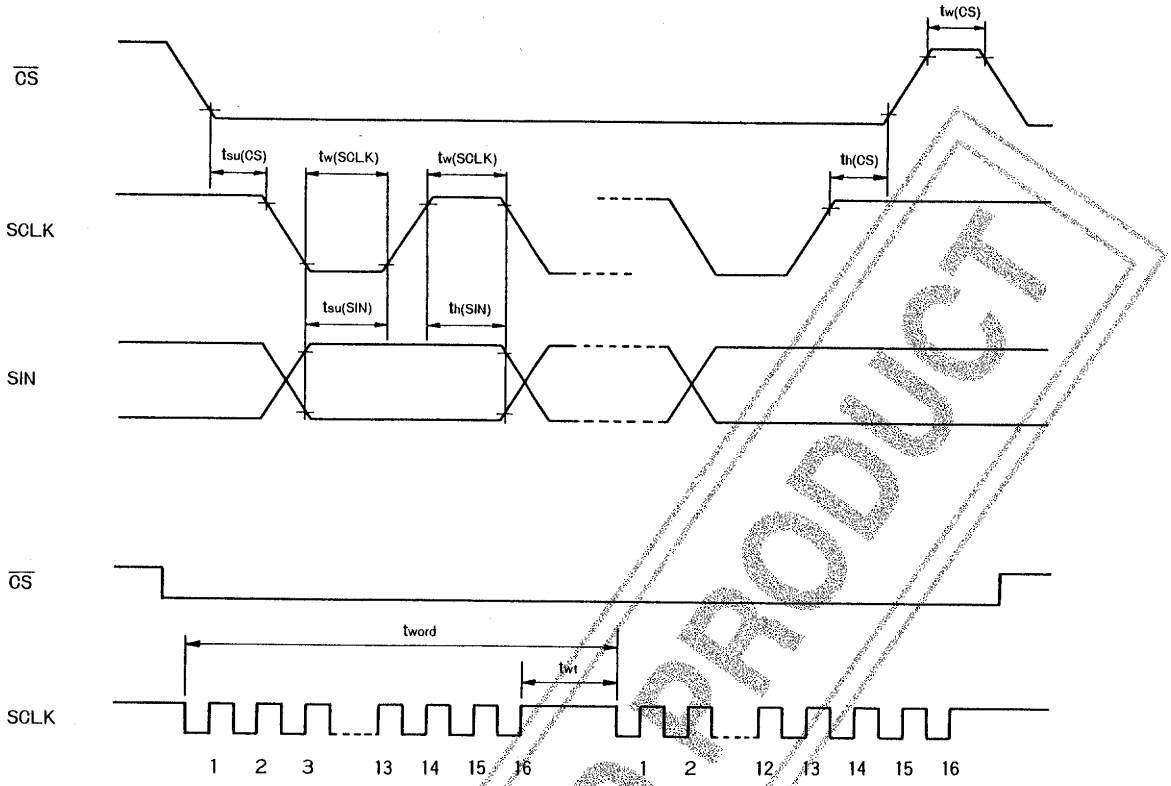
Parameter	Symbol	Condition	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{w(SCLK)}$	SCLK	200			ns
	$t_{w(CS)}$	$\overline{CS}$ ($\overline{CS}$=H-level period)	1			µs
Data setup time	$t_{su(CS)}$	$\overline{CS}$	200			ns
	$t_{su(SIN)}$	SIN	200			ns
Data hold time	$t_{h(CS)}$	$\overline{CS}$	2			µs
	$t_{h(SIN)}$	SIN	200			ns
1-word write period	t_{word}	16-bit data write period	10			µs
	t_{wt}	RAM data write period	1			µs

Pin Assignment



Top view

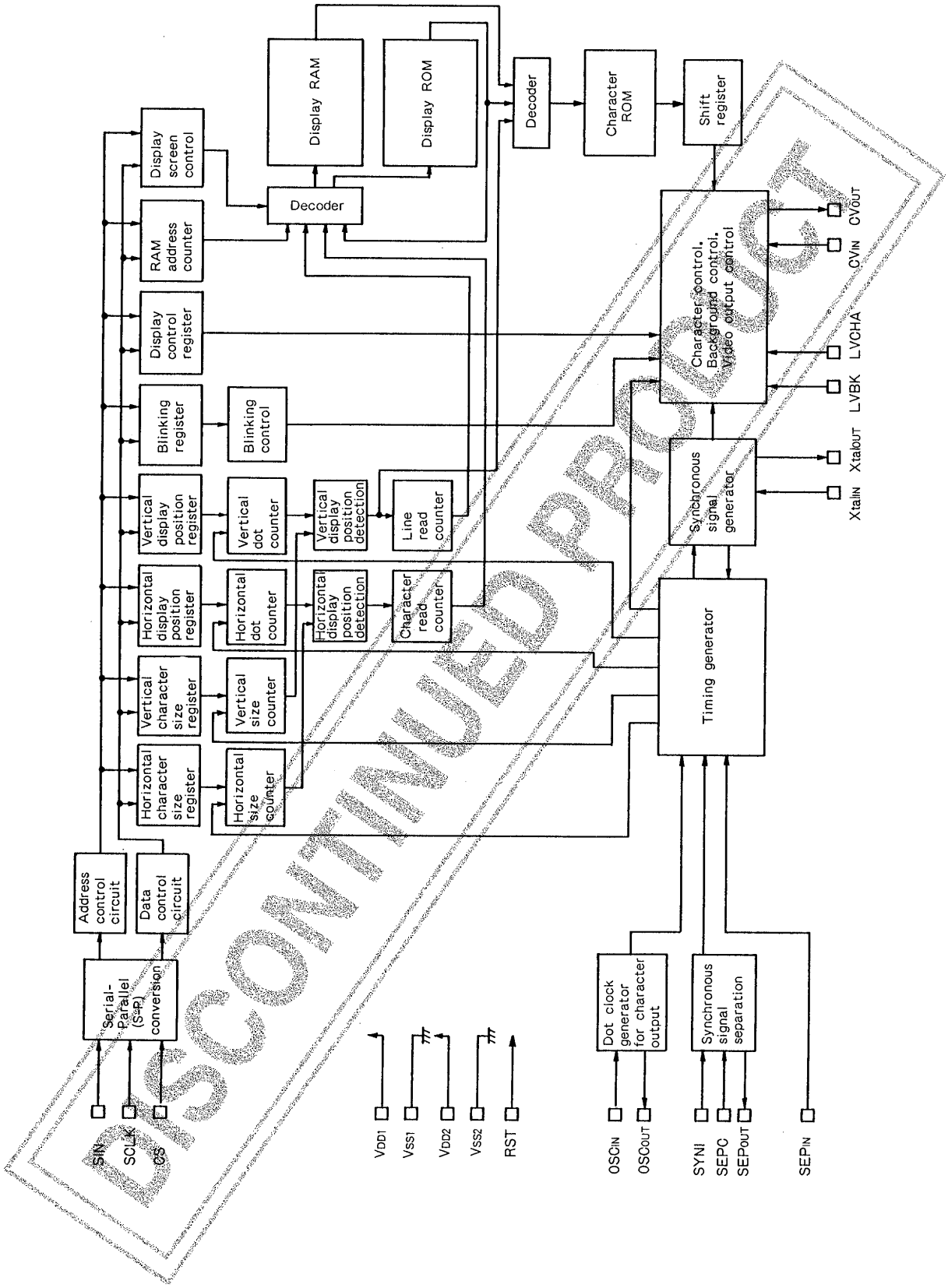
Serial Data Input Timings



Pin Description

Pin No.	Pin symbol	Pin Name	Functions
1	V_{SS1}	Ground pin	GND pin (digital grounding)
2	$Xtal_{IN}$	Xtal oscillation pin	Oscillation pins for connecting a crystal oscillator and capacitor to generate internal synchronous signals
3	$Xtal_{OUT}$		
4	TEST	Test pin	Test output pin
5	$\overline{RST}$	Reset input pin	System reset input pin
6	SCLK	Clock input pin	Clock input pin for serial data input
7	SIN	Data input pin	Serial data input pin. Serial 16-bit data input is supported
8	$\overline{CS}$	Enable input pin	Enable input pin for serial data input. If this pin becomes active (active low), the serial data input is enabled
9	LVBK	Input pin for blank level adjustment	Level input pin for adjusting blank levels
10	LVCHA	Input pin for character level adjustment	Level input pin for adjusting character levels
11	V_{DD2}	Power supply pin	Power supply pin for adjusting composite video signal levels (analog power supply)
12	CV_{OUT}	Video signal output pin	Output pin for composite video signal
13	V_{SS2}	Ground pin	GND pin (analog grounding)
14	CV_{IN}	Video signal input pin	Input pin for composite video signal
15	V_{DD1}	Supply voltage pin	Supply voltage pin (+5V)
16	SYNI	Synchronous signal separation circuit input pin	Input pin for synchronous signal separation circuit
17	SEPC	Synchronous signal separation circuit adjustment pin	Adjustment pin for synchronous signal separation circuit (A capacitor is connected to this pin)
18	SEP_{OUT}	Composite synchronous signal output pin	Composite synchronous signal output pin for synchronous signal separation circuit
19	SEP_{IN}	Vertical synchronous signal input pin	Vertical synchronous signal input pin. The input signal to this pin is generated by integrating the output signal from the SEPOUT pin. Add an integral circuit between the SEPOUT pin and the SEPIN pin
20	OSC_{OUT}	LC oscillation pin	Oscillation pins for connecting a coil and capacitor to generate character output dot clocks
21	OSC_{IN}		
22	V_{DD1}	Supply voltage pin (+5V)	Supply voltage (+5V)

System Block Diagram



Display Screen

The maximum display screen consists of horizontal 24 characters and vertical 12 lines. The numbe of display characters is 288 (max.). The display characters can consist of display line ROM (12 lines) data and display RAM (176 characters).

- Fixed characters can be specified by making an access to the display line ROM.
- Variable characters can be generated by programming the display RAM.

24 characters

12 lines

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.
Address range from 0D (000h) to 175D (0AFh) used as the display RAM.
Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

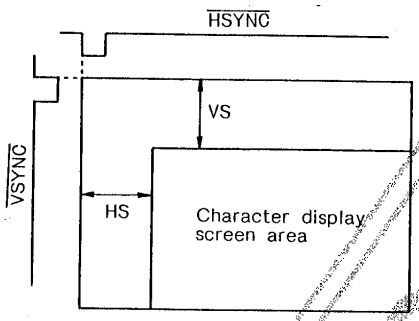
Bit / Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
↓									Blinking		Character code						Display RAM area
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the first line
177 (0B1h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the second line
178 (0B2h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the third line
179 (0B3h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fourth line
180 (0B4h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fifth line
181 (0B5h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the sixth line
182 (0B6h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the seventh line
183 (0B7h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eighth line
184 (0B8h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the ninth line
185 (0B9h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the tenth line
186 (0BAh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eleventh line
187 (0BBh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position. Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position. Vertical character size.
190 (0BEh)	0	0	0	0	INI / NON		-	OSC STP	DSP ON	-	SYS RST	-	-	-	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TST MOD	-	-	BLK 1	BLK 0	-	BLINK 2	BLINK 1	BLINK 0	EX	-	BCOL	Control register

Memory Configuration (display RAM and control RAM)

Memory address and data signals consist of 16 bits.
Address range from 0D (000h) to 175D (0AFh) used as the display RAM.
Address range from 176D (0B0h) to 191D (0BFh) is used as the display control register data area.

Bit / Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
↓									Blinking		Character code						Display RAM area
175 (0AFh)	0	0	0	0	0	0	0	0	BLINK	0	C5	C4	C3	C2	C1	C0	
176 (0B0h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the first line
177 (0B1h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the second line
178 (0B2h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the third line
179 (0B3h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fourth line
180 (0B4h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the fifth line
181 (0B5h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the sixth line
182 (0B6h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the seventh line
183 (0B7h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eighth line
184 (0B8h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the ninth line
185 (0B9h)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the tenth line
186 (0BAh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the eleventh line
187 (0BBh)	0	0	0	0	-	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM specification. First character of the twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position. Horizontal character size.
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position. Vertical character size.
190 (0BEh)	0	0	0	0	INI / NON	-		OSC STP	DSP ON	-	SYS RST	-	-	-	PHASE 1	PHASE 0	Video signal and etc.
191 (0BFh)	0	0	0	0	TST MOD	-	-	BLK 1	BLK 0	-	BLINK 2	BLINK 1	BLINK 0	EX	-	BCOL	Control register

(2) Address 189D ($0BD_H$)

DA 0 to C	Register name	Contents: Status	Contents: Function	Remarks
0	VP0 (LSB)	0 / 1	If a vertical display start position is defined as the VS, the VS can be calculated as follows: $VS=H\times(4\sum_{n=0}^{5}2^{n}VPn)$ H: Horizontal synchronization pulse cycle 	The vertical display start position is specified by using six bits VP5 to VP0. The LSB (VP0) has a bit weight of 4H.
1	VP1	0 / 1		
2	VP2	0 / 1		
3	VP3	0 / 1		
4	VP4	0 / 1		
5	VP5 (MSB)	0 / 1		
6	VSZ10	0 / 1	VSZ11 \ VSZ10: 0 → 0: $1T_C$/1 dot; 1: $2T_C$/1 dot; 1 → 0: $3T_C$/1 dot; 1: $4T_C$/1 dot	Vertical character size for the first line
7	VSZ11	0 / 1		
8	VSZ20	0 / 1	VSZ21 \ VSZ20: 0 → 0: $1T_C$/1 dot; 1: $2T_C$/1 dot; 1 → 0: $3T_C$/1 dot; 1: $4T_C$/1 dot	Vertical character size for the second line
9	VSZ21	0 / 1		
A	VSZ30	0 / 1	VSZ31 \ VSZ30: 0 → 0: $1T_C$/1 dot; 1: $2T_C$/1 dot; 1 → 0: $3T_C$/1 dot; 1: $4T_C$/1 dot	Vertical character size for lines third to twelfth
B	VSZ31	0 / 1		
C	-	0 / 1		

*: If the $\overline{RST}$ pin becomes active (the IC is reset), the contents of all the registers will be set to “0”.

(3) Address 190D ($0BE_H$)

DA 0 to C	Register name	Contents: Status	Contents: Function	Remarks
0	PHASE0	0	PHASE1=0, PHASE0=0: Background color = π/2	Background color
		1	PHASE1=0, PHASE0=1: Background color = π	
1	PHASE1	0	PHASE1=1, PHASE0=0: Background color = 3π/2	
		1	PHASE1=1, PHASE0=1: Background color = In-phase	
2	-	0		
		1		
3	-	0		
		1		
4	-	0		
		1		
5	SYSRST	0		With CS pin level=L, the IC is reset. If the pin level changes to H the IC reset will be released
		1	All the registers are reset and the display mode is inactivated	
6	-	0		
		1		
7	DSPON	0	Character OFF	
		1	Character ON	
8	OSCSTP	0	The oscillation circuit does not enter a stop state if the display mode is inactivated	To stop the crystal oscillation circuit and LC oscillation circuit
		1	The oscillation circuit enters the stop state if the display mode is inactivated	
9	-	0		
		1		
A	-	0		
		1		
B	$\overline{INT}$/ NON	0	Interlace (262.5H/1 field)	Display operation mode selection: interlace and non-interlace
		1	Non-interlace (263H/1 field)	
C	-	0		
		1		

*: If the $\overline{RST}$ pin becomes active (the IC is reset), the contents of all the registers will be set to “0”.

(4) Address 191D ($0BF_H$)

DA 0 to C	Register name	Contents: Status	Contents: Function	Remarks
0	BCOL	0	Active background coloring (available only in internal synchronization mode)	
		1	Inactive background coloring (background level adjustable only)	
1	-	0		
		1		
2	EX	0	External synchronization	$\overline{HSYNC}$ and $\overline{VSYNC}$ signals selection: internal and external
		1	Internal synchronization	
3	BLINK0	0	BLINK1=0, BLINK0=0: Blinking OFF mode	Duty ratio control for blinking mode
		1	BLINK1=0, BLINK0=1: Duty: 25%	
4	BLINK1	0	BLINK1=1, BLINK0=0: Duty: 50%	
		1	BLINK1=1, BLINK0=1: Duty: 75%	
5	BLINK2	0	Blinking cycle: 1 second	Blinking cycle control
		1	Blinking cycle: 0.5 second	
6	-	0		
		1		
7	BLK0	0	BLK1=0, BLK0=0: Blanking OFF mode	Blanking size control
		1	BLK1=0, BLK0=1: Character size	
8	BLK1	0	BLK1=1, BLK0=0: Partial screen size	
		1	BLK1=1, BLK0=1: Entire screen size	
9	-	0		
		1		
A	-	0		
		1		
B	TSTMOD	0	Normal operation	Should be fixed to "0"
		1	Test mode	
C	-	0		
		1		

*: If the $\overline{RST}$ pin becomes active (the IC is reset), the contents of all the registers will be set to “0”.

Memory Configuration (display line ROM)

The display line ROM address range is from 0D (000_H) to 1535D ($5FF_H$). Data consists of 7 bits.

Bit Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Remarks
000 (000h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/ RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the first line
↓																	
0023 (017h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/ RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the first line
0024 (018h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/ RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: First character of the second line
↓									$\overline{ROM}$/ RAM	Character code							
1535 (5FFh)	0	0	0	0	0	0	0	0	$\overline{ROM}$/ RAM	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Line ROM: Twenty-fourth character of the sixty-fourth line

DA 0 to 8	Register name	Contents		Remarks
		Status	Function	
0	ADR0	0	Used to specify the desired character ROM address. To specify the desired display and control RAM address, set bit 7 (DA7) to '1' and seven bits ADR0 to ADR6 to '0'. To access the character ROM, addresses 0D (000) to 63D ($3F_H$) can be used. Set bit 6 (ADR6) to '0'.	
		1		
1	ADR1	0		
		1		
2	ADR2	0		
		1		
3	ADR3	0		
		1		
4	ADR4	0		
		1		
5	ADR5	0		
		1		
6	ADR6	0		
7	$\overline{ROM}$/RAM	0	Direct read access to the character ROM.	
		1	Read access to the character ROM through the display RAM	

Display Line ROM: Line Address Table

Line No.	Address No.	Line No.	Address No.
1st line	00_{HEX} (0000)	33rd line	300_{HEX} (0768)
2nd line	18_{HEX} (0024)	34th line	318_{HEX} (0792)
3rd line	30_{HEX} (0048)	35th line	330_{HEX} (0816)
4th line	48_{HEX} (0072)	36th line	348_{HEX} (0840)
5th line	60_{HEX} (0096)	37th line	360_{HEX} (0864)
6th line	78_{HEX} (0120)	38th line	378_{HEX} (0888)
7th line	90_{HEX} (0144)	39th line	390_{HEX} (0912)
8th line	$A8_{HEX}$ (0168)	40th line	$3A8_{HEX}$ (0936)
9th line	$C0_{HEX}$ (0192)	41st line	$3C0_{HEX}$ (0960)
10th line	$D8_{HEX}$ (0216)	42nd line	$3D8_{HEX}$ (0984)
11st line	$F0_{HEX}$ (0240)	43rd line	$3F0_{HEX}$ (1008)
12th line	108_{HEX} (0264)	44th line	408_{HEX} (1032)
13th line	120_{HEX} (0288)	45th line	420_{HEX} (1056)
14th line	138_{HEX} (0312)	46th line	438_{HEX} (1080)
15th line	150_{HEX} (0336)	47th line	450_{HEX} (1104)
16th line	168_{HEX} (0360)	48th line	468_{HEX} (1128)
17th line	180_{HEX} (0384)	49th line	480_{HEX} (1152)
18th line	198_{HEX} (0408)	50th line	498_{HEX} (1176)
19th line	$1B0_{HEX}$ (0432)	51st line	$4B0_{HEX}$ (1200)
20th line	$1C8_{HEX}$ (0456)	52nd line	$4C8_{HEX}$ (1224)
21st line	$1E0_{HEX}$ (0480)	53rd line	$4E0_{HEX}$ (1248)
22nd line	$1F8_{HEX}$ (0504)	54th line	$4F8_{HEX}$ (1272)
23rd line	210_{HEX} (0528)	55th line	510_{HEX} (1296)
24th line	228_{HEX} (0552)	56th line	528_{HEX} (1320)
25th line	240_{HEX} (0576)	57th line	540_{HEX} (1344)
26th line	258_{HEX} (0600)	58th line	558_{HEX} (1368)
27th line	270_{HEX} (0624)	59th line	570_{HEX} (1392)
28th line	288_{HEX} (0648)	60th line	588_{HEX} (1416)
29th line	$2A0_{HEX}$ (0672)	61st line	$5A0_{HEX}$ (1440)
30th line	$2B8_{HEX}$ (0696)	62nd line	$5B8_{HEX}$ (1464)
31st line	$2D0_{HEX}$ (0720)	63rd line	$5D0_{HEX}$ (1488)
32nd line	$2E8_{HEX}$ (0744)	64th line	$5E8_{HEX}$ (1512)

Sample Display Screen

Twelve display lines of the display 64-line ROM are specified. Variable characters are prepared in the display control RAM. The display RAM address area is automatically allocated to addresses from 0D (000H) to 175D (AFH) in the display order.

The display characters indicated by bold lines are specified through the display RAM access.
The display characters indicated by slender lines are specified directly through the display ROM access.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 1Fh	RAM 000 00h	RAM 001 01h	RAM 002 02h	RAM 003 03h	RAM 004 04h	RAM 005 05h	ROM 022 16h	ROM 023 17h
2	ROM 024 18h	RAM 006 06h	RAM 007 07h	RAM 008 08h	RAM 009 09h	ROM 010 1Dh	ROM 030 1Eh	ROM 031 1Fh	ROM 032 20h	ROM 033 21h	RAM 010 0Ah	RAM 011 0Bh	RAM 012 0Ch	RAM 013 0Dh	RAM 014 0Eh	RAM 015 0Fh	ROM 040 28h	ROM 041 29h	ROM 042 2Ah	ROM 043 2Bh	ROM 044 2Ch	ROM 045 2Dh	ROM 046 2Eh	ROM 047 2Fh
3	ROM 048 30h	RAM 016 10h	RAM 017 11h	RAM 018 12h	RAM 019 13h	RAM 020 14h	ROM 054 36h	ROM 055 37h	ROM 056 38h	ROM 057 39h	RAM 021 15h	RAM 022 16h	RAM 023 17h	RAM 024 18h	RAM 025 19h	RAM 026 1Ah	RAM 027 1Bh	RAM 028 1Ch	RAM 029 1Dh	RAM 030 1Eh	ROM 068 44h	ROM 069 45h	ROM 070 46h	ROM 071 47h
4	ROM 072 48h	ROM 073 49h	ROM 074 4Ah	ROM 075 4Bh	ROM 076 4Ch	RAM 031 1Fh	RAM 032 20h	RAM 033 21h	RAM 034 22h	ROM 081 51h	RAM 035 23h	RAM 036 24h	ROM 084 54h	RAM 037 25h	RAM 038 26h	ROM 087 57h	RAM 039 27h	RAM 040 28h	ROM 090 5Ah	ROM 091 5Bh	ROM 092 5Ch	ROM 093 5Dh	ROM 094 5Eh	ROM 095 5Fh
5	ROM 096 60h	RAM 041 29h	RAM 042 2Ah	RAM 043 2Bh	RAM 044 2Ch	RAM 045 2Dh	RAM 046 2Eh	RAM 047 2Fh	RAM 048 30h	ROM 105 69h	RAM 049 31h	RAM 050 32h	ROM 108 6Ch	RAM 051 33h	RAM 052 34h	ROM 111 6Fh	RAM 053 35h	RAM 054 36h	ROM 114 72h	ROM 115 73h	ROM 116 74h	ROM 117 75h	ROM 118 76h	ROM 119 77h
6	ROM 120 78h	RAM 055 37h	RAM 056 38h	RAM 057 39h	RAM 058 3Ah	RAM 059 3Bh	RAM 060 3Ch	RAM 061 3Dh	ROM 128 80h	RAM 062 3Eh	RAM 063 3Fh	RAM 064 40h	RAM 065 41h	ROM 133 85h	RAM 066 42h	RAM 067 43h	RAM 068 44h	RAM 069 45h	RAM 070 46h	ROM 139 8Bh	RAM 071 47h	RAM 072 48h	ROM 142 8Eh	ROM 143 8Fh
7	RAM 073 49h	RAM 074 4Ah	RAM 075 4Bh	RAM 076 4Ch	RAM 077 4Dh	RAM 078 4Eh	RAM 079 4Fh	RAM 080 50h	RAM 081 51h	RAM 082 52h	RAM 083 53h	RAM 084 54h	ROM 156 9Ch	ROM 157 9Dh	ROM 158 9Eh	ROM 159 8Fh	ROM 160 A0h	ROM 161 A1h	ROM 162 A2h	ROM 163 A3h	ROM 164 A4h	ROM 165 A5h	ROM 166 A6h	ROM 167 A7h
8	RAM 085 55h	RAM 086 56h	RAM 087 57h	RAM 088 58h	RAM 089 59h	RAM 090 5Ah	RAM 091 5Bh	RAM 092 5Ch	RAM 093 5Dh	RAM 094 5Eh	RAM 095 5Fh	RAM 096 60h	ROM 180 B4h	ROM 181 B5h	ROM 182 B6h	ROM 183 B7h	ROM 184 B8h	ROM 185 B9h	ROM 186 BAh	ROM 187 BBh	ROM 188 BCh	ROM 189 BDh	ROM 190 BEh	ROM 191 BFh
9	ROM 192 C0h	ROM 193 C1h	ROM 194 C2h	ROM 195 C3h	ROM 196 C4h	ROM 197 C5h	ROM 198 C6h	ROM 199 C7h	ROM 200 C8h	ROM 201 C9h	ROM 202 CAh	ROM 203 CBh	RAM 097 61h	RAM 098 62h	RAM 099 63h	RAM 100 64h	RAM 101 65h	RAM 102 66h	RAM 103 67h	RAM 104 68h	RAM 105 69h	RAM 106 6Ah	RAM 107 6Bh	RAM 108 6Ch
10	ROM 216 D8h	ROM 217 D9h	ROM 218 DAh	ROM 219 DBh	ROM 220 DCh	RAM 109 6Dh	RAM 110 6Eh	RAM 111 6Fh	RAM 112 70h	RAM 113 71h	RAM 114 72h	RAM 115 73h	RAM 116 74h	RAM 117 75h	RAM 118 76h	RAM 119 77h	RAM 120 78h	RAM 121 79h	RAM 122 7Ah	ROM 235 EBh	ROM 236 ECh	ROM 237 EDh	ROM 238 EEh	ROM 239 EFh
11	ROM 240 F0h	ROM 241 F1h	ROM 242 F2h	ROM 243 F3h	ROM 244 F4h	ROM 245 F5h	ROM 246 F6h	ROM 247 F7h	ROM 248 F8h	ROM 249 F9h	ROM 250 FAh	ROM 251 FBh	ROM 252 FCh	ROM 253 FDh	ROM 254 FEh	RAM 123 7Bh	RAM 124 7Ch	ROM 257 101h	RAM 125 7Dh	RAM 126 7Eh	ROM 260 104h	RAM 127 7Fh	RAM 128 80h	ROM 263 107h
12	RAM 129 81h	RAM 130 82h	RAM 131 83h	RAM 132 84h	RAM 133 85h	RAM 134 86h	RAM 135 87h	RAM 136 88h	RAM 137 89h	RAM 138 8Ah	RAM 139 8Bh	RAM 140 8Ch	RAM 141 8Dh	RAM 142 8Eh	RAM 143 8Fh	RAM 144 90h	RAM 145 91h	RAM 146 92h	RAM 147 93h	RAM 148 94h	RAM 149 95h	RAM 150 96h	RAM 151 97h	ROM 287 11Fh

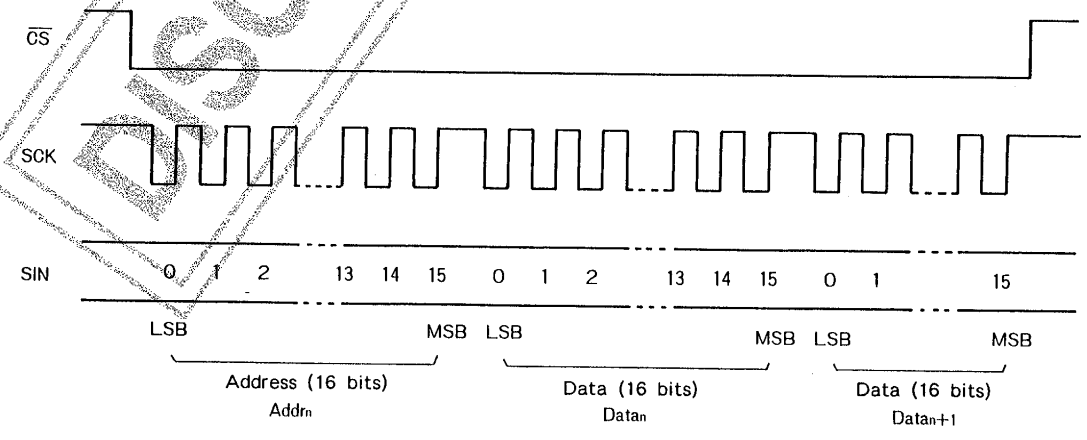
Input Timings of External Control Data

Address and data information is input serially to this chip from an external device.

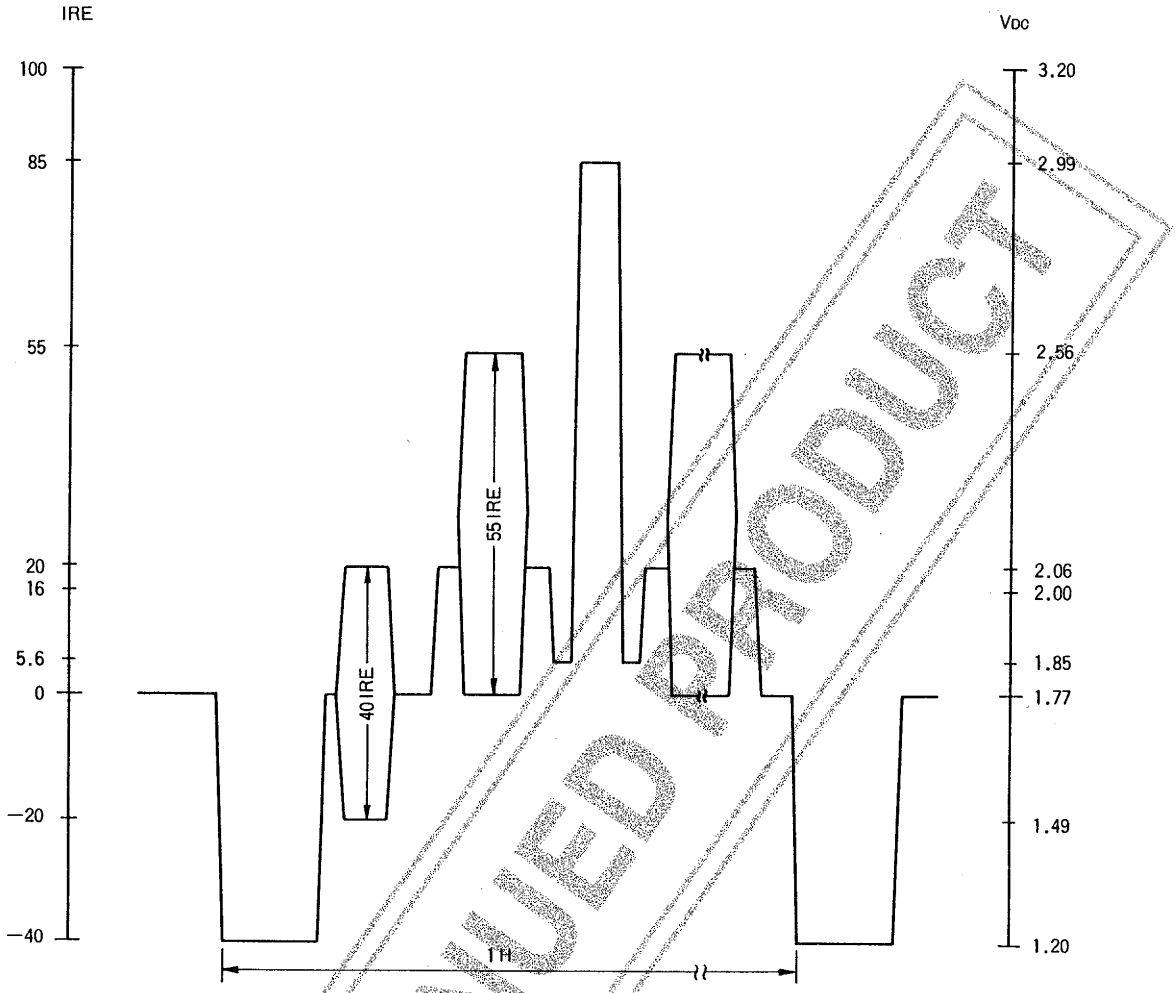
(1) Address data consist of 16 bits.
The 8 low-order bits have significance. Always set 8 high-order bits to '0'.

(2) Data consists of 16 bits.
- Only 8 low-order bits of input data to addresses from 000H to 0AFH have significance. Always set 8 high-order bits to '0'.
- Only 11 low-order bits of input data to addresses from 0B0H to 0BBH have significance. Always set 5 high-order bits to '0'.
- Only 12 low-order bits of input data to addresses from 0BCH to 0BFH have significance. Always set 4 high-order bits to '0'.

(3) The data input format is shown below. The first 16 bits after the $\overline{CS}$ pin (active low) becomes active are processes as an address data. The subsequent groups of 16 bits are handled as the data.



Composite Video Signal Output Level (Internal Generation)



Output level (IRE)	Output voltage (VDC)
100	3.200
85	2.986
46.1	2.430
20	2.057
5.8	1.854
0	1.771
−20	1.486
−40	1.200

V_{DD}=5.000V_{DC}

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