Ordering number : ENN*4245A

CMOS LSI

LC74711

Controller LSI for On-screen Displays

Preliminary

Overview

The LC74711 is a CMOS LSI for applications involving microcomputer control of on-screen character and graphics displays. Built-in character ROM supplies 128 alphanumerics and each character is generated in a 12 by 18 pixel format. The display is capable of supporting a maximum of 288 characters within a 24 characters by 12 line array.

Functions and Applications

(1) Screen construction:
24 characters x 12 lines

(2) Number of characters displayed:
Maximum 288 characters capacity

(3) Display control ROM (line ROM):
64 lines (line unit control: 24 character construction)

(4) Display RAM:
176 characters (supporting extended character selection)

(5) Character construction: 12 (horizontal) x 18 (vertical) pixels

(6) Character set: 128 types of characters

(7) Character size:
4 horizontal types and 4 vertical types

(8) Display starting position: 64 types horizontally and 64 types vertically

(9) Blinking: Character units

(10) Blinking types: 2 types with approximate 1.0 s and 0.5 s cycles and 3-type selection for 25%, 50% and 75% duty

(11) Blanking: Font complete blanking (12 x 18 pixels)

(12) Background color: 8 background tints (during internal synchronizing operation: 4 fsc when using crystal oscillator)

(13) External control input: Serial data input

(14) Synchronizing signal: Internal synchronizing, supports external synchronizing changeover

(15) Built-in synchronizing separator circuit

(16) Video output: NTSC system composite video output

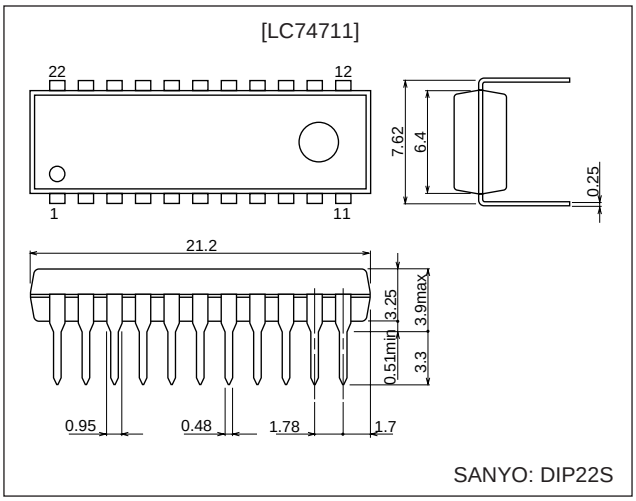
(17) Superimpose: Characters superimposed over composite video output

(18) Package: DIP-22S

Package Dimensions

unit : mm

3059-DIP22S



SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Specifications

Absolute Maximum Ratings

Item	Symbol	Conditions/Pins	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD1}, V_{DD2}	V_{SS}–0.3 to V_{SS}+7.0	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS}–0.3 to V_{DD}+0.3	V
Maximum output voltage	V_{OUT} max		V_{SS}–0.3 to V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	300	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = –30 to +70°C

Item	Symbol	Conditions/Pins	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	V_{DD1} pin	4.5	5.0	5.5	V
	V_{DD2}	V_{DD2} pin	4.5	5.0	$1.27V_{DD1}$	V
Input “H” level voltage	V_{IH}	$\overline{CS}$, SIN, $\overline{RST}$, SCLK, SEPIN pin	$0.8V_{DD1}$		V_{DD1}+0.3	V
Input “L” level voltage	V_{IL}	$\overline{CS}$, SIN, $\overline{RST}$, SCLK, SEPIN pin	V_{SS}–0.3		$0.2V_{DD1}$	V
Composite video input voltage	V_{IN1}	CV_{IN} pin		$2V_{P-P}$		V
	V_{IN2}	SYNI pin		$2V_{P-P}$	$2.5V_{P-P}$	
Oscillation frequency	F_{OSC1}	Xtal oscillation pin (2 fsc)		7.159		MHz
	F_{OSC2}	Xtal oscillation pin (4 fsc)		14.318		MHz
	F_{OSC3}	LC oscillation pin (when using LC oscillation)	5	7	10	MHz

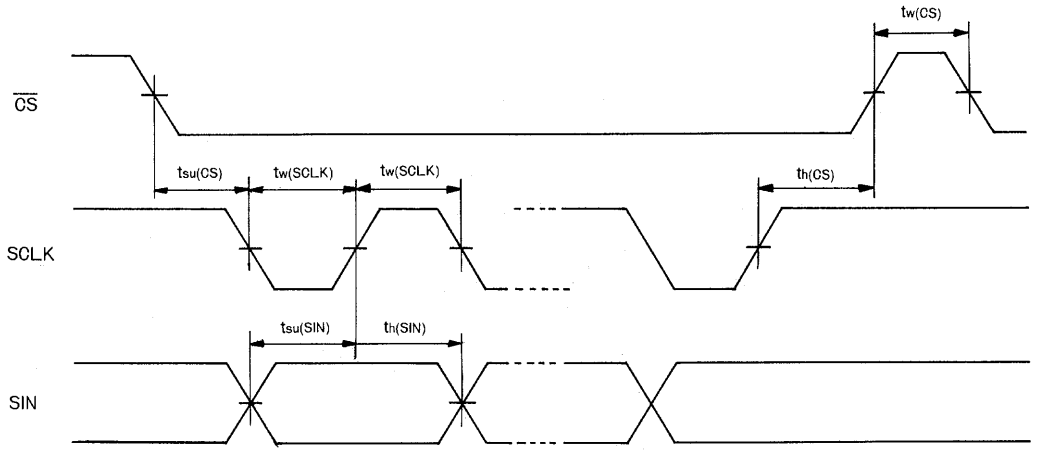
Electrical Characteristics at Ta = –30 to +70 °C, default of V_{DD1} = 5 V

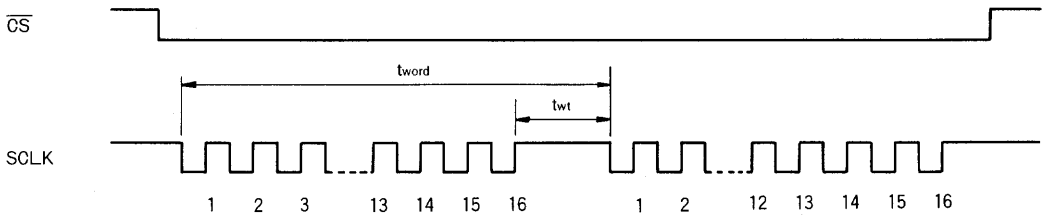
Item	Symbol	Pins	Conditions	Ratings			Unit
				min	typ	max	
Output off leak current	I_{leak}	CV OUT pin				10	µA
Output “H” level voltage	V_{OH1}	SEP OUT pin	V_{DD1} = 4.5V, I_{OH} = –1.0mA	3.5			V
Output “L” level voltage	V_{OL1}	SEP OUT pin	V_{DD1} = 4.5V, I_{OL} = 1.0mA			1.0	V
Input current	I_{IH}	$\overline{CS}$, SIN, $\overline{RST}$, SCLK, SEPIN pin	V_{IN} = V_{DD1}			1	µA
	I_{IL}	OSCIN pin	V_{IN} = V_{SS}	–1			µA
Current consumption during operation	I_{DD1}	V_{DD1} pin	All output are OPEN Xtal = 14.318MHz, LC = 7MHz			10	mA
	I_{DD2}	V_{DD2} pin	V_{DD2} = 5.0V			15	mA

Timing Characteristics at Ta = –30 to +70°C, V_{DD1} = 5 ±0.5 V

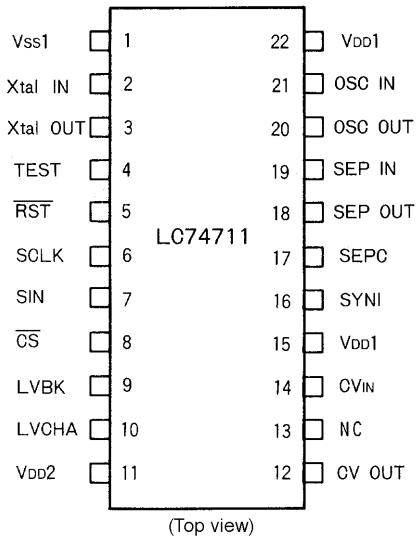
Item	Symbol	Conditions/Pins	Ratings			Unit
			min	typ	max	
Input minimum pulse width	t_w (SCLK)	SCLK pin	200			ns
	t_w (CS)	$\overline{CS}$ pin (with $\overline{CS}$ set to “H” period)	1			µs
Data setup time	t_{su} (CS)	$\overline{CS}$ pin	200			ns
	t_{su} (SIN)	SIN pin	200			ns
Data hold time	t_h (CS)	$\overline{CS}$ pin	2			µs
	t_h (SIN)	SIN pin	200			ns
Single word and write time	t_{word}	16-bit write time	10			µs
	t_{wt}	RAM data write time	1			µs

Serial Data Input Timing





Pin Assignment

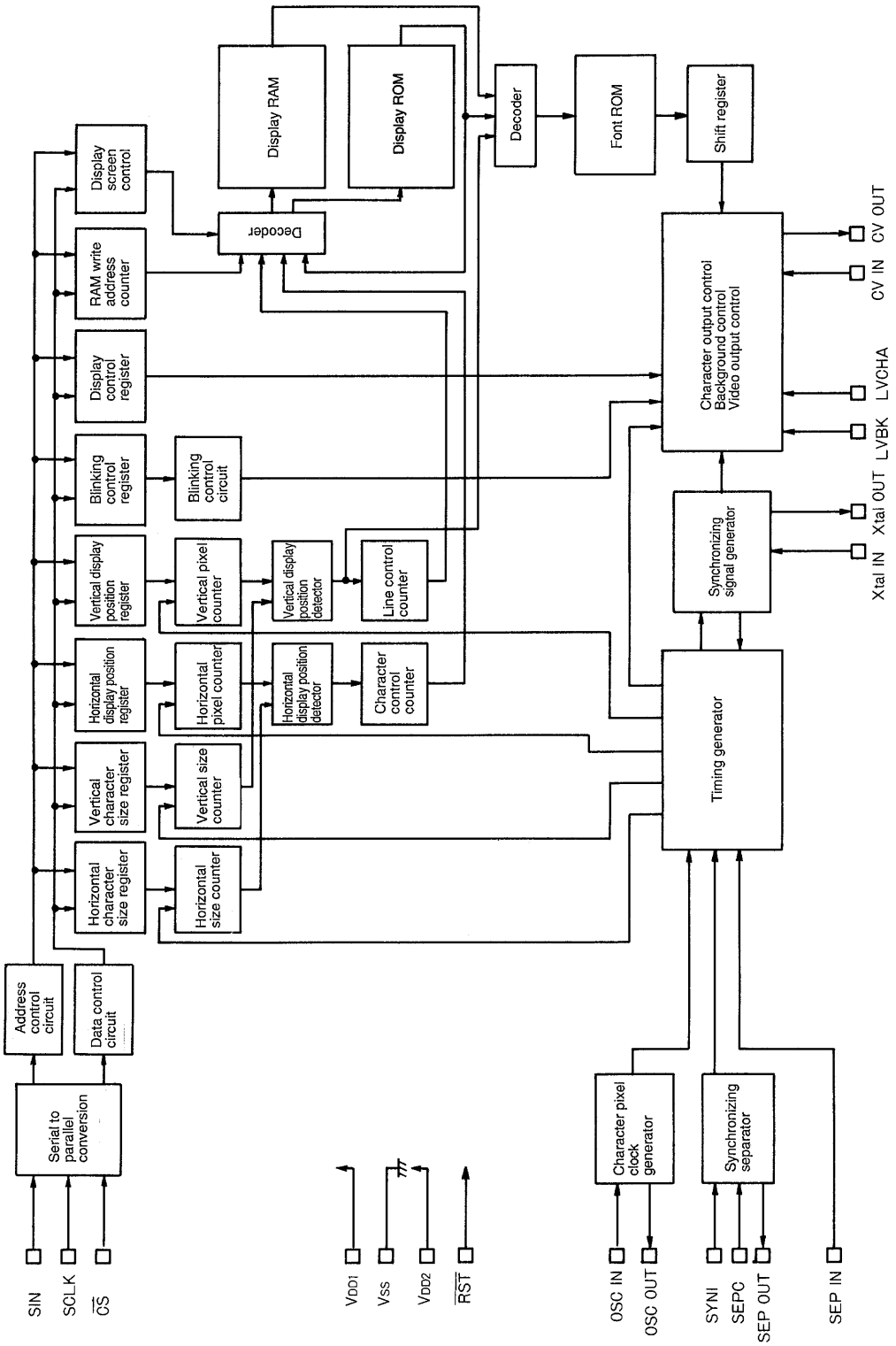


(Top view)

Pin Functions

Pin No.	Pin Symbol	Pin name	Functions
1	V_{SS1}	Ground pin	Pin for connecting to ground (GND) (grounding pin for digital system).
2	Xtal IN	Xtal oscillation pin	Pin for connecting to capacitor or crystal of crystal oscillator for internal synchronizing signal oscillation applications.
3	Xtal OUT		
4	TEST	Test output pin	Pin for test data output.
5	$\overline{RST}$	Reset input pin	Pin for system reset input (hysteresis input).
6	SCLK	Clock input pin	Pin for clock input using serial data input (hysteresis input).
7	SIN	Data input pin	Pin for serial data input (hysteresis input). Input in 16-bit units.
8	$\overline{CS}$	Enable input pin	Pin for enable input for serial data processing (hysteresis input). "L" serial data input switches to enable.
9	LVBK	Blanking level adjustment input pin	Pin for level input for blanking level adjusting.
10	LVCHA	Character level adjustment input pin	Pin for level input for character level adjusting.
11	V_{DD2}	Supply pin	Pin for power supply for adjusting signal level of composite video (power supply for analog system).
12	CV OUT	Video signal output pin	Pin for composite video signal output.
13	NC		Non connection.
14	CV IN	Video signal input pin	Pin for composite video signal input.
15	V_{DD1}	Power supply pin	Pin for power supply (+5V).
16	SYNI	Synchronizing separator circuit input pin	Pin for input of separator circuit composite synchronizing signal.
17	SEPC	Synchronizing separator circuit adjustment pin	Pin for adjusting synchronizing separator circuit (connecting capacitor).
18	SEP OUT	Composite synchronizing signal output pin	Pin for output of composite synchronizing signal for synchronizing separator circuit.
19	SEP IN	Vertical synchronizing signal input pin	Pin for input of vertical synchronizing signal and integrating output signal of SEP OUT pin. Applied when connecting an integrating circuit to the SEP OUT pin.
20	OSC OUT	LC oscillation pin	Pin for connecting a capacitor or oscillator coil for pixel clock generation and character output applications.
21	OSC IN		
22	V_{DD1}	Power supply pin (+5V)	Pin for power supply (+5V).

System Block Diagram



Screen Construction

Display mode supports 24 characters and 12 lines.
Maximum number of displayed characters is 288 characters.
When character size is enlarged, the maximum number of characters displayed is reduced to less than 288 characters.
Display line ROM (12-line setting) or display RAM (176 characters).

- Displays using line ROM specify the fixed character set.
- Extended character set are available using display RAM and program setting of characters.

24 characters

12 lines

00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71
72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119
120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167
168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215
216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263
264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287

Memory Construction (display RAM and control RAM)

Memory addresses and data 16-bit processing.
Addresses 0 (000 $_{HEX}$) to 175 (OAF $_{HEX}$) are reserved for display memory (RAM) data.
Addresses 176 (0B0 $_{HEX}$) to 191 (0BF $_{HEX}$) are reserved for display control register data.

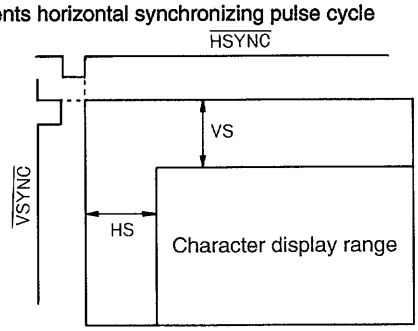
bit / Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
000 (000h)	0	0	0	0	0	0	0	0	BLANK	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
↓									Blinking		Character code						Display RAM
175 (0AFh)	0	0	0	0	0	0	0	0	BLANK	C_6	C_5	C_4	C_3	C_2	C_1	C_0	
176 (0B0h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of first line
177 (0B1h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of second line
178 (0B2h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of third line
179 (0B3h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fourth line
180 (0B4h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of fifth line
181 (0B5h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of sixth line
182 (0B6h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of seventh line
183 (0B7h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eighth line
184 (0B8h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of ninth line
185 (0B9h)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of tenth line
186 (0BAh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of eleventh line
187 (0BBh)	0	0	0	0	0	ADRA	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character of twelfth line
188 (0BCh)	0	0	0	0	HSZ 31	HSZ 30	HSZ 21	HSZ 20	HSZ 11	HSZ 10	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display position Horizontal character size
189 (0BDh)	0	0	0	0	VSZ 31	VSZ 30	VSZ 21	VSZ 20	VSZ 11	VSZ 10	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display position Vertical character size
190 (0BEh)	0	0	0	0	$\overline{INT}$ / NON	$\overline{LC}$ / XTAL	$\overline{2fsc}$ / 4fsc	OSC STP	DSP ON	—	SYS RST	—	—	PHASE 2	PHASE 1	PHASE 0	Video signal and other
191 (0BFh)	0	0	0	0	TST MOD	—	—	BLK 1	BLK 0	—	BLINK 2	BLINK 1	BLINK 0	EX	CBOFF	BCOL	Control register

(1) Address 188 (0 BC_{HEX})

<table>
<tr><th rowspan="2">DA
0 to C</th><th rowspan="2">Register
Name</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>Setting</th><th>Function</th></tr>
<tr><td>0</td><td>HP0
(LSB)</td><td>0
1</td><td rowspan="8">When the horizontal display starting position is set to HS,
$HS = Tc \times (4\sum_{n=0}^{5} 2^n HPn)$
T_C: represents oscillation cycle of OSC IN and OUT oscillator during operation mode</td><td rowspan="8">Horizontal display starting position sets using 6-bit found at HP5 to HP0. Single bit significance is $4T_C$.</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>5</td><td>HP5
(MSB)</td><td>0
1</td></tr>
<tr><td>6</td><td>HSZ10</td><td>0
1</td><td rowspan="2">HSZ11 \ HSZ10 | 0 | 1
0 | $1T_C$/1 dot | $2T_C$/1 dot
1 | $3T_C$/1 dot | $4T_C$/1 dot</td><td rowspan="2">First line horizontal character size.</td></tr>
<tr><td>7</td><td>HSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>HSZ20</td><td>0
1</td><td rowspan="2">HSZ21 \ HSZ20 | 0 | 1
0 | $1T_C$/1 dot | $2T_C$/1 dot
1 | $3T_C$/1 dot | $4T_C$/1 dot</td><td rowspan="2">Second line horizontal character size.</td></tr>
<tr><td>9</td><td>HSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>HSZ30</td><td>0
1</td><td rowspan="2">HSZ31 \ HSZ30 | 0 | 1
0 | $1T_C$/1 dot | $2T_C$/1 dot
1 | $3T_C$/1 dot | $4T_C$/1 dot</td><td rowspan="2">Lines 3 to 12 horizontal character sizes.</td></tr>
<tr><td>B</td><td>HSZ31</td><td>0
1</td></tr>
<tr><td>C</td><td>—</td><td>0
1</td><td></td><td></td></tr>
</table>

Note: * When reset using the $\overline{RST}$ pin, all registers are set to 0 (zero).

(2) Address 189 (0 BD_{HEX})

<table>
<tr><th rowspan="2">DA
0 to C</th><th rowspan="2">Register
Name</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>Setting</th><th>Function</th></tr>
<tr><td>0</td><td>VP0
(LSB)</td><td>0
1</td><td rowspan="6">When the vertical display starting position is set to VS,
$VS = H \times (4\sum_{n=0}^{5} 2^n VPn)$
H: represents horizontal synchronizing pulse cycle
 
</td><td rowspan="6">Vertical display starting position sets using 6-bit found at VP5 to VP0. Single bit significance is 4H.</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>5</td><td>VP5
(MSB)</td><td>0
1</td></tr>
<tr><td>6</td><td>VSZ10</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ11 \ VSZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table></td><td rowspan="2">First line vertical character size.</td></tr>
<tr><td>7</td><td>VSZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>VSZ20</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ21 \ VSZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table></td><td rowspan="2">Second line vertical character size.</td></tr>
<tr><td>9</td><td>VSZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>VSZ30</td><td>0
1</td><td rowspan="2"><table><tr><th>VSZ31 \ VSZ30</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1H/1 dot</td><td>2H/1 dot</td></tr><tr><td>1</td><td>3H/1 dot</td><td>4H/1 dot</td></tr></table></td><td rowspan="2">Lines 3 to 12 vertical character sizes.</td></tr>
<tr><td>B</td><td>VSZ31</td><td>0
1</td></tr>
<tr><td>C</td><td>—</td><td>0
1</td><td></td><td></td></tr>
</table>

Note: * When reset using the $\overline{RST}$ pin, all registers are set to 0 (zero).

(3) Address 190 (0 BE_{HEX})

<table>
<tr><th rowspan="2">DA
0 to C</th><th rowspan="2">Register
Name</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>Setting</th><th>Function</th></tr>
<tr><td>0</td><td>PHASE0</td><td>0</td><td rowspan="8"><table><tr><th>PHASE2</th><th>PHASE1</th><th>PHASE0</th><th>Background tint</th></tr><tr><td>0</td><td>0</td><td>0</td><td>π/2</td></tr><tr><td>0</td><td>0</td><td>1</td><td>π</td></tr><tr><td>0</td><td>1</td><td>0</td><td>3π/2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>In-phase</td></tr><tr><td>1</td><td>0</td><td>0</td><td>π/4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>3π/4</td></tr><tr><td>1</td><td>1</td><td>0</td><td>5π/4</td></tr><tr><td>1</td><td>1</td><td>1</td><td>7π/4</td></tr></table></td><td rowspan="2">Background tint
Background color phase responding to color burst.</td></tr>
<tr><td>1</td><td>PHASE1</td><td>0</td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>2</td><td>PHASE2</td><td>0</td><td></td><td></td></tr>
<tr><td></td><td></td><td>1</td><td></td><td></td></tr>
<tr><td>3</td><td>—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>4</td><td>—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>5</td><td>SYSRST</td><td>0</td><td></td><td rowspan="2">$\overline{CS}$ pin resets for “L” and cancels reset using “H”.</td></tr>
<tr><td></td><td></td><td>1</td><td>All registers reset and display set to off</td></tr>
<tr><td>6</td><td>—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
<tr><td>7</td><td>DSPON</td><td>0</td><td>Character display off</td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td>Character display on</td></tr>
<tr><td>8</td><td>OSCSTP</td><td>0</td><td>Crystal oscillator circuit and LC oscillator circuit is not stopped</td><td rowspan="2">External synchronizing mode enabled only when character display is off.</td></tr>
<tr><td></td><td></td><td>1</td><td>Crystal oscillator circuit and LC oscillator circuit is stopped</td></tr>
<tr><td>9</td><td>$\overline{2fsc}$
/4fsc</td><td>0</td><td>Clock frequency 2 fsc</td><td rowspan="2">Crystal oscillator circuit oscillation frequency.</td></tr>
<tr><td></td><td></td><td>1</td><td>Clock frequency 4 fsc</td></tr>
<tr><td>A</td><td>$\overline{LC}$
/XTAL</td><td>0</td><td>Using LC oscillation for pixel clock</td><td rowspan="2">When the LC oscillation circuit is not used, OSC IN pin is fixed at V_{DD}.</td></tr>
<tr><td></td><td></td><td>1</td><td>Using crystal oscillation for pixel clock</td></tr>
<tr><td>B</td><td>$\overline{INT}$
/NON</td><td>0</td><td>Interlaced (312.5 H/1 field)</td><td rowspan="2">Changeover is permitted between interlace and non-interlaced displays.</td></tr>
<tr><td></td><td></td><td>1</td><td>Non-interlaced (313 H/1 field)</td></tr>
<tr><td>C</td><td>—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td></td><td></td><td>1</td><td></td></tr>
</table>

Note: * When reset using the $\overline{RST}$ pin, all registers are set to 0 (zero).

(4) Address 191 ($0BF_{HEX}$)

<table>
<tr><th rowspan="2">DA
0 to C</th><th rowspan="2">Register
Name</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>Setting</th><th>Function</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">BCOL</td><td>0</td><td>With background tint (only enabled with internal synchronizing)</td><td rowspan="4"></td></tr>
<tr><td>1</td><td>No background tint (background level setting only)</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">CBOFF</td><td>0</td><td>Burst signal always output</td></tr>
<tr><td>1</td><td>When BCOL is set to “H”, burst signal also does not output</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">EX</td><td>0</td><td>External synchronizing</td><td rowspan="2">$\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ signal changeover to external or internal supported.</td></tr>
<tr><td>1</td><td>Internal synchronizing</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">BLINK0</td><td>0</td><td rowspan="4"><table><tr><th>BLINK1 \ BLINK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blinking off</td><td>25% duty</td></tr><tr><td>1</td><td>50% duty</td><td>75% duty</td></tr></table></td><td rowspan="4">Blinking duty comparative variability.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BLINK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">BLINK2</td><td>0</td><td>Blinking cycle approximately 0.5 s</td><td rowspan="2">Variable blinking cycle.</td></tr>
<tr><td>1</td><td>Blinking cycle approximately 1 s</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BLK0</td><td>0</td><td rowspan="4"><table><tr><th>BLK1 \ BLK0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Blanking off</td><td>Character size</td></tr><tr><td>1</td><td>Trimming size</td><td>Total overall size</td></tr></table></td><td rowspan="4">Variable blanking size.</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">8</td><td rowspan="2">BLK1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">9</td><td rowspan="2">—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">A</td><td rowspan="2">—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">B</td><td rowspan="2">TSTMOD</td><td>0</td><td>Normal operation mode</td><td rowspan="2">Fixes to zero (0) condition.</td></tr>
<tr><td>1</td><td>Test operation mode</td></tr>
<tr><td rowspan="2">C</td><td rowspan="2">—</td><td>0</td><td></td><td rowspan="2"></td></tr>
<tr><td>1</td><td></td></tr>
</table>

Note: * When reset using the $\overline{\text{RST}}$ pin, all registers are set to 0 (zero).

Memory Construction (Display Line ROM)

Memory addresses are arrayed within 0 (000 $_{HEX}$) to 1535 (5FF $_{HEX}$) and have an 8-bit data construction.

bit / Address	DA F	DA E	DA D	DA C	DA B	DA A	DA 9	DA 8	DA 7	DA 6	DA 5	DA 4	DA 3	DA 2	DA 1	DA 0	Notes
0000 (000h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character and first line.
↓																	
0023 (017h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for twenty-fourth character and first line.
0024 (018h)	0	0	0	0	0	0	0	0	$\overline{ROM}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for first character and second line.
↓									$\overline{ROM}$/RAM	Character code							
1535 (5FFh)	0	0	0	0	0	0	0	0	$\overline{ROM}$/RAM	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	Display line ROM setting for twenty-fourth character and sixty-fourth line.

DA 0 to 8	Register Name	Contents: Setting	Contents: Function	Notes
0	ADR0	0	Character ROM address setting When display control RAM is specified, DA7 equals "1" and ADR0 to ADR6 are set to "0" Character ROM address setting range is 0 to 127 (7F $_{HEX}$)	
		1		
1	ADR1	0		
		1		
2	ADR2	0		
		1		
3	ADR3	0		
		1		
4	ADR4	0		
		1		
5	ADR5	0		
		1		
6	ADR6	0		
		1		
7	$\overline{ROM}$/RAM	0	Character ROM is accessed and read directly	
		1	Character ROM is accessed and read through display RAM	

Line Address Table for Display Line ROM

Line	Address	Line	Address
1 line	00HEX (0000)	33 line	300HEX (0768)
2 line	18HEX (0024)	34 line	318HEX (0792)
3 line	30HEX (0048)	35 line	330HEX (0816)
4 line	48HEX (0072)	36 line	348HEX (0840)
5 line	60HEX (0096)	37 line	360HEX (0864)
6 line	78HEX (0120)	38 line	378HEX (0888)
7 line	90HEX (0144)	39 line	390HEX (0912)
8 line	A8HEX (0168)	40 line	3A8HEX (0936)
9 line	C0HEX (0192)	41 line	3C0HEX (0960)
10 line	D8HEX (0216)	42 line	3D8HEX (0984)
11 line	F0HEX (0240)	43 line	3F0HEX (1008)
12 line	108HEX (0264)	44 line	408HEX (1032)
13 line	120HEX (0288)	45 line	420HEX (1056)
14 line	138HEX (0312)	46 line	438HEX (1080)
15 line	150HEX (0336)	47 line	450HEX (1104)
16 line	168HEX (0360)	48 line	468HEX (1128)
17 line	180HEX (0384)	49 line	480HEX (1152)
18 line	198HEX (0408)	50 line	498HEX (1176)
19 line	1B0HEX (0432)	51 line	4B0HEX (1200)
20 line	1C8HEX (0456)	52 line	4C8HEX (1224)
21 line	1E0HEX (0480)	53 line	4E0HEX (1248)
22 line	1F8HEX (0504)	54 line	4F8HEX (1272)
23 line	210HEX (0528)	55 line	510HEX (1296)
24 line	228HEX (0552)	56 line	528HEX (1320)
25 line	240HEX (0576)	57 line	540HEX (1344)
26 line	258HEX (0600)	58 line	558HEX (1368)
27 line	270HEX (0624)	59 line	570HEX (1392)
28 line	288HEX (0648)	60 line	588HEX (1416)
29 line	2A0HEX (0672)	61 line	5A0HEX (1440)
30 line	2B8HEX (0696)	62 line	5B8HEX (1464)
31 line	2D0HEX (0720)	63 line	5D0HEX (1488)
32 line	2E8HEX (0744)	64 line	5E8HEX (1512)

Screen Construction (Sample Display)

Setting of 12-line display using display line ROM (64 lines).
Within line ROM, setting of extended characters is made available through display control RAM.
Display control RAM addresses are automatically allocated to display array from 0 to 175 (AF_{HEX}).

▨ (thick line) indicates character setting using display control RAM.
□ (thin line) indicates character setting using line ROM.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	ROM 000 00h	ROM 001 01h	ROM 002 02h	ROM 003 03h	ROM 004 04h	ROM 005 05h	ROM 006 06h	ROM 007 07h	ROM 008 08h	ROM 009 09h	ROM 010 0Ah	ROM 011 0Bh	ROM 012 0Ch	ROM 013 0Dh	ROM 014 0Eh	ROM 015 0Fh	RAM 000 00H	RAM 001 01H	RAM 002 02H	RAM 003 03H	RAM 004 04H	RAM 005 05H	ROM 022 16h	ROM 023 17h
2	ROM 024 18h	RAM 006 06H	RAM 007 07H	RAM 008 08H	RAM 009 09H	ROM 029 1Dh	ROM 030 1Eh	ROM 031 1Fh	ROM 032 20h	ROM 033 21h	RAM 010 0AH	RAM 011 0BH	RAM 012 0CH	RAM 013 0DH	RAM 014 0EH	RAM 015 0FH	ROM 040 28h	ROM 041 29h	ROM 042 2Ah	ROM 043 2Bh	ROM 044 2Ch	ROM 045 2Dh	ROM 046 2Eh	ROM 047 2Fh
3	ROM 048 18h	RAM 016 10H	RAM 017 11H	RAM 018 12H	RAM 019 13H	RAM 020 14H	ROM 054 36h	ROM 055 37h	ROM 056 38h	ROM 057 39h	RAM 021 15H	RAM 022 16H	RAM 023 17H	RAM 024 18H	RAM 025 19H	RAM 026 1AH	RAM 027 1BH	RAM 028 1CH	RAM 029 1DH	RAM 030 1EH	ROM 068 44h	ROM 069 45h	ROM 070 46h	ROM 071 47h
4	ROM 072 48h	ROM 073 49h	ROM 074 4ah	ROM 075 4bh	ROM 076 4ch	RAM 031 1FH	RAM 032 20H	RAM 033 21H	RAM 034 22H	ROM 081 51h	RAM 035 23H	RAM 036 24H	ROM 084 54h	RAM 037 25H	RAM 038 26H	ROM 084 54h	RAM 039 27H	RAM 040 28H	ROM 060 5Ah	ROM 091 5Bh	ROM 092 5Ch	ROM 093 5Dh	ROM 094 5Eh	ROM 095 5Fh
5	ROM 096 60h	RAM 041 29H	RAM 042 2AH	RAM 043 2BH	RAM 044 2CH	RAM 045 2DH	RAM 046 2EH	RAM 047 2FH	RAM 048 30H	ROM 105 69h	RAM 049 31H	RAM 050 32H	ROM 108 6Ch	RAM 051 33H	RAM 052 34H	ROM 111 6Fh	RAM 053 35H	RAM 054 36H	ROM 114 72h	ROM 115 73h	ROM 116 74h	ROM 117 75h	ROM 118 76h	ROM 119 77h
6	ROM 120 78h	RAM 055 37H	RAM 056 38H	RAM 057 39H	RAM 058 3AH	RAM 059 3BH	RAM 060 3CH	RAM 061 3DH	ROM 128 80h	RAM 062 3EH	RAM 063 3FH	RAM 064 40H	RAM 065 41H	ROM 133 85h	RAM 066 42H	RAM 067 43H	RAM 068 44H	RAM 069 45H	RAM 070 46H	ROM 139 8Bh	RAM 071 47H	RAM 072 48H	ROM 142 8Eh	ROM 143 8Fh
7	RAM 073 49H	RAM 074 4AH	RAM 075 4BH	RAM 076 4CH	RAM 077 4DH	RAM 078 4EH	RAM 079 4FH	RAM 080 50H	RAM 081 51H	RAM 082 52H	RAM 083 53H	RAM 084 54H	ROM 156 9Ch	ROM 157 9Dh	ROM 158 9Eh	ROM 159 9Fh	ROM 160 A0h	ROM 161 A1h	ROM 162 A2h	ROM 163 A3h	ROM 164 A4h	ROM 165 A5h	ROM 166 A6h	ROM 167 A7h
8	RAM 082 52H	RAM 086 56H	RAM 087 57H	RAM 088 58H	RAM 089 59H	RAM 090 5AH	RAM 091 5BH	RAM 092 5CH	RAM 093 5DH	RAM 094 5EH	RAM 095 5FH	RAM 096 60H	ROM 180 B4h	ROM 181 B5h	ROM 182 B6h	ROM 183 B7h	ROM 184 B8h	ROM 185 B9h	ROM 186 BAh	ROM 187 BBh	ROM 188 BCh	ROM 189 BDh	ROM 190 BEh	ROM 191 BFh
9	ROM 192 C0h	ROM 193 C1h	ROM 194 C2h	ROM 195 C3h	ROM 196 C4h	ROM 197 C5h	ROM 198 C6h	ROM 199 C7h	ROM 200 C8h	ROM 201 C9h	ROM 202 CAh	ROM 203 CBh	RAM 097 61H	RAM 098 62H	RAM 099 63H	RAM 100 64H	RAM 101 65H	RAM 102 66H	RAM 103 67H	RAM 104 68H	RAM 105 69H	RAM 106 6AH	RAM 107 6BH	RAM 108 6CH
10	ROM 216 D8h	ROM 217 D9h	ROM 218 DAh	ROM 219 DBh	ROM 220 DCh	RAM 109 6DH	RAM 110 6EH	RAM 111 6FH	RAM 112 70H	RAM 113 71H	RAM 114 72H	RAM 115 73H	RAM 116 74H	RAM 117 75H	RAM 118 76H	RAM 119 77H	RAM 120 78H	RAM 121 79H	RAM 122 7AH	ROM 235 EBh	ROM 236 ECh	ROM 237 EDh	ROM 238 EEh	ROM 239 EFh
11	ROM 240 F0h	ROM 241 F1h	ROM 242 F2h	ROM 243 F3h	ROM 244 F4h	ROM 245 F5h	ROM 246 F6h	ROM 247 F7h	ROM 248 F8h	ROM 249 F9h	ROM 250 FAh	ROM 251 FBh	ROM 252 FCh	ROM 253 FDh	ROM 254 FEh	RAM 123 7BH	RAM 124 7CH	ROM 257 101h	RAM 125 7DH	RAM 126 7EH	ROM 260 104h	RAM 127 7FH	RAM 128 80H	ROM 263 107h
12	RAM 129 81H	RAM 130 82H	RAM 131 83H	RAM 132 84H	RAM 133 85H	RAM 134 86H	RAM 135 87H	RAM 136 88H	RAM 137 89H	RAM 138 8AH	RAM 139 8BH	RAM 140 8CH	RAM 141 8DH	RAM 142 8EH	RAM 143 8FH	RAM 144 90H	RAM 145 91H	RAM 146 92H	RAM 147 93H	RAM 148 94H	RAM 149 95H	RAM 150 96H	RAM 151 97H	ROM 287 11Fh

Input Timing of External Control Data
Input format is set at 16-bit, serial input for address and data input.
Address and Data Serial Input

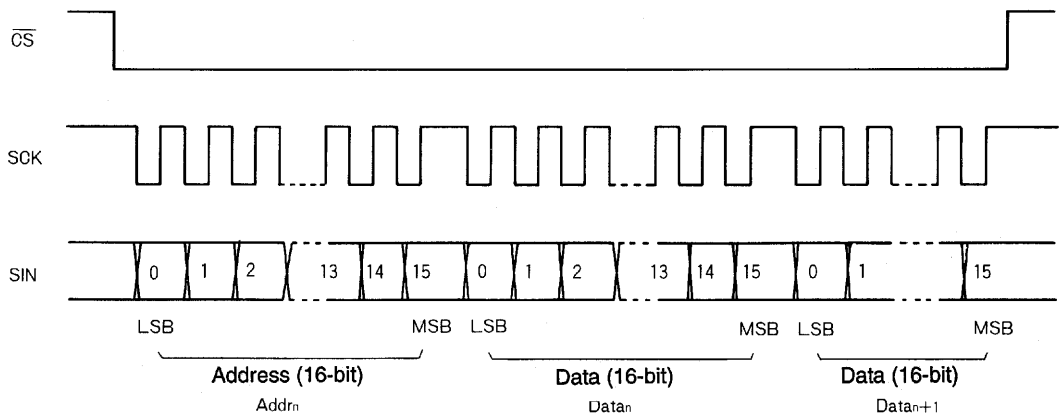
① Address Input with 16-bit Construction
Lower 8 bits are reserved for address assignments while the upper 8 bits are fixed to “0”.

② Data Input with 16-bit Construction

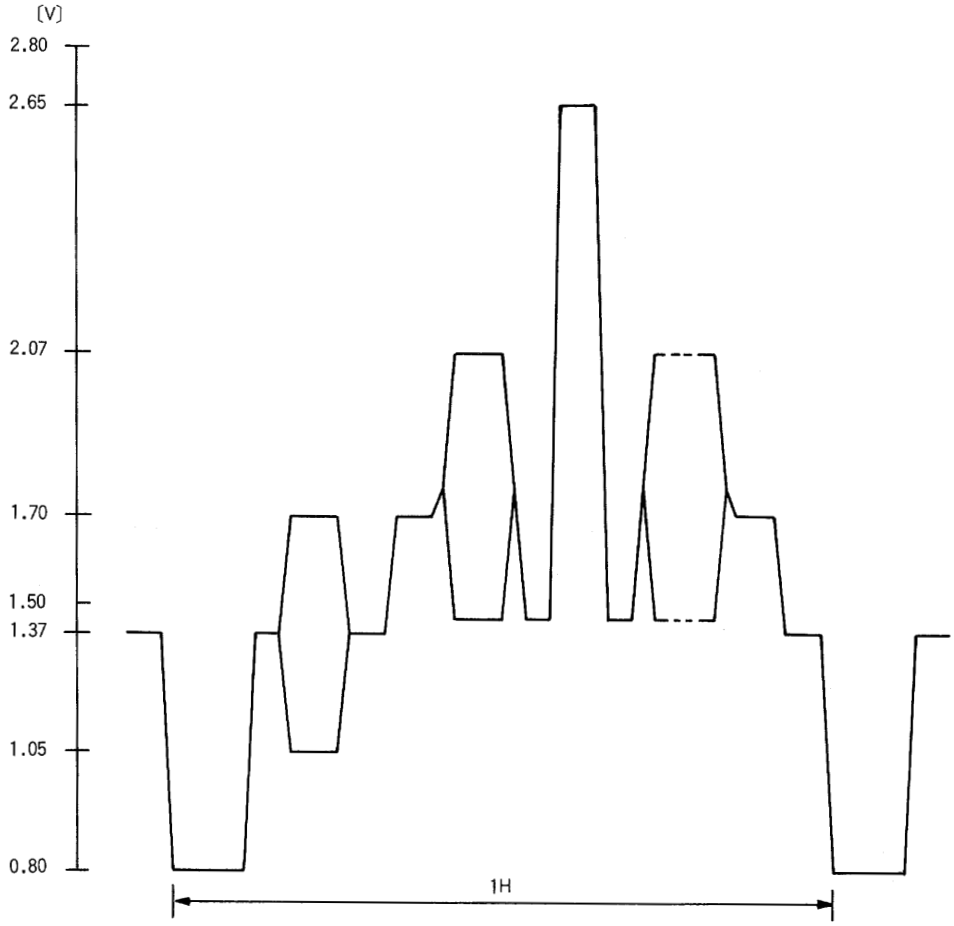
- Lower 8 bits having addresses 000 $_{HEX}$ through 0AF $_{HEX}$ are reserved for data assignments while the upper 8 bits are fixed to “0”.
- Lower 11 bits having addresses 0B0 $_{HEX}$ through 0BB $_{HEX}$ are reserved for data assignments while the upper 5 bits are fixed to “0”.
- Lower 12 bits having addresses 0BC $_{HEX}$ through 0BF $_{HEX}$ are reserved for data assignments while the upper 4 bits are fixed to “0”.

③ Data Input Format

After the onset of $\overline{CS}$, the first 16 bits are processed as address information, and thereafter information is processed as data in 16-bit units. Addresses are automatically allocated in 16-bit increments.



Composite Video Signal Output Level (Internal generation level: synchronization chip level = 0.8 V)



Output Level	Output Voltage (V_{DC})
Character level	2.650
Background color “H” level	2.075
Burst “L” level	1.700
Background color “L” level	1.500
Trimming level	1.500
Pedestal level	1.375
Burst “L” level	1.050
Synchronization chip level	0.800

V_{DD2} = 5.000V_{DC}