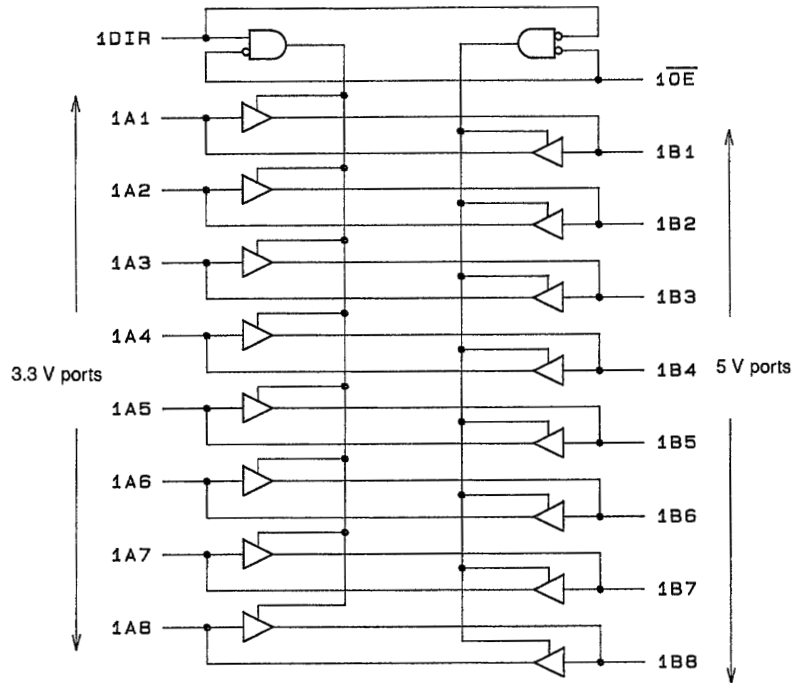
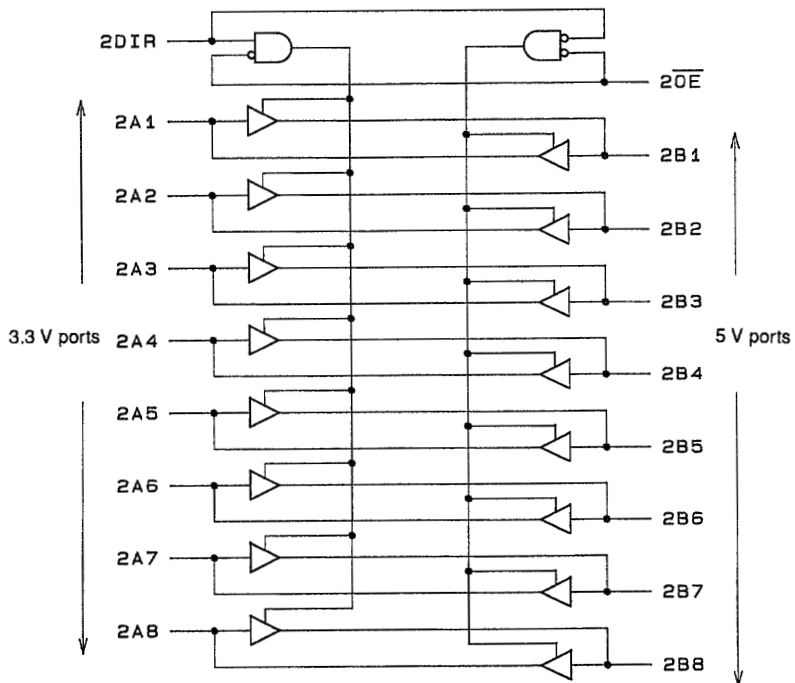




Function Block Diagram



A02712



A02713

Power Supply Operating Sequences

Power on: Either apply  $V_{CC1}$  first and then  $V_{CC2}$ , or apply both at the same time.

Power off: Either turn off  $V_{CC2}$  first and then  $V_{CC1}$ , or turn off both at the same time.

**Pin Functions**

Pin	Function
× $\overline{OE}$	Output enable input (active low)
× DIR	Direction control input
× AX	A side input or three-state output
× BX	B side input or three-state output

**Specifications**

**Absolute Maximum Ratings\*1**

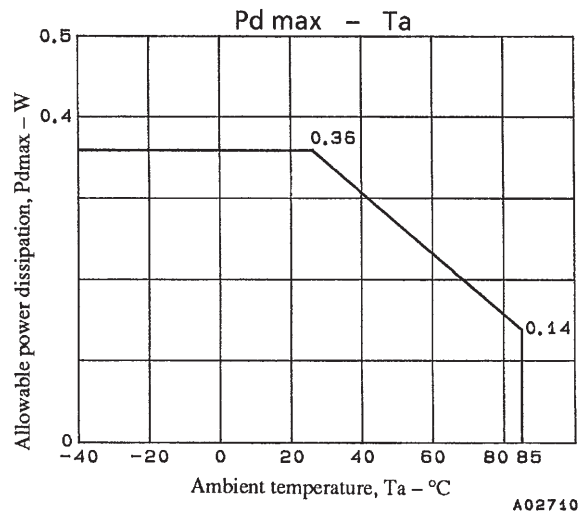
Parameter	Symbol	Conditions	Ratings	Unit
Pin voltage referenced to GND	$V_{TERM}^{*2}$		-0.5 to +7.0	V
Pin voltage referenced to GND	$V_{TERM}^{*3}$		-0.5 to $V_{CC1}$ ( $V_{CC2}$ ) + 0.5	V
Operating temperature	$T_{opr}$		-40 to +85	°C
Temperature when bias is applied	$T_{BIAS}$		-55 to +125	°C
Storage temperature	$T_{stg}$		-55 to +125	°C
Power dissipation	$P_T$		*4	W
DC output current	$I_{OUT}$		-60 to +60	mA

- Note: 1. Applying stresses in excess of the absolute maximum ratings may permanently damage the device. The values specified here are stress ratings only, and do not refer to operation under conditions outside either these conditions or the operating conditions. Operating for extended periods at the absolute maximum ratings may adversely influence device reliability. Unless otherwise specified, pin voltages must not exceed  $V_{CC1}$  (or  $V_{CC2}$ ) + 0.5 V.  
 2. Inputs and the  $V_{CC1}$  pin  
 3. Outputs, I/O pins, and the  $V_{CC2}$  pin  
 4. See Figure 1.

**Function Truth Table\***

Input		Output
× $\overline{OE}$	× DIR	
L	L	Bus B data output to bus A
L	H	Bus A data output to bus B
H	X	High-impedance state.

- Note: \* H = High level  
 L = Low level  
 X = Don't care



**Figure 1**

**Capacitances (Ta = 25°C)**

Parameter*	Symbol	Conditions	min	typ	max	Unit
Input capacitance	$C_{IN}$			5.5	8.0	pF
I/O capacitance	$C_{I/O}$			4.5	6.0	pF

- Note: \* These capacitance values are logic values, and are not tested.

## LC74FCT164245, 74FCT164245T

### DC Electrical Characteristics in the Operating Ranges (A port: 3.3 V)

The following conditions apply unless otherwise specified.

$V_{CC1} = 5.0 \text{ V} \pm 10\%$ ,  $V_{CC2} = 3.3 \text{ V} \pm 0.3 \text{ V}$   $T_a = -40 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	Conditions*1	min	typ*2	max	Unit
Input high level voltage	$V_{IH}$	Logic high level guaranteed	2.0		$V_{CC1} + 0.5$	V
Input low level voltage	$V_{IL}$	Logic low level guaranteed	-0.5		+0.8	V
Input high level current (input pins)	$I_{IH}$	$V_{CC2} = \text{max}$				$\pm 0.5$
Input high level current (I/O pins)						$\pm 0.5$
Input low level current (input pins)	$I_{IL}$	$V_{CC2} = \text{max}$	$V_I = \text{GND}$			$\pm 0.5$
Input low level current (I/O pins)						$\pm 0.5$
High impedance output current	$I_{OZH}$	$V_{CC2} = \text{max}$	$V_O = V_{CC2}$			$\pm 0.5$
	$I_{OZL}$		$V_O = \text{GND}$			$\pm 0.5$
Output high level voltage	$V_{OH}$	$V_{CC2} = \text{min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -8 \text{ mA}$	2.4	3.0	V
			$I_{OH} = -0.1 \text{ mA}$	$V_{CC2} - 0.2$		V
Output low level voltage	$V_{OL}$	$V_{CC2} = \text{min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 24 \text{ mA}$		0.3	0.5
			$I_{OL} = 0.1 \text{ mA}$			0.2
Quiescent current	$I_{CC2}$	$V_{CC2} = \text{max}$ , $V_{IN} = \text{GND}$ or $V_{CC2}$		0.35	2.0	mA

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

2. Typical values are values for  $V_{CC1} = 5.0 \text{ V}$ ,  $V_{CC2} = 3.3 \text{ V}$ , and an ambient temperature of  $+25^\circ\text{C}$ .

### DC Electrical Characteristics in the Operating Ranges (B port: 5 V)

The following conditions apply unless otherwise specified.

$V_{CC1} = 5.0 \text{ V} \pm 10\%$ ,  $V_{CC2} = 3.3 \text{ V} \pm 0.3 \text{ V}$   $T_a = -40 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	Conditions*1	min	typ*2	max	Unit
Input high level voltage	$V_{IH}$	Logic high level guaranteed	2.0			V
Input low level voltage	$V_{IL}$	Logic low level guaranteed			0.8	V
Input high level current (input pins)	$I_{IH}$	$V_{CC1} = \text{max}$	$V_I = V_{CC1}$			$\pm 5$
Input high level current (I/O pins)						$\pm 15$
Input low level current (input pins)	$I_{IL}$	$V_{CC1} = \text{max}$	$V_I = \text{GND}$			$\pm 5$
Input low level current (I/O pins)						$\pm 15$
High impedance output current (Three-state output pins)	$I_{OZH}$	$V_{CC1} = \text{max}$	$V_O = 2.7 \text{ V}$			$\pm 10$
	$I_{OZL}$		$V_O = 0.5 \text{ V}$			$\pm 10$
Quiescent current	$I_{CC}$	$V_{CC1} = \text{max}$ , $V_{IN} = \text{GND}$ or $V_{CC1}$		0.08	1.5	mA

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

2. Typical values are values for  $V_{CC1} = 5.0 \text{ V}$ ,  $V_{CC2} = 3.3 \text{ V}$ , and an ambient temperature of  $+25^\circ\text{C}$ .

### LC74FCT164245T Output Drive Characteristics (B port: 5 V)

Parameter	Symbol	Conditions*1	min	typ*2	max	Unit
Output high level voltage	$V_{OH}$	$V_{CC1} = \text{min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -3 \text{ mA}$	2.5	3.5	V
			$I_{OH} = -15 \text{ mA}$	2.4	3.5	V
			$I_{OH} = -32 \text{ mA}^{*3}$	2.0	3.0	V
Output low level voltage	$V_{OL}$	$V_{CC1} = \text{min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 40 \text{ mA}$		0.2	0.55

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

2. Typical values are values for  $V_{CC1} = 5.0 \text{ V}$ ,  $V_{CC2} = 3.3 \text{ V}$ , and an ambient temperature of  $+25^\circ\text{C}$ .

3. Do not test more than one output at a time. The test time must not exceed 1 second.

## LC74FCT164245, 74FCT164245T

### LC74FCT164245 Output Drive Characteristics (B port: 5 V)

Parameter	Symbol	Conditions*1	min	typ*2	max	Unit
Output low level current	$I_{ODL}$	$V_{CC1} = 5\text{ V}, V_{IN} = V_{IH}\text{ or }V_{IL}, V_{OUT} = 1.5\text{ V}^{*3}$	60	115	150	mA
Output high level current	$I_{ODH}$	$V_{CC1} = 5\text{ V}, V_{IN} = V_{IH}\text{ or }V_{IL}, V_{OUT} = 1.5\text{ V}^{*3}$	-60	-115	-150	mA
Output high level voltage	$V_{OH}$	$V_{CC1} = \text{min}, V_{IN} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -0.1\text{ mA}$	$V_{CC1} - 0.2$		V
			$I_{OH} = -24\text{ mA}$	2.4	3.3	V
Output low level voltage	$V_{OL}$	$V_{CC1} = \text{min}, V_{IN} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 24\text{ mA}$	0.3	0.55	V

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

2. Typical values are values for  $V_{CC1} = 5.0\text{ V}$ ,  $V_{CC2} = 3.3\text{ V}$ , and an ambient temperature of  $+25^\circ\text{C}$ .

3. Do not test more than one output at a time. The test time must not exceed 1 second.

### Power Supply Current Characteristics

Parameter	Symbol	Conditions*1	min	typ*2	max	Unit
Quiescent current High-level TTL inputs	$\Delta I_{CC}$	$V_{CC1} = \text{max}, V_{CC2} = \text{max}, V_{IN} = V_{CC2} - 0.6\text{ V}^{*3}$		1.2	30	$\mu\text{A}$
Operating supply current*4	$I_{CCD}$	$V_{CC1} = \text{max}, V_{CC2} = \text{max}$ , outputs open, $\times \overline{OE} = \times \text{DIR} = \text{GND}$ , toggling a single input, 50% duty cycle	$V_{IN} = V_{CC2}$ , $V_{IN} = \text{GND}$	75	120	$\mu\text{A}/\text{MHz}$
Total supply current*5	$I_C$	$V_{CC1} = \text{max}, V_{CC2} = \text{max}$ , outputs open, $f_i = 10\text{ MHz}$ , $\times \overline{OE} = \times \text{DIR} = \text{GND}$ , toggling a single bit, 50% duty cycle	$V_{IN} = V_{CC2} - 0.6\text{ V}$ , $V_{IN} = \text{GND}$	1.2	4.7	mA
		$V_{CC1} = \text{max}, V_{CC2} = \text{max}$ , outputs open, $f_i = 2.5\text{ MHz}$ , $\times \overline{OE} = \times \text{DIR} = \text{GND}$ , toggling a 16 bits, 50% duty cycle	$V_{IN} = V_{CC2} - 0.6\text{ V}$ , $V_{IN} = \text{GND}$	3.5	8.5	

Note: 1. Values stipulated in the electrical characteristics for the corresponding product must be used for the test conditions for the maximum and minimum values.

2. Typical values are values for  $V_{CC1} = 5.0\text{ V}$ ,  $V_{CC2} = 3.3\text{ V}$ , and at an ambient temperature of  $+25^\circ\text{C}$ .

3. For the TTL drive inputs ( $V_{IN} = 2.4\text{ V}$ ), connect all the other inputs to  $V_{CC1}$  or GND.

4. Although this parameter cannot be directly measured, it is provided for calculating the total power dissipation.

5.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_H \cdot N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent current } (I_{CCL}, I_{CCH}, \text{ and } I_{CCZ})$   
 $\Delta I_{CC} = \text{Supply current for the high-level TTL inputs}$   
 $D_H = \text{Duty cycle for the high-level TTL inputs}$   
 $N_T = \text{The number of TTL inputs in } D_H$   
 $I_{CCD} = \text{Operating current due to input transition pairs (HLH or LHL)}$   
 $f_{CP} = \text{Clock frequency for register devices (zero for non-register devices)}$   
 $N_{CP} = \text{The number of clocks input in } f_{CP}$   
 $f_i = \text{Input frequency}$   
 $N_i = \text{The number of inputs in } f_i$

### LC74FCT164245/164245T Switching Characteristics in the Operating Ranges

Parameter	Symbol	Conditions*1	min*1	typ	max	Unit
Transmission delay (From A to B or from B to A)	$t_{PLH}$ , $t_{PHL}$	$C_L = 50\text{ pF}, R_L = 500\ \Omega$	1.5		7.0	ns
Output enable time (From $\times \overline{OE}$ to A or B)	$t_{PZH}^{*1}$ , $t_{PZL}^{*1}$		1.5		12.0	ns
Output disable time (From $\times \overline{OE}$ to A or B)	$t_{PHZ}^{*1}$ , $t_{PLZ}^{*1}$		1.5		7.5	ns
Output enable time (From $\times \text{DIRS}$ to A or B*3)	$t_{PZH}^{*2}$ , $t_{PZL}^{*2}$		1.5		9.5	ns
Output disable time (From $\times \text{DIRS}$ to A or B*3)	$t_{PHZ}^{*2}$ , $t_{PLZ}^{*2}$		1.5		7.5	ns

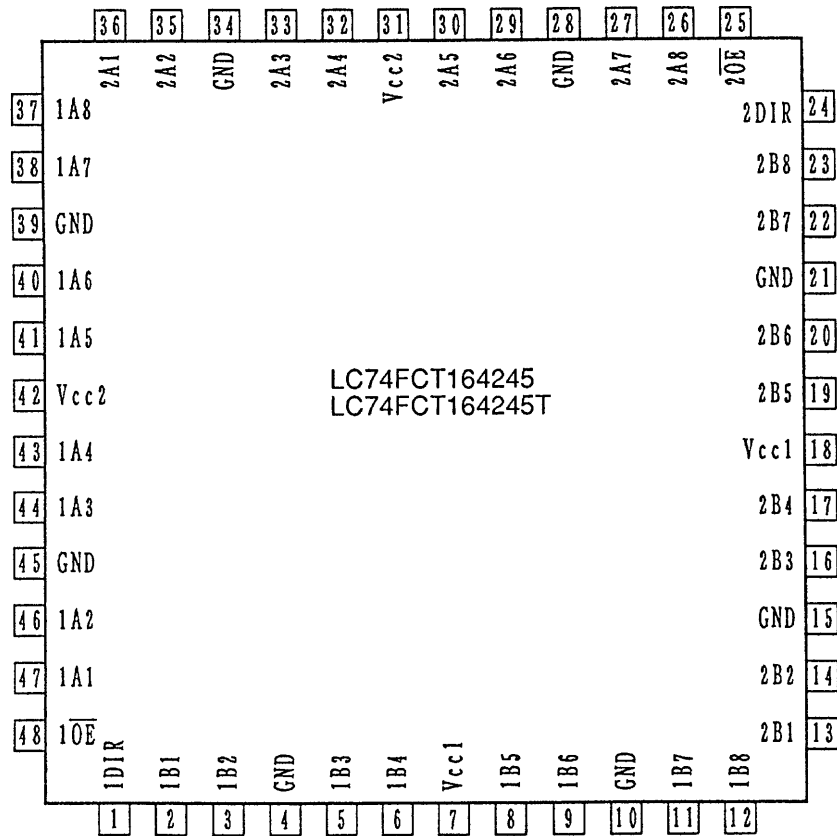
Note: 1. See the figures for the test circuit and waveforms.

2. Although the minimum values are guaranteed, the transmission delay is not tested.

3. This parameter is guaranteed but not tested.

## LC74FCT164245, 74FCT164245T

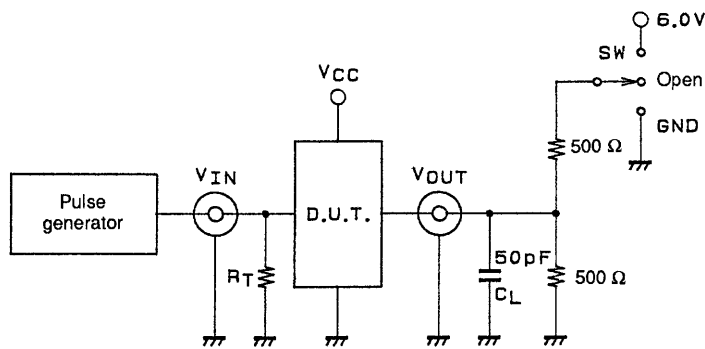
### Pin Assignment



Top view

### Test Circuit and Waveform Diagrams

#### Test Circuit for All Outputs



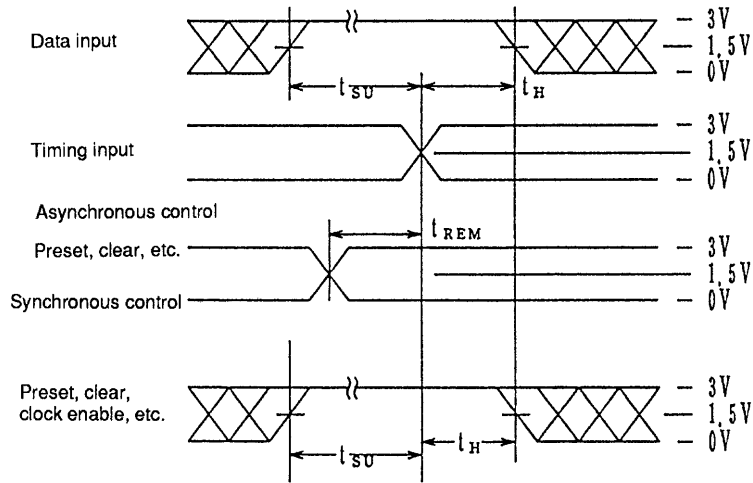
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#### Switch Positions

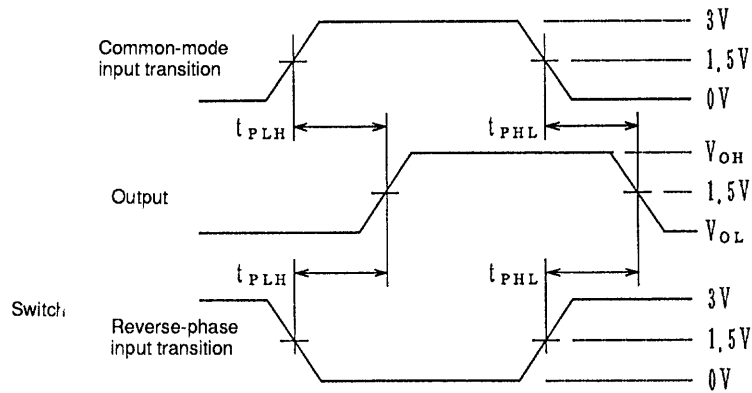
Test	Switch
Open drain, Disable low level, Enable low level	6.0 V
Disable high level, Enable high level	GND
All other tests	Open

Definitions:  $C_L$  = Load capacitance: including the jig and probe capacitances  
 $R_T$  = Terminating resistance: equivalent to the pulse generator's  $Z_{out}$ .

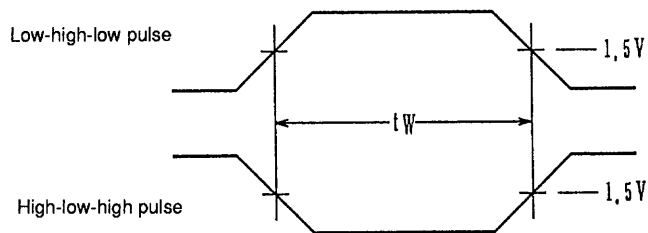
Setup, Hold, and Release Timing



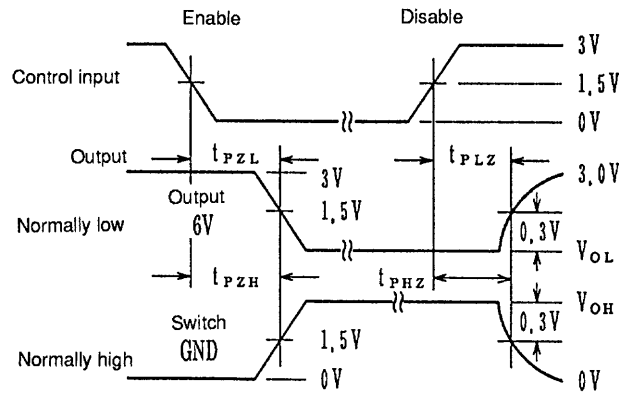
Transmission Delay



Pulse Width



Enable and Disable Timing



- Note: 1. These diagrams are for the input enable low level and the input control disable high level cases.  
 2. Pulse generator setup for all pulses: rate  $\leq 1.0$  MHz,  $Z_o \leq 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns

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