Ordering number : EN*4818

CMOS LSI

LC7861KE

Digital Signal Processor for Compact Disc Players

Preliminary

Overview

The LC7861KE is a CMOS LSI that implements the signal processing and servo control required by compact disk players, laser disks, CD-V, CD-I and related products.

The LC7861KE provides several types of signal processing to reduce the cost of CD player units, including demodulation of the optical pickup EFM signal, de-interleaving and error detection and correction. It also processes a rich set of servo system commands sent from the control microprocessor. It can directly interface to the dedicated serial inputs provided by the Sanyo LC78815 and LC78816 D/A converters.

Functions

- Input signal processing: The LC7861KE takes an HF signal as input, digitizes (slices) that signal at a precise level, converts that signal to an EFM signal, and generates a PLL clock with an average frequency of 4.3218 MHz by comparing the phases of that signal and a VCO output.
- Precise reference clock and necessary internal timing generation using an external 16.9344 MHz crystal oscillator
- Disk motor speed control using a frame phase difference signal generated from the playback clock and the reference clock
- Frame synchronization signal detection, protection and interpolation to assure stable data readout
- EFM signal demodulation and conversion to 8-bit symbol data
- Subcode data separation from the EFM demodulated signal and output of that data to an external microprocessor
- Subcode Q signal output to a microprocessor over the serial interface after performing a CRC error check
- Demodulated EFM signal buffering in internal RAM to handle up to ±4 frames of disk rotational jitter
- Demodulated EFM signal reordering in the prescribed order for data unscrambling and de-interleaving
- Error detection, correction, and flag processing (dual error correction scheme: C1 plus dual C2 correction)
- The LC7861KE sets the C2 flags based on the C1 flag and a C2 check, and then performs signal interpolation or previous value hold depending on the C2 flag. The interpolation circuit uses a quadruple interpolation scheme. The circuit holds the previous value for up to four consecutive C2 flags.
- Support for command input from a control microprocessor: commands include track jump, focus start, disk motor start/stop, muting on/off and track count (8-bit serial input)
- Built-in digital output circuits
- Arbitrary track counting to support high-speed data access
- Zero cross muting
- Support for double speed dubbing
- Complete support for CD-ROM products. The LC7861KE directly interfaces with the Sanyo LC89510 and can also handle CD-ROM XA applications.
- Output signals for use by external D/A converters to improve the output data continuity by oversampling and digital filtering

Features

- Compact and space-saving 64-pin QIP package
- Silicon-gate CMOS design (low power dissipation)
- Single 5 V power supply (suitable for portable sets)
- DEMO pin for improved operability in adjustment

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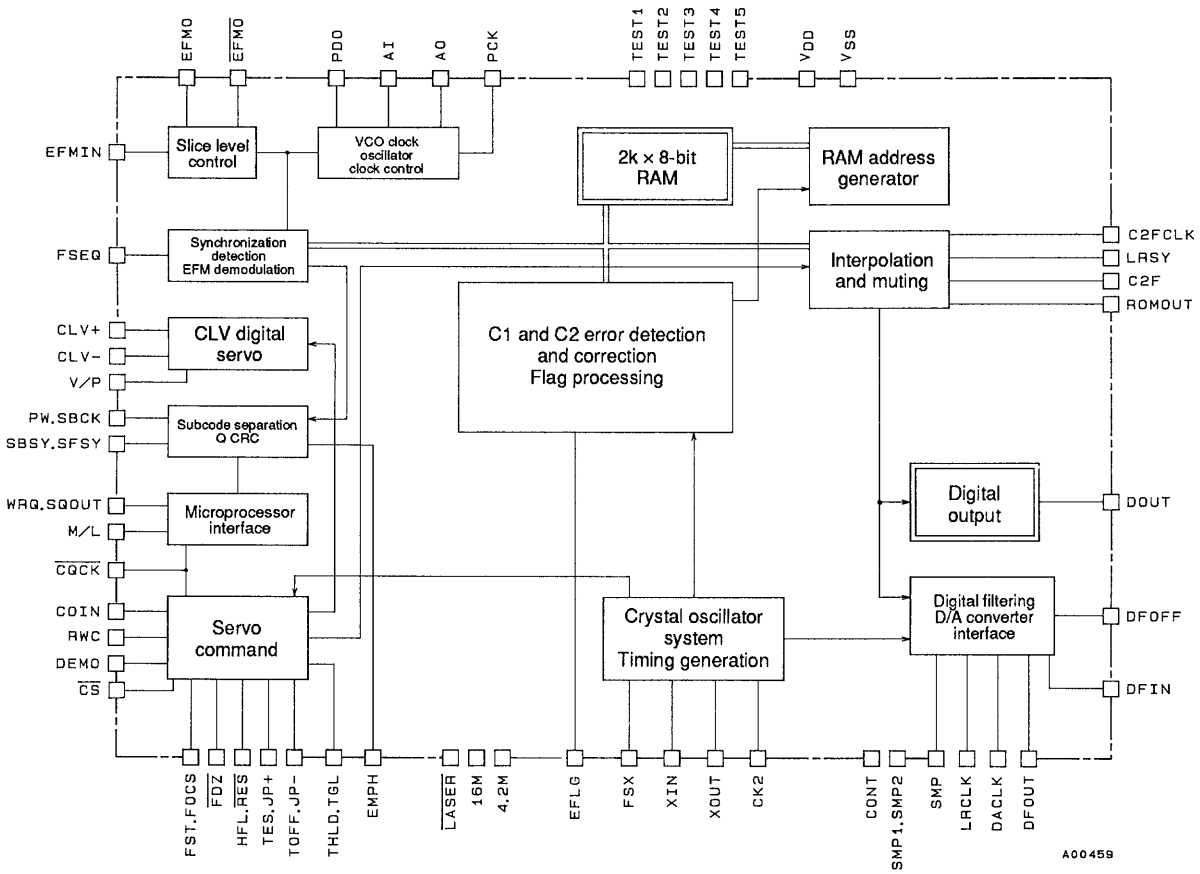
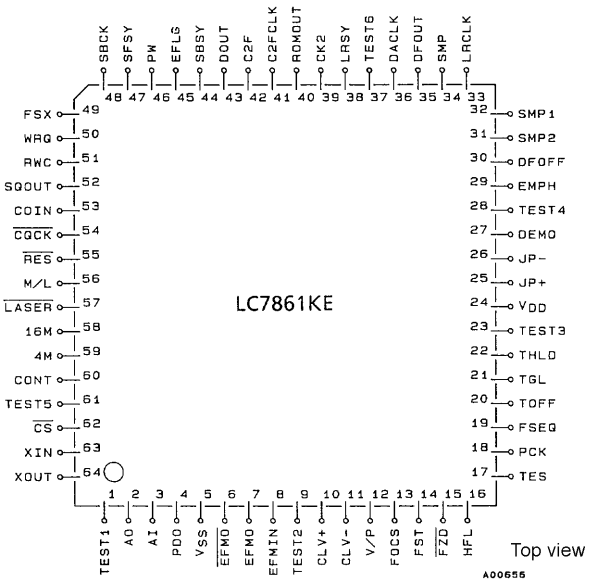
Equivalent Circuit Block Diagram

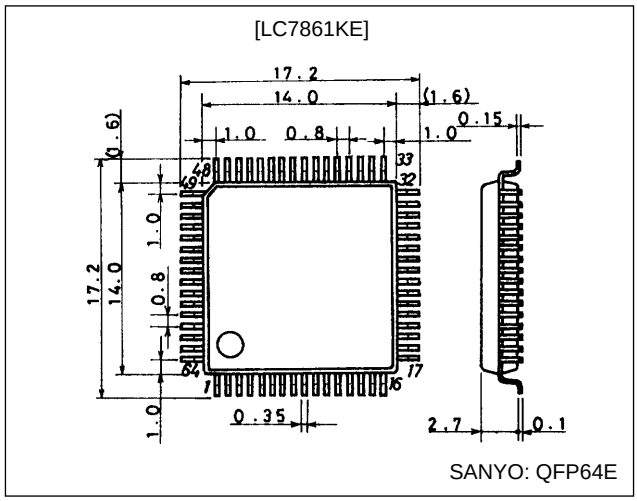


Pin Assignment



Package Dimensions

unit: mm



Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		V_{SS} – 0.3 to +7.0	V
Input voltage	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	V_{OUT}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max		300	mW
Operating temperature	Topr		–30 to +75	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	4.5		5.5	V
Input high level voltage	V_{IH} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, DFOFF, M/L, $\overline{RES}$	0.7 V_{DD}		V_{DD}	V
	V_{IH} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	2.2		V_{DD}	V
	V_{IH} (3)	EFMIN	0.6 V_{DD}		V_{DD}	V
	V_{IH} (4)	TES	0.8 V_{DD}		V_{DD}	V
Input low level voltage	V_{IL} (1)	TEST1 to 5, AI, $\overline{FZD}$, HFL, DEMO, DFOFF, M/L, $\overline{RES}$	V_{SS}		0.3 V_{DD}	V
	V_{IL} (2)	SBCK, RWC, COIN, $\overline{CQCK}$, $\overline{CS}$	V_{SS}		0.8	V
	V_{IL} (3)	EFMIN	V_{SS}		0.4 V_{DD}	V
	V_{IL} (4)	TES	V_{SS}		0.2 V_{DD}	V
Data setup time	$t_{set\ up}$	COIN, RWC: Figure 1	400			ns
Data hold time	t_{hold}	RWC: Figure 1	400			ns
High level clock pulse width	$t_{WøH}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Low level clock pulse width	$t_{WøL}$	SBCK, $\overline{CQCK}$: Figures 1, 2 and 3	400			ns
Data read access time	t_{RAC}	Figures 2 and 3	0		400	ns
Command output time	t_{RWC}	RWC: Figure 1	1000			ns
Sub-Q read enable time	t_{SQE}	Figure 2, no RWC signal		11.2		ms
Subcode read cycle	t_{sc}	Figure 3		136		µs
Subcode read enable	t_{se}	Figure 3	400			ns
Crystal oscillator frequency	fX'tal	X_{IN}, X_{OUT}		16.9344		MHz
Operating frequency range	fop (1)	AI	2.0		20	MHz
	fop (2)	EFMIN: $V_{IN} \geq 1$ Vp-p			10	MHz

Electrical Characteristics at Ta = 25°C, V_{SS} = 0 V, V_{DD} = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{DD}			17	30	mA
Input high level current	I_{IH} (1)	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{DD}			5	µA
	I_{IH} (2)	TEST1 to 5, DEMO, TESTA, $\overline{CS}$: V_{IN} = V_{DD} = 5.5 V	25		75	µA
Input low level current	I_{IL}	AI, EFMIN, $\overline{FZD}$, TES, SBCK, COIN, $\overline{CQCK}$, $\overline{RES}$, HFL, RWC, M/L: V_{IN} = V_{SS}	–5			µA
Output high level voltage	V_{OH} (1)	AO, PDO, EFMO, $\overline{EFMO}$, CLV^+, CLV^-, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX, V/P: I_{OH} = –1 mA	V_{DD} – 1			V
	V_{OH} (2)	DOUT: I_{OH} = –12 mA	V_{DD} – 0.5			V
	V_{OH} (3)	$\overline{LASER}$, SQOUT, 16M, 4.2M, CONT, SMP, SMP1, SMP2, LRCLK, WRQ, C2F, DFOUT, DACLK, SFSY, LRSY, SBSY, CK2, PW, ROMOUT, C2FCLK: I_{OH} = –0.5 mA	V_{DD} – 1			V

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output low level voltage	V_{OL} (1)	AO, PDO, EFMO, $\overline{\text{EFMO}}$, CLV^+, CLV^-, FOCS, FSEQ, PCK, TOFF, TGL, THLD, JP^+, JP^-, EMPH, EFLG, FSX, V/P: I_{OL} = 1 mA			1	V
	V_{OL} (2)	DOUT: I_{OL} = 12 mA			0.5	V
	V_{OL} (3)	$\overline{\text{LASER}}$, SQOUT, 16M, 4.2M, CONT, SMP, SMP1, SMP2, LRCLK, WRQ, DFOUT, DACLK, SFSY, CK2, PW, ROMOUT, C2FCLK, CF2, LRSY, SBSY: I_{OL} = 2 mA			0.4	V
	V_{OL} (4)	FST: I_{OL} = 5 mA			0.75	V
Output off leakage current	I_{OFF} (1)	PDO, FST: $V_{OH} = V_{DD}$			5	µA
	I_{OFF} (2)	PDO, FST: $V_{OL} = V_{SS}$	–5			µA

Wave Form

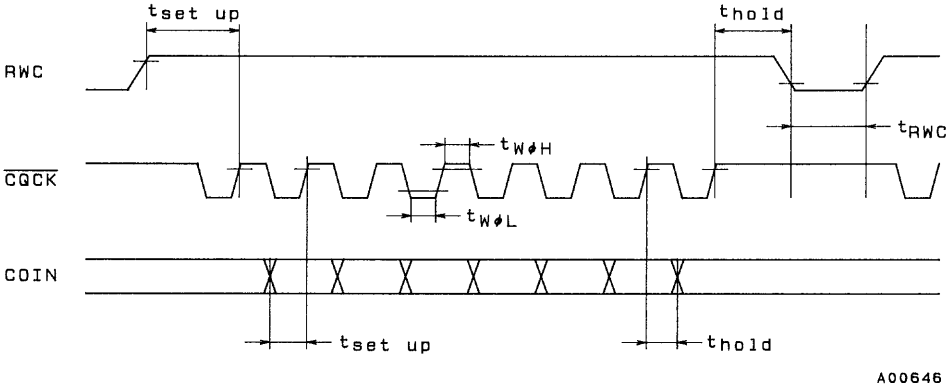

Figure 1 Command Input

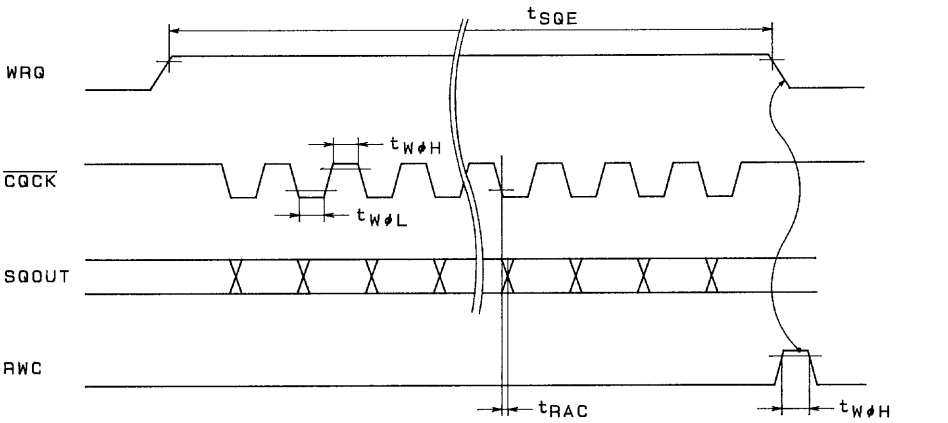

Figure 2 Subcode Q Output

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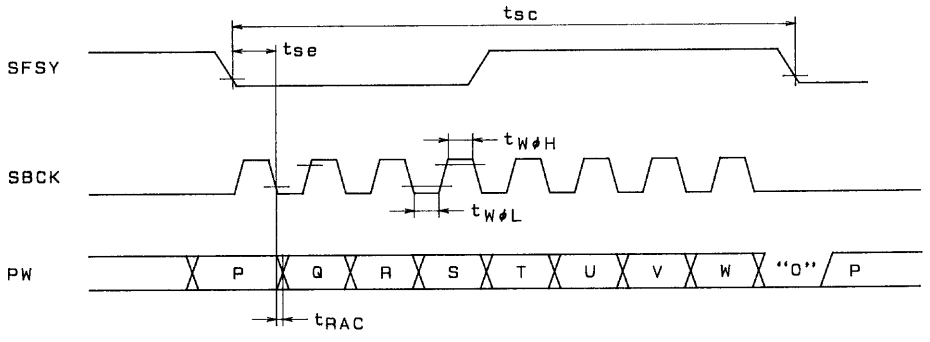

Figure 3 Subcode Output

Pin Functions

No.	Name	I/O	Description
1	TEST1	I	LSI test pin. Normally left open.
2	AO	O	Inputs for the LA9210 internal VCO output. (8.6436 MHz) Set up PDO so that the frequency increases when the EFM signal and the phase output are positive.
3	AI	I	
4	PDO	O	
5	V_{SS}	—	GND
6	$\overline{\text{EFMO}}$	O	Supply an HF signal with a 1 to 2 Vp-p level to EFMIN. EFMO and $\overline{\text{EFMO}}$ output EFM signals with opposite phases that passed through an amplitude limiter circuit. These are used for slice level control.
7	EFMO	O	
8	EFMIN	I	
9	TEST2	I	LSI test pin. Normally left open.
10	CLV^+	O	Disk motor control output.
11	CLV^-	O	
12	V/P	O	Outputs a high level during CLV rough servo and a low level during phase control.
13	FOCS	O	FOCS outputs a high level when the focus servo is off. The lens is lowered by FST, and when FOCS is high the lens is raised gradually. FOCS is reset when an $\overline{\text{FZD}}$ input occurs. These are used for focus pull-in.
14	FST	O	
15	$\overline{\text{FZD}}$	I	
16	HFL	I	PCK is the 4.3218 monitor pin. It outputs a high level when the synchronization (positive FS) detected from the EFM signal matches the counter synchronization (interpolation FS). (The output is latched for a single frame.)
17	TES	I	
18	PCK	O	
19	FSEQ	O	
20	TOFF	O	The LC7861KE outputs a kick pulse from JP^+ and JP^- in response to a track jump command. A track jump of the specified number of tracks (1, 4, 16, 32, 64, and 128) is performed.
21	TGL	O	
22	THLD	O	
23	TEST3	I	LSI test pin. Normally left open.
24	V_{DD}	—	+5 V
25	JP^+	O	
26	JP^-	O	
27	DEMO	I	Sound output function for end product adjustment manufacturing steps.
28	TEST4	I	LSI test pin. Normally left open.
29	EMPH	O	De-emphasis is required when high.
30	DFOFF	I	Digital filter on/off switch. Filtering is turned off on a high level input.
31	SMP2	O	Outputs for an external D/A converter. These include a latch signal, an L/R switching signal, and a sample and hold signal.
32	SMP1	O	
33	LRCLK	O	
34	SMP	O	
35	DFOUT	O	
36	DACLK	O	
37	DFIN	O	LSI test pin. Normally left open.
38	LRSY	O	CD-ROM application output signals
39	CK2	O	
40	ROMOUT	O	
41	C2FCLK	O	
42	C2F	O	
43	DOUT	O	Digital output
44	SBSY	O	Subcode block synchronization signal
45	EFLG	O	C1, C2, single and double error correction monitor pin
46	PW	O	SFSY is the subcode frame synchronization signal. The P, Q, R, S, T, U, V and W subcodes can be read out by applying 8 clock cycles to SBCK.
47	SFSY	O	
48	SBCK	I	
49	FSX	O	7.35 kHz synchronization signal output
50	WRQ	O	WRQ goes high when the subcode Q data passes the CRC check. An external controller can read out data from SQOUT by monitoring this pin and applying a $\overline{\text{CQCK}}$ signal. Set M/L to low when data is required LSB first.
51	RWC	I	
52	SQOUT	O	

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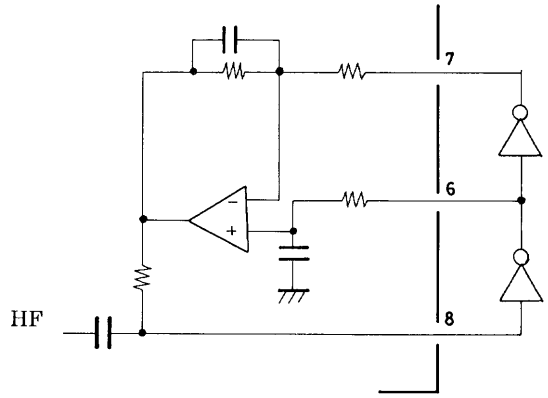
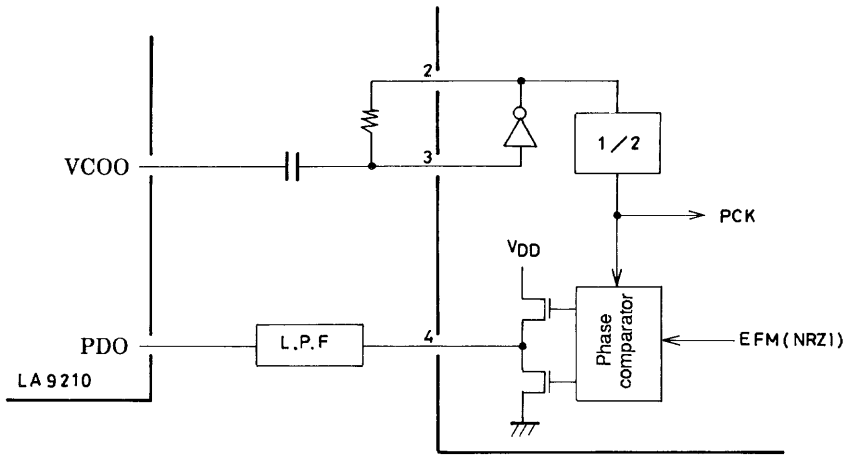
No.	Name	I/O	Description
53	COIN	I	The control microprocessor can send commands to the LC7861KE by setting RWC high and then sending command data synchronized with $\overline{CQCK}$. It is also possible to read out the TOC memory data by sending $\overline{CQCK}$ from the SQOUT pin by command switching.
54	$\overline{CQCK}$	I	
55	$\overline{RES}$	I	This pin must be set low briefly after power is first applied.
56	M/L	I	
57	$\overline{LASER}$	O	Output pin controllable by serial data sent from the microprocessor.
58	16M	O	16.9344 MHz output pin
59	4.2M	O	4.2336 MHz output pin
60	CONT	O	Output pin controllable by serial data sent from the microprocessor.
61	TEST5	I	LSI test pin. Normally left open.
62	$\overline{CS}$	I	Chip select pin. The LC7861KE becomes active when this pin is low. (A pull-down resistor is built-in.)
63	X_{IN}	I	Connections for a 16.9344 MHz crystal oscillator
64	X_{OUT}	O	

Pin Applications

1. HF signal input circuit; Pin 8: EFMIN, pin 7: EFMO, pin 6: $\overline{EFMO}$
   An EFM signal (NRZ) with an optimal slice level can be acquired by inputting the HF signal to EFMIN.



2. PLL clock generation circuit; Pin 4: PDO, Pin 3: AI, Pin 2: AO



A VCO can be constructed by combining the LC7861KE with the Sanyo LA9210M. The PDO pin swings in the positive direction when the VCO phase lags.

3. 1/2 VCO; Pin 18: PCK
   PCK is a monitor pin that outputs an average frequency of 4.3218 MHz, which is the VCO frequency divided by two.

4. Synchronization detection monitor; Pin 19: FSEQ
   Pin 19 goes high when the frame synchronization (a positive polarity synchronization signal) from the EFM signal read in by PCK and the timing generated by the counter (the interpolation synchronization signal) agree. This pin is a synchronization detection monitor. (It is held high for a single frame.)

5. CLV servo circuit; Pin 10: CLV^+, pin 11: CLV^-, pin 12: V/P

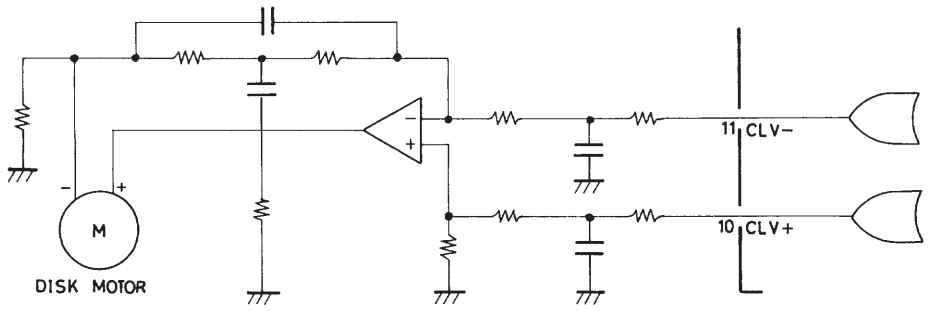
MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 1 0 0	DISC MOTOR START (accelerate)	
0 0 0 0 0 1 0 1	DISC MOTOR CLV (CLV)	
0 0 0 0 0 1 1 0	DISC MOTOR BRAKE (decelerate)	
0 0 0 0 0 1 1 1	DISC MOTOR STOP (stop)	o

The CLV^+ pin provides the signal that accelerates the disk in the forward direction and the CLV^- pin provides the signal that decelerates the disk. Commands from the control microprocessor select one of four modes; accelerate, decelerate, CLV and stop. The table below lists the CLV^+ and CLV^- outputs in each of these modes.

Mode	CLV^+	CLV^-
Accelerate	High	Low
Decelerate	Low	High
CLV	*	*
Stop	Low	Low

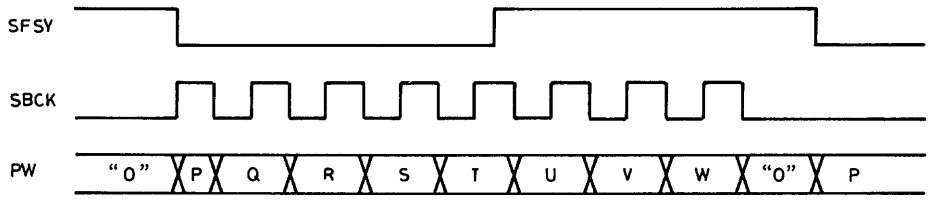
Note: *In CLV mode the LC7861KE detects the disk speed from the HF signal and provides proper linear speed using several different control schemes by switching the DSP internal modes. The PWM period is 7.35 kHz, the 1/64 duty period is 1.114s, and V/P outputs a high level during rough servo and a low level during phase control.

Internal mode	CLV^+	CLV^-	V/P
Rough servo (velocity too low)	High	Low	High
Rough servo (velocity too high)	Low	High	High
Phase control (PCK locked)	PWM	PWM	Low
Low speed (no HF signal)	1/64 duty	Low	High

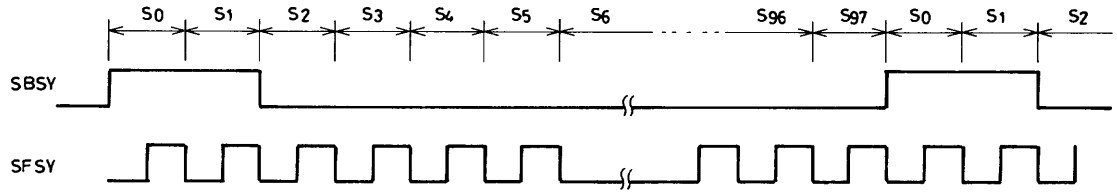


Note: After a CLV servo control command, the TOFF pin will be at the low level only for CLV mode, and will be high for all other modes. Controlling the TOFF pin by microprocessor command is only possible in CLV mode.

6. Subcode P, Q, and R to W output circuit; Pin 46: PW, pin 44: SBSY, pin 47: SFSY, pin 48: SBCK
PW is the subcode signal output pin, and all the codes, P, Q, and R to W can be read out by sending eight clocks to the SBCK pin within 136 µs after the fall of SFSY. The signal that appears on the PW pin changes on the falling edge of SBCK. If a clock is not applied to SBCK, the P code will be output from PW. SFSY is a signal that is output for each subcode frame cycle, and the rising edge of this signal indicates standby for the output of the subcode symbol (P to W). Subcode data P is output on the fall of this signal.



SBSY is a signal output for each subcode block. This signal goes high for the S0 and S1 synchronization signals. The fall of this signal indicates the end of the subcode synchronization signals and the start of the data in the subcode block. (EIAJ format)

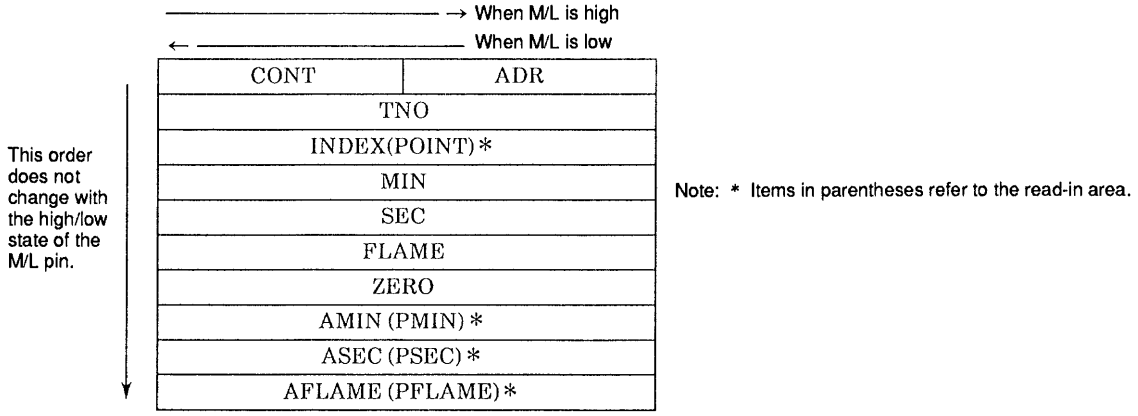


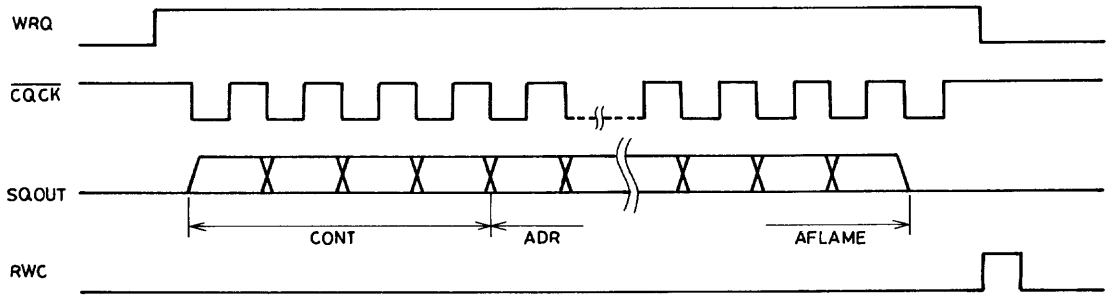
7. Subcode Q output circuit; Pin 50: WRQ, pin 51: RWC, pin 52: SQOUT, pin 54: $\overline{\text{CQCK}}$, pin 56: M/L, pin 62: $\overline{\text{CS}}$

MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 1	ADDRESS FREE	
1 0 0 0 1 0 0 1	ADDRESS 1	o
1 0 0 0 1 1 1 0	OSC ON	o
1 0 0 0 1 1 0 1	OSC OFF	

Subcode Q can be read from the SQOUT pin by applying a clock to the $\overline{\text{CQCK}}$ pin.
Of the eight bits in the subcode, the Q signal is used for song (track) access and display. The WRQ will be high only if the data passed the CRC error check and the subcode Q format internal address is 1*. The control microprocessor can read out data from SQOUT in the order shown below by detecting this high level and applying $\overline{\text{CQCK}}$. When $\overline{\text{CQCK}}$ is applied the DSP disables register update internally. The microprocessor should give update permission by setting RWC high briefly after reading has completed. WRQ will fall to low at this time. Since WRQ falls to low 11.2 ms after going high, $\overline{\text{CQCK}}$ must be applied during the high period. Data can be read out in an LSB first format if the M/L pin is set low, and in an MSB first format if that pin is set low.

Note: * That state will be ignored if an address free command is sent. This is provided to handle CDV applications.



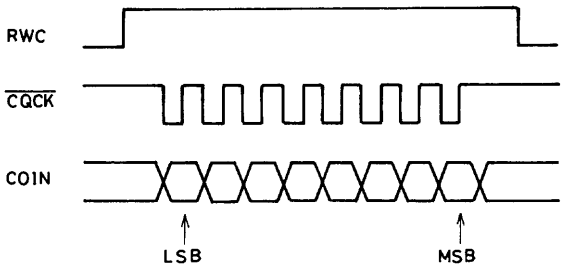


Note: 1. Normally, the WRQ pin indicates the subcode Q standby state. However, it is used for a different monitoring purpose in track count mode. (See the item on track counting for details.)
2. The LC7861KE becomes active when the $\overline{CS}$ pin is low, and data is output from the SQOUT pin. When the $\overline{CS}$ pin is high, the SQOUT pin goes to the high impedance state.
3. The "OSC OFF" command turns off the VCO and the crystal oscillator.

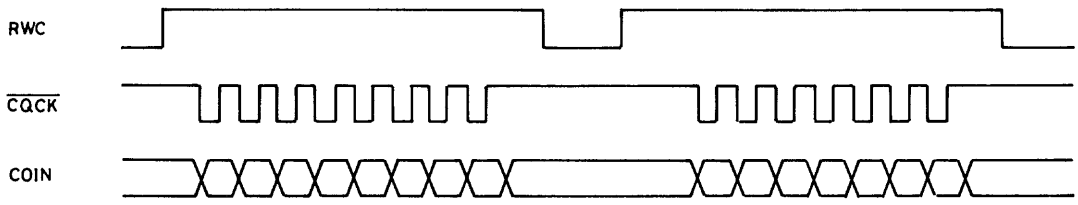
8. Servo command function; Pin 51: RWC, pin 53:COIN, pin 54: $\overline{CQCK}$, pin 62: $\overline{CS}$
Instructions can be input to the LC7861KE by setting RWC high and sending commands in synchronization with the $\overline{CQCK}$. The LC7861KE is basically upwardly compatible with the earlier LC7860K and LC7863K with respect to the control microprocessor. The commands can be classified as follows. New commands not supported by the earlier LC7860K and LC7863K are marked with a " o " in the command table.

Focus start Track jump Mute control Disc motor control Other control commands	1-byte commands
Track count	2-byte command

• One-byte commands



• Two-byte commands



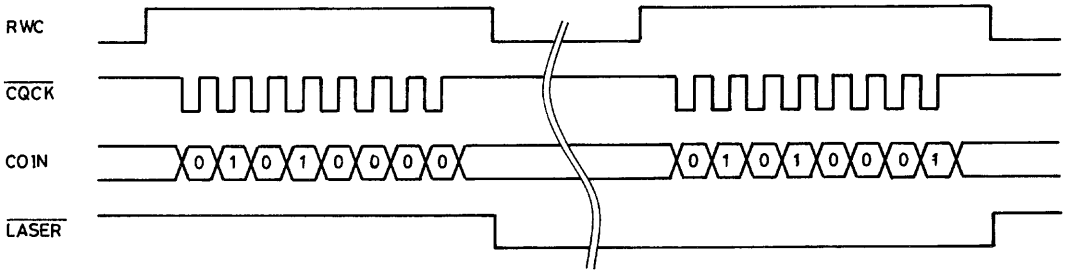
Commands are executed starting at the fall of the RWC signal.

9. Focus servo circuit; Pin 13: FOCS, pin 14: FST, pin 15: $\overline{\text{FZD}}$, pin 57: $\overline{\text{LASER}}$
Commands

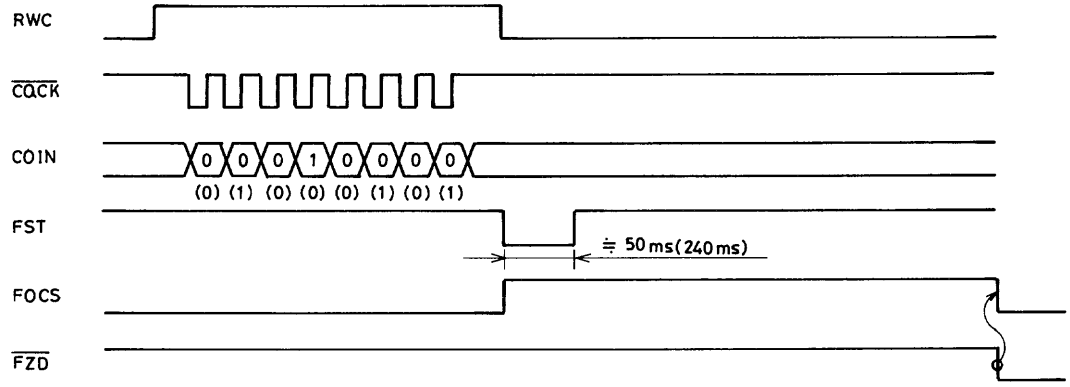
MSB LSB	Command	$\overline{\text{RES}}$ = low
0 0 0 0 1 0 0 0	FOCUS START #1	
1 0 1 0 0 0 1 0	FOCUS START #2	
0 0 0 0 1 0 1 0	LASER ON	
1 0 0 0 1 0 1 0	LASER OFF	o
0 0 0 0 0 0 0 0	NOTHING	

When a focus start instruction (either FOCUS START #1 or FOCUS START #2) is input as a servo command, first the charge on capacitor C1 is discharged by FST and the objective lens is lowered. Next, the capacitor is charged by FOCS, and the lens is slowly raised. $\overline{\text{FZD}}$ falls when the lens reaches the focus point. When this signal is received, FOCS is reset and the focus servo turns on. After sending the command, the microprocessor should check DRF to confirm focus before proceeding to the next part of the program. If focus is not achieved by the time C1 is fully charged, the microprocessor should issue another focus command and iterate the focus servo operation.

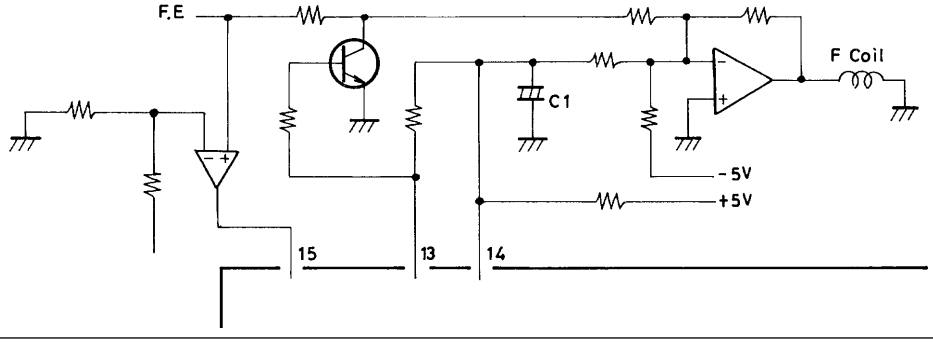
- LASER control



- Focus start (Values in parentheses are for the LASER START #2 command. The only difference is in the FST low period.)

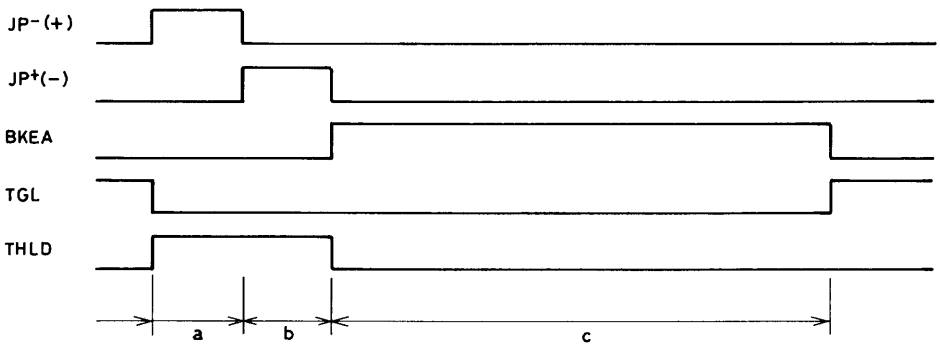


— An $\overline{\text{FZD}}$ falling edge will not be accepted during the period that FST is low.
— After issuing a focus start command, initialization will be performed if RWC is set high. Therefore, do not issue the next command during focus start until the focus coil drive S curve has completed.
— When focus cannot be achieved (i.e., when $\overline{\text{FZD}}$ does not go low) the FOCS signal will remain in the high state, so the microprocessor should initialize the system by issuing a NOTHING command.
— When the RESET pin is set low, the $\overline{\text{LASER}}$ pin is set high directly.
— Focus start using the DEMO coil executes a mode #1 focus start.



10. Track jump circuit; Pin 16: HFL, pin 17: TES, pin 20: TOFF, pin 21: TGL, pin 22: THLD, pin 25: JP^+, pin 26: JP^-

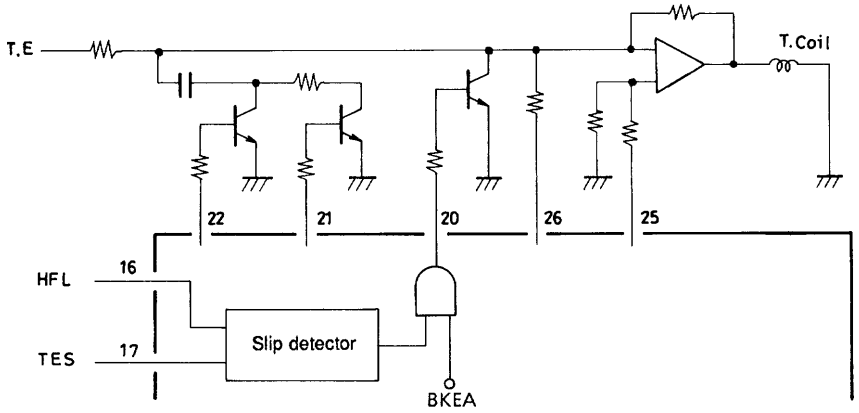
MSB LSB	Command	$\overline{RES}$ = low
1 0 1 0 0 0 0 0	TRACK JUMP (earlier version)	o
1 0 1 0 0 0 0 1	TRACK JUMP (new command)	
1 0 0 0 1 1 0 0	TRACK JUMP BRAKE	
0 0 0 0 1 1 1 1	TOFF	
1 0 0 0 1 1 1 1	TON	o
0 0 0 1 0 0 0 1	1 TRACK JUMP IN #1	
0 0 0 1 0 0 1 0	1 TRACK JUMP IN #2	
0 0 1 1 0 0 0 1	1 TRACK JUMP IN #3	
0 0 0 1 0 0 1 1	4 TRACK JUMP IN	
0 0 0 1 0 1 0 0	16 TRACK JUMP IN	
0 0 1 1 0 0 0 0	32 TRACK JUMP IN	
0 0 0 1 0 1 0 1	64 TRACK JUMP IN	
0 0 0 1 0 1 1 1	128 TRACK JUMP IN	
0 0 0 1 1 0 0 1	1 TRACK JUMP OUT #1	
0 0 0 1 1 0 1 0	1 TRACK JUMP OUT #2	
0 0 1 1 1 0 0 1	1 TRACK JUMP OUT #3	
0 0 0 1 1 0 1 1	4 TRACK JUMP OUT	
0 0 0 1 1 1 0 0	16 TRACK JUMP OUT	
0 0 1 1 1 0 0 0	32 TRACK JUMP OUT	
0 0 0 1 1 1 0 1	64 TRACK JUMP OUT	
0 0 0 1 1 1 1 1	128 TRACK JUMP OUT	
0 0 0 1 0 1 1 0	256 TRACK CHECK	



When the LC7861KE receives a track jump instruction as a servo command, it first generates accelerating pulses (period a) and next generates deceleration pulses (period b). The passage of the braking period (period c) completes the specified jump. During the braking period, the LC7861KE detects the beam slip direction from the TES and HFL inputs. TOFF is used to cut the components in the TE signal that aggravate slip. The jump destination track is captured by increasing the servo gain with TGL. In all the disk motor control operations, the TOFF pin only goes low during CLV mode, and will be high during the start, stop, and brake operations. Note that the TOFF pin can be turned on and off independently by microprocessor issued commands. However, this function is only valid when disk motor control is in CLV mode. The table lists the relationships between accelerating pulses, deceleration pulses and the braking period.

Command	Standard track jump mode			New track jump mode		
	a	b	c	a	b	c
1 TRACK JUMP IN (OUT) #1	233 µs	233 µs	100 ms	233 µs	233 µs	100 ms
1 TRACK JUMP IN (OUT) #2	0.5-track jump	233 µs	100 ms	0.5-track jump	a period	100 ms
1 TRACK JUMP IN (OUT) #3	0.5-track jump	233 µs	Does not occur	0.5-track jump	a period	Does not occur
4 TRACK JUMP IN (OUT)	2-track jump	466 µs	100 ms	2-track jump	a period	100 ms
16 TRACK JUMP IN (OUT)	9-track jump	7-track jump	100 ms	9-track jump	a period	100 ms
32 TRACK JUMP IN (OUT)	18-track jump	14-track jump	100 ms	18-track jump	14-track jump	100 ms
64 TRACK JUMP IN (OUT)	36-track jump	28-track jump	100 ms	36-track jump	28-track jump	100 ms
128 TRACK JUMP IN (OUT)	72-track jump	56-track jump	100 ms	72-track jump	56-track jump	100 ms
256 TRACK CHECK	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		100 ms	TOFF goes high after 256 tracks are jumped. The a and b pulses are not output.		100 ms
TRACK JUMP BRAKE	There are no a or b periods.		100ms	There are no a or b periods.		100 ms

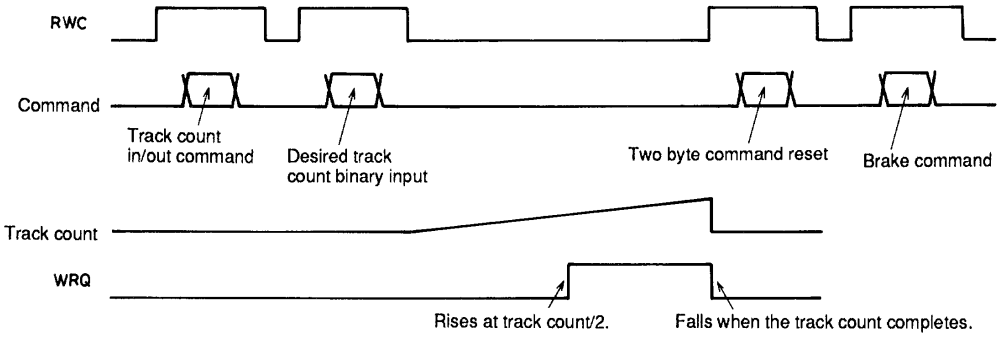
Note: 1. As indicated in the table, actuator signals are not output during the 256 TRACK CHECK function. This is a mode in which the TES signal is counted in the TRACKING LOOP OFF state. Therefore, feed motor forwarding is required.
2. The servo command register is automatically reset after the track jump sequence (a, b, c) completes.
3. If another track jump command is issued during a track jump operation, the content of that new command will be executed starting immediately.
4. The maximum braking time (period c) has been changed from the 17 ms of the earlier LC7861NE to 100 ms in the LC7861KE.



11. Track counting circuit; Pin 16: HFL, pin 17: TES, pin 20: TOFF

MSB LSB	Command	$\overline{RES}$ = low
1 1 1 1 0 0 0 0	TRACK COUNT IN	
1 1 1 1 1 0 0 0	TRACK COUNT OUT	
1 1 1 1 1 1 1 1	TWO-BYTE COMMAND RESET	o
1 0 0 0 1 1 0 0	TRACK JUMP BRAKE	

The LC7861KE will count the specified number of tracks when the microprocessor sends an arbitrary binary value in the range 16 to 254 after issuing either a track count in or a track count out command. The TOFF pin will output a high level during the track count operation and the tracking loop will be turned off. Therefore, feed motor forwarding is required.



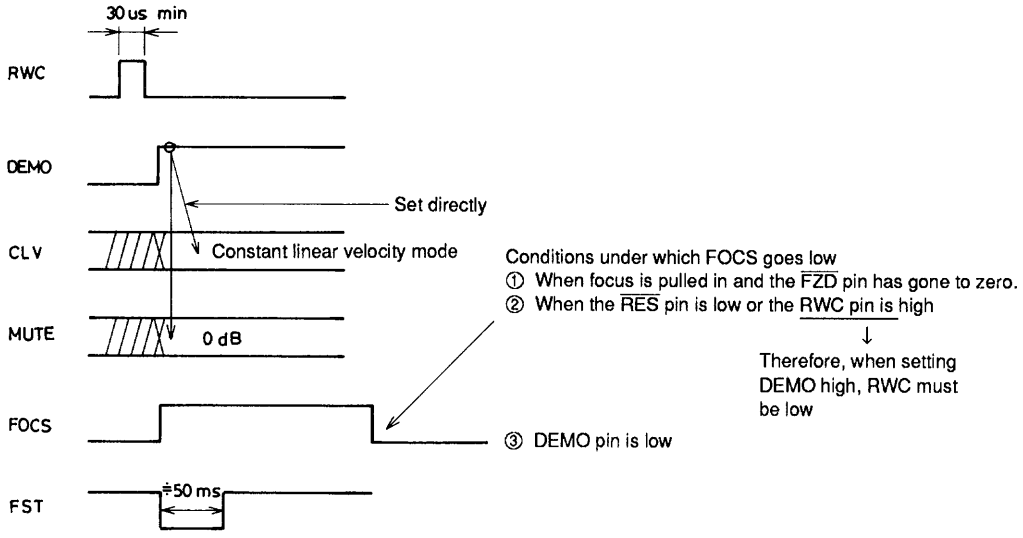
Note: 1. When the desired track count is input in binary, the track count operation is started by the fall of RWC.
2. When a track count in/out command is issued the function of the WRQ signal switches from the normal mode subcode Q standby monitor function to a track count monitor function. This signal goes high when the track count is half completed, and goes low when the count finishes. The control microprocessor should monitor this signal to determine when the track count completes.
3. If a two-byte command reset command is not issued, the track count operation will be repeated. That is, to skip over 20,000 tracks, issue a track count 200 command once, and then count the WRQ signal 100 times.
4. After performing a track count operation, use the brake command to have the pickup lock onto the track.

The track count operations in items 10 and 11 basically count the TES signal from the LA9210. The following two clocks are provided internally in the LC7861KE as track counting clocks. To use the earlier track count function, initialize the LC7861KE with a 23H command when power is first applied.

MSB LSB	Command	$\overline{RES}$ = low
0 0 1 0 0 0 1 0	NEW TRACK COUNT FUNCTION (using the TES/HFL combination)	o
0 0 1 0 0 0 1 1	EARLIER TRACK COUNT FUNCTION (directly counts the TES signal)	

The earlier track count function uses the TES signal directly as the internal track counter clock.
To reduce counting errors resulting from noise on the rising and falling edges of the TES signal, the new track count function prevents noise induced errors by using the combination of the TES and HFL signals, and implements a more reliable track count function. However, dirt and scratches on the disk can result in HFL signal dropouts that may result in missing track count pulses. Thus care is required when using this function.

12. Adjustment process sound output function; Pin 27: DEMO

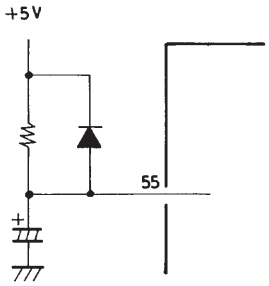


By setting this pin high, muting can be set to 0 dB, the disk motor can be set to CLV, and a focus start operation can be performed, even without issuing any commands from the control microprocessor. Also, since the $\overline{LASER}$ pin becomes active, if the mechanism and servo systems are complete, sound can be produced without the presence of a microprocessor.

13. Reset circuit; Pin 55: $\overline{RES}$

When power is first applied, this pin should be briefly set low and then set high. This will set the muting to –∞ dB and stop the disk motor.

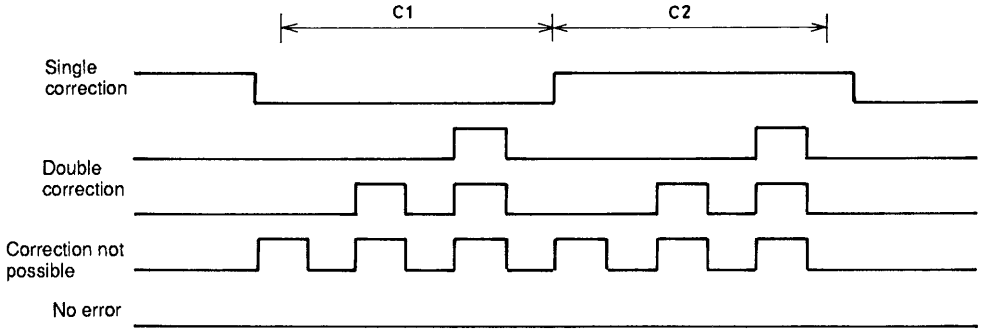
Constant linear velocity servo	START	[STOP]	BRAKE	CLV
Muting control	0 dB	–12 dB	[∞]	
Q subcode address conditions	[Address 1]	Address free		
Laser control	ON (low)	[OFF]	(high)	
Track jump mode	[Standard]	New		
Track count mode	Standard	[New]		



14. De-emphasis ON/OFF; Pin 29: EMPH

The preemphasis on/off bit in subcode Q control information is output from the EMPH pin. De-emphasis should be performed when this signal is high.

15. Error flag output; Pin 45: EFLG, pin 49: FSX

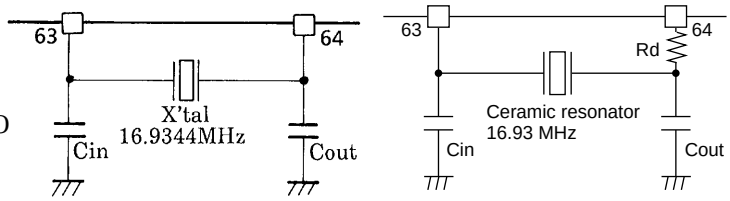


The FSX signal is generated by dividing the crystal oscillator clock, and is a 7.35 kHz frame synchronization signal. The error correction state for each frame is output from EFLG. The playback OK/NG state can be easily determined from the extent of the high level that appears here.

16. Crystal clock oscillator; Pin 63: X_{IN}, pin 64: X_{OUT}

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 1 1 0	OSC ON	o
1 0 0 0 1 1 0 1	OSC OFF	
1 1 0 0 0 0 0 1	DOUBLE SPEED MODE	
1 1 0 0 0 0 1 0	NORMAL MODE	o
0 1 1 0 0 0 0 0	VCO 8M	o
0 1 1 0 0 0 0 1	VCO 16M	

The clock that is used as the time base is generated by connecting a 16.9344 MHz crystal oscillator between these pins. This oscillator can be turned on and off under command control. (The OSC OFF command turns off both the VCO and crystal oscillators.)
Also, the LC7861KE can be set up to handle double speed operation under command control. The table lists the relationships between the crystal and VCO oscillators.



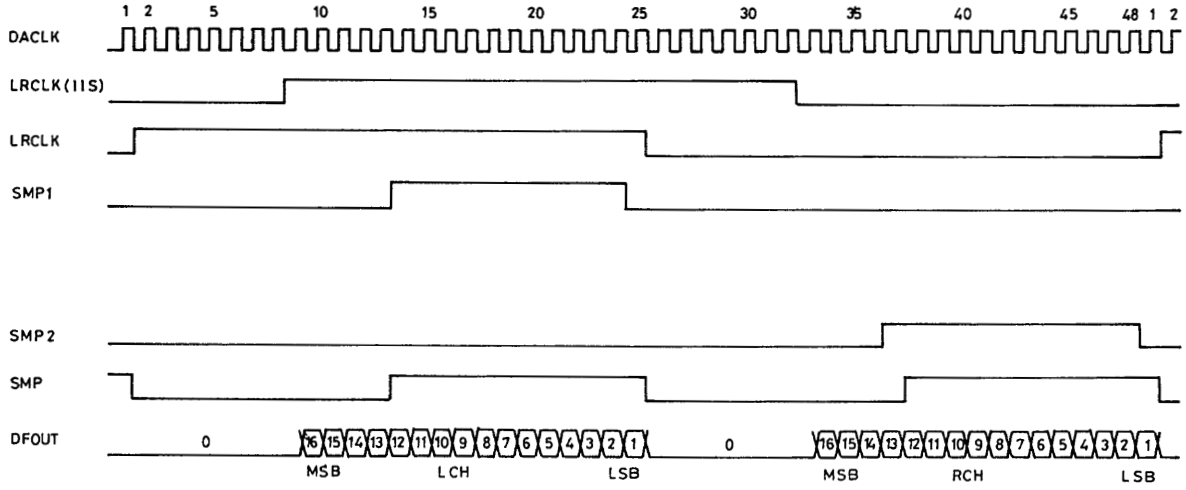
VCO playback speed	Mode 8M		Mode 16M	
	Normal speed mode	Double speed mode	Normal speed mode	Double speed mode
After reset	o	—	—	—
AI pin external input (8M VCO)	8.6436 MHz			
AI pin external input (17M VCO)			17.2872 MHz	17.2872 MHz
AI pin external input (LA9210)	8.6436 MHz	17.2872 MHz		
PCK monitor output	4.3218 MHz	8.6436 MHz	4.3218 MHz	8.6436 MHz

Crystal Clock Oscillator Recommended Values

Manufacturer	Oscillator	Cin/Cout
CITIZEN WATCH CO., LTD. (Crystal)	CSA-309 HC-49/U-S (16.9344 MHz)	5 pF to 12 pF (Cin = Cout)
TDK CO., LTD (Ceramic resonator)	FCR16.93M2G	Rd = 100 Ω (±20%) Cin = Cout = 15 pF (±20%)
	FCR16.93MCG	Rd = 47 Ω (±20%) Cin = Cout = 30 pF (built in)

Note: Since the conditions on the circuit board actually used will vary, the values of the load capacitances Cin and Cout must be verified on the circuit board actually used.a

17. D/A converter interface; Pin 30: DFOFF, pin 34: SMP, pin 33: LRCLCK, pin 35: DFOUT, pin 36: DACLK, pin 32: SMP1, pin 31: SMP2
Data for the D/A converter is output MSB first from DFOUT synchronized with the falling edge of DACLK.



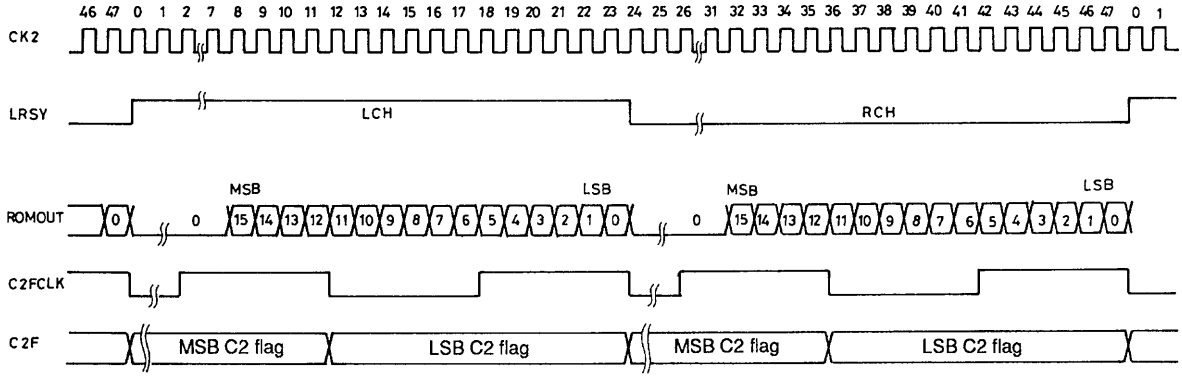
Note: DACLK = 4.2336 MHz (when DFOFF is low)
DACLK = 2.1168 MHz (when DFOFF is high)

MSB	LSB	Command	$\overline{RES}$ = low
0 1 1 0 0 0 1 0		IIS ON	
0 1 1 0 0 0 1 1		IIS OFF	o
1 0 0 0 1 0 0 0		CDROM XA	
1 0 0 0 1 0 1 1		CONT AND CD-ROM XA RESET	o

When a CD-ROM XA command is issued, data that is neither interpolated nor muted will be output from the DFOUT and DOUT pins. (This command is used for CD-ROM XA application.) The CD-ROM XA reset command also functions as a pin 60 CONT reset, so caution is required.

18. CD-ROM outputs; Pin 39: CK2, pin 37: LRSY, pin 40: ROMOUT, pin 42: C2F, pin 41: C2FCLK
Data is output MSB first from the ROM OUT pin in synchronization with the LRSY signal. This data is appropriate for input to a CD-ROM LSI, since it is not interpolated, previous value held, or processed by the digital filter circuits. CK2 is a 2.1168 MHz clock, and data is output on the CK2 rising edge. C2F is the flag information for data in 8-bit units. C2FCLK is the synchronization signal for that flag.

LC8951 and LC7861 Interface



19. Mute control circuit

MSB	LSB	Command	$\overline{RES}$ = low
0 0 0 0 0 0 0 1		MUTE: 0 dB	
0 0 0 0 0 0 1 0		MUTE: –12 dB	
0 0 0 0 0 0 1 1		MUTE: ∞ dB	o

An attenuation of 12 dB (MUTE –12 dB) or full muting (MUTE ∞ dB) can be applied by issuing the appropriate command from the table. Since zero cross muting is used, there is no noise associated with this function. Zero cross is defined for this function as the top seven bits being all ones or all zeros.

20. 4.2M and 16M pins; Pin 59: 4.2M, pin 58: 16M
The 16.9344 MHz external crystal oscillator 16.9344 MHz buffer output signal is output from the 16M pin. That frequency divided by four (a 4.2336 MHz frequency) is output from the 4.2M pin. When the oscillator is turned off both these pins will be fixed at either high or low. These frequencies do not change when a double speed command is issued.

21. Digital output circuit; Pin 43: DOUT
This is an output pin for use with a digital audio interface. Data is output in the EIAJ format. This signal is a signal that has passed through the interpolation and muting circuits. This pin has a built-in driver circuit and can directly drive a transformer.

22. CD-ROM XA; Pin 60: CONT
The LC7861KE switches to CD-ROM XA mode when an 88H command is issued and data that has not passed through the interpolation circuit is output from the DFOUT pin. The LC7861KE returns to normal mode when an 8BH command is issued, and interpolated data is output. Note that the 8BH command also functions as a CONT pin (pin 60) reset.

MSB LSB	Command	$\overline{RES}$ = low
1 0 0 0 1 0 0 0	CD-ROM XA ON	
1 0 0 0 1 0 1 1	CD-ROM XA OFF	o

23. CONT pin; Pin 60: CONT

MSB LSB	Command	$\overline{RES}$ = low
0 0 0 0 1 1 1 0	CONT	Low
1 0 0 0 1 0 1 1	CONT AND CD-ROM XA RESET	o

Pin 60 will goes high when this command is issued.

24. Other pins; Pin 1: TEST1, pin 9: TEST2, pin 23: TEST3, pin 28: TEST4, pin 37: TEST6, pin 61: TEST5
These pins are used for testing the LSI's internal circuits. Since the pins TEST1 to TEST 5 have built-in pull-down resistors, they can be left open in normal operation.

Circuit Block Operating Descriptions

1. RAM address control
The LC7861KE incorporates an 8-bit × 2k-word RAM on chip. This RAM is used as a buffer memory, and has an EFM demodulated data jitter handling capacity of ±4 frames. The LC7861KE continuously checks the remaining buffer capacity and controls the data write address to fall in the center of the buffer capacity by making fine adjustments to the PCK side of the CLV servo circuit and the frequency divisor. If the ±4 frame buffer capacity is exceeded, the LC7861KE forcibly sets the write address to the ±0 position. However, since the errors that occur due to this operation cannot be handled with error flag processing, the IC applies muting to the output for a 128 frame period.

Position	Division ratio or processing	
–4 or less	Force to ±0	
–3	589	Increase ratio
–2	589	
–1	589	
±0	588	Standard ratio
+1	587	Decrease ratio
+2	587	
+3	587	
+4 or more	Force to ±0	

2. C1 and C2 error correction
The EFM demodulated data is written to internal RAM to compensate for jitter, and the LC7861KE performs the following processing with a constant timing based on the crystal oscillator clock. First, the LC7861KE performs C1 error checking and correction in the C1 block, determines the C1 flags, and writes the C1 flag register. Next, the LC7861KE performs C2 error checking and correction in the C2 block, determines the C2 flags, and writes data to internal RAM.

C1 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Correction · Flag set
3 errors or more	Correction not possible · Flag set

C2 flag	Error correction and flag processing
No errors	No correction required · Flag reset
1 error	Correction · Flag reset
2 errors	Depends on C1 flags*1
3 errors or more	Depends on C1 flags*2

Note: 1. If the positions of the errors determined by the C2 check agree with the those specified by the C1 flags, the correction is performed and the flags are cleared. However, if the number of C1 flags is 7 or higher, C2 correction may fail. In this case correction is not performed and the C1 flags are taken as the C2 flags without change. Error correction is not possible if one error position agrees and the other does not. Furthermore, if the number of C1 flags is 5 or under, the C1 check result can be seen as unreliable. Accordingly, the flags will be set in this case. Cases where the number of C1 flags is 6 or more are handled in the same way, and the C1 flags are taken as the C2 flags without change. When there is not even one agreement between the error positions, error correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flags are set in this case. The other C1 flags are taken as the C2 flags without change.

2. When data is determined to have three or more errors and be uncorrectable, correction is, of course, impossible. Here, if the number of C1 flags was 2 or under, data that was seen as correct after C1 correction is now seen as incorrect data. The flag is set in this case. The other C1 flags are taken as the C2 flags without change.