Ordering number : ENA0575

SANYO Semiconductors
DATA SHEET

# LC7942KD — CMOS IC Dot-Matrix LCD Drivers

## Overview

The LC7942KD is a common driver LSI for driving large dot-matrix LCD displays. It features a built-in 64-bit bidirectional shift register and a 4-level LCD driver. It can also be connected in cascade to increase the number of bits. The LC7942KD is designed to be used with LC7940KD (QIP100D) or LC7941KDR (QIP100DR) segment drivers to drive large LCD panels.

## Features

- 64 built-in LCD display drive circuits
- 1/64 to 1/128 display duty cycle
- Input/outputs for cascade conection
- Bias supply voltages can be supplied externally
- Operating supply voltage and ambient temperature:
  2.7 to 5.5V logic supply ($V_{DD}$) at Ta = -20 to +85°C
  8 to 20V LCD supply ($V_{DD}$-$V_{EE}$) at Ta = -20 to +85°C
- CMOS process
- package: QIP80D

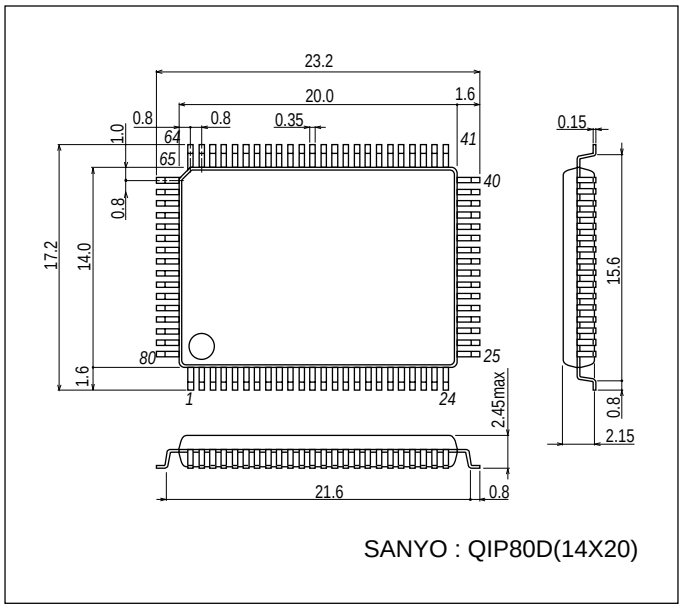



SANYO Semiconductor Co., Ltd.
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Package Dimensions

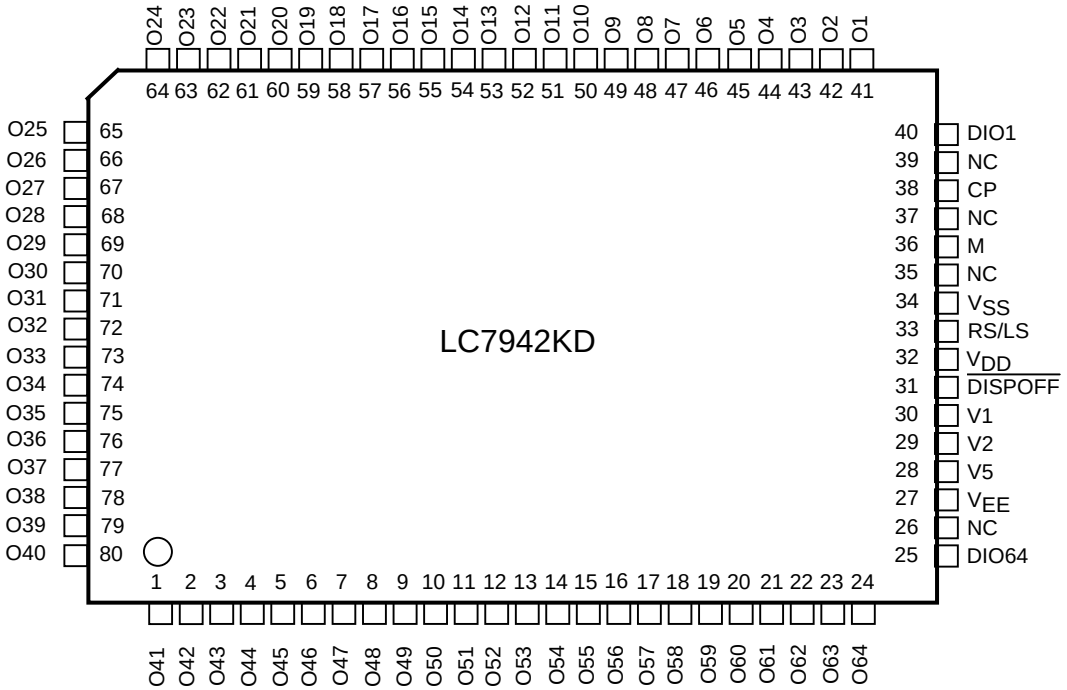
unit: mm (typ)

3177



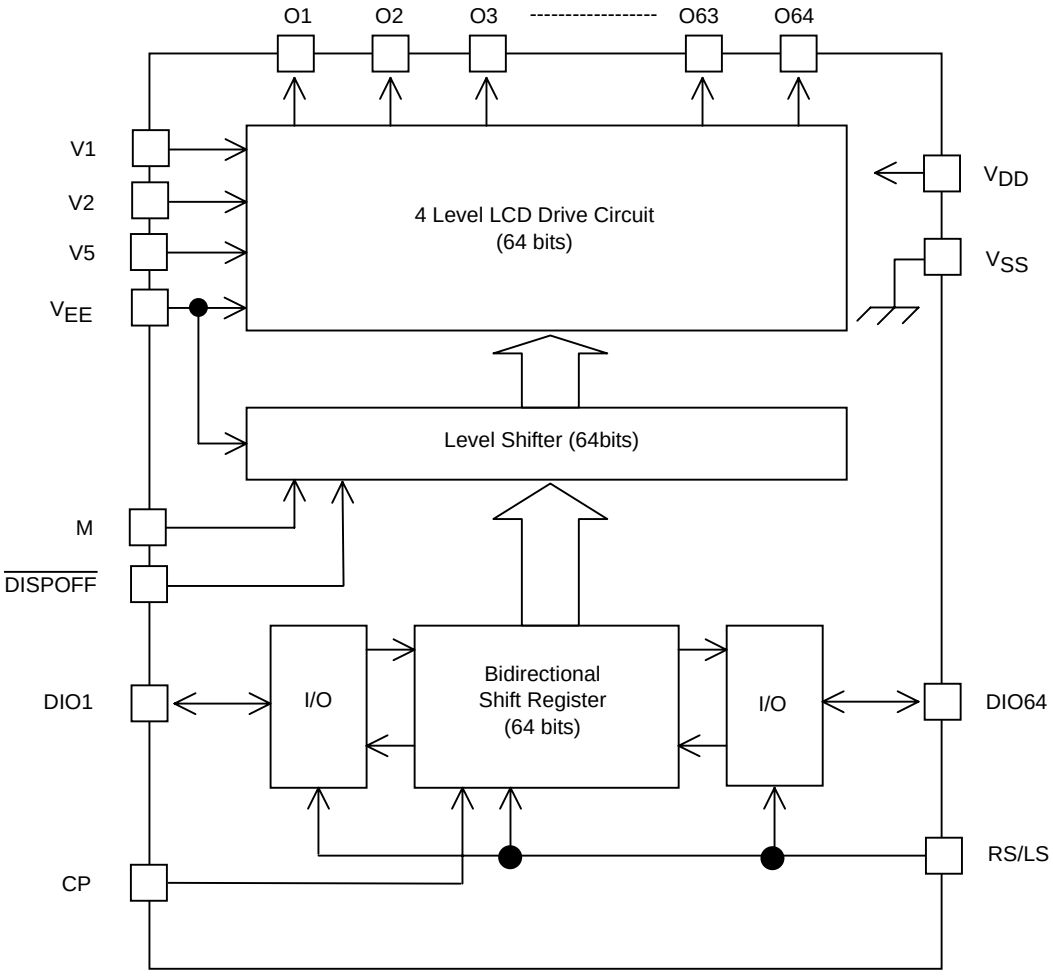

SANYO : QIP80D(14X20)

## Pin Assignment




Top view

## Block Diagram



## Pin Function

<table>
<tr><th>Pin No.</th><th>Pin name</th><th>Input/Output</th><th>Functions</th></tr>
<tr><td>32<br>34<br>27</td><td>$V_{DD}$<br>$V_{SS}$<br>$V_{EE}$</td><td>Supply</td><td>$V_{DD}$-$V_{SS}$ is the logic supply.<br>$V_{DD}$-$V_{EE}$ is the LCD supply.</td></tr>
<tr><td>30<br>29<br>28</td><td>V1<br>V2<br>V5</td><td>Supply</td><td>LCD panel drive voltage supplies.<br>V1 and $V_{EE}$ are selected levels.<br>V2 and V5 are non-selected levels.</td></tr>
<tr><td>38</td><td>CP</td><td>I</td><td>Display data input clock (falling-edge trigger).</td></tr>
<tr><td>40<br>25<br>33</td><td>DIO1<br>DIO64<br>RS/LS</td><td>I/O<br>I/O<br>I</td><td>
<table>
<tr><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO64</th></tr>
<tr><td>L (right shift)</td><td>O1→O64</td><td>IN</td><td>OUT</td></tr>
<tr><td>H (left shift)</td><td>O64→O1</td><td>OUT</td><td>IN</td></tr>
</table>
</td></tr>
<tr><td>36</td><td>M</td><td>I</td><td>LCD panel drive voltage alternating control signal.</td></tr>
<tr><td>31</td><td>$\overline{\text{DISPOFF}}$</td><td>I</td><td>O1 to O64 output control input pins.</td></tr>
<tr><td>41 to 80<br>1 to 24</td><td>O1 to O40<br>O41 to O64</td><td>Output</td><td>LCD drive outputs<br>The output drive level is determined by the display data, M signal and $\overline{\text{DISPOFF}}$ input as shown below.
<table>
<tr><th>M</th><th>Data</th><th>$\overline{\text{DISPOFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>$V_{EE}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don’t care (To be set to either “H” or “L”)</td></tr>
<tr><td>26<br>35<br>37<br>39</td><td>NC</td><td>-</td><td>No connection</td></tr>
</table>

## Specifications

### Absolute Maximum Ratings at Ta=25±2°C, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage (logic) | $V_{DD}$ max | - | -0.3 to +7.0 | V |
| Maximum supply voltage (LCD) | $V_{DD}$-$V_{EE}$ max | *1 | 0 to 22 | V |
| Maximum input voltage | $V_{IN}$ max | - | -0.3 to $V_{DD}$ +0.3 | V |
| Operating temperature range | Topr | - | -20 to +85 | °C |
| Storage temperature range | Tstg | - | -40 to +125 | °C |

Note *1 The voltages V1, V2, and V5 must obey the relationships:
$V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD}$-V2≤7V, V5-$V_{EE}$≤7V

### Allowable Operating Ranges at Ta = -20 to 85°C, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Supply voltage (logic) | $V_{DD}$ | - | 2.7 | - | 5.5 | V |
| Supply voltage (LCD) | $V_{DD}$-$V_{EE}$ | *2, 3 | 8 | - | 20 | V |
| Input high level voltage | $V_{IH}$ | DIO1, DIO64, CP, M, RS/LS, $\overline{\text{DISPOFF}}$ | 0.8$V_{DD}$ | - | - | V |
| Input low level voltage | $V_{IL}$ | DIO1, DIO64, CP, M, RS/LS, $\overline{\text{DISPOFF}}$ | - | - | 0.2$V_{DD}$ | V |
| CP (Shift clock) | $f_{CP}$ | CP | - | - | 1 | MHz |
| CP (pulse width) | $t_{WC}$ | CP | 125 | - | - | ns |
| Setup time | $t_{SETUP}$ | DIO1→CP, DIO64→CP | 100 | - | - | ns |
| Hold time | $t_{HOLD}$ | DIO1→CP, DIO64→CP | 100 | - | - | ns |
| CP rise time | $t_R$ | CP | - | - | 50 | ns |
| CP fall time | $t_F$ | CP | - | - | 50 | ns |

Note *2 The voltages V1, V2, and V5 must obey the relationships:
$V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD}$-V2≤7V, V5-$V_{EE}$≤7V

*3 When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

**Electrical Characteristics** at Ta = 25±2°C, $V_{SS}$ = 0V, $V_{DD}$= 2.7 to 5.5V

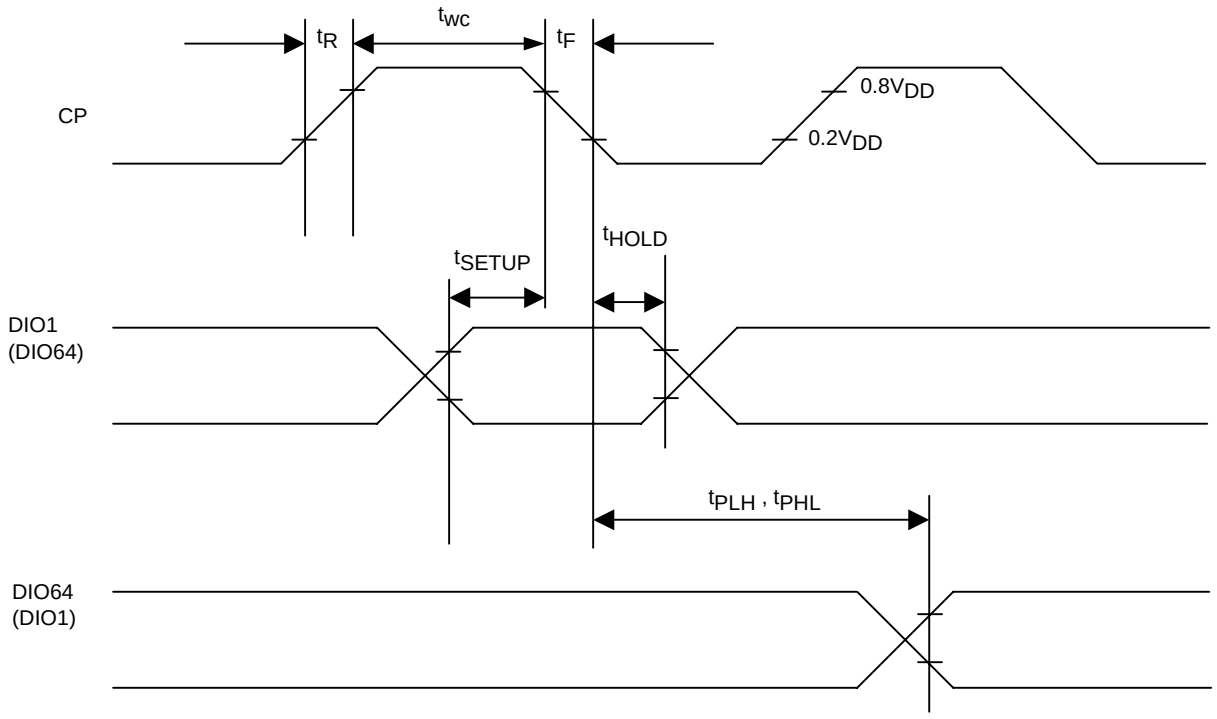
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Input high level current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$, $V_{DD}$ = 5.5V, DIO1, DIO64, CP, M, RS/LS, $\overline{DISPOFF}$ | - | - | 1 | μA |
| Input low level current | $I_{IL}$ | $V_{IN}$ = $V_{SS}$, $V_{DD}$ = 5.5V, DIO1, DIO64, CP, M, RS/LS, $\overline{DISPOFF}$ | -1 | - | - | μA |
| Output high level voltage | $V_{OH}$ | $I_{OH}$ = -0.4mA, DIO1, DIO64 | $V_{DD}$-0.4 | - | - | V |
| Output low level voltage | $V_{OL}$ | $I_{OL}$ = 0.4mA, DIO1, DIO64 | - | - | 0.4 | V |
| Driver on resistance | $R_{ON}$ | $V_{DD}$-$V_{EE}$ = 18V. $\|V_{DE}$-$V_O\|$ = 0.25V $V_{DD}$ = 4.5V *4; O1 to O64 | - | - | 1.5 | kΩ |
| $V_{DD}$ static Current | $I_{DD}$ | $V_{DD}$-$V_{EE}$ = 18V, CP = $V_{DD}$ | - | - | 100 | μA |

Note *4 $V_{DE}$ = V1 or V2 or V5 or $V_{EE}$, V1 = $V_{DD}$, V2 = 10/11($V_{DD}$-$V_{EE}$), V5 = 1/11($V_{DD}$-$V_{EE}$)

**Switching Characteristics** at Ta = 25±2°C, $V_{SS}$ = 0V, $V_{DD}$ = 2.7 to 5.5V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Output delay time | $t_{PLH}$ | CL=30pF; CP→DIO1, CP→DIO64 | - | - | 250 | ns |
| | $t_{PHL}$ | CL=30pF; CP→DIO1, CP→DIO64 | - | - | 250 | ns |

## Switching Characteristics Diagram



## Application Notes LCD Panel