Ordering number : EN4349B

CMOS LSI

# LC79431D

## Dot Matrix LCD Driver

## Overview

The LC79431D is a large-scale dot matrix LCD common driver LSI. The LC79431D contains an 80-bit bidirectional shift register and a 4-level LCD driver. The input/output pins for cascade connection can be used to further increase the bit count. The LC79431D can be used in conjunction with segment driver LC79400D or LC79401D (QFP100D) to drive a wide-screen LCD panel.

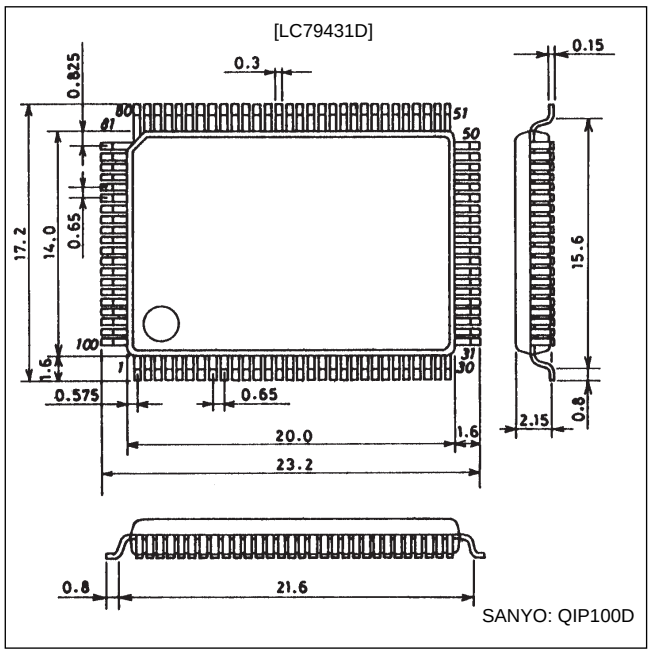
## Features

- On-chip LCD drive circuit (80 bits)
- Display duty of 1/64 to 1/256 selectable
- On-chip input/output pins support a further increase in bit count
- Supports externally supplied bias voltage
- Operating supply voltage/operating temperature are:
  $V_{DD}$ (logic block) : 5 V ±10 % / –20 to +75 °C
  $V_{DD}$–$V_{EE}$ (LCD block) : 12 V to 32 V / –20 to +75°C
- CMOS process

## Package Dimensions

unit : mm

**3180-QFP100D**




## Specifications

### Absolute Maximum Ratings at Ta = 25±2°C, $V_{SS}$ = 0V

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Maximum supply voltage (logic) | $V_{DD}$ max | –0.3 to +7.0 | V |
| Maximum supply voltage (LCD) | $V_{DD0} - V_{EE}$ max * | 0 to 35 | V |
| Maximum input voltage | $V_{IN}$ max | –0.3 to $V_{DD}$ +0.3 | V |
| Storage temperature range | Tstg | –40 to +125 | °C |

Note: * The voltages V1, V2, and V5 must obey the relationships: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.

## Allowable Operating Ranges at Ta = –20 to +75°C, $V_{SS}$ = 0V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage (logic) | $V_{DD}$ | | 4.5 | | 5.5 | V |
| Supply voltage (LCD) | $V_{DD} - V_{EE}$ | *1, *2 | 12 | | 32 | V |
| Input high level voltage | $V_{IH}$ | DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISP OFF}}$ | 0.8$V_{DD}$ | | | V |
| Input low level voltage | $V_{IL}$ | DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISP OFF}}$ | | | 0.2$V_{DD}$ | V |
| CP (shift clock) | $f_{CP}$ | CP | | | 1 | MHz |
| CP (pulse width) | $t_{WC}$ | CP | 63 | | | ns |
| Setup time | $t_{SETUP}$ | DIO1 → CP, DIO80 → CP, | 100 | | | ns |
| Hold time | $t_{HOLD}$ | DIO1 → CP, DIO80 → CP, | 100 | | | ns |
| CP rise/fall time | $t_R$ | CP | | | 50 | ns |
| | $t_F$ | CP | | | 50 | ns |

Note: 1. The voltages V1, V2, and V5 must obey the relationships: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, $V_{DD} - V2 \leq 7V$, $V5 - V_{EE} \leq 7V$.
2. When applying power, apply power to the LCD drive block after applying power to the logic block or apply power to both the blocks simultaneously. When turning off power, turn off power to the logic block after turning off power to the LCD drive block or turn off power to both the blocks simultaneously.

## Electrical Characteristics at Ta = 25±2°C, $V_{SS}$ = 0V, $V_{DD}$ = 5V±10%

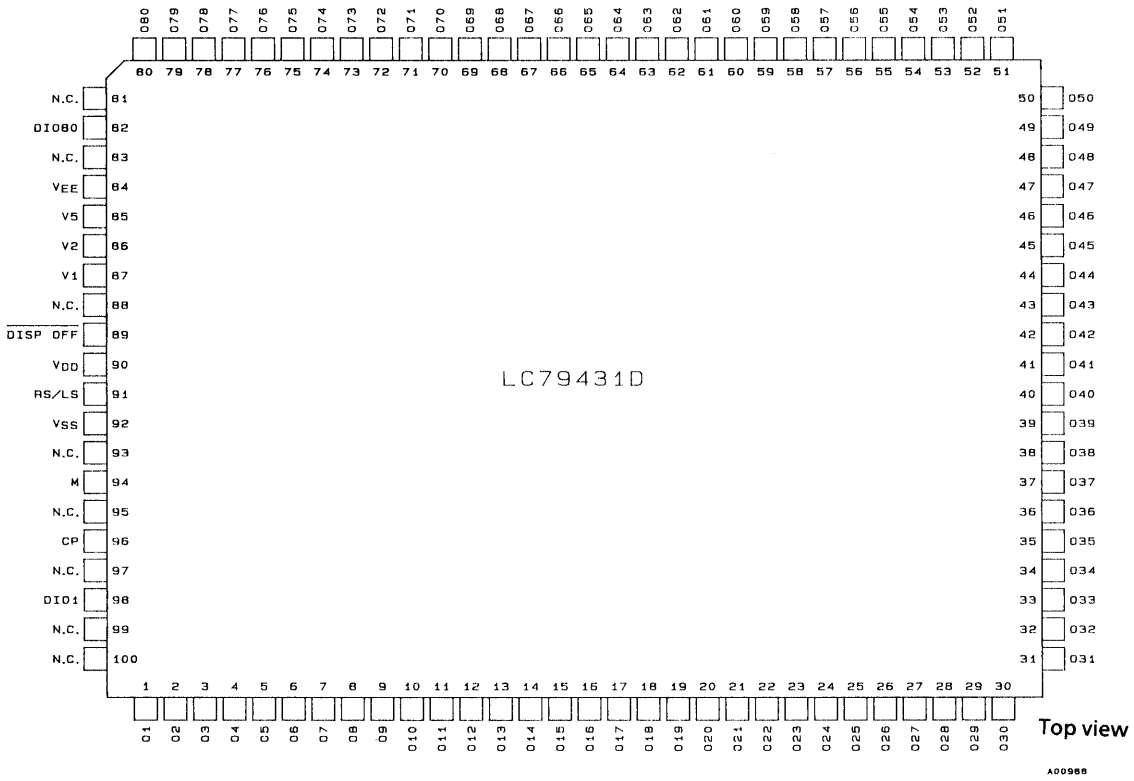
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level current | $I_{IH}$ | $V_{IN} = V_{DD}$, $V_{DD}$ = 5.5 V; DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISP OFF}}$ | | | 1 | µA |
| Input low level current | $I_{IL}$ | $V_{IN} = V_{SS}$, $V_{DD}$ = 5.5 V; DIO1, DIO80, CP, M, RS/LS, $\overline{\text{DISP OFF}}$ | –1 | | | µA |
| Output high level voltage | $V_{OH}$ | $I_{OH}$ = – 0.4 mA, $V_{DD}$ = 4.5 V; DIO1, DIO80 | $V_{DD}$–0.4 | | | V |
| Output low level voltage | $V_{OL}$ | $I_{OL}$ = 0.4 mA, $V_{DD}$ = 4.5 V; DIO1, DIO80 | | | 0.4 | V |
| Drive-on resistor | $R_{ON}$ (1) | $V_{DD} - V_{EE}$ = 30 V, $\lvert V_{DE} - Vo \rvert$ = 0.5V $V_{DD}$ = 4.5 V *; O1 to O80 | | | 1.0 | kΩ |
| | $R_{ON}$ (2) | $V_V - V_{EE}$ = 20 V, $\lvert V_{DE} - Vo \rvert$ = 0.5V, $V_{DD}$ = 4.5 V *; O1 to O80 | | | 1.0 | kΩ |
| Current drain (1) | $I_{SS}$ | $V_{DD}$–$V_{EE}$ = 30 V, CP = 14 kHz, no load, $V_{DD}$ = 5.5 V; $V_{SS}$ | | | 100 | µA |
| Current drain (2) | $I_{EE}$ | $V_{DD} - V_{EE}$ = 30V, CP = 14 kHz, no load, $V_{DD}$ = 5.5 V; $V_{EE}$ | | | 100 | µA |
| Input capacitance | $C_{IN}$ | f = 1 MHz; CP | | 5 | | pF |

Note: * $V_{DE}$ = V1 or V2 or V5 or $V_{EE}$, V1 = $V_{DD}$, V2 = 16/17 ($V_{DD} - V_{EE}$), V5 = 1/17 ($V_{DD} - V_{EE}$)

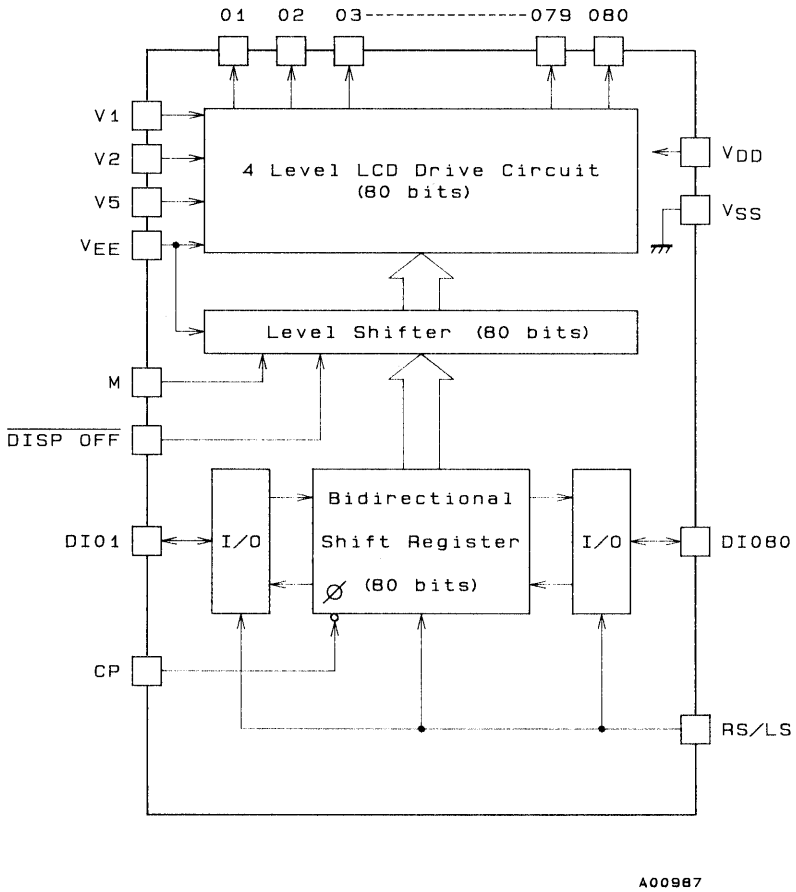
## Switching Characteristics at Ta = 25±2°C, $V_{SS}$ = 0V, $V_{DD}$ = 5V±10%

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Output delay time | $t_{PLH}$ | $C_L$ = 15pF; CP → DIO1, CP → DIO80 | | | 250 | ns |
| | $t_{PHL}$ | $C_L$ = 15pF; CP → DIO1, CP → DIO80 | | | 250 | ns |

## Pin Assignment




## Equivalent Circuit Block Diagram



## Pin Descriptions

<table>
<tr><th>Pin No</th><th>Pin name</th><th>Input/Output</th><th>Functions</th></tr>
<tr><td>90<br>92<br>84</td><td>$V_{DD}$<br>$V_{SS}$<br>$V_{EE}$</td><td>Power supply</td><td>$V_{DD}$ to $V_{SS}$: Power supply for logic block<br><br>$V_{DD}$ to $V_{EE}$: Power supply for LCD drive block</td></tr>
<tr><td>87<br>86<br>85</td><td>V1<br>V2<br>V5</td><td>Power supply</td><td>LCD drive level power supply<br>V1 to $V_{EE}$ : Select level<br>V2 to V5 : Nonselect level</td></tr>
<tr><td>96</td><td>CP</td><td>Input</td><td>Bidirectional shift register’s shift clock (triggering on the trailing edge)</td></tr>
<tr><td>98<br>82<br>91</td><td>DIO1<br>DIO80<br>RS/LS</td><td>Input/Output<br>Input/Output<br>Input</td><td>
<table>
<tr><th>RS/LS</th><th>Data Transfer Direction</th><th>DIO1</th><th>DIO80</th></tr>
<tr><td>L(Shift right)</td><td>O1 → O80</td><td>IN</td><td>OUT</td></tr>
<tr><td>H (Shift left)</td><td>O80 → O1</td><td>OUT</td><td>IN</td></tr>
</table>
</td></tr>
<tr><td>94</td><td>M</td><td>Input</td><td>LCD drive output alternating signal</td></tr>
<tr><td>89</td><td>$\overline{\text{DISP OFF}}$</td><td>Input</td><td>O1 to O80 output controlling input pin</td></tr>
<tr><td>1<br>:<br>80</td><td>O1<br>:<br>O80</td><td>Output</td><td>LCD drive output<br>The combination of scanning data, M signal, and $\overline{\text{DISP OFF}}$ signal can be used to create output levels as shown below.
<table>
<tr><th>M</th><th>Data</th><th>$\overline{\text{DISP OFF}}$</th><th>Output</th></tr>
<tr><td>L</td><td>L</td><td>H</td><td>V2</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>$V_{EE}$</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>V5</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>V1</td></tr>
<tr><td>*</td><td>*</td><td>L</td><td>V1</td></tr>
</table>
* Don’t care (To be set to either “H” or “L”)</td></tr>
</table>

## Switching Characteristics Diagram