Ordering number : EN*5735

CMOS LSI

LC821031

Image-Processing IC for Facsimile, Copier, and OCR Products

Preliminaly

Overview

The LC821031 converts analog video signals from CCD and contact sensors to high-quality binary image data. It includes both an 8-bit A/D converter and a 6-bit D/A converter for setting the reference potential and creates high-quality multi-valued data using a gamma conversion technique that supports arbitrary gamma curves. It also provides both black and white all-pixel distortion correction and multi-valued resolution conversion. It then applies two-dimensional filtering to this multi-valued data to separate the document image into text, photograph, and halftone areas. After converting the image to a binary image using an error diffusion technique that acquires high-quality images, it applies reduction in both the primary and secondary scan directions. Since the LC821031 limits the number of pixels processed per line to 3072 pixels, it needs no external memory to implement this processing. Thus the LC821031 implements the image processing used by facsimile, copier, and OCR products.

Features

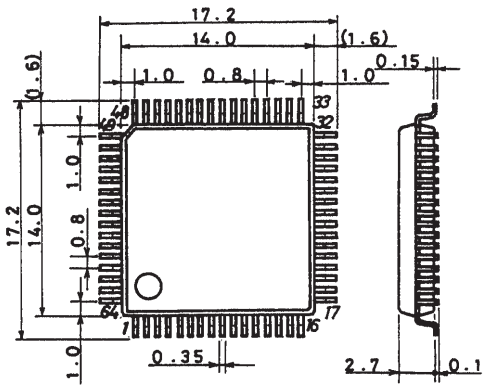
- Number of pixels processed: 3072 pixels/line
- Processing speed: 250 ns/pixel, maximum (When CLKIN = 32 MHz)
- 8-bit A/D converter (Includes a sensor signal timing adjustment function.)
- 6-bit D/A converter for setting the A/D converter reference potential
- Sensor drive circuit (Supports most CCD and CIS devices.)
- Digital clamp (single-point clamping and even/odd clamping)
- Distortion correction (white correction: all-pixel correction, black correction: all-pixel correction)
- Gamma correction (Supports user-defined curves: 8-bit data)
- Image area separation
- Simple binary coding (fixed threshold and density adaptive threshold)
- Halftone processing: error diffusion method (64 levels)
- Multi-value resolution conversion (Conversion ratios of 1:2, 2:3, 3:2, and 2:1)
- Binary image reduction (Main scan line direction: decimation, fine black line retention, fine white line retention; secondary scan line direction: decimation, fine line retention)
- Fabricated in a CMOS process for single 5-V power-supply and low power.

Package Dimensions

unit: mm

3159-QFP64E

[LC821031]



SANYO: QIP64E

Specifications

Absolute Maximum Ratings at Ta = 25°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		–0.3 to +7.0	V
Input and output voltage	V_I, V_O		–0.3 to V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering conditions		Hand soldering: 3 seconds	350	°C
		Reflow soldering: 10 seconds	235	°C

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Allowable Operating Ranges at Ta = –30 to +70°C, GND = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		4.5		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

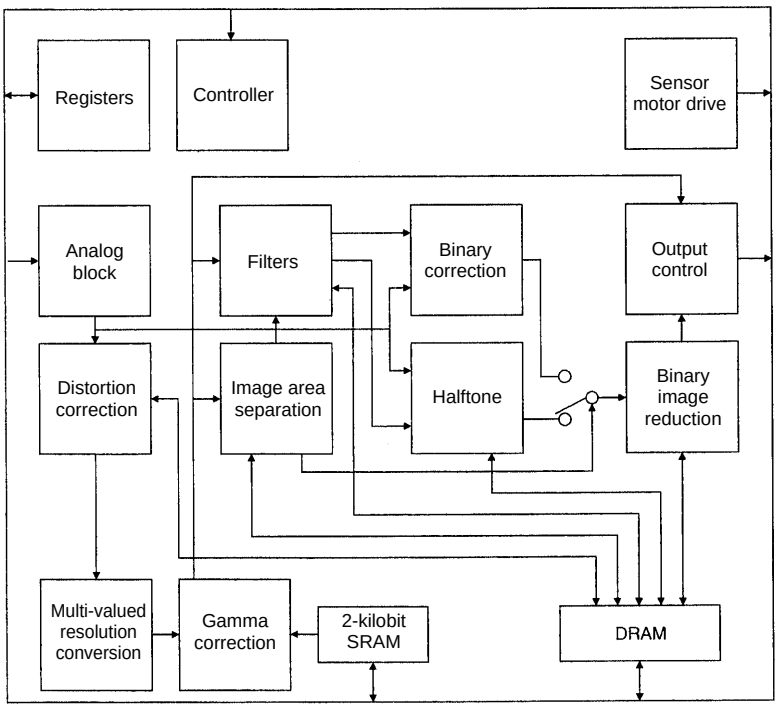
DC Characteristics at Ta = –30 to +70°C, GND = 0 V, V_{DD} = 4.5 to 5.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage	V_{IH}		2.2			V
Input low-level voltage	V_{IL}				0.8	V
Input leakage current	$I_{IH, L}$	$V_{IN} = V_{DD}, V_{SS}$	–10		+10	µA
Output high-level voltage	V_{OH}	I_{OH} = –3 mA	2.4			V
Output low-level voltage	V_{OL}	I_{OL} = 3 mA			0.4	V
Output leakage current	I_L	When high-impedance	–10		+10	µA
Current drain	I_{DD}	CLKIN = 32 MHz		40	70	mA

Analog Characteristics

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[D/A Converter]						
Resolution				6		bit
Internal resistance				4.8		kΩ
[A/D Converter] ATAPL potential: 0.8 V, ATAPH potential: 4.2 V						
Resolution				8		bit
Linearity error					±1	LSB
Differential linearity error					±1	LSB
Internal resistance				330		Ω

Block Diagram



Pin Functions

I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Not Connected

Pin No.	Symbol	I/O	Function
1	D7	B	CPU interface data bus D7 is the MSB, and D0 is the LSB.
2	D6	B	
3	D5	B	
4	D4	B	
5	D3	B	
6	D2	B	
7	D1	B	
8	D0	B	
9	DGND	P	Digital system ground
10	DV_{DD}	P	Digital system power supply
11	A8	I	CPU interface address bus A12 is the MSB, and A0 is the LSB.
12	A7	I	
13	A6	I	
14	A5	I	
15	A4	I	
16	A3	I	
17	DGND	P	Digital system ground
18	A2	I	CPU interface address bus
19	A1	I	
20	A0	I	
21	$\overline{WR}$	I	CPU interface write signal
22	$\overline{RD}$	I	CPU interface read signal
23	A12	I	CPU interface address bus
24	DV_{DD}	P	Digital system power supply
25	CLKIN	I	System clock input
26	A11	I	CPU interface address bus
27	A10	I	
28	A9	I	
29	$\overline{CS}$	I	CPU interface chip select signal
30	ICLK	I	External sampling point signal input
31	TRIG	I	External trigger signal input
32	$\overline{RESET}$	I	System reset
33	SAMP/LININT	O	A/D converter sampling point monitor signal output/LINE signal output
34	TEST	I	Test pin (Must be tied to the digital system ground in normal operation.)
35	$\overline{REF}$	I	DRAM refresh signal input
36	AGND	P	Analog system ground
37	DALRL	I	Low reference for the D/A converter used for the A/D converter low reference.
38	DAHRL	I	Low reference for the D/A converter used for the A/D converter high reference.

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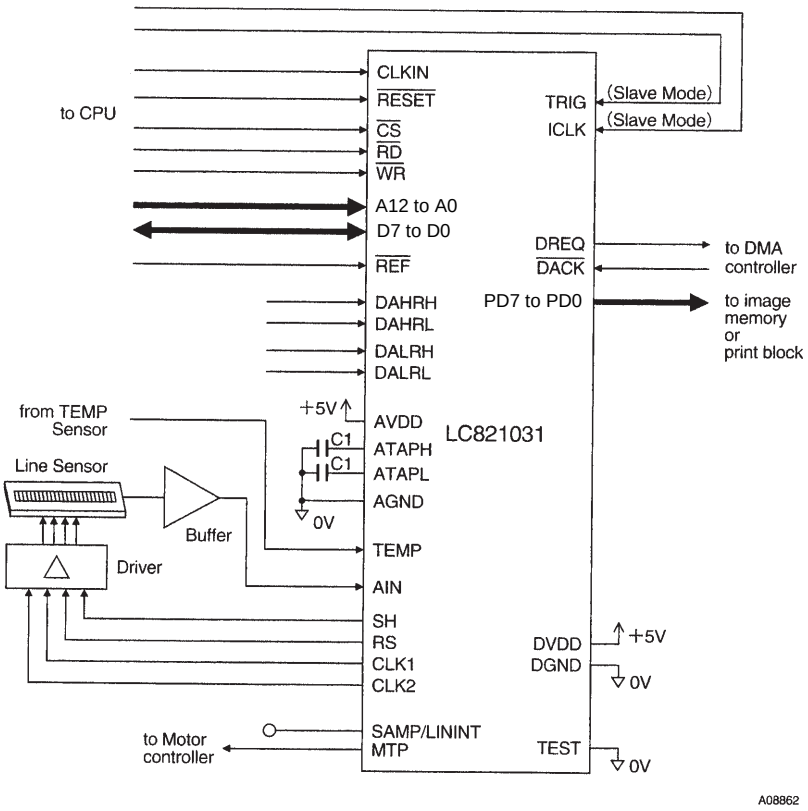
I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: Not Connected

Pin No.	Symbol	I/O	Function
39	AIN	I	Sensor signal input
40	TEMP	I	Temperature signal input
41	ATAPH	O	Analog middle level for the A/D converter high reference
42	DAHRH	I	High reference for the D/A converter used for the A/D converter high reference.
43	AV_{DD}	P	Analog system power supply
44	DALRH	I	High reference for the D/A converter used for the A/D converter low reference.
45	ATAPL	O	Analog middle level for the A/D converter low reference
46	AGND	P	Analog system ground
47	PD7/SD	O	DMA output/serial data output
48	PD6/SDCK	O	DMA output/serial data transfer clock
49	DGND	P	Digital system ground
50	PD5/SDE	O	DMA output/serial data output valid period signal
51	PD4/PP4	B	DMA output/general-purpose I/O ports
52	PD3/PP3	B	
53	PD2/PP2	B	
54	PD1/PP1	B	
55	PD0/PP0	B	
56	DV_{DD}	P	Digital system power supply
57	$\overline{\text{DACK}}$/PP5	B	DMA data acknowledge signal input pin/general-purpose I/O port
58	DREQ/PP6	B	DMA data request signal output/general-purpose I/O port
59	MTP/PP7	B	Motor drive timing signal output/general-purpose I/O port
60	CLK2	O	Sensor drive signal outputs
61	CLK1	O	
62	RS	O	
63	SH	O	
64	DGND	P	Digital system ground

Note: Unused input pins must not be left open. These pins must be connected either to the digital system power supply or to the digital system ground.

Sample Application Circuit



- Use a 0.01 μF monolithic capacitor for C1.
- Applications must set up the polarity of the image signal from the sensor so that white data is at the highest potential and black data is at the lowest. If the peak level in the image signal from the sensor does not reach 4.2 V, a level conversion circuit should be added to allow the application to take advantage of the dynamic range of the internal D/A converter.
- Although AGND and DGND are fully isolated from each other within the IC, AV_{DD} and DV_{DD} are connected through the substrate. Therefore applications must be designed so that there is no potential difference between AV_{DD} and DV_{DD}. Also, the rise and fall of these power-supply potentials must occur within 3 ms of each other.